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4:1 HDMI/DVI Switch with Equalization

AD8191

FEATURES

- Four inputs, one output HDMI™/DVI links
  - Four TMDS channels per link
    - Supports 250 Mbps to 1.65 Gbps data rates
    - Supports 25 MHz to 165 MHz pixel clocks
    - Equalized inputs for operation with long HDMI cables (20 meters at 1080p)
    - Fully buffered unidirectional inputs/outputs
    - Globally switchable, 50 Ω on-chip terminations
    - Pre-emphasized outputs
    - Low added jitter
    - Single-supply operation (3.3 V)
  - Four auxiliary channels per link
    - Bidirectional unbuffered inputs/outputs
    - Flexible supply operation (3.3 V to 5 V)
    - HDCP standard compatible
    - Allows switching of DDC bus and two additional signals
- Multiple channel bundling modes
  - 1x (4:1) HDMI/DVI link switch (default)
  - 2x (8:1) TMDS channel and auxiliary signal switch
  - 1x (16:1) TMDS channel and auxiliary signal switch
- Output disable feature
  - Reduced power dissipation
  - Removable output termination
  - Allows building of larger arrays
- Two AD8191s support HDMI/DVI dual-link
- Standards compatible: HDMI receiver, DVI, HDCP
- Serial (I^2C® slave) and parallel control interface
- 100-lead, 14 mm × 14 mm LQFP, Pb-free package

APPLICATIONS

- Multiple input displays
- Projectors
- A/V receivers
- Set-top boxes
- Advanced television (HDTV) sets

FUNCTIONAL BLOCK DIAGRAM

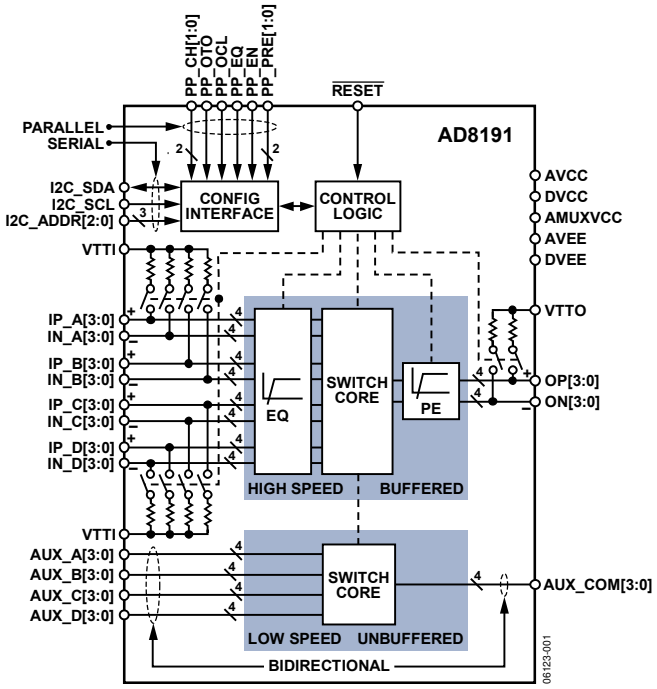

Figure 1.

TYPICAL APPLICATION

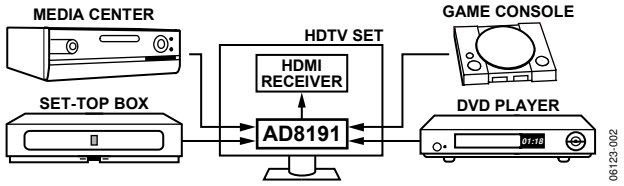

Figure 2. Typical HDTV Application

GENERAL DESCRIPTION

The AD8191 is a HDMI/DVI switch featuring equalized TMDS inputs and pre-emphasized TMDS outputs, ideal for systems with long cable runs. Outputs can be set to a high impedance state to reduce the power dissipation and/or allow the construction of larger arrays using the wire-OR technique. Flexible channel bundling modes (for both the TMDS channels and the auxiliary signals) allow the AD8191 to be configured as a 4:1 single HDMI/DVI link switch, a dual 8:1 switch, or a single 16:1 switch.

The AD8191 is provided in a 100-lead LQFP, Pb-free, surface mount package specified to operate over the −40°C to +85°C temperature range.

PRODUCT HIGHLIGHTS

1. Supports data rates up to 1.65 Gbps, enabling 1080p HDMI formats and UXGA (1600 × 1200) DVI resolutions.
2. Input cable equalizer enables use of long cables at the input (more than 20 meters of 24 AWG cable at 1080p).
3. Auxiliary switch routes a DDC bus and two additional signals for a single-chip, HDMI 1.2a receive-compliant solution.

Rev. 0

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AD8191* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- AD8191: 4:1 HDMI/DVI Switch with Equalization Data Sheet

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Technical Articles

- Analysis of Common Failures of HDMI CT
- Video Portables and Cameras Get HDMI Outputs

DESIGN RESOURCES

- AD8191 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD8191 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

10/06—Revision 0: Initial Version

SPECIFICATIONS

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, DVCC = 3.3 V, AMUXVCC = 5 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Maximum Data Rate (DR) per Channel	NRZ	1.65			Gbps
Bit Error Rate (BER)	PRBS $2^{23} - 1$			10^{-9}	
Added Deterministic Jitter	DR ≤ 1.65 Gbps, PRBS $2^{23} - 1$		40		ps (p-p)
Added Random Jitter			2		ps (rms)
Differential Intrapair Skew	At output		1		ps
Differential Interpair Skew[1]	At output		40		ps
EQUALIZATION PERFORMANCE					
Receiver (Highest Setting)[2]	Boost frequency = 825 MHz		12		dB
Transmitter (Highest Setting)[3]	Boost frequency = 825 MHz		6		dB
INPUT CHARACTERISTICS					
Input Voltage Swing	Differential	150		1200	mV
Input Common-Mode Voltage (V_{ICM})		AVCC − 800		AVCC	mV
OUTPUT CHARACTERISTICS					
High Voltage Level	Single-ended high speed channel	AVCC − 10		AVCC + 10	mV
Low Voltage Level	Single-ended high speed channel	AVCC − 600		AVCC − 400	mV
Rise/Fall Time (20% to 80%)		75	135	200	ps
INPUT TERMINATION					
Resistance	Single-ended		50		Ω
AUXILIARY CHANNELS					
On Resistance, R_{AUX}			100		Ω
On Capacitance, C_{AUX}	DC bias = 2.5 V, ac voltage = 3.5 V, f = 100 kHz		8		pF
Input/Output Voltage Range		DVEE		AMUXVCC	V
POWER SUPPLY					
AVCC	Operating range	3	3.3	3.6	V
QUIESCENT CURRENT					
AVCC	Outputs disabled	30	40	44	mA
	Outputs enabled, no pre-emphasis	48	60	64	mA
	Outputs enabled, maximum pre-emphasis	88	100	110	mA
VTTI	Input termination on[4]	5	40	54	mA
VTTO	Output termination on, no pre-emphasis	35	40	46	mA
	Output termination on, maximum pre-emphasis	72	80	90	mA
DVCC		3.2	7	8	mA
AMUXVCC			0.01	0.1	mA
POWER DISSIPATION					
	Outputs disabled	115	271	361	mW
	Outputs enabled, no pre-emphasis	384	574	671	mW
	Outputs enabled, maximum pre-emphasis	704	910	1050	mW
TIMING CHARACTERISTICS					
Switching/Update Delay	High speed switching register: HS_CH			200	ms
	All other configuration registers			1.5	ms
$\overline{\text{RESET}}$ Pulse Width		50			ns

Parameter	Conditions/Comments	Min	Typ	Max	Unit
SERIAL CONTROL INTERFACE[5]					
Input High Voltage, V_{IH}		2			V
Input Low Voltage, V_{IL}				0.8	V
Output High Voltage, V_{OH}		2.4			V
Output Low Voltage, V_{OL}				0.4	V
PARALLEL CONTROL INTERFACE					
Input High Voltage, V_{IH}		2			V
Input Low Voltage, V_{IL}				0.8	V

[1] Differential interpair skew is measured between the TMDS pairs of a single link.
[2] AD8191 output meets the transmitter eye diagram as defined in the DVI Standard Revision 1.0 and the HDMI Standard Revision 1.2a.
[3] Cable output meets the receiver eye diagram mask as defined in the DVI Standard Revision 1.0 and the HDMI Standard Revision 1.2a.
[4] Typical value assumes only the selected HDMI/DVI link is active with nominal signal swings and that the unselected HDMI/DVI links are deactivated. Minimum and maximum limits are measured at the respective extremes of input termination resistance and input voltage swing.
[5] The AD8191 is an I^2C slave and its serial control interface is based on the 3.3 V I^2C bus specification.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
AVCC to AVEE	3.7 V
DVCC to DVEE	3.7 V
DVEE to AVEE	±0.3 V
VTTI	AVCC + 0.6 V
VTTO	AVCC + 0.6 V
AMUXVCC	5.5 V
Internal Power Dissipation	2.2 W
High Speed Input Voltage	AVCC − 1.4 V < V_{IN} < AVCC + 0.6 V
High Speed Differential Input Voltage	2.0 V
Low Speed Input Voltage	DVEE − 0.3 V < V_{IN} < AMUXVCC + 0.6 V
I^2C and Parallel Logic Input Voltage	DVEE − 0.3 V < V_{IN} < DVCC + 0.6 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions: a device soldered in a 4-layer JEDEC circuit board for surface-mount packages. θ_{JC} is specified for no airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
100-Lead LQFP	56	19	°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8191 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package.

Exceeding a junction temperature of 175°C for an extended period can result in device failure. To ensure proper operation, it is necessary to observe the maximum power rating as determined by the coefficients in Table 3.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

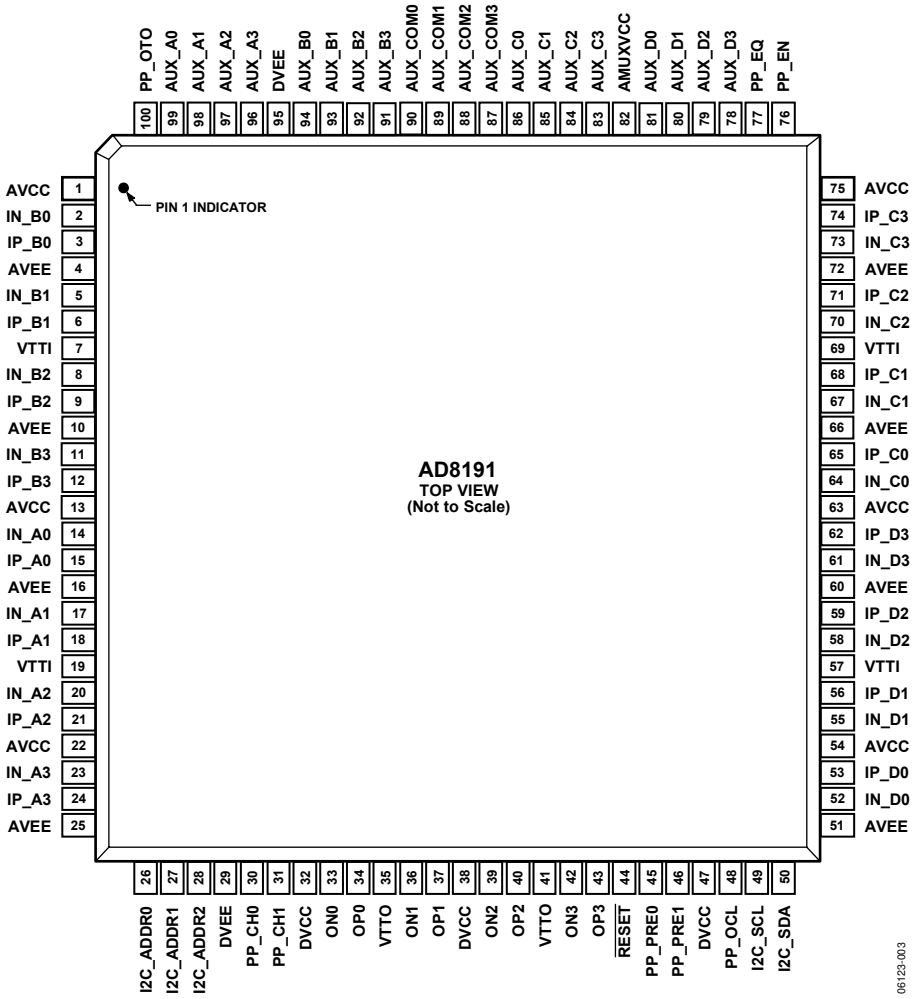

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 13, 22, 54, 63, 75	AVCC	Power	Positive Analog Supply. 3.3 V nominal.
2	IN_B0	HS I	High Speed Input Complement.
3	IP_B0	HS I	High Speed Input.
4, 10, 16, 25, 51, 60, 66, 72	AVEE	Power	Negative Analog Supply. 0 V nominal.
5	IN_B1	HS I	High Speed Input Complement.
6	IP_B1	HS I	High Speed Input.
7, 19, 57, 69	VTTI	Power	Input Termination Supply. Nominally connected to AVCC.
8	IN_B2	HS I	High Speed Input Complement.
9	IP_B2	HS I	High Speed Input.
11	IN_B3	HS I	High Speed Input Complement.
12	IP_B3	HS I	High Speed Input.
14	IN_A0	HS I	High Speed Input Complement.
15	IP_A0	HS I	High Speed Input.

Pin No.	Mnemonic	Type[1]	Description
17	IN_A1	HS I	High Speed Input Complement.
18	IP_A1	HS I	High Speed Input.
20	IN_A2	HS I	High Speed Input Complement.
21	IP_A2	HS I	High Speed Input.
23	IN_A3	HS I	High Speed Input Complement.
24	IP_A3	HS I	High Speed Input.
26	I2C_ADDR0	Control	I^2C Address 1st LSB.
27	I2C_ADDR1	Control	I^2C Address 2nd LSB.
28	I2C_ADDR2	Control	I^2C Address 3rd LSB.
29, 95	DVEE	Power	Negative Digital and Auxiliary Multiplexer Power Supply. 0 V nominal.
30	PP_CH0	Control	Quad Switching Mode High Speed Source Selection Parallel Interface LSB.
31	PP_CH1	Control	Quad Switching Mode High Speed Source Selection Parallel Interface MSB.
32, 38, 47	DVCC	Power	Positive Digital Power Supply. 3.3 V nominal.
33	ON0	HS O	High Speed Output Complement.
34	OP0	HS O	High Speed Output.
35, 41	VTTO	Power	Output Termination Supply. Nominally connected to AVCC.
36	ON1	HS O	High Speed Output Complement.
37	OP1	HS O	High Speed Output.
39	ON2	HS O	High Speed Output Complement.
40	OP2	HS O	High Speed Output.
42	ON3	HS O	High Speed Output Complement.
43	OP3	HS O	High Speed Output.
44	$\overline{\text{RESET}}$	Control	Configuration Registers Reset. Normally pulled up to AVCC.
45	PP_PRE0	Control	High Speed Pre-Emphasis Selection Parallel Interface LSB.
46	PP_PRE1	Control	High Speed Pre-Emphasis Selection Parallel Interface MSB.
48	PP_OCL	Control	High Speed Output Current Level Parallel Interface.
49	I2C_SCL	Control	I^2C Clock.
50	I2C_SDA	Control	I^2C Data.
52	IN_D0	HS I	High Speed Input Complement.
53	IP_D0	HS I	High Speed Input.
55	IN_D1	HS I	High Speed Input Complement.
56	IP_D1	HS I	High Speed Input.
58	IN_D2	HS I	High Speed Input Complement.
59	IP_D2	HS I	High Speed Input.
61	IN_D3	HS I	High Speed Input Complement.
62	IP_D3	HS I	High Speed Input.
64	IN_C0	HS I	High Speed Input Complement.
65	IP_C0	HS I	High Speed Input.
67	IN_C1	HS I	High Speed Input Complement.
68	IP_C1	HS I	High Speed Input.
70	IN_C2	HS I	High Speed Input Complement.
71	IP_C2	HS I	High Speed Input.
73	IN_C3	HS I	High Speed Input Complement.
74	IP_C3	HS I	High Speed Input.
76	PP_EN	Control	High Speed Output Enable Parallel Interface.
77	PP_EQ	Control	High Speed Equalization Selection Parallel Interface.
78	AUX_D3	LS I/O	Low Speed Input/Output.

Pin No.	Mnemonic	Type[1]	Description
79	AUX_D2	LS I/O	Low Speed Input/Output.
80	AUX_D1	LS I/O	Low Speed Input/Output.
81	AUX_D0	LS I/O	Low Speed Input/Output.
82	AMUXVCC	Power	Positive Auxiliary Multiplexer Supply. 5V typical.
83	AUX_C3	LS I/O	Low Speed Input/Output.
84	AUX_C2	LS I/O	Low Speed Input/Output.
85	AUX_C1	LS I/O	Low Speed Input/Output.
86	AUX_C0	LS I/O	Low Speed Input/Output.
87	AUX_COM3	LS I/O	Low Speed Common Input/Output.
88	AUX_COM2	LS I/O	Low Speed Common Input/Output.
89	AUX_COM1	LS I/O	Low Speed Common Input/Output.
90	AUX_COM0	LS I/O	Low Speed Common Input/Output.
91	AUX_B3	LS I/O	Low Speed Input/Output.
92	AUX_B2	LS I/O	Low Speed Input/Output.
93	AUX_B1	LS I/O	Low Speed Input/Output.
94	AUX_B0	LS I/O	Low Speed Input/Output.
96	AUX_A3	LS I/O	Low Speed Input/Output.
97	AUX_A2	LS I/O	Low Speed Input/Output.
98	AUX_A1	LS I/O	Low Speed Input/Output.
99	AUX_A0	LS I/O	Low Speed Input/Output.
100	PP_OTO	Control	High Speed Output Termination Selection Parallel Interface.

[1] HS = high speed, LS = low speed, I = input, O = output.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, DVCC = 3.3 V, AMUXVCC = 5 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, pattern = PRBS $2^7 - 1$, data rate = 1.65 Gbps, unless otherwise noted.

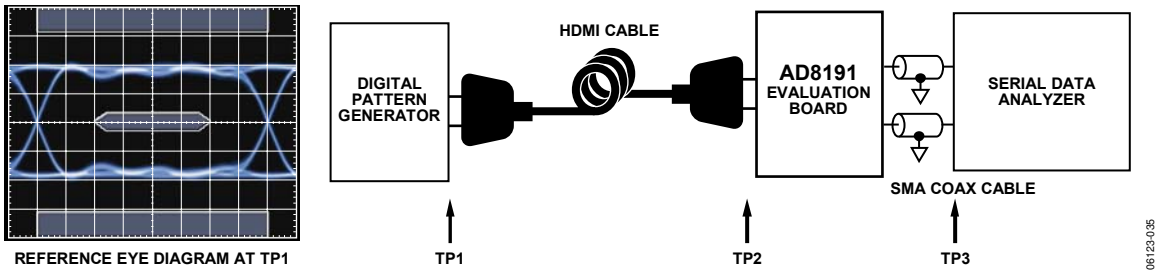

Figure 4. Test Circuit Diagram for RX Eye Diagram

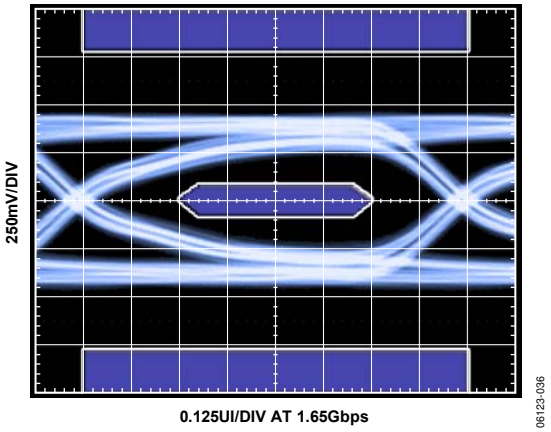

Figure 5. RX Eye Diagram at TP2 (Cable = 2 meters, 30 AWG)

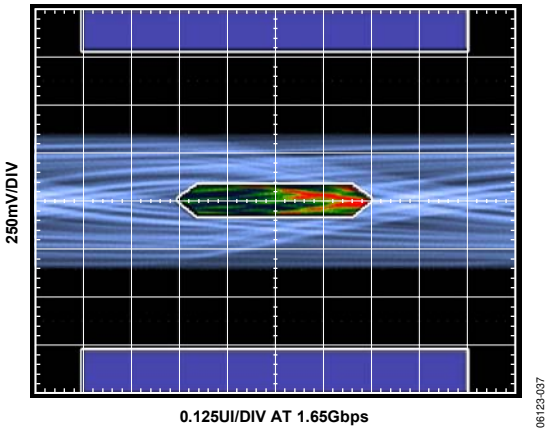

Figure 6. RX Eye Diagram at TP2 (Cable = 20 meters, 24 AWG)

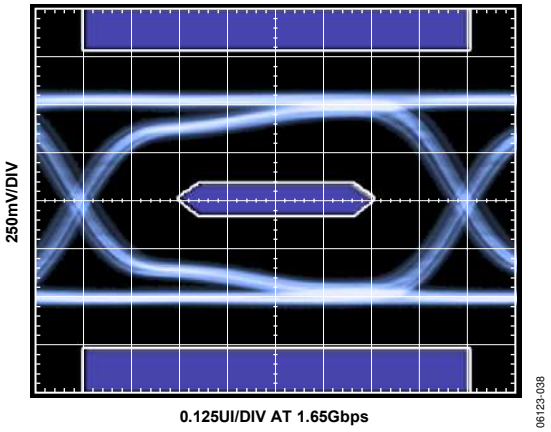

Figure 7. RX Eye Diagram at TP3, EQ = 6 dB (Cable = 2 meters, 30 AWG)

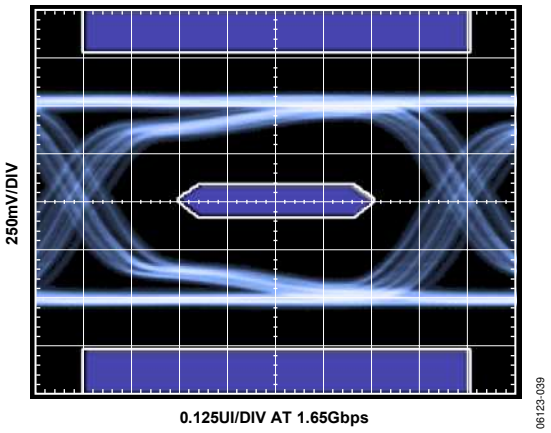

Figure 8. RX Eye Diagram at TP3, EQ = 12 dB (Cable = 20 meters, 24 AWG)

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, DVCC = 3.3 V, AMUXVCC = 5 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, pattern = PRBS $2^7 - 1$, data rate = 1.65 Gbps, unless otherwise noted.

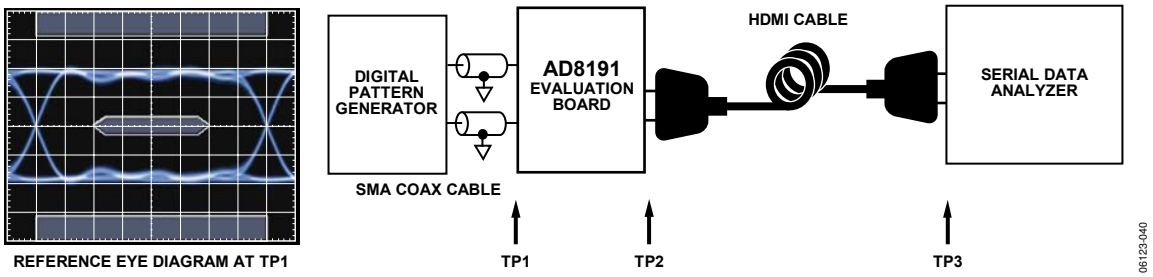

Figure 9. Test Circuit Diagram for TX Eye Diagrams

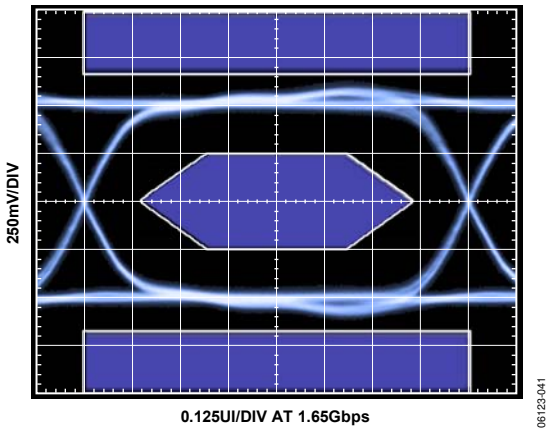

Figure 10. TX Eye Diagram at TP2, PE = 2 dB

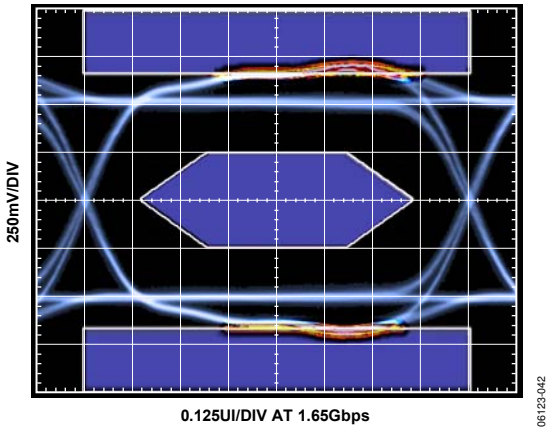

Figure 11. TX Eye Diagram at TP2, PE = 6 dB

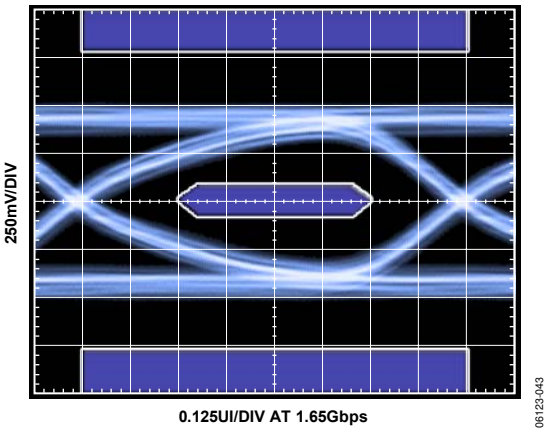

Figure 12. TX Eye Diagram at TP3, PE = 2 dB (Cable = 2 meters, 30 AWG)

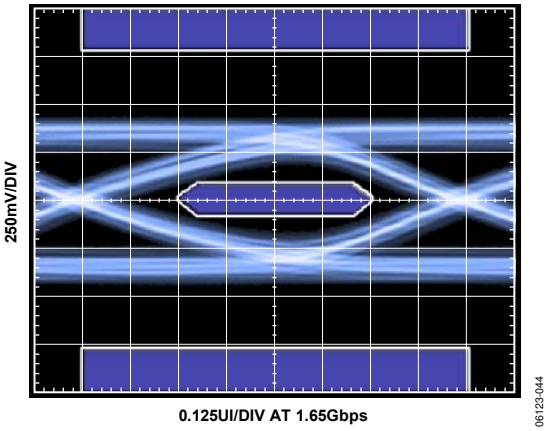

Figure 13. TX Diagram at TP3, PE = 6 dB (Cable = 10 meters, 28 AWG)

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, DVCC = 3.3 V, AMUXVCC = 5 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, pattern = PRBS $2^7 - 1$, data rate = 1.65 Gbps, unless otherwise noted.

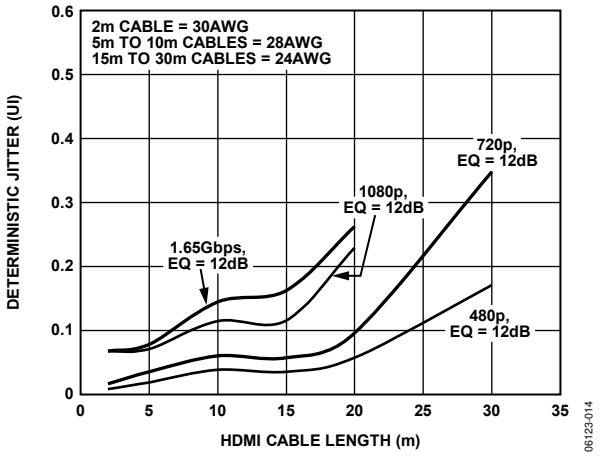

Figure 14. Jitter vs. Input Cable Length (See Figure 4 for Test Setup)

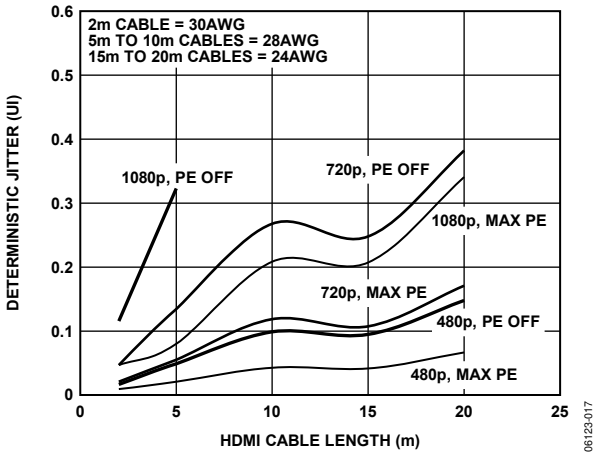

Figure 17. Jitter vs. Output Cable Length (See Figure 9 for Test Setup)

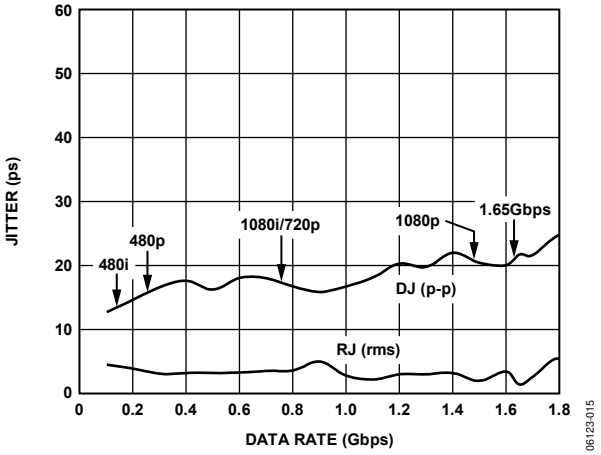

Figure 15. Jitter vs. Data Rate

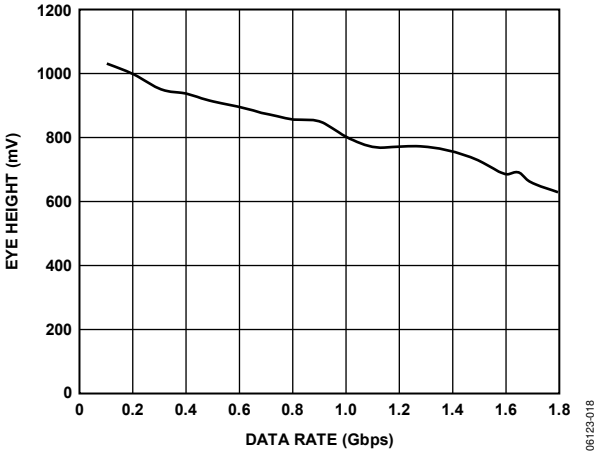

Figure 18. Eye Height vs. Data Rate

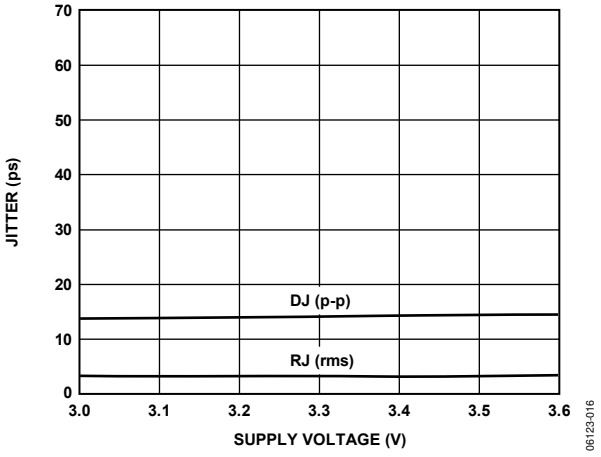

Figure 16. Jitter vs. Supply Voltage

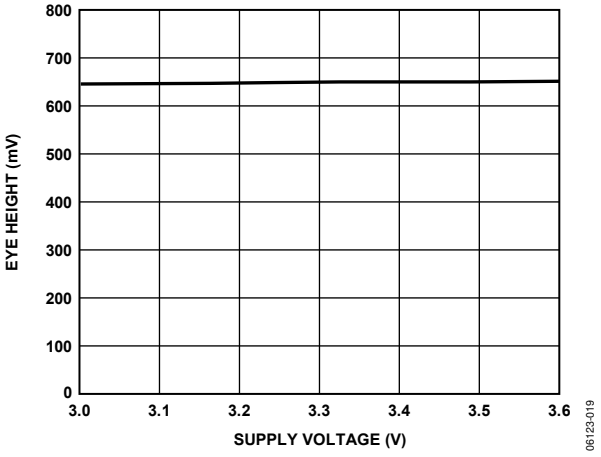

Figure 19. Eye Height vs. Supply Voltage

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, DVCC = 3.3 V, AMUXVCC = 5 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, pattern = PRBS $2^7 - 1$, data rate = 1.65 Gbps, unless otherwise noted.

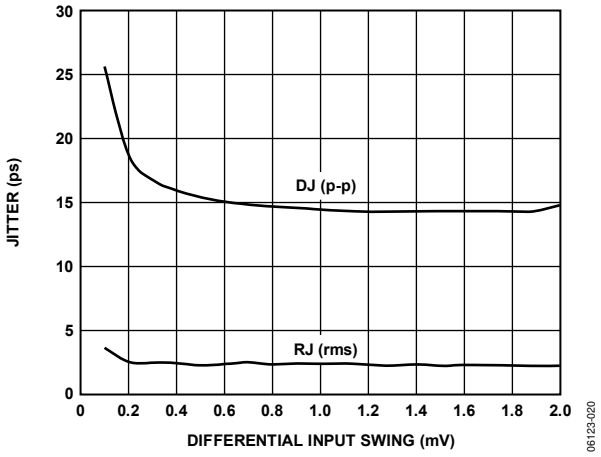

Figure 20. Jitter vs. Differential Input Swing

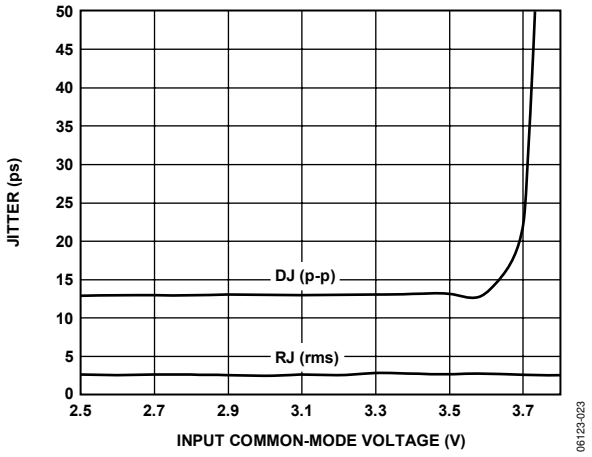

Figure 23. Jitter vs. Input Common-Mode Voltage

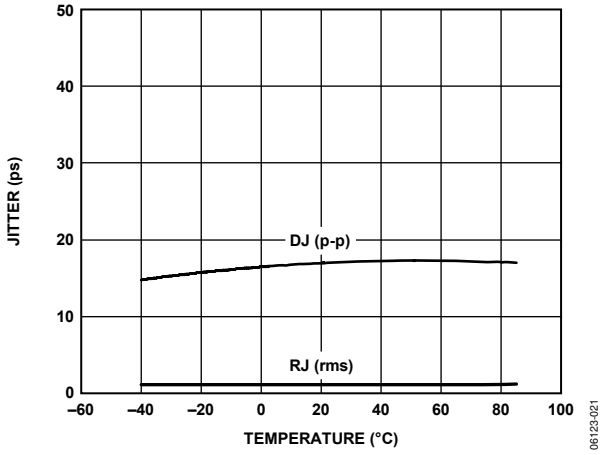

Figure 21. Jitter vs. Temperature

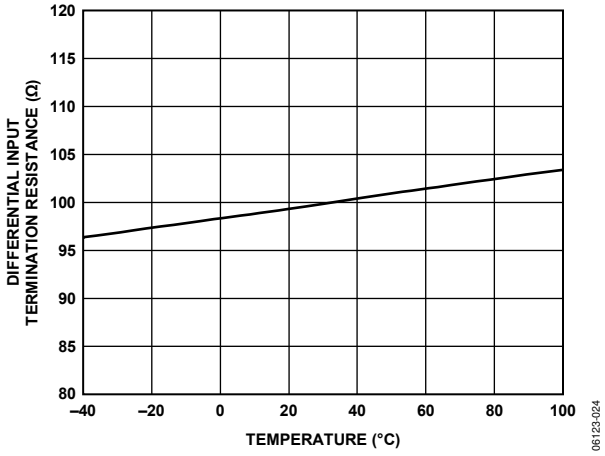

Figure 24. Differential Input Termination Resistance vs. Temperature

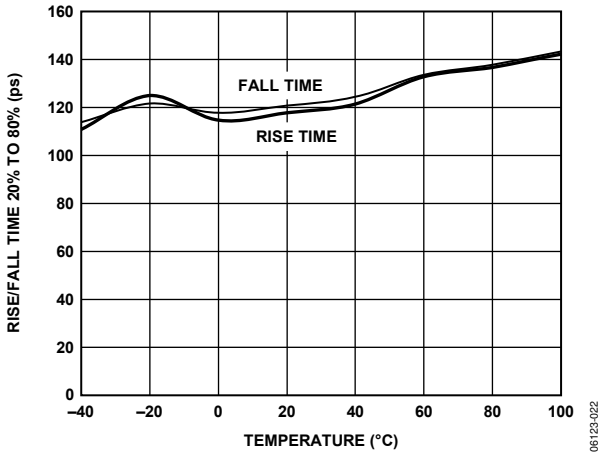

Figure 22. Rise and Fall Time vs. Temperature

THEORY OF OPERATION

INTRODUCTION

The primary function of the AD8191 is to switch one of four (HDMI or DVI) single-link sources to one output. Each HDMI/DVI link consists of four differential, high speed channels and four auxiliary single-ended, low speed control signals. The high speed channels include a data-word clock and three transition minimized differential signaling (TMDS) data channels running at 10× the data-word clock frequency for data rates up to 1.65 Gbps. The four low speed control signals are 5 V tolerant bidirectional lines that can carry configuration signals, HDCP encryption, and other information, depending upon the specific application.

All four high speed TMDS channels in a given link are identical; that is, the pixel clock can be run on any of the four TMDS channels. Transmit and receive channel compensation is provided for the high speed channels where the user can (manually) select among a number of fixed settings.

The AD8191 switching logic has three modes: quad mode (a quad 4:1 switch), dual mode (a dual 8:1 switch) and single mode (one 16:1 switch).

The AD8191 has two control interfaces. Users have the option of controlling the part through either the parallel control interface or the I²C serial control interface. The AD8191 has eight user-programmable I²C slave addresses to allow multiple AD8191s to be controlled by a single I²C bus. A $\overline{\text{RESET}}$ pin is provided to restore the control registers of the AD8191 to default values. In all cases, serial programming values override any prior parallel programming values and any use of the serial control interface disables the parallel control interface until the AD8191 is reset.

When using the serial control interface, all three switching modes (quad, dual, and single) are accessible and the high speed channel switching mode is controlled independently of the auxiliary signal switching mode. When using the parallel control interface, only the quad switching mode is accessible, and the same channel select bus (PP_CH[1:0]) simultaneously switches both the high speed channels and the auxiliary signals.

INPUT CHANNELS

Each high speed input differential pair terminates to the 3.3 V VTTI power supply through a pair of single-ended 50 Ω on-chip resistors, as shown in Figure 25. The input terminations can be optionally disconnected for approximately 100 ms following a source switch. The user can program which of the 16 high speed input channels employs this feature by selectively programming the associated RX_PT bits in the input termination pulse register through the serial control interface. Additionally, all the input terminations can be disconnected by programming the RX_TO bit in the receiver settings register. By default, the input termination is enabled. The input terminations are enabled and cannot be switched when programming the AD8191 through the parallel control interface.

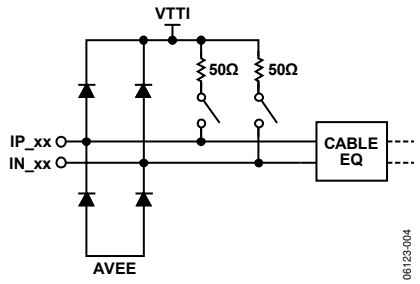

Figure 25. High Speed Input Simplified Schematic

The input equalizer can be manually configured to provide two different levels of high frequency boost: 6 dB or 12 dB. The user can individually control the equalization level of the eight high speed input channels by selectively programming the associated RX_EQ bits in the receive equalizer register through the serial control interface. Alternately, the user can globally control the equalization level of all eight high speed input channels by setting the PP_EQ pin of the parallel control interface. No specific cable length is suggested for a particular equalization setting because cable performance varies widely between manufacturers; however, in general, the equalization of the AD8191 can be set to 12 dB without degrading the signal integrity, even for short input cables. At the 12 dB setting, the AD8191 can equalize more than 20 meters of 24 AWG cable at 1.65 Gbps.

OUTPUT CHANNELS

Each high speed output differential pair is terminated to the 3.3 V VTTO power supply through a 50 Ω on-chip resistor (Figure 26). This termination is user-selectable; it can be turned on or off by programming the TX_PTO bit of the transmitter settings register through the serial control interface, or by setting the PP_OTO pin of the parallel control interface.

The output termination resistors of the AD8191 back-terminate the output TMDS transmission lines. These back-terminations act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the AD8191 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal.

The AD8191 output has a disable feature that places the outputs in a tristate mode. This mode is enabled by programming the HS_EN bit of the high speed device modes register through the serial control interface or by setting the PP_EN pin of the parallel control interface. Larger wire-OR'ed arrays can be constructed using the AD8191 in this mode.

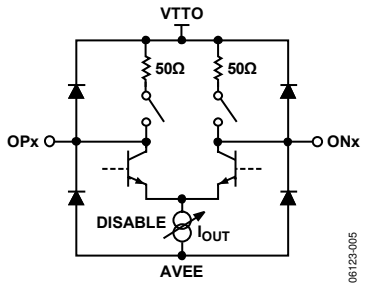

Figure 26. High Speed Output Simplified Schematic

The AD8191 requires output termination resistors when the high speed outputs are enabled. Termination can be internal and/or external. The internal terminations of the AD8191 are enabled by programming the TX_PTO bit of the transmitter settings register or by setting the PP_OTO pin of the parallel control interface. The internal terminations of the AD8191 default to the setting indicated by PP_OTO upon reset. External terminations can be provided either by on-board resistors or by the input termination resistors of an HDMI/DVI receiver. If both the internal terminations are enabled and external terminations are present, set the output current level to 20 mA by programming the TX_OCL bit of the transmitter settings register through the serial control interface or by setting the PP_OCL pin of the parallel control interface. The output current level defaults to the level indicated by PP_OCL upon reset. If only external terminations are provided (if the internal terminations are disabled), set the output current level to 10 mA by programming the TX_OCL bit of the transmitter settings register or by setting the PP_OCL pin of the parallel control interface. The high speed outputs must be disabled if there are no output termination resistors present in the system.

The output pre-emphasis can be manually configured to provide one of four different levels of high frequency boost. The specific boost level is selected by programming the TX_PE bits of the transmitter settings register through the serial control interface, or by setting the PP_PE bus of the parallel control interface. No specific cable length is suggested for a particular pre-emphasis setting because cable performance varies widely between manufacturers.

HIGH SPEED (TMDS) SWITCHING MODES

The AD8191 has three high speed switching modes: quad, dual, and single. These are selected by programming the HS_SM bits of the high speed device modes register through the serial control interface.

Quad Switching Mode

This is the default mode. In quad mode, the AD8191 behaves like a 4:1 HDMI/DVI link multiplexer routing groups of four TMDS input channels to the four-channel output. This mode is accessible through both the serial and the parallel control interfaces. When using the serial control interface, the user selects which TMDS link is routed to the output by programming the HS_CH bits of the high speed device modes register in accordance with the switch mapping listed in Table 8. When using the parallel control interface, the user selects which TMDS link is routed to the output by setting the PP_CH bus of the parallel control interface in accordance with the switch mapping listed in Table 26.

Dual Switching Mode

In this mode, the AD8191 behaves as a locked dual [8:1] TMDS channel switch. The two 8:1 switches share the channel select input and, therefore, switch together. The user selects which two out of the eight possible input groups are routed to output by programming the HS_CH bits of the high speed device modes register in accordance with the switch mapping listed in Table 9. This mode is only accessible through the serial control interface.

Single Switching Mode

In this mode, the AD8191 behaves as a single 16:1 TMDS channel multiplexer; one of the 16 input channels is routed to all of the outputs. The user selects which input channel is routed to the outputs by programming the HS_CH bits in the high speed device modes register in accordance with the switch mapping listed in Table 10. This mode is only accessible through the serial control interface.

AUXILIARY SWITCH

The auxiliary (low speed) lines have no amplification. They are routed using a passive switch that is bandwidth compatible with standard speed I^2C. The schematic equivalent for this passive connection is shown in Figure 27.

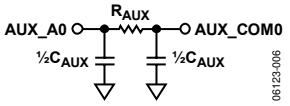

Figure 27. Auxiliary Channel Simplified Schematic, AUX_A0 to AUX_COM0 Routing Example

When turning off the AD8191, care needs to be taken with the AMUXVCC supply to ensure that the auxiliary multiplexer pins remain in a high impedance state. A scenario that illustrates this requirement is one where the auxiliary multiplexer is used to switch the display data channel (DDC) bus. In some applications, additional devices can be connected to the DDC bus (such as an EEPROM with EDID information) upstream of the AD8191. Extended display identification data (EDID) is a VESA standard-defined data format for conveying display configuration information to sources to optimize display use. EDID devices may need to be available via the DDC bus, regardless of the state of the AD8191 and any downstream circuit. For this configuration, the auxiliary inputs of the powered down AD8191 need to be in a high impedance state to avoid pulling down on the DDC lines and preventing these other devices from using the bus.

When the AD8191 is powered from a simple resistor network, as shown in Figure 28, it uses the 5 V supply that is required from any HDMI/DVI source to guarantee high impedance of

the auxiliary multiplexer pins. The AMUXVCC supply does not draw any static current; therefore, it is recommended that the resistor network tap the 5 V supplies as close to the connectors as possible to avoid any additional voltage drop.

This precaution does not need to be taken if the DDC peripheral circuitry is connected to the bus downstream of the AD8191.

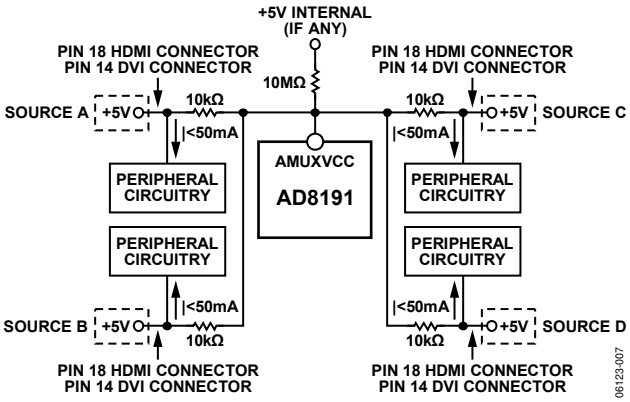

Figure 28. Suggested AMUXVCC Power Scheme

AUXILIARY (LOW SPEED) SWITCHING MODES

The AD8191 has three auxiliary switching modes: quad, dual, and single. These are selected by programming the AUX_SM bits of the auxiliary device modes register through the serial control interface. The auxiliary switching mode is independent of the high speed switching mode whenever the part is controlled through the serial control interface. When the part is controlled through the parallel control interface, however, only quad mode is accessible and the auxiliary switching mode cannot be independently controlled.

Quad Switching Mode

This is the default mode. In quad mode, the AD8191 behaves like a 4:1 auxiliary link multiplexer, routing groups of four auxiliary input signals to the four-signal output. The user can select which group of inputs is routed to the output by programming the AUX_CH bits of the auxiliary device modes register through the serial control interface in accordance with the switch mapping listed in Table 13. Alternately, the user can select which group of inputs is routed to the output by setting the PP_CH bus of the parallel control interface in accordance with the switch mapping listed in Table 27.

Dual Switching Mode

In this mode, the AD8191 behaves as a locked dual [8:1] auxiliary signal switch. The two 8:1 switches share the channel select input and, therefore, switch together. The user selects which two out of the eight possible input groups are routed to the output by programming the AUX_CH bits of the auxiliary device modes register in accordance with the switch mapping listed in Table 14. This mode is only accessible through the serial control interface.

Single Switching Mode

In this mode the AD8191 behaves as a single 16:1 TMDS channel multiplexer; a single channel, out of a possible 16, is routed to all of the outputs. The user selects which input channel is routed to the outputs by programming the AUX_CH bits of the auxiliary device modes register in accordance with the switch mapping listed in Table 15. This mode is only accessible through the serial control interface.

SERIAL CONTROL INTERFACE

RESET

On initial power-up, or at any point in operation, the AD8191 register set can be restored to preprogrammed default values by pulling the $\overline{\text{RESET}}$ pin to low in accordance with the specifications in Table 1. During normal operation, however, the $\overline{\text{RESET}}$ pin must be pulled up to 3.3 V. Following a reset, the preprogrammed default values of the AD8191 register set correspond to the state of the parallel interface configuration registers, as listed in Table 24. The AD8191 can be controlled through the parallel control interface until the first serial control event occurs. As soon as any serial control event occurs, the serial programming values, corresponding to the state of the serial interface configuration registers (Table 5), override any prior parallel programming values, and the parallel control interface is disabled until the part is subsequently reset.

WRITE PROCEDURE

To write data to the AD8191 register set, an I^2C master (such as a microcontroller) needs to send the appropriate control signals to the AD8191 slave device. The signals are controlled by the I^2C master, unless otherwise specified. For a diagram of the procedure, see Figure 29. The steps for a write procedure are as follows:

1. Send a start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low).
2. Send the AD8191 part address (seven bits). The upper four bits of the AD8191 part address are the static value [1001] and the three LSBs are set by Input Pin I2C_ADDR2, Input Pin I2C_ADDR1, and Input Pin I2C_ADDR0 (LSB). This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8191 to acknowledge the request.
5. Send the register address (eight bits) to which data is to be written. This transfer should be MSB first.
6. Wait for the AD8191 to acknowledge the request.
7. Send the data (eight bits) to be written to the register whose address was set in Step 5. This transfer should be MSB first.
8. Wait for the AD8191 to acknowledge the request.
9. Perform one of the following:
   - 9a. Send a stop condition (while holding the I2C_SCL line high, pull the I2C_SDA line high) and release control of the bus to end the transaction (shown in Figure 29).
   - 9b. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 in this procedure to perform another write.
   - 9c. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 of the read procedure (in the Read Procedure section) to perform a read from another address.
   - 9d. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 8 of the read procedure (in the Read Procedure section) to perform a read from the same address set in Step 5.

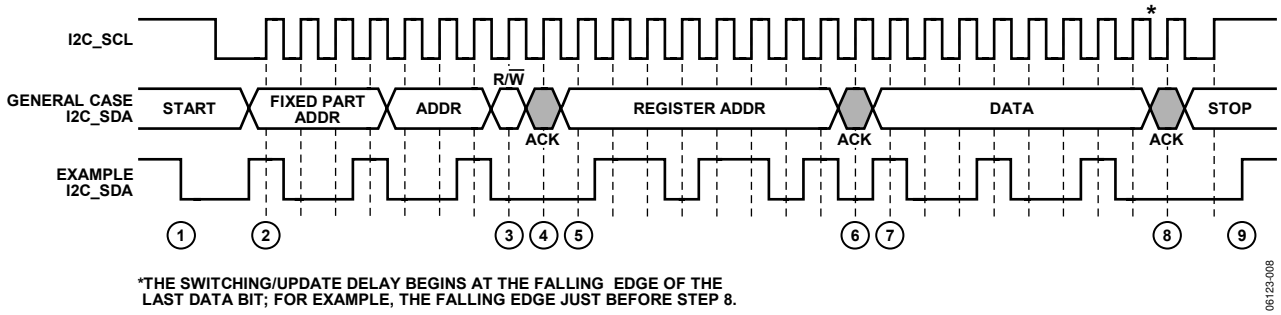

Figure 29. I^2C Write Diagram

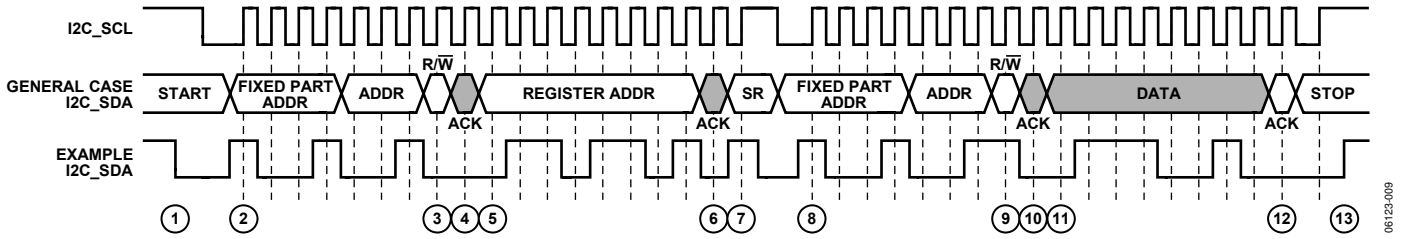

Figure 30. I²C Read Diagram

READ PROCEDURE

To read data from the AD8191 register set, an I²C master (such as a microcontroller) needs to send the appropriate control signals to the AD8191 slave device. The signals are controlled by the I²C master, unless otherwise specified. For a diagram of the procedure, see Figure 30. The steps for a read procedure are as follows:

1. Send a start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low).
2. Send the AD8191 part address (seven bits). The upper four bits of the AD8191 part address are the static value [1001] and the three LSBs are set by Input Pin I2C_ADDR2, Input Pin I2C_ADDR1, and Input Pin I2C_ADDR0 (LSB). This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8191 to acknowledge the request.
5. Send the register address (eight bits) from which data is to be read. This transfer should be MSB first.
6. Wait for the AD8191 to acknowledge the request.
7. Send a repeated start condition (Sr) by holding the I2C_SCL line high and pulling the I2C_SDA line low.
8. Resend the AD8191 part address (seven bits) from Step 2. The upper four bits of the AD8191 part address are the static value [1001] and the three LSBs are set by the Input Pin I2C_ADDR2, I2C_ADDR1 and Input Pin I2C_ADDR0 (LSB). This transfer should be MSB first.
9. Send the read indicator bit (1).
10. Wait for the AD8191 to acknowledge the request.
11. The AD8191 serially transfers the data (eight bits) held in the register indicated by the address set in Step 5. This data is sent MSB first.
12. Acknowledge the data from the AD8191.
13. Perform one of the following:

    13a. Send a stop condition (while holding the I2C_SCL line high, pull the SDA line high) and release control of the bus to end the transaction (shown in Figure 30).

    13b. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 of the write procedure (previous Write Procedure section) to perform a write.

    13c. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 of this procedure to perform a read from another address.

    13d. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 8 of this procedure to perform a read from the same address.

PARALLEL CONTROL INTERFACE

The AD8191 can be controlled through the parallel interface using the PP_EN, PP_CH[1:0], PP_EQ, PP_PRE[1:0], PP_OTO, and PP_OCL pins. Logic levels for the parallel interface pins are set in accordance with the specifications listed in Table 1. Setting these pins updates the parallel control interface registers, as listed in Table 24. Following a reset, the AD8191 can be controlled through the parallel control interface until the first serial control event occurs. As soon as any serial control event occurs, the serial programming values override any prior parallel programming values, and the parallel control interface is disabled until the part is subsequently reset. The default serial programming values correspond to the state of the serial interface configuration registers, as listed in Table 5.

SERIAL INTERFACE CONFIGURATION REGISTERS

The serial interface configuration registers can be read and written using the I²C serial control interface, Pin I2C_SDA, and Pin I2C_SCL. The least significant bits of the AD8191 I²C part address are set by tying the Pin I2C_ADDR2, Pin I2C_ADDR1, and Pin I2C_ADDR0 to 3.3 V (Logic 1) or 0 V (Logic 0). As soon as the serial control interface is used, the parallel control interface is disabled until the AD8191 is reset as described in the Serial Control Interface section.

Table 5. Serial (I²C) Interface Register Map

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr.	Default
High Speed Device Modes		High speed switch enable	High speed switching mode select		High speed source select				0x00	0x40
		HS_EN	HS_SM[1]	HS_SM[0]	HS_CH[3]	HS_CH[2]	HS_CH[1]	HS_CH[0]		
Auxiliary Device Modes		Auxiliary switch enable	Auxiliary switching mode select		Auxiliary switch source select				0x01	0x40
		AUX_EN	AUX_SM[1]	AUX_SM[0]	AUX_CH[3]	AUX_CH[2]	AUX_CH[1]	AUX_CH[0]		
Receiver Settings								High speed input termination select	0x10	0x01
								RX_TO		
Input Termination Pulse 1	Source A and Source B : input termination pulse-on-source switch select (disconnect termination for a short period of time)								0x11	0x00
	RX_PT[7]	RX_PT[6]	RX_PT[5]	RX_PT[4]	RX_PT[3]	RX_PT[2]	RX_PT[1]	RX_PT [0]		
Input Termination Pulse 2	Source C and Source D: input termination pulse-on-source switch select (disconnect termination for a short period of time)								0x12	0x00
	RX_PT[15]	RX_PT[14]	RX_PT[13]	RX_PT[12]	RX_PT[11]	RX_PT[10]	RX_PT[9]	RX_PT[8]		
Receive Equalizer 1	Source A and Source B: input equalization level select								0x13	0x00
	RX_EQ[7]	RX_EQ[6]	RX_EQ[5]	RX_EQ[4]	RX_EQ[3]	RX_EQ[2]	RX_EQ[1]	RX_EQ[0]		
Receive Equalizer 2	Source C and Source D: input equalization level select								0x14	0x00
	RX_EQ[15]	RX_EQ[14]	RX_EQ[13]	RX_EQ[12]	RX_EQ[11]	RX_EQ[10]	RX_EQ[9]	RX_EQ[8]		
Transmitter Settings					High speed output pre-emphasis level select		High speed output termination select	High speed output current level select	0x20	0x03
					TX_PE[1]	TX_PE[0]	TX_PTO	TX_OCL		

HIGH SPEED DEVICE MODES REGISTER

HS_EN: High Speed (TMDS) Channels Enable Bit

Table 6. HS_EN Description

HS_EN	Description
0	High speed channels off, low power/standby mode
1	High speed channels on

HS_SM[1:0]: High Speed (TMDS) Switching Mode Select Bus

Table 7. HS_SM Description

HS_SM[1:0]	Description
00	Quad mode, 4× [4:1]
01	Dual mode, 2× [8:1]
10	Single mode, 1× [16:1]
11	Illegal value; previous value of HS_SM[1:0] retained

HS_CH[3:0]: High Speed (TMDS) Switch Source Select Bus

Table 8. Quad Mode, 4× [4:1], High Speed Switch Mapping

HS_CH[3:0]	O[3:0]	Description
XX00	A[3:0]	High Speed Source A switched to output
XX01	B[3:0]	High Speed Source B switched to output
XX10	C[3:0]	High Speed Source C switched to output
XX11	D[3:0]	High Speed Source D switched to output

Table 9. Dual Mode, 2× [8:1], High Speed Switch Mapping

HS_CH[3:0]	O[3:2]	O[1:0]	Description
X000	A1	A0	The A0 and A1 high speed channels switched to output
X001	A3	A2	The A2 and A3 high speed channels switched to output
X010	B1	B0	The B0 and B1 high speed channels switched to output
X011	B3	B2	The B2 and B3 high speed channels switched to output
X100	C1	C0	The C0 and C1 high speed channels switched to output
X101	C3	C2	The C2 and C3 high speed channels switched to output
X110	D1	D0	The D0 and D1 high speed channels switched to output
X111	D3	D2	The D2 and D3 high speed channels switched to output

Table 10. Single Mode, 1× [16:1], High Speed Switch Mapping

HS_CH[3:0]	O[3:0]	Description
0000	A0	High Speed Channel A0 switched to output
0001	A1	High Speed Channel A1 switched to output
0010	A2	High Speed Channel A2 switched to output
0011	A3	High Speed Channel A3 switched to output
0100	B0	High Speed Channel B0 switched to output
0101	B1	High Speed Channel B1 switched to output
0110	B2	High Speed Channel B2 switched to output
0111	B3	High Speed Channel B3 switched to output
1000	C0	High Speed Channel C0 switched to output
1001	C1	High Speed Channel C1 switched to output
1010	C2	High Speed Channel C2 switched to output
1011	C3	High Speed Channel C3 switched to output
1100	D0	High Speed Channel D0 switched to output
1101	D1	High Speed Channel D1 switched to output
1110	D2	High Speed Channel D2 switched to output
1111	D3	High Speed Channel D3 switched to output

AUXILIARY DEVICE MODES REGISTER

AUX_EN: Auxiliary (Low Speed) Switch Enable Bit

Table 11. AUX_EN Description

AUX_EN	Description
0	Auxiliary switch off, no low speed input/output to low speed common input/output connection
1	Auxiliary switch on

AUX_SM[1:0]: Auxiliary (Low Speed) Switching Mode Select Bus

Table 12. AUX_SM[1:0] Description

AUX_SM[1:0]	Description
00	Quad Mode, 4× [4:1]
01	Dual Mode, 2× [8:1]
10	Single Mode, 1× [6:1]
11	Illegal value; previous value of AUX_SM[1:0] retained

AUX_CH[3:0]: Auxiliary (Low Speed) Switch Source Select Bus

Table 13. Quad Mode, 4× [4:1], Auxiliary Switch Mapping

AUX_CH[3:0]	AUX_COM[3:0]	Description
XX00	AUX_A[3:0]	Auxiliary Source A switched to output
XX01	AUX_B[3:0]	Auxiliary Source B switched to output
XX10	AUX_C[3:0]	Auxiliary Source C switched to output
XX11	AUX_D[3:0]	Auxiliary Source D switched to output

Table 14. Dual Mode, 2× [8:1], Auxiliary Switch Mapping

AUX_CH[3:0]	AUX_COM[3:2]	AUX_COM[1:0]	Description
X000	AUX_C0	AUX_A0	The A0 and C0 auxiliary channels switched to output
X001	AUX_C1	AUX_A1	The A1 and C1 auxiliary channels switched to output
X010	AUX_C2	AUX_A2	The A2 and C2 auxiliary channels switched to output
X011	AUX_C3	AUX_A3	The A3 and C3 auxiliary channels switched to output
X100	AUX_D0	AUX_B0	The B0 and D0 auxiliary channels switched to output
X101	AUX_D1	AUX_B1	The B1 and D1 auxiliary channels switched to output
X110	AUX_D2	AUX_B2	The B2 and D2 auxiliary channels switched to output
X111	AUX_D3	AUX_B3	The B3 and D3 auxiliary channels switched to output

Table 15. Single Mode, 1× [16:1], Auxiliary Switch Mapping

AUX_CH[3:0]	AUX_COM[3:0]	Description
0000	AUX_A0	Auxiliary Channel A0 switched to output
0001	AUX_A1	Auxiliary Channel A1 switched to output
0010	AUX_A2	Auxiliary Channel A2 switched to output
0011	AUX_A3	Auxiliary Channel A3 switched to output
0100	AUX_B0	Auxiliary Channel B0 switched to output
0101	AUX_B1	Auxiliary Channel B1 switched to output
0110	AUX_B2	Auxiliary Channel B2 switched to output
0111	AUX_B3	Auxiliary Channel B3 switched to output
1000	AUX_C0	Auxiliary Channel C0 switched to output
1001	AUX_C1	Auxiliary Channel C1 switched to output
1010	AUX_C2	Auxiliary Channel C2 switched to output
1011	AUX_C3	Auxiliary Channel C3 switched to output
1100	AUX_D0	Auxiliary Channel D0 switched to output
1101	AUX_D1	Auxiliary Channel D1 switched to output
1110	AUX_D2	Auxiliary Channel D2 switched to output
1111	AUX_D3	Auxiliary Channel D3 switched to output

RECEIVER SETTINGS REGISTER

RX_TO: High Speed (TMDS) Channels Input Termination On/Off Select Bit

Table 16. RX_TO Description

RX_TO	Description
0	Input termination off
1	Input termination on (can be pulsed on and off according to settings in the input termination pulse register)

INPUT TERMINATION PULSE REGISTER 1 AND REGISTER 2

RX_PT[X]: High Speed (TMDS) Input Channel X Pulse-On-Source Switch Select Bit

Table 17. RX_PT[X] Description

RX_PT[X]	Description
0	Input termination for TMDS Channel X always connected when source is switched
1	Input termination for TMDS Channel X disconnected for 100 ms when source switched

Table 18. RX_PT[X] Mapping

RX_PT[X]	Corresponding Input TMDS Channel
Bit 0	B0
Bit 1	B1
Bit 2	B2
Bit 3	B3
Bit 4	A0
Bit 5	A1
Bit 6	A2
Bit 7	A3
Bit 8	C3
Bit 9	C2
Bit 10	C1
Bit 11	C0
Bit 12	D3
Bit 13	D2
Bit 14	D1
Bit 15	D0

RECEIVE EQUALIZER REGISTER 1 AND REGISTER 2

RX_EQ[X]: High Speed (TMDS) Input X Equalization Level Select Bit

Table 19. RX_EQ[X] Description

RX_EQ[X]	Description
0	Low equalization (6 dB)
1	High equalization (12 dB)

Table 20. RX_EQ[X] Mapping

RX_EQ[X]	Corresponding Input TMDS Channel
Bit 0	B0
Bit 1	B1
Bit 2	B2
Bit 3	B3
Bit 4	A0
Bit 5	A1
Bit 6	A2
Bit 7	A3
Bit 8	C3
Bit 9	C2
Bit 10	C1
Bit 11	C0
Bit 12	D3
Bit 13	D2
Bit 14	D1
Bit 15	D0

TRANSMITTER SETTINGS REGISTER

TX_PE[1:0]: High Speed (TMDS) Output Pre-Emphasis Level Select Bus (For All TMDS Channels)

Table 21. TX_PE[1:0] Description

TX_PE[1:0]	Description
00	No pre-emphasis (0 dB)
01	Low pre-emphasis (2 dB)
10	Medium pre-emphasis (4 dB)
11	High pre-emphasis (6 dB)

TX_PTO: High Speed (TMDS) Output Termination On/Off Select Bit (For All Channels)

Table 22. TX_PTO Description

TX_PTO	Description
0	Output termination off
1	Output termination on

TX_OCL:High Speed (TMDS) Output Current Level Select Bit (For All Channels)

Table 23. TX_OCL Description

TX_OCL	Description
0	Output current set to 10 mA
1	Output current set to 20 mA

PARALLEL INTERFACE CONFIGURATION REGISTERS

The parallel interface configuration registers can be directly set using the PP_EN, PP_CH[1:0], PP_EQ, PP_PRE[1:0], PP_OTO, and PP_OCL pins. This interface is only accessible after the part is reset and before any registers are accessed using the serial control interface. The state of each pin is set by tying it to 3.3 V (Logic 1) or 0 V (Logic 0).

Table 24. Parallel Interface Register Map

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High Speed Device Modes		High speed switch enable	High speed switching mode select (quad)		High speed source select			
		PP_EN	0	0	0	0	PP_CH[1]	PP_CH[0]
Auxiliary Device Modes		Auxiliary switch enable	Auxiliary switching mode select (quad)		Auxiliary switch source select			
		1	0	0	0	0	PP_CH[1]	PP_CH[0]
Receiver Settings								Input term. on/off select (termination always on)
								1
Input Termination Pulse 1	Source A and Source B input termination pulse-on-source switch select (termination always on)							
	0	0	0	0	0	0	0	0
Input Termination Pulse 2	Source C and Source D input termination pulse-on-source switch select (termination always on)							
	0	0	0	0	0	0	0	0
Receive Equalizer 1	Source A and Source B input equalization level select							
	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ
Receive Equalizer 2	Source C and Source D input equalization level select							
	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ	PP_EQ
Transmitter Settings					Output pre-emphasis level select		Output termination on/off select	Output current level select
					PP_PE[1]	PP_PE[0]	PP_OTO	PP_OCL

HIGH SPEED DEVICE MODES REGISTER

The high speed (TMDS) switching mode is fixed to quad mode when using the parallel interface.

PP_EN: High Speed (TMDS) Channels Enable Bit

Table 25. PP_EN Description

PP_EN	Description
0	High speed channels off, low power/standby mode
1	High speed channels on

PP_CH[1:0]: High Speed (TMDS) Switch Source Select Bus

Table 26. Quad High speed Switch Mode Mapping

PP_CH[1:0]	O[3:0]	Description
00	A[3:0]	High Speed Source A switched to output
01	B[3:0]	High Speed Source B switched to output
10	C[3:0]	High Speed Source C switched to output
11	D[3:0]	High Speed Source D switched to output

AUXILIARY DEVICE MODES REGISTER

The auxiliary (low speed) switch is always enabled and the auxiliary switching mode is fixed to quad mode when using the parallel interface.

PP_CH[1:0]: Auxiliary Switch Source Select Bus

Table 27. Quad Auxiliary Switch Mode Mapping

PP_CH[1:0]	AUX_COM[3:0]	Description
00	AUX_A[3:0]	Auxiliary Source A switched to output
01	AUX_B[3:0]0	Auxiliary Source B switched to output
10	AUX_C[3:0]	Auxiliary Source C switched to output
11	AUX_D[3:0]	Auxiliary Source D switched to output

RECEIVER SETTINGS REGISTER

High speed (TMDS) channels input termination is fixed to on when using the parallel interface.

INPUT TERMINATION PULSE REGISTER 1 AND REGISTER 2

High speed input (TMDS) channels pulse-on-source switching fixed to off when using the parallel interface.

RECEIVE EQUALIZER REGISTER 1 AND REGISTER 2

PP_EQ: High Speed (TMDS) Inputs Equalization Level Select Bit (For All TMDS Input Channels)

The input equalization cannot be set individually (per channel) when using the parallel interface; one equalization setting affects all input channels.

Table 28. PP_EQ Description

PP_EQ	Description
0	Low equalization (6 dB)
1	High equalization (12 dB)

TRANSMITTER SETTINGS REGISTER

PP_PE[1:0]: High Speed (TMDS) Output Pre-Emphasis Level Select Bus (For All TMDS Channels)

Table 29. PP_PE[1:0] Description

PP_PE[1:0]	Description
00	No pre-emphasis (0 dB)
01	Low pre-emphasis (2 dB)
10	Medium pre-emphasis (4 dB)
11	High pre-emphasis (6 dB)

PP_OTO: High Speed (TMDS) Output Termination On/Off Select Bit (For All TMDS Channels)

Table 30. PP_OTO Description

PP_OTO	Description
0	Output termination off
1	Output termination on

PP_OCL: High Speed (TMDS) Output Current Level Select Bit (For All TMDS Channels)

Table 31. TX_OCL Description

PP_OCL	Description
0	Output current set to 10 mA
1	Output current set to 20 mA