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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

2:1 HDMI/DVI Switch with Equalization and DDC/CEC Buffers

AD8192

FEATURES

2 inputs, 1 output HDMI/DVI links
HDMI 1.3a receive and transmit compliant
±7 kV HBM ESD on HDMI input pins
4 TMDS channels per link
- **Supports 250 Mbps to 2.25 Gbps data rates and beyond**
- **Supports 25 MHz to 225 MHz pixel clocks and beyond**
- **Fully buffered unidirectional inputs/outputs**
- **Switchable 50 Ω on-chip input terminations with programmable or automatic control on channel switch**
- **Equalized inputs and pre-emphasized outputs**
- **Low added jitter**
- **Output disable feature for reduced power dissipation**
- **Switched output termination for building of larger arrays**

Bidirectional and cascadable DDC buffers (SDA/SCL)
- **DDC bus logic level translation (3.3 V, 5 V)**

Bidirectional and cascadable CEC buffer with integrated pull-up resistors (27 kΩ)
Hot plug detect pulse low on channel switch
Standards compatible: DVI, HDMI 1.3a, HDCP, I²C
Serial (I²C slave) control interface
56-lead, 8 mm × 8 mm LFCSP, RoHS-compliant package

APPLICATIONS

Front panel buffer for advanced television (HDTV) sets
Standalone HDMI switcher
Multiple input displays
Projectors
A/V receivers
Set-top boxes

GENERAL DESCRIPTION

The AD8192 is a complete HDMI™/DVI link switch featuring equalized TMDS inputs and pre-emphasized TMDS outputs ideal for systems with long cable runs. The TMDS outputs can be set to a high impedance state to reduce the power dissipation and/or allow the construction of larger arrays using the wire-OR technique. The AD8192 includes bidirectional buffering for the DDC bus and CEC line, with integrated pull-up resistors for the CEC line. The AD8192 is available in a space-saving, 56-lead LFCSP surface-mount, lead-free plastic package specified to operate over the −40°C to +85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

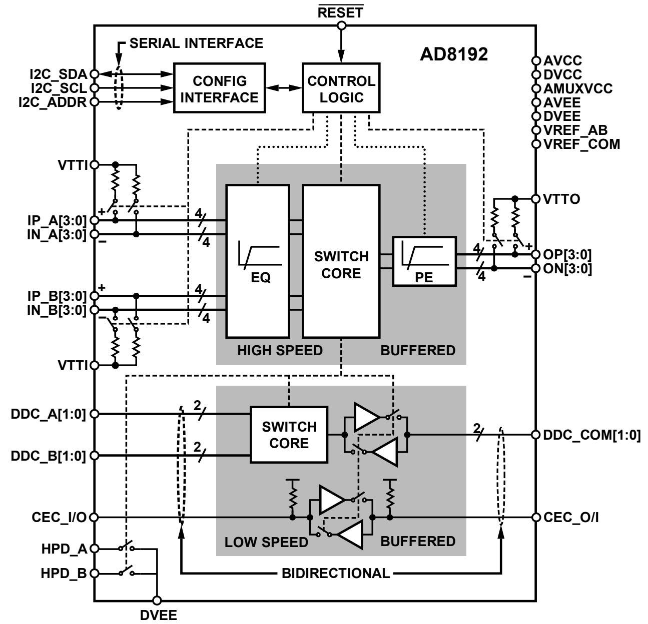

Figure 1.

TYPICAL APPLICATION

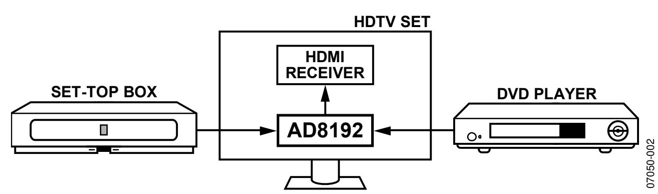

Figure 2. Typical Application for HDTV Sets

PRODUCT HIGHLIGHTS

1. Fully HDMI 1.3a transmit and receive compliant.
2. Supports data rates up to 2.25 Gbps, enabling greater than 1080p HDMI formats with deep color (12-bit) and UXGA (1600 × 1200) DVI resolutions.
3. Input cable equalizer enables use of long cables; more than 20 m (24 AWG) at data rates up to 2.25 Gbps.
4. Auxiliary switch isolates and buffers the DDC bus and the CEC line, improving total system capacitance limit.
5. Hot plug detect (HPD) signal is pulsed low on link switch.
6. Manually or automatically switched input terminations.

Advantiv™
Advanced Television Solutions by Analog Devices

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
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AD8192* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD8192 Evaluation Board

DOCUMENTATION

Data Sheet

- AD8192: 2:1 HDMI/DVI Switch with Equalization and DDC/ CEC Buffers Data Sheet

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Technical Articles

- Analysis of Common Failures of HDMI CT

DESIGN RESOURCES

- AD8192 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD8192 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

5/08—Revision 0: Initial Version

SPECIFICATIONS

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, DVCC = 3.3 V, AMUXVCC = 5 V, VREF_AB = 5 V, VREF_COM = 5 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

Table 1. TMDS Performance Specifications

Parameter	Conditions/Comments	Min	Typ	Max	Unit
TMDS DYNAMIC PERFORMANCE					
Maximum Data Rate (DR) per Channel	NRZ	2.25			Gbps
Bit Error Rate (BER)	PRBS $2^{23} - 1$			10^{-9}	
Added Data Jitter	DR ≤ 2.25 Gbps, PRBS $2^7 - 1$, no equalization		23		ps (p-p)
Added Clock Jitter			1		ps (rms)
Differential Intrapair Skew	At output		1		ps
Differential Interpair Skew	At output		30		ps
TMDS EQUALIZATION PERFORMANCE					
Receiver (Highest Setting)[1]	Boost frequency = 1.125 GHz		12		dB
Transmitter (Highest Setting)[2]	Boost frequency = 1.125 GHz		6		dB
TMDS INPUT CHARACTERISTICS					
Input Voltage Swing	Differential	150		1200	mV
Input Common-Mode Voltage (V_{ICM})		AVCC − 800		AVCC	mV
TMDS OUTPUT CHARACTERISTICS					
High Voltage Level	Single-ended high speed channel	AVCC − 200		AVCC + 10	mV
Low Voltage Level	Single-ended high speed channel	AVCC − 600		AVCC − 400	mV
Rise/Fall Time (20% to 80%)[3]	DR = 2.25 Gbps	50	90	150	ps
TMDS TERMINATION					
Input Termination Resistance	Single-ended		50		Ω
Output Termination Resistance	Single-ended		50		Ω

[1] Output meets transmitter eye diagram as defined in the DVI Standard Revision 1.0 and HDMI Standard Revision 1.3a.
[2] Cable output meets receiver eye diagram mask as defined in the DVI Standard Revision 1.0 and HDMI Standard Revision 1.3a.
[3] Output rise/fall time measurement excludes external components such as HDMI connector or external ESD protection diodes. See Applications Information section for more information.

Table 2. Auxiliary Channel Performance Specifications

Parameter	Symbol	Conditions/Comments	Min	Typ	Max	Unit
DDC CHANNELS						
Input Capacitance	C_{AUX}	DC bias = 2.5 V, ac voltage = 3.5 V p-p, f = 100 kHz		10	15	pF
Input Low Voltage	V_{IL}				0.5	V
Input High Voltage	V_{IH}		0.7 × VREF[1]			V
Output Low Voltage	V_{OL}	I_{OL} = 5 mA			0.4	V
Output High Voltage	V_{OH}			VREF[1]		V
Rise Time		10% to 90%, no capacitive load		140		ns
Fall Time		90% to 10%, C_{LOAD} = 400 pF		100	200	ns
Leakage					10	µA
CEC CHANNEL						
Input Capacitance	C_{AUX}	DC bias = 1.65 V, ac voltage = 2.5 V p-p, f = 100 kHz		5	25	pF
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Output Low Voltage	V_{OL}	R_{PULLUP} = 3 kΩ to +3.3 V			0.6	V
Output High Voltage, V_{OH}			2.5	AVCC		V

Parameter	Symbol	Conditions/Comments	Min	Typ	Max	Unit
Rise Time		10% to 90%, C_{LOAD} = 1500 pF, R_{PULLUP} = 27 kΩ; or C_{LOAD} = 7200 pF, R_{PULLUP} = 3 kΩ		50	100	μs
Fall Time		90% to 10%, C_{LOAD} = 1500 pF, R_{PULLUP} = 27 kΩ; or C_{LOAD} = 7200 pF, R_{PULLUP} = 3 kΩ		5	10	μs
Leakage		Off-leakage test conditions from *HDMI Compliance Test Specification* Test ID: 8-14			1.8	μA
HOT PLUG DETECT						
Output Low Voltage	V_{OL}	R_{PULLUP} = 800 Ω to +5 V			0.4	V

[1] VREF refers to the voltage at the VREF_AB or VREF_COM pins. VREF should be at the same supply voltage as that to which the external pull-up resistors are connected.

Table 3. Power Supply and Control Logic Specifications

Parameter	Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
AVCC	Operating range (3.3 V ± 5%)	3.135	3.3	3.465	V
AMUXVCC	Operating range (5 V ± 10%)	4.5	5	5.5	V
VREF_AB		3	5	5.5	V
VREF_COM		3	5	5.5	V
QUIESCENT CURRENT					
AVCC	Outputs disabled		40	45	mA
AVCC	Outputs enabled, no pre-emphasis		60	70	mA
AVCC	Outputs enabled, maximum pre-emphasis		100	120	mA
VTTI	Input termination on[1]		40	54	mA
VTTO	Outputs enabled, output termination on		40	50	mA
	Output termination on, maximum pre-emphasis		80	100	mA
DVCC			10	15	mA
VREF_AB			1	10	μA
VREF_COM			1	10	μA
AMUXVCC			10	20	mA
POWER DISSIPATION					
	Outputs disabled		215	318	mW
	Outputs enabled, no pre-emphasis		545	765	mW
	Outputs enabled, maximum pre-emphasis		881	1200	mW
I²C® AND LOGIC INPUTS[2]					
Input High Voltage, V_{IH}	Serial interface	2.4			V
Input Low Voltage, V_{IL}	Serial interface			0.8	V
I²C AND LOGIC OUTPUTS					
Output Low Voltage, V_{OL}	Serial interface, I_{OL} = +3 mA		0.4		V

[1] Assumes that the unselected HDMI/DVI link is deactivated through the hot plug detect line, as required by the DVI Standard Revision 1.0 and HDMI Standard Revision 1.3a.
[2] The AD8192 is an I²C slave and its control interface is based on the 3.3 V I²C bus specification.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVCC to AVEE	3.7 V
DVCC to DVEE	3.7 V
DVEE to AVEE	±0.3 V
VTTI	AVCC + 0.6 V
VTTO	AVCC + 0.6 V
AMUXVCC	5.5 V
VREF_AB	5.5 V
VREF_COM	5.5 V
Internal Power Dissipation	2.41 W
High Speed Input Voltage	AVCC − 1.4 V < V_{IN} < AVCC + 0.6 V
High Speed Differential Input Voltage	2.0 V
Low Speed Input Voltage	DVEE − 0.3 V < V_{IN} < AMUXVCC + 0.6 V
I^2C Logic Input Voltage	DVEE − 0.3 V < V_{IN} < DVCC + 0.6 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature	150°C
ESD HBM Input Pins Only	±7 kV
ESD HBM All Other Pins	±1.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

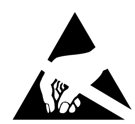
THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a four-layer JEDEC circuit board for surface-mount packages. θ_{JC} is specified for the exposed pad soldered to the circuit board with no airflow.

Table 5. Thermal Resistance

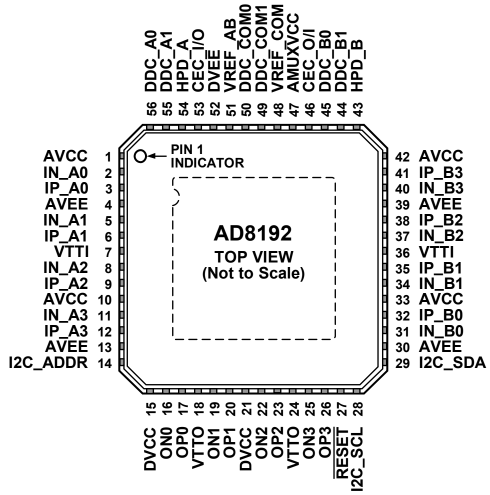
Model	θ_{JA}	θ_{JC}	Unit
56-Lead LFCSP	27	2.1	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE AD8192 LFCSP HAS AN EXPOSED PADDLE (ePAD) ON THE UNDERSIDE OF THE PACKAGE WHICH AIDS IN HEAT DISSIPATION. THE ePAD MUST BE ELECTRICALLY CONNECTED TO THE AVEE SUPPLY PLANE IN ORDER TO MEET THERMAL SPECIFICATIONS.

07050-003

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 10, 33, 42	AVCC	Power	Positive Analog Supply. 3.3 V nominal.
2	IN_A0	HS I/O	High Speed Input Complement.
3	IP_A0	HS I/O	High Speed Input.
4, 13, 30, 39, ePAD	AVEE	Power	Negative Analog Supply. 0 V nominal.
5	IN_A1	HS I/O	High Speed Input Complement.
6	IP_A1	HS I/O	High Speed Input.
7, 36	VTTI	Power	Input Termination Supply. Nominally connected to AVCC.
8	IN_A2	HS I/O	High Speed Input Complement.
9	IP_A2	HS I/O	High Speed Input.
11	IN_A3	HS I/O	High Speed Input Complement.
12	IP_A3	HS I/O	High Speed Input.
14	I2C_ADDR	Control	I^{2}C Address LSB.
15, 21	DVCC	Power	Positive Digital Power Supply. 3.3 V nominal.
16	ON0	HS I/O	High Speed Output Complement.
17	OP0	HS I/O	High Speed Output.
18, 24	VTTO	Power	Output Termination Supply. Nominally connected to AVCC.
19	ON1	HS I/O	High Speed Output Complement.
20	OP1	HS I/O	High Speed Output.
22	ON2	HS I/O	High Speed Output Complement.
23	OP2	HS I/O	High Speed Output.
25	ON3	HS I/O	High Speed Output Complement.
26	OP3	HS I/O	High Speed Output.
27	$\overline{\text{RESET}}$	Control	Configuration Registers Reset. Normally pulled to AVCC.
28	I2C_SCL	Control	I^{2}C Clock.
29	I2C_SDA	Control	I^{2}C Data.
31	IN_B0	HS I/O	High Speed Input Complement.
32	IP_B0	HS I/O	High Speed Input.
34	IN_B1	HS I/O	High Speed Input Complement.
35	IP_B1	HS I/O	High Speed Input.

Pin No.	Mnemonic	Type[1]	Description
37	IN_B2	HS I/O	High Speed Input Complement.
38	IP_B2	HS I/O	High Speed Input.
40	IN_B3	HS I/O	High Speed Input Complement.
41	IP_B3	HS I/O	High Speed Input.
43	HPD_B	LS O	Hot Plug Detect Output.
44	DDC_B1	LS I/O	Display Data Channel Input/Output.
45	DDC_B0	LS I/O	Display Data Channel Input/Output.
46	CEC_O/I	LS I/O	Consumer Electronics Control Output/Input.
47	AMUXVCC	Power	Positive Auxiliary Switch Supply. 5 V typical.
48	VREF_COM	Reference	Positive Auxiliary Switch Supply Common Side.
49	DDC_COM1	LS I/O	Display Data Channel Common Input/Output.
50	DDC_COM0	LS I/O	Display Data Channel Common Input/Output.
51	VREF_AB	Reference	Positive Auxiliary Switch Supply Source Side.
52	DVEE	Power	Negative Digital and Auxiliary Switch Power Supply. 0 V nominal.
53	CEC_I/O	LS I/O	Consumer Electronics Control Input/Output.
54	HPD_A	LS O	Hot Plug Detect Output.
55	DDC_A1	LS I/O	Display Data Channel Input/Output.
56	DDC_A0	LS I/O	Display Data Channel Input/Output.

[1] HS = high speed, LS = low speed, I = input, O = output.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS 2^7 − 1, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

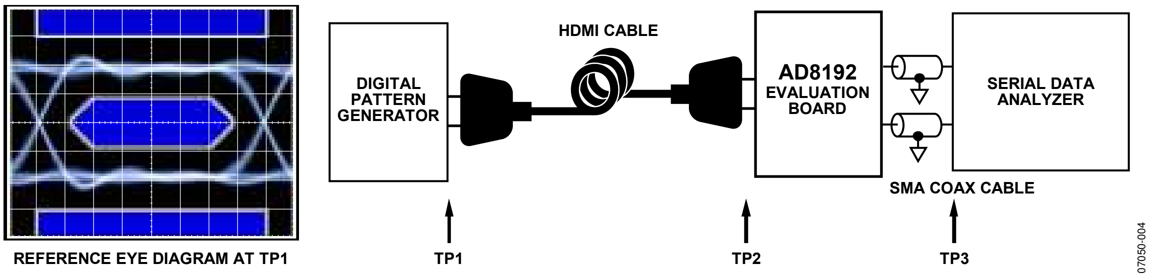


Figure 4. Test Circuit Diagram for Rx Eye Diagrams

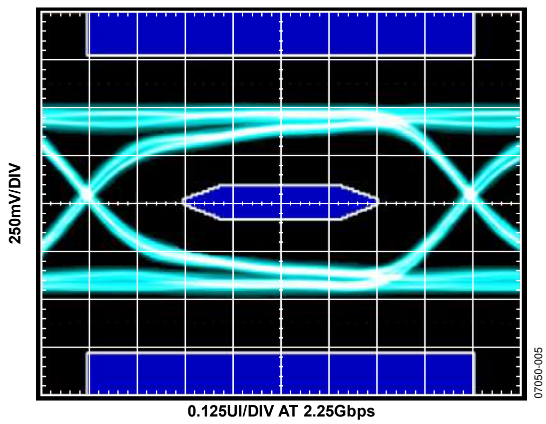


Figure 5. Rx Eye Diagram at TP2 (Cable = 2 m, 30 AWG)

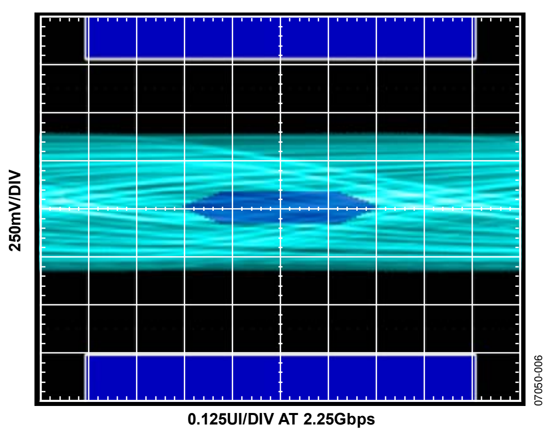


Figure 6. Rx Eye Diagram at TP2 (Cable = 20 m, 24 AWG)

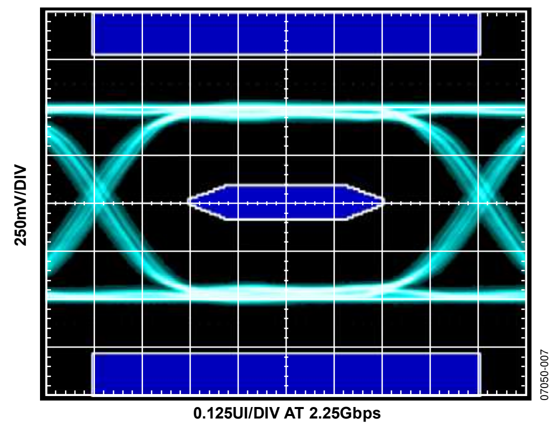


Figure 7. Rx Eye Diagram at TP3, EQ = 12 dB (Cable = 2 m, 30 AWG)

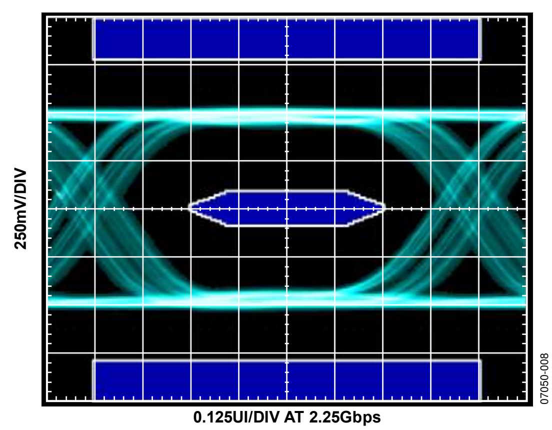


Figure 8. Rx Eye Diagram at TP3, EQ = 12 dB (Cable = 20 m, 24 AWG)

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

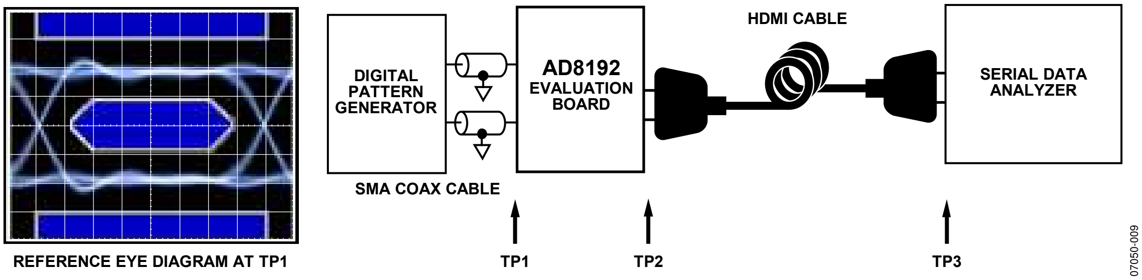


Figure 9. Test Circuit Diagram for Tx Eye Diagrams

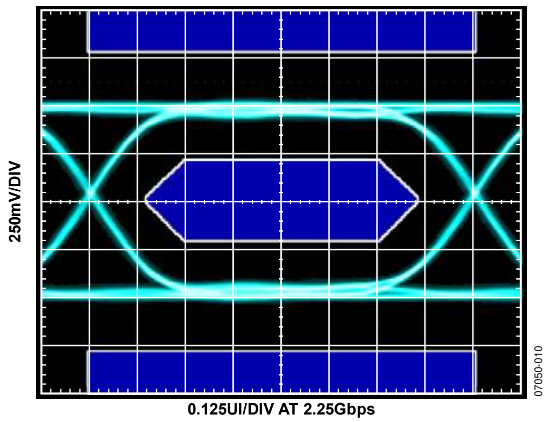


Figure 10. Tx Eye Diagram at TP2, PE = 0 dB

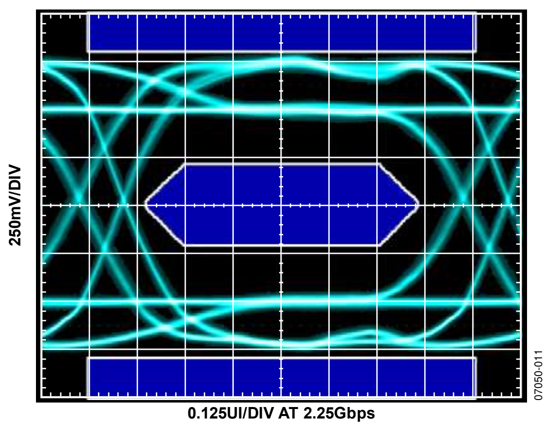


Figure 11. Tx Eye Diagram at TP2, PE = 6 dB

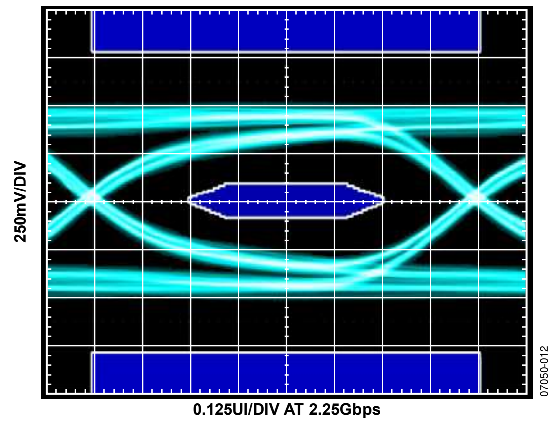


Figure 12. Tx Eye Diagram at TP3, PE = 0 dB (Cable = 2 m, 24 AWG)

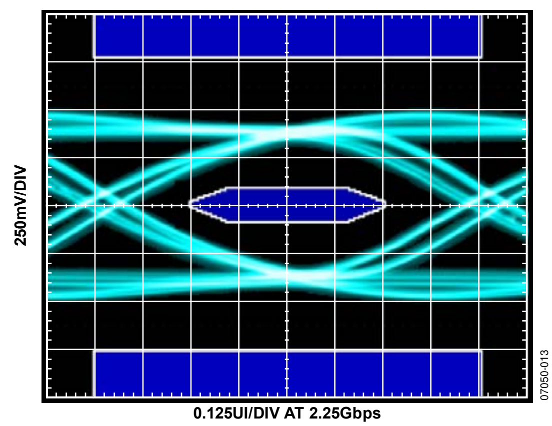


Figure 13. Tx Eye Diagram at TP3, PE = 6 dB (Cable = 10 m, 24 AWG)

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

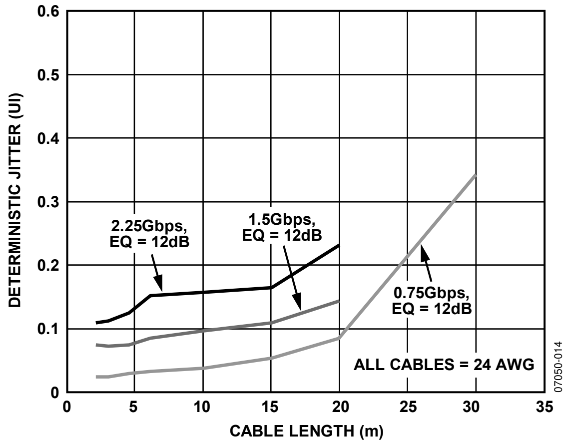


Figure 14. Jitter vs. Input Cable Length (See Figure 4 for Test Setup)

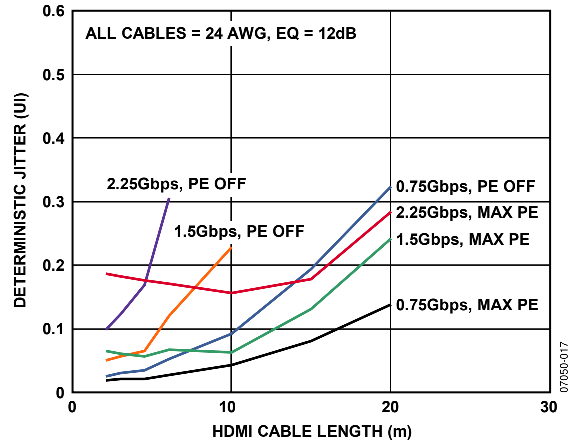


Figure 17. Jitter vs. Output Cable Length (See Figure 9 for Test Setup)

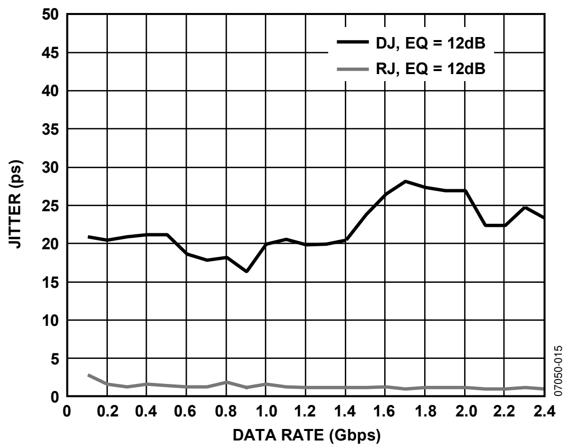


Figure 15. Jitter vs. Data Rate

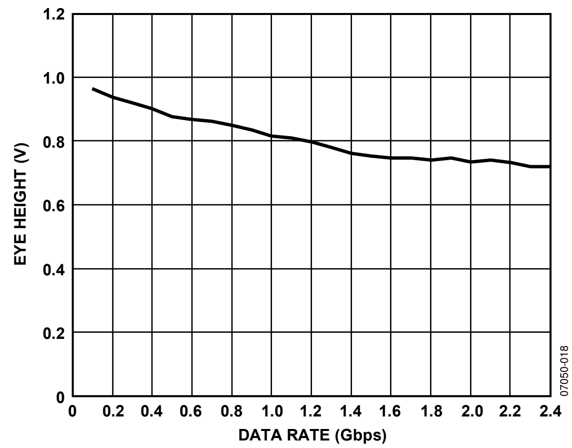


Figure 18. Eye Height vs. Data Rate

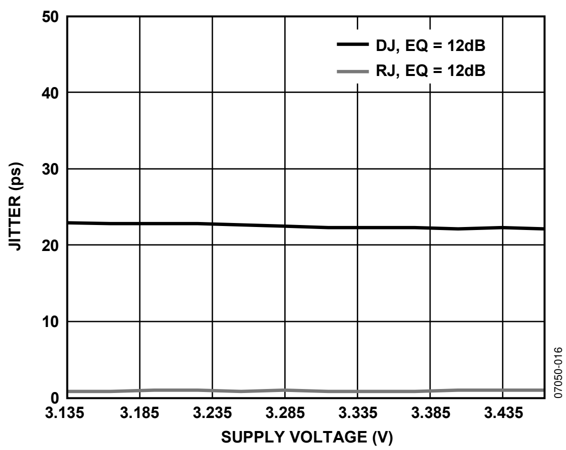


Figure 16. Jitter vs. Supply Voltage

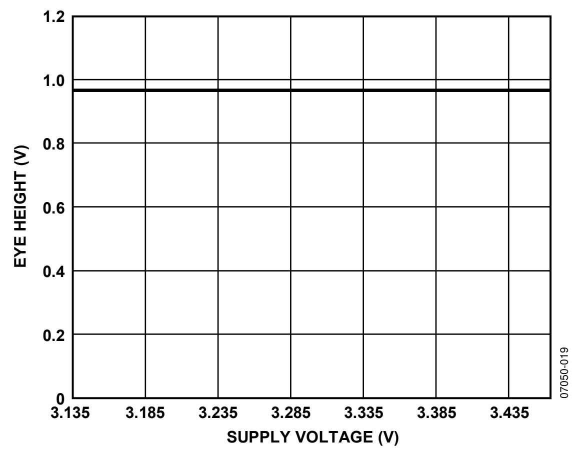


Figure 19. Eye Height vs. Supply Voltage

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, DVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

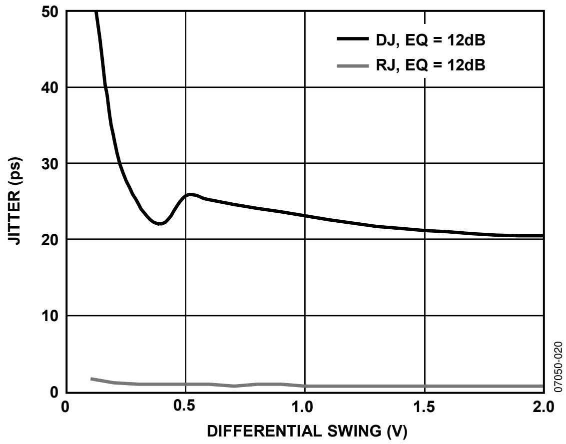


Figure 20. Jitter vs. Differential Input Swing

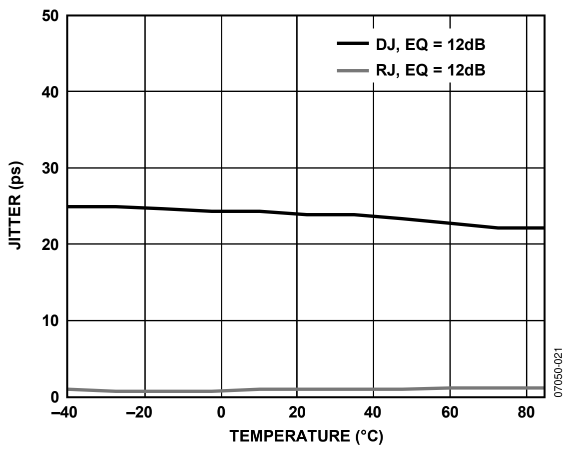


Figure 21. Jitter vs. Temperature

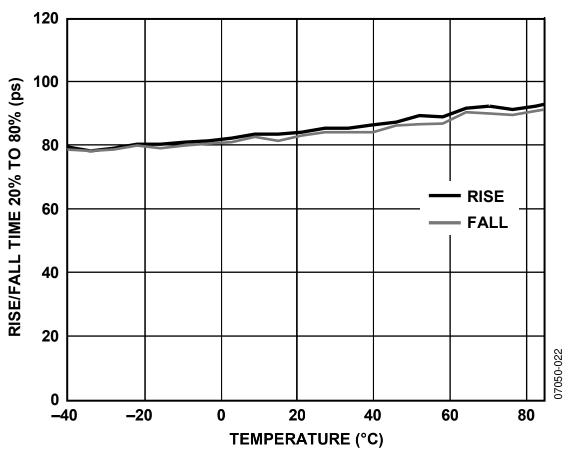


Figure 22. Rise and Fall Time vs. Temperature

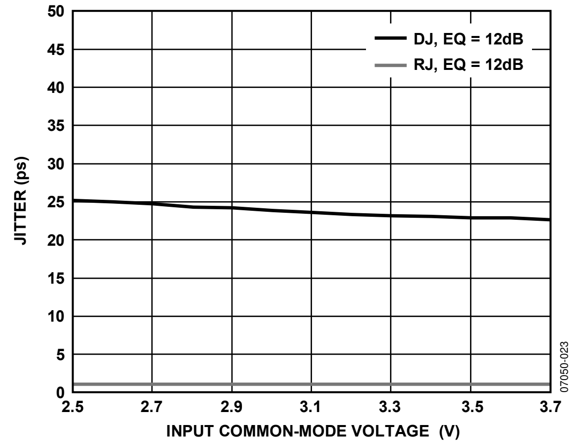


Figure 23. Jitter vs. Input Common-Mode Voltage

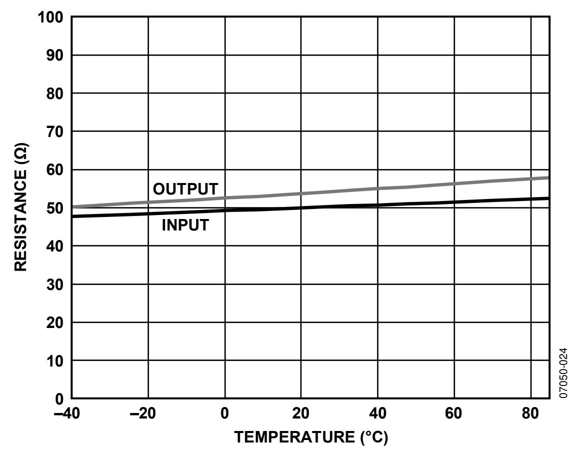


Figure 24. Single-Ended Termination Resistance vs. Temperature

THEORY OF OPERATION

The primary function of the AD8192 is to switch one of two (HDMI or DVI) single link sources to one output. Each HDMI/DVI link consists of four differential, high speed channels and four auxiliary single-ended, low speed control signals. The high speed channels include a data-word clock and three transition minimized differential signaling (TMDS) data channels running at 10× the data-word clock frequency for data rates up to 2.25 Gbps. The low speed control signals include the display data channel (DDC) bus (SDA and SCL), the consumer electronics control (CEC) line, and the hot plug detect (HPD) signal.

All four high speed TMDS channels are identical; that is, the pixel clock can be run on any of the four TMDS channels. Transmit and receive channel compensation is provided for the high speed channels where the user can (manually) select among a number of fixed settings.

The AD8192 isolates and buffers the DDC bus. It additionally isolates and buffers the CEC line and includes integrated pull-ups for the CEC line. The AD8192 also pulses the HPD signal low upon channel switching.

The AD8192 has I^2C serial programming with two user programmable I^2C slave addresses. The I^2C slave address of the AD8192 is 0b100100X. The least significant bit, represented by X in the address, is set by tying the I2C_ADDR pin to either 3.3 V (for the value X = 1) or to 0 V (for X = 0).

INPUT CHANNELS

Each high speed input differential pair terminates to the 3.3 V VTTI power supply through a pair of single-ended 50 Ω on-chip resistors, as shown in Figure 25. The state of the input terminations can be configured automatically or programmed manually through the serial control interface. The termination state is placed in the automatic mode by programming 0 in the RX_TO bit of the receiver settings register. In the automatic mode, the selected input has all terminations enabled, and the deselected input has all input terminations disabled. This state is automatically updated upon channel switching. In the manual mode, 1 is programmed into the RX_TO bit of the receiver settings register, and the state of each individual input termination is set by programming the associated RX_PT bits in the input termination control register.

The input equalizer can be manually configured to provide two different levels of high frequency boost: 6 dB or 12 dB. The equalizer level defaults to 12 dB after reset. The user can individually program the equalization level of the eight high speed input channels by selectively setting the associated RX_EQ bits in the receive equalizer register. No specific cable length is suggested for a particular equalization setting because cable performance varies widely among manufacturers; however, in general, the equalization of the AD8192 can be set to 12 dB without degrading the signal integrity, even for short input cables.

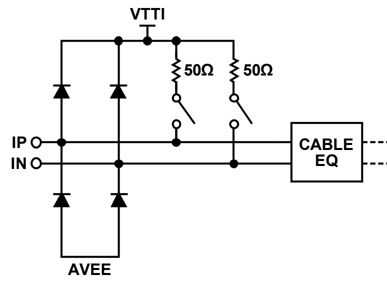


Figure 25. High Speed Input Simplified Schematic

OUTPUT CHANNELS

Each high speed output differential pair is terminated to the +3.3 V VTTO power supply through a pair of 50 Ω on-chip resistors, as shown in Figure 26. This termination is user-selectable; it can be turned on or off by programming the TX_PTO bit of the transmitter settings register.

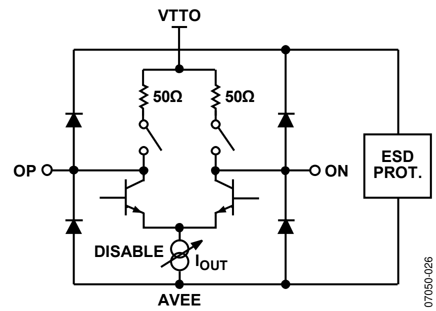


Figure 26. High Speed Output Simplified Schematic

The output termination resistors of the AD8192 back terminate the output TMDS transmission lines. These back terminations, as recommended in the HDMI 1.3a specification, act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the AD8192 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal.

The output has a disable feature that places the outputs in tristate mode (HS_EN bit of the high speed device modes register). Bigger wire-OR'ed arrays can be constructed using the AD8192 in this mode.

The AD8192 requires output termination resistors when the high speed outputs are enabled. Termination can be internal and/or external. The internal terminations of the AD8192 are enabled by programming the TX_PTO bit of the transmitter settings register (the default upon reset). External terminations can be provided either by on-board resistors or by the input termination resistors of an HDMI/DVI receiver. If both the internal terminations are enabled and external terminations are present, set the output current level to 20 mA by programming the TX_OCL bit of the transmitter settings register (the default upon reset). If only external terminations are provided (if the internal terminations are disabled), set the output current level to 10 mA by programming the TX_OCL bit of the transmitter settings register. The high speed outputs must be disabled if there are no output termination resistors present in the system.

The output equalizer (pre-emphasis) can be manually configured to provide one of four different levels of high frequency boost. The specific boost level is selected by programming the TX_PE bits of the transmitter settings register. No specific cable length is suggested for a particular pre-emphasis setting because cable performance varies widely among manufacturers.

SWITCHING MODE

The AD8192 is a 2:1 HDMI/DVI source switch. The user can select which high speed TMDS input is routed to the output by programming the HS_CH bit of the high speed modes register and which low speed DDC input/output is routed to the DDC common input/output by programming the AUX_CH bit of the auxiliary device register.

PRE-EMPHASIS

The pre-emphasized TMDS outputs precompensate the transmitted signal to account for losses in systems with long cable runs. These long cable runs selectively attenuate the high frequency energy of the signal, leading to degraded transition times and eye closure. Similar to a receive equalizer, the goal of the pre-emphasis filter is to boost the high frequency energy in the signal. However, unlike the receive equalizer, the pre-emphasis filter is applied before the channel, thus predistorting the transmitted signal to account for the loss of the channel. The series connection of the pre-emphasis filter and the channel results in a flatter frequency response than that of the channel, thereby leading to improved high frequency energy, improved transition times, and improved eye opening on the far end of the channel. Using a pre-emphasis filter for compensating channel losses allows for longer cable runs with or without a receive equalizer on the far end of the channel. When there is no receive equalizer on the far end of the channel, the pre-emphasis filter should allow longer cable runs than is acceptable with no pre-emphasis. In the case of both a pre-emphasis filter on the near end and a receive equalizer on the far end of the channel, the allowable cable run should be longer than either compensation could achieve alone. The pulse response of a pre-emphasized waveform is shown in Figure 27. The output voltage levels and symbol descriptions are listed in Table 7 and Table 8, respectively.

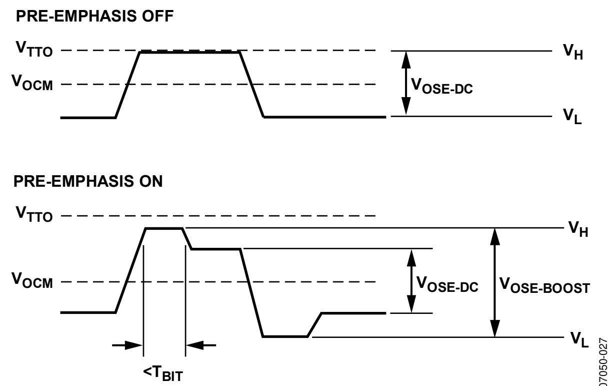


Figure 27. Pre-Emphasis Pulse Response

Table 7. Output Voltage Levels

PE Setting	OCL Setting	Boost (dB)	I_T (mA)	V_{OSE-DC} (mV p-p)	$V_{OSE-BOOST}$ (mV p-p)	DC-Coupled V_{OCM} (V)	DC-Coupled V_H (V)	DC-Coupled V_L (V)
0	0	0	10	250	250	3.175	3.3	3.050
1	0	2	12.5	250	312.5	3.144	3.3	2.988
2	0	4	15	250	375	3.133	3.3	2.925
3	0	6	20	250	500	3.050	3.3	2.8
0	1	0	20	500	500	3.050	3.3	2.8
1	1	2	25	500	625	2.988	3.3	2.675
2	1	4	30	500	750	2.925	3.3	2.550
3	1	6	40	500	1000	2.8	3.3	2.3

Table 8. Symbol Definitions

Symbol	Formula	Definition
V_{OSE-DC}	$I_T\big\vert_{PE=0} \times 25\,\Omega$ [1]	Single-ended output voltage swing after settling
$V_{OSE-BOOST}$	$I_T \times 25\,\Omega$ [1]	Boosted single-ended output voltage swing
V_{OCM} (DC-Coupled)	$VTTO - \frac{I_T}{2} \times 25\,\Omega$ [1]	Common-mode voltage when the output is dc-coupled
V_{OCM} (AC-Coupled)	$VTTO - \frac{I_T}{2} \times 50\,\Omega$	Common-mode voltage when the output is ac-coupled
V_H	$V_{OCM} + V_{OSE-BOOST}/2$	High single-ended output voltage excursion
V_L	$V_{OCM} - V_{OSE-BOOST}/2$	Low single-ended output voltage excursion

[1] The 25 Ω resistance in the equation is the parallel combination of the on-chip 50 Ω termination resistor and the external 50 Ω termination resistor.

AUXILIARY MULTIPLEXER

The auxiliary (low speed) lines provide switching and buffering for the DDC bus and buffering for the CEC line. The DDC buffers are bidirectional and fully support arbitration, clock synchronization, and other relevant features of a standard mode I^2C bus. The CEC buffer is bidirectional and includes integrated on-chip pull-up resistors.

The HPD lines going into the AD8192 are normally high impedance but are pulled low for greater than 100 ms when a channel switch occurs.

The user has the option of slaving the auxiliary line switch select to the high speed switch select by programming the AUX_LK bit of the auxiliary device register. This causes the auxiliary input channel to switch automatically when the user programs the HS_CH bit of the high speed modes register.

The unselected auxiliary inputs of the AD8192 are placed into a high impedance mode when the device is powered up and the DDC inputs of the AD8192 are high impedance when the device is powered off. This prevents contention on the DDC bus, enabling a design to include an EDID upstream of the AD8192.

DDC LOGIC LEVELS

The AD8192 supports the use of flexible (3.3 V, 5 V) logic levels on the DDC bus. The logic level for the DDC_A and DDC_B buses are set by the voltage on VREF_AB, and the logic level for the DDC_COM bus is set by the voltage on VREF_COM. For example, if the DDC_COM bus is using 5 V I^2C, then the VREF_COM power supply pin should be connected to a +5 V power supply. If the DDC_AB buses are using 3.3 V I^2C, then the VREF_AB power supply pin should be connected to a +3.3 V power supply.

INPUT/OUTPUT MAPPING CONTROL

The input/output mapping of the AD8192 is completely programmable. This allows a designer to integrate the AD8192 into virtually any application without requiring the use of vias on the TMDS traces in the PCB layout.

The user can independently control the input/output mapping of the TMDS channels for both Source A and Source B by programming the A[3:0]_HS_MAP[0:1] bits of the Source A input/output mapping register and the B[3:0]_HS_MAP[0:1] bits of the Source B input/output mapping register, respectively.

The user can independently control the polarity of the eight input channels by programming the A_SG and B_SG bits of the source sign select register. This allows a designer to invert the order of the p and n signals of a given TMDS pair inside the AD8192 instead of on the PCB.

SERIAL CONTROL INTERFACE

RESET

On initial power-up, or at any point during operation, the AD8192 register set can be restored to the default values by pulling the $\overline{\text{RESET}}$ pin to low according to the specification in Table 1. During normal operation, however, the $\overline{\text{RESET}}$ pin must be pulled up to 3.3 V.

WRITE PROCEDURE

To write data to the AD8192 register set, an I²C master (such as a microcontroller) needs to send the appropriate control signals to the AD8192 slave device. The signals are controlled by the I²C master unless otherwise specified. For a diagram of the procedure, see Figure 28. The steps for a write procedure are as follows:

1. Send a start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low).
2. Send the AD8192 part address (seven bits). The upper six bits of the AD8192 part address are the static value [100100] and the LSB is set by Input Pin I2C_ADDR. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8192 to acknowledge the request.
5. Send the register address (eight bits) to which data is to be written. This transfer should be MSB first.
6. Wait for the AD8192 to acknowledge the request.
7. Send the data (eight bits) to be written to the register whose address was set in Step 5. This transfer should be MSB first.
8. Wait for the AD8192 to acknowledge the request.
9. Do one of the following:
   a. Send a stop condition (while holding the I2C_SCL line high, pull the I2C_SDA line high) and release control of the bus to end the transaction (shown in Figure 28).
   b. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 in this procedure to perform another write.
   c. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 of the read procedure (in the Read Procedure section) to perform a read from another address.
   d. Send a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 8 of the read procedure (in the Read Procedure section) to perform a read from the same address set in Step 5.

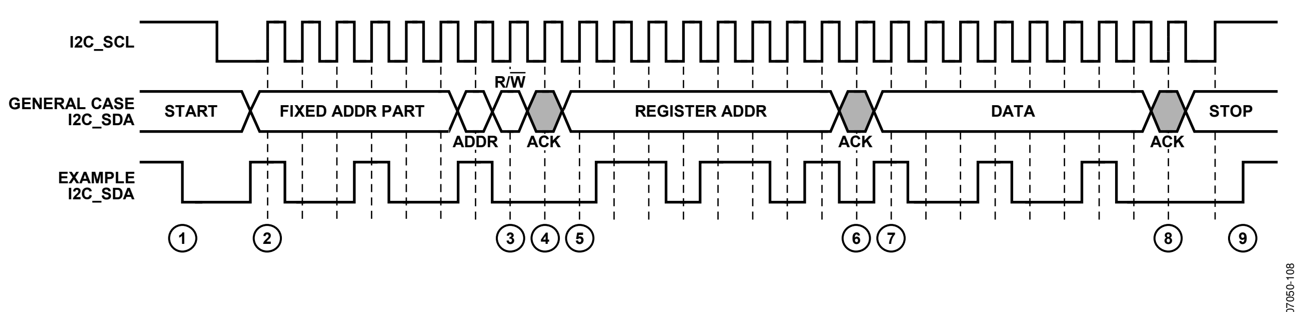


Figure 28. I²C Write Procedure

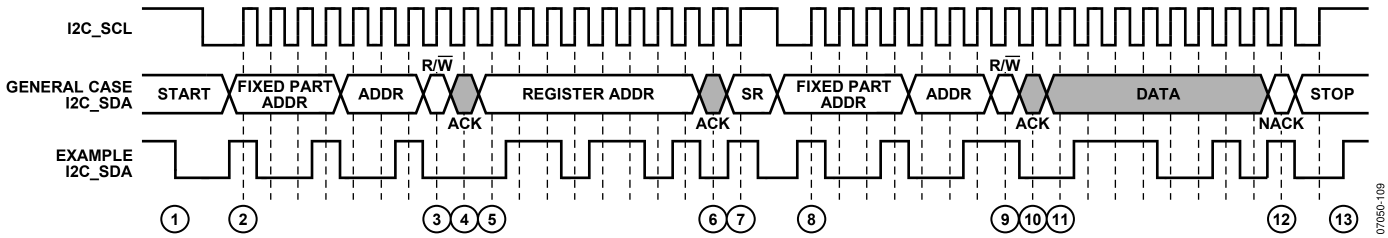


Figure 29. I²C Read Procedure

READ PROCEDURE

To read data from the AD8192 register set, an I²C master (such as a microcontroller) needs to send the appropriate control signals to the AD8192 slave device. The signals are controlled by the I²C master unless otherwise specified. For a diagram of the procedure, see Figure 29. The steps for a read procedure are as follows:

1. Send a start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low).
2. Send the AD8192 part address (seven bits). The upper six bits of the AD8192 part address are the static value [100100], and the LSB is set by Input Pin I2C_ADDR. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8192 to acknowledge the request.
5. Send the register address (eight bits) from which data is to be read. This transfer should be MSB first.
6. Wait for the AD8192 to acknowledge the request.
7. Send a repeated start condition (Sr) by holding the I2C_SCL line high and pulling the I2C_SDA line low.
8. Resend the AD8192 part address (seven bits) from Step 2. The upper six bits of the AD8192 part address compose the static value [100100]. The LSB is set by Input Pin I2C_ADDR. This transfer should be MSB first.
9. Send the read indicator bit (1).
10. Wait for the AD8192 to acknowledge the request.
    The AD8192 serially transfers the data (eight bits) held in the register indicated by the address set in Step 5. This data is sent MSB first.
11. Capture the data from the AD8192.
12. Do one of the following:
    a. Send a no acknowledge followed by a stop condition (while holding the I2C_SCL line high, pull the SDA line high) and release control of the bus to end the transaction (shown in Figure 29).
    b. Send a no acknowledge followed by a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 of the write procedure (see the previous Write Procedure section) to perform a write.
    c. Send a no acknowledge followed by a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 2 of this procedure to perform a read from another address.
    d. Send a no acknowledge followed by a repeated start condition (while holding the I2C_SCL line high, pull the I2C_SDA line low) and continue with Step 8 of this procedure to perform a read from the same address.

CONFIGURATION REGISTERS

The serial interface configuration registers can be read and written using the I²C serial interface, Pin I2C_SDA, and Pin I2C_SCL. The least significant bit of the AD8192 I²C part address is set by tying the Pin I2C_ADDR to 3.3 V (I2C_ADDR = 1b) or 0 V (I2C_ADDR = 0b).

Table 9. Register Map

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr.	Default
High Speed Device Modes		High speed switch enable						High speed source select	0x00	0x40
		HS_EN						HS_CH		
Auxiliary Device Modes	Auxiliary switch mode lock	Auxiliary switch enable						Auxiliary switch source select	0x01	0xC0
	AUX_LK	AUX_EN						AUX_CH		
Receiver Settings								Input termination control mode select	0x10	0x01
								RX_TO		
Input Termina-tion Control	Input termination select								0x11	0x00
	RX_PT[7]	RX_PT[6]	RX_PT[5]	RX_PT[4]	RX_PT[3]	RX_PT[2]	RX_PT[1]	RX_PT[0]		
Receive Equalizer	Input equalization level select								0x14	0xFF
	RX_EQ[7]	RX_EQ[6]	RX_EQ[5]	RX_EQ[4]	RX_EQ[3]	RX_EQ[2]	RX_EQ[1]	RX_EQ[0]		
Transmitter Settings					Output pre-emphasis level select		Output termination on/off select	Output current level select	0x20	0x03
					TX_PE[1]	TX_PE[0]	TX_PTO	TX_OCL		
Source Sign Control	Source B input sign select				Source A input sign select				0x80	0x00
	B_SG[3]	B_SG[2]	B_SG[1]	B_SG[0]	A_SG[3]	A_SG[2]	A_SG[1]	A_SG[0]		
Source A Input/ Output Mapping	Sourch A high speed input/output mapping								0x81	0xE4
	A3_HS_MAP[1]	A3_HS_MAP[0]	A2_HS_MAP[1]	A2_HS_MAP[0]	A1_HS_MAP[1]	A1_HS_MAP[0]	A0_HS_MAP[1]	A0_HS_MAP[0]		
Source B Input/ Output Mapping	Source B high speed input/output mapping								0x82	0xE4
	B3_HS_MAP[1]	B3_HS_MAP[0]	B2_HS_MAP[1]	B2_HS_MAP[0]	B1_HS_MAP[1]	B1_HS_MAP[0]	B0_HS_MAP[1]	B0_HS_MAP[0]		

HIGH SPEED DEVICE MODES REGISTER

HS_EN: High Speed (TMDS) Switch Enable Bit

Table 10. HS_EN Description

HS_EN	Description
0b	High speed channels off, low power/standby mode
1b	High speed channel on

HS_CH: High Speed (TMDS) Source Select Bit

Table 11. HS_CH Mapping

HS_CH	O[3:0]	Description
0b	A[3:0]	High Speed Source A switched to output
1b	B[3:0]	High Speed Source B switched to output

AUXILIARY DEVICE MODES REGISTER

AUX_LK: Auxiliary (Low Speed) Switch Mode Lock Bit

Table 12. AUX_LK Description

AUX_LK	Description
0b	Auxiliary switch lock off, auxiliary source is switched independently of the high speed source
1b	Auxiliary switch lock on, auxiliary switch source select is slaved to the high speed switch source select bit

AUX_EN: Auxiliary (Low Speed) Switch Enable Bit

Table 13. AUX_EN Description

AUX_EN	Description
0b	Auxiliary switch off, no low speed input/output to low speed common input/output connection
1b	Auxiliary switch on

AUX_CH: Auxiliary (Low Speed) Switch Source Select Bit

Table 14. AUX_CH Mapping

AUX_CH	AUX_COM[3:0]	Description
0b	AUX_A[3:0]	Auxiliary Source A switched to output
1b	AUX_B[3:0]	Auxiliary Source B switched to output

RECEIVER SETTINGS REGISTER

RX_TO: High Speed (TMDS) Input Termination Mode Control Select Bit

Table 15. RX_TO Description

RX_TO	Description
0b	Input termination mode is manual, individual terminations can be enabled/disabled according to settings in the input termination pulse register
1b	Input termination for TMDS Channel x is always connected

INPUT TERMINATION CONTROL REGISTER

RX_PT[x]: High Speed (TMDS) Input Termination x, Select Bit

Table 16. RX_PT[x] Description

RX_PT[x]	Description
0b	Input termination mode for TMDS Channel x is always disconnected
1b	Input termination for TMDS Channel x is always connected

Table 17. RX_PT[x] Mapping

RX_PT[x]	Corresponding Input TMDS Channel
Bit 0	A0
Bit 1	A1
Bit 2	A2
Bit 3	A3
Bit 4	B3
Bit 5	B2
Bit 6	B1
Bit 7	B0

RECEIVE EQUALIZER REGISTER

RX_EQ[x]: High Speed (TMDS) Input x, Equalization Level Select Bit

Table 18. RX_EQ[x] Description

RX_EQ[x]	Description
0b	Low equalization (6 dB)
1b	High equalization (12 dB)

Table 19. RX_EQ[x] Mapping

RX_EQ[x]	Corresponding Input TMDS Channel
Bit 0	A0
Bit 1	A1
Bit 2	A2
Bit 3	A3
Bit 4	B3
Bit 5	B2
Bit 6	B1
Bit 7	B0

TRANSMITTER SETTINGS REGISTER

TX_PE[x]: High Speed (TMDS) Output Pre-Emphasis Level Select Bus (For All TMDS Channels)

Table 20. TX_PE[x] Description

TX_PE[x]	Description
00b	No pre-emphasis (0 dB)
01b	Low pre-emphasis (2 dB)
10b	Medium pre-emphasis (4 dB)
11b	High pre-emphasis (6 dB)

TX_PTO: High Speed (TMDS) Output Termination On/Off Select Bit (For All Channels)

Table 21. TX_PTO Description

TX_PTO	Description
0b	Output termination off
1b	Output termination on

TX_OCL: High Speed (TMDS) Output Current Level Select Bit (For All Channels)

Table 22. TX_OCL Description

TX_OCL	Description
0b	Output current set to 10 mA
1b	Output current set to 20 mA

SOURCE SIGN CONTROL REGISTER

A_SG[x]: High Speed (TMDS) Input A, Channel x Sign Select Bits

Defines the input/input complement polarity of the Channel x.

Table 23. A_SG[x] Description

A_SG[x]	Description
0b	Channel sign is positive
1b	Channel sign is inverted

Table 24. A_SG[x] Mapping

A_SG[x]	OP[x]	ON[x]
0b	IP_A[x]	IN_A[x]
1b	IN_A[x]	IP_A[x]

B_SG[x]: High Speed (TMDS) Input B, Channel x Sign Select Bits

These bits define the input/input complement polarity of the Channel x.

Table 25. B_SG[x] Description

B_SG[x]	Description
0b	Channel sign is positive
1b	Channel sign is inverted

Table 26. B_SG[x] Mapping

B_SG[x]	OP[x]	ON[x]
0b	IP_B[x]	IN_B[x]
1b	IN_B[x]	IP_B[x]

SOURCE A INPUT/OUTPUT MAPPING REGISTER

A[x]_HS_MAP[1:0]: High Speed (TMDS) Input A, Output Channel x, Select Bits

These bits define the input/output mapping of the high speed channels when Source A is selected.

Table 27. A[x]_HS_MAP[1:0] Mapping

A[x]_HS_MAP[1:0]	O[x]
00b	A0
01b	A1
10b	A2
11b	A3

SOURCE B INPUT/OUTPUT MAPPING REGISTER

B[x]_HS_MAP[1:0]: High speed (TMDS) Input B, Output Channel x, Select Bits

These bits define the input/output mapping of the high speed channels when Source B is selected.

Table 28. B[x]_HS_MAP[1:0] Mapping

B[x]_HS_MAP[1:0]	O[x]
00b	B0
01b	B1
10b	B2
11b	B3

APPLICATIONS INFORMATION

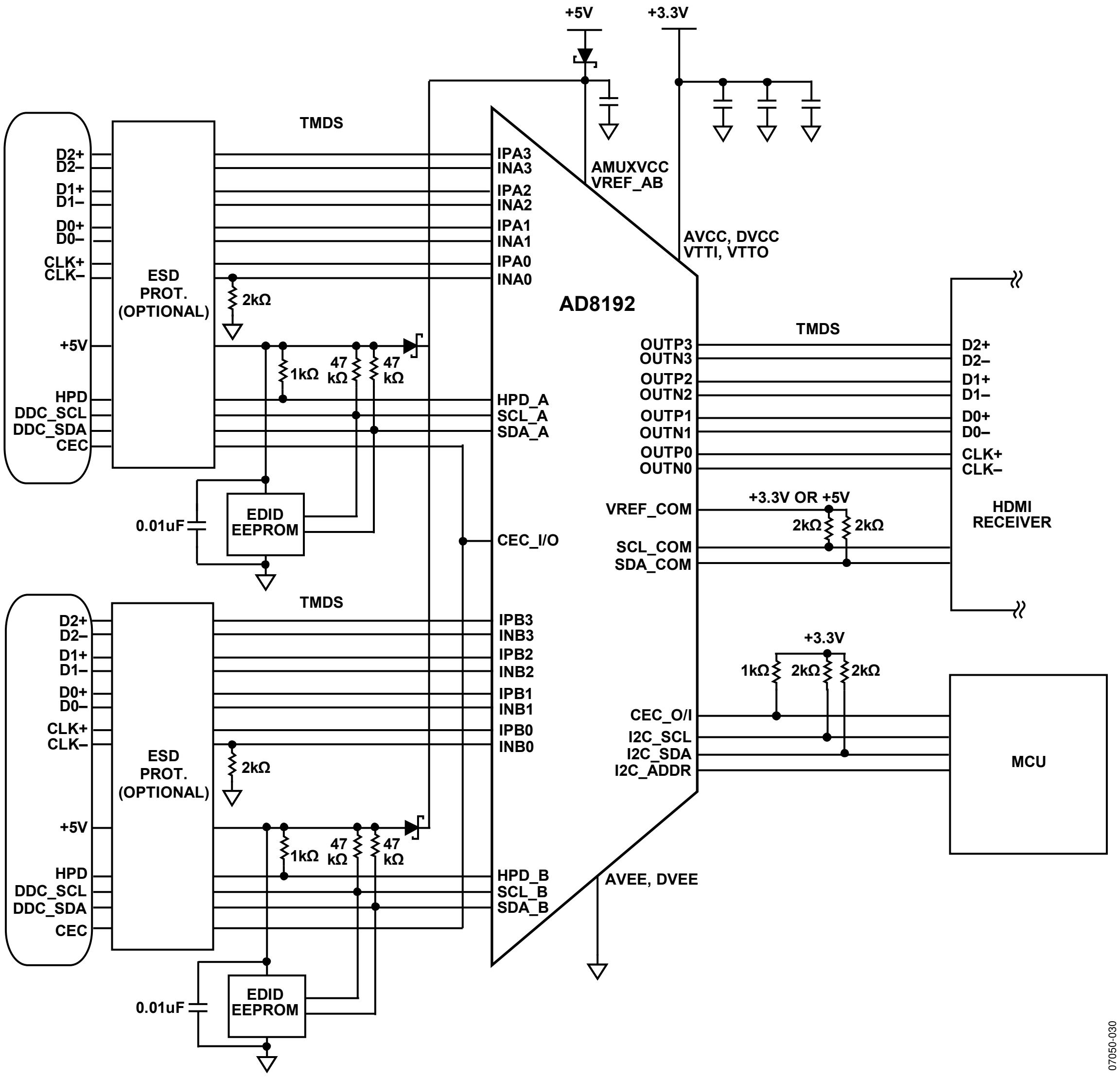


Figure 30. Typical Simplified Schematic

The AD8192 is an HDMI/DVI switch featuring equalized TMDS inputs, pre-emphasized TMDS outputs, and buffered auxiliary signals. It is intended for use as a 2:1 switch in systems with long cable runs on both the input and/or the output, and is fully HDMI 1.3a transmit and receive compliant.

PINOUT

By default, the AD8192 is designed to have an HDMI/DVI receiver pinout at its input and a transmitter pinout at its output. However, the input/output mapping of the AD8192 is completely programmable via the serial control interface. This allows a designer to integrate the AD8192 into virtually any application without requiring the use of vias on the TMDS traces in the PCB layout.

In addition to 12 dB of input equalization, the AD8192 provides up to 6 dB of output pre-emphasis that boosts the output TMDS signals and allows the AD8192 to precompensate when driving long PCB traces or output cables. The net effect of the input equalization and output pre-emphasis of the AD8192 is that the AD8192 can compensate for the signal degradation of both input and output cables; it acts to reopen a closed input data eye and transmit a full swing HDMI signal to an end receiver.

The AD8192 also provides a distinct advantage in receive-type applications because it is a fully buffered HDMI/DVI switch; the AD8192 fully buffers and electrically decouples the outputs from the inputs for both the TMDS and the auxiliary lines. Therefore, the effects of any vias placed on the output signal lines are not seen at the input of the AD8192. The programmable output terminations also improve signal quality at the output of the AD8192. Thus, the PCB designer has significantly increased flexibility in the placement and routing of the output signal path with the AD8192 over other solutions.

CABLE LENGTHS AND EQUALIZATION

The AD8192 offers two levels of programmable equalization for the high speed inputs: 6 dB and 12 dB. The equalizer of the AD8192 supports video data rates of up to 2.25 Gbps and can equalize more than 20 meters of 24 AWG HDMI cable at 2.25 Gbps, which corresponds to the video format 1080p with 12-bit deep color. The length of cable that can be used in a typical HDMI/DVI application depends on a large number of factors including

- Cable quality: the quality of the cable in terms of conductor wire gauge and shielding. Thicker conductors have lower signal degradation per unit length.
- Data rate: the data rate being sent over the cable. The signal degradation of HDMI cables increases with data rate.
- Edge rates: the edge rates of the source input. Slower input edges result in more significant data eye closure at the end of a cable.
- Receiver sensitivity: the sensitivity of the terminating receiver.

As such, specific cable types and lengths are not recommended for use with a particular equalizer setting. In nearly all applications, the AD8192 equalization level can be set to high, or 12 dB, for all input cable configurations at all data rates, without degrading the signal integrity.

TMDS OUTPUT RISE/FALL TIMES

The TMDS outputs of the AD8192 are designed for optimal performance even when external components are connected such as external ESD protection, common-mode filters, and the HDMI connector. In applications where the output of the AD8192 is connected to an HDMI output connector, additional ESD protection is recommended. The capacitance of the additional ESD protection circuits for the TMDS outputs should be as low as possible. In a typical application, the output rise/fall times are compliant with the HDMI 1.3a specification at the output of the HDMI connector.

FRONT PANEL BUFFER FOR ADVANCED TV

A front panel input provides easy access to an HDMI connector for connecting an HD camcorder or video game console to an HDTV. In designs where the main PCB is not near the side or front of the HDTV, a front panel buffer must be connected to the main board by a cable. The AD8192 enables the implementation of a front or side panel HDMI input for an HDTV by buffering the HDMI signals and compensating for the cable interconnect to the main board.

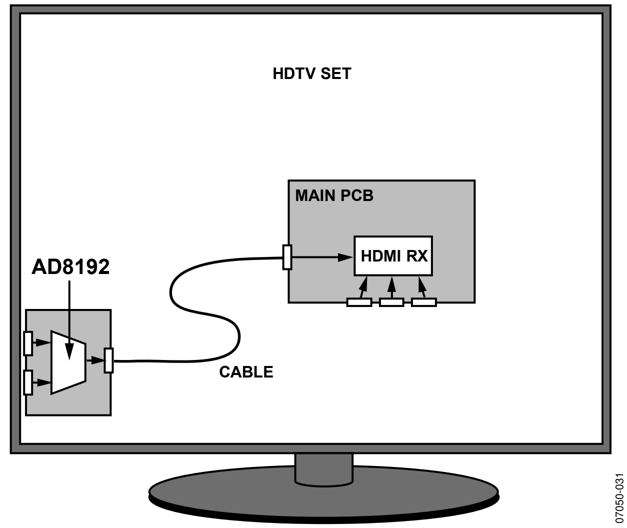


Figure 31. AD8192 as a Front Panel Buffer for an HDTV

HDMI SWITCHER

In home theatre applications where more HDMI inputs are needed, a multiple input HDMI switcher can be used to extend the number of available HDMI inputs. This switch can be contained within an audio/video receiver (AVR) or as a standalone unit. The AD8192 can be cascaded to create larger arrays as shown in Figure 32.

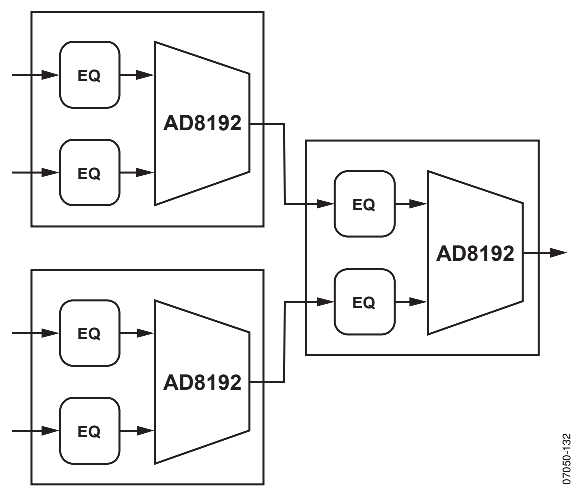


Figure 32. AD8192 Cascaded as a 4:1 HDMI Switcher

CASCADING MULTIPLE DEVICES

Unlike traditional I^2C bidirectional buffers, the DDC/CEC buffers in the AD8192 can be cascaded to create larger arrays such as those shown in Figure 32. The TMDS signals can also be cascaded, although it is important to use caution because cascading high gain equalizers can increase the output jitter beyond acceptable limits. In such cases, set the programmable equalizer in the AD8192 to low (6 dB).

PCB LAYOUT GUIDELINES

The AD8192 switches two distinctly different types of signals, both of which are required for HDMI and DVI video. These signal groups require different treatment when laying out a PCB.

The first group of signals carries the AV data. HDMI/DVI video signals are differential, unidirectional, and high speed (up to 2.25 Gbps). The channels that carry the video data must be controlled impedance, terminated at the receiver, and capable of operating up to at least 2.25 Gbps. It is especially important to note that the differential traces that carry the TMDS signals should be designed with a controlled differential impedance of 100 Ω. The AD8192 provides single-ended 50 Ω terminations on-chip for both its inputs and outputs, and both the input and output terminations can be enabled or disabled through the serial interface. Transmitter termination is not fully specified by the HDMI standard but its inclusion improves the overall system signal integrity.

The AV data carried on these high speed channels is encoded by a technique called transition minimized differential signaling (TMDS) and in the case of HDMI, is also encrypted according to the high bandwidth digital copy protection (HDCP) standard.

The second group of signals consists of low speed auxiliary control signals used for communication between a source and a sink. Depending upon the application, these signals can include the DDC bus (this is an I^2C bus used to send EDID information and HDCP encryption keys between the source and the sink), the CEC line, and the HPD line. These auxiliary signals are bidirectional, low speed, and transferred over a single-ended transmission line that does not need to have controlled impedance. The primary concern with laying out the auxiliary lines is ensuring that they conform to the I^2C bus standard and do not have excessive capacitive loading.

TMDS Signals

In the HDMI/DVI standard, four differential pairs carry the TMDS signals. In DVI, three of these pairs are dedicated to carrying RGB video and sync data. For HDMI, audio data interleaves with the video data; the DVI standard does not incorporate audio information. The fourth high speed differential pair is used for the AV data-word clock and runs at one-tenth the speed of the TMDS data channels.

The four high speed channels of each input of the AD8192 are identical. No concession was made to lower the bandwidth of the fourth channel for the pixel clock; therefore, any channel can be used for any TMDS signal. An external 2 kΩ pull-down resistor on the TMDS CLKN signal is recommended for improved noise immunity as shown in Figure 30.

The AD8192 buffers the TMDS signals and the input traces can be considered electrically independent of the output traces. In most applications, the quality of the signal on the input TMDS traces is more sensitive to the PCB layout. Regardless of the data being carried on a specific TMDS channel, or whether the TMDS line is at the input or the output of the AD8192, all four high speed signals should be routed on a PCB in accordance with the same RF layout guidelines.

Layout for the TMDS Signals

The TMDS differential pairs can be either microstrip traces (routed on the outer layer of a board) or stripline traces (routed on an internal layer of the board). If microstrip traces are used, there should be a continuous reference plane on the PCB layer directly below the traces. If stripline traces are used, they must be sandwiched between two continuous reference planes in the PCB stack up. Additionally, the p and n of each differential pair must have a controlled differential impedance of 100 Ω. The characteristic impedance of a differential pair is a function of several variables including the trace width, the distance separating the two traces, the spacing between the traces and the reference plane, and the dielectric constant of the PCB binder material. Interlayer vias introduce impedance discontinuities that can cause reflections and jitter on the signal path; therefore, it is preferable to route the TMDS lines exclusively on one layer of the board, particularly for the input traces. Additionally, to prevent unwanted signal coupling and interference, route the TMDS signals away from other signals and noise sources on the PCB.

Both traces of a given differential pair must be equal in length to minimize intrapair skew. Maintaining the physical symmetry of a differential pair is integral to ensuring its signal integrity; excessive intrapair skew can introduce jitter through duty cycle distortion (DCD). The p and n of a given differential pair should always be routed together to establish the required 100 Ω differential impedance. Leave enough space between the differential pairs of a given group to prevent the n of one pair from coupling to the p of another pair. For example, one technique is to make the interpair distance 4 to 10 times wider than the intrapair spacing.

Any one group of four TMDS traces (either Input A, Input B, or the outputs) should have closely matched trace lengths to minimize interpair skew. Severe interpair skew can cause the data on the four different channels of a group to arrive out of alignment with one another. A good practice is to match the trace lengths for a given group of four channels to within 0.05 inches on FR4 material.

Minimizing intrapair and interpair skew becomes increasingly important as data rates increase. Any introduced skew constitutes a correspondingly larger fraction of a bit period at higher data rates.

Though the AD8192 features input equalization and output pre-emphasis, minimizing the length of the TMDS traces is needed to reduce overall system signal degradation. Commonly used PCB material, such as FR4, is lossy at high frequencies, therefore, long traces on the circuit board increase signal attenuation, resulting in decreased signal swing and increased jitter through intersymbol interference (ISI).

Controlling the Characteristic Impedance of a TMDS Differential Pair

The characteristic impedance of a differential pair depends on a number of variables including the trace width, the distance between the two traces, the height of the dielectric material between the trace and the reference plane below it, and the dielectric constant of the PCB binder material. To a lesser extent, the characteristic impedance also depends upon the trace thickness and the presence of solder mask. There are many combinations that can produce the correct characteristic impedance. Generally, working with the PCB fabricator is required to obtain a set of parameters to produce the desired results.

One consideration is how to guarantee a differential pair with a differential impedance of 100 Ω over the entire length of the trace. One technique to accomplish this is to change the width of the traces in a differential pair based on how closely one trace is coupled to the other. When the two traces of a differential pair are close and strongly coupled, they should have a width that produces a100 Ω differential impedance. When the traces split apart to go into a connector, for example, and are no longer so strongly coupled, the width of the traces needs to be increased to yield a differential impedance of 100 Ω in the new configuration.

Ground Current Return

In some applications, it can be necessary to invert the output pin order of the AD8192. This requires a designer to route the TMDS traces on multiple layers of the PCB. When routing differential pairs on multiple layers, it is necessary to also reroute the corresponding reference plane to provide one continuous ground current return path for the differential signals. Standard plated through-hole vias are acceptable for both the TMDS traces and the reference plane. An example of this is illustrated in Figure 33.

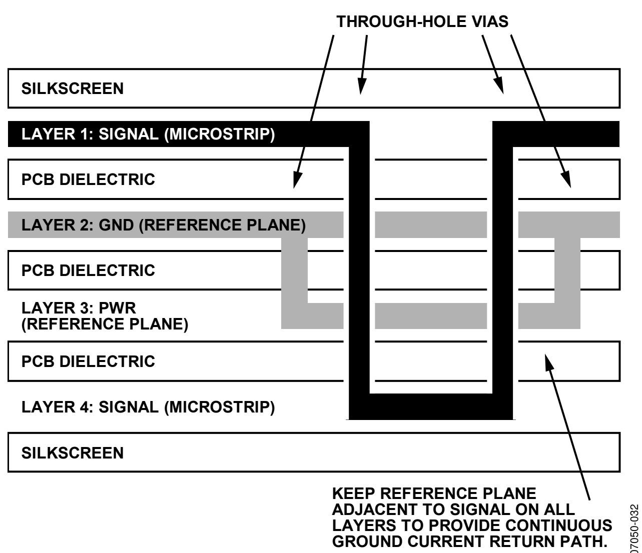


Figure 33. Example Routing of Reference Plane

TMDS Terminations

The AD8192 provides internal 50 Ω single-ended terminations for all of its high speed inputs and outputs. It is not necessary to include external termination resistors for the TMDS differential pairs on the PCB.

The output termination resistors of the AD8192 back terminate the output TMDS transmission lines. These back terminations act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the AD8192 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal.

Auxiliary Control Signals

There are four single-ended control signals associated with each source or sink in an HDMI/DVI application. These are hot plug detect (HPD), consumer electronics control (CEC), and two display data channel (DDC) lines. The two signals on the DDC bus are SDA and SCL (serial data and serial clock, respectively). The DDC and CEC signals are buffered and switched through the AD8192, and the HPD signal is pulsed low by the AD8192. These signals do not need to be routed with the same strict considerations as the high speed TMDS signals.

In general, it is sufficient to route each auxiliary signal as a single-ended trace. These signals are not sensitive to impedance discontinuities, do not require a reference plane, and can be routed on multiple layers of the PCB. However, it is best to follow strict layout practices whenever possible to prevent the PCB design from affecting the overall application. The specific routing of the HPD, CEC, and DDC lines depends upon the application in which the AD8192 is being used.

For example, the maximum speed of signals present on the auxiliary lines are 100 kHz I^2C data on the DDC lines, therefore, any layout that enables 100 kHz I^2C to be passed over the DDC bus should suffice. The HDMI 1.3a specification, however, places a strict 50 pF limit on the amount of capacitance that can be measured on either SDA or SCL at the HDMI input connector. This 50 pF limit includes the HDMI connector, the PCB, and whatever capacitance is seen at the input of the AD8192, or an equivalent receiver. There is a similar limit of 150 pF of input capacitance for the CEC line. The benefit of the AD8192 is that it buffers these lines, isolating the output capacitance so that only the capacitance at the input side contributes to the specified limit. Good board design is still required, however.

The parasitic capacitance of traces on a PCB increases with trace length. To help ensure that a design satisfies the HDMI specification, the length of the CEC and DDC lines on the PCB should be made as short as possible. Additionally, if there is a reference plane in the layer adjacent to the auxiliary traces in the PCB stackup, relieving or clearing out this reference plane immediately under the auxiliary traces significantly decreases the amount of parasitic trace capacitance. An example of the board stackup is shown in Figure 34.

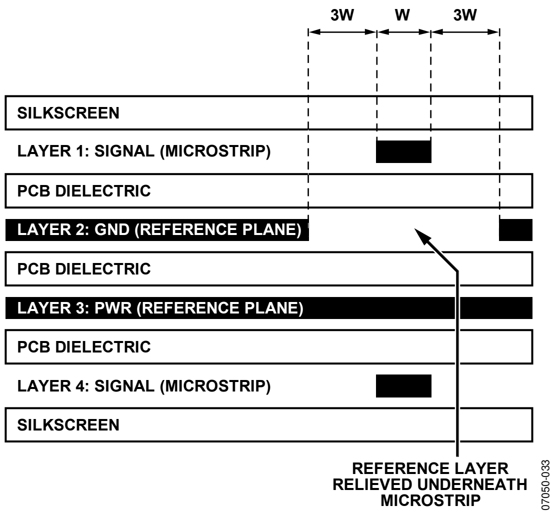


Figure 34. Example Board Stackup

HPD is a dc signal presented by a sink to a source to indicate that the source EDID is available for reading. The placement of this signal is not critical, but it should be routed as directly as possible.

When the AD8192 is powered up, the DDC/CEC inputs of the selected channel are actively buffered and routed to the outputs, and the unselected auxiliary inputs are high impedance. When the AD8192 is powered off, all DDC/CEC inputs are placed in a high impedance state. This prevents contention on the DDC bus, enabling a design to include an EDID in front of the AD8192.

Power Supplies

The AD8192 has five separate power supplies referenced to two separate grounds. The supply/ground pairs are

- AVCC/AVEE
- VTTI/AVEE
- VTTO/AVEE
- DVCC/DVEE
- AMUXVCC/DVEE
- VREF_AB/DVEE
- VREF_COM/DVEE

The AVCC/AVEE (3.3 V) and DVCC/DVEE (3.3 V) supplies power the core of the AD8192. The VTTI/AVEE supply (3.3 V) powers the input termination. Similarly, the VTTO/AVEE supply (3.3 V) powers the output termination. The AMUXVCC/ DVEE supply (3.3 V to 5 V) powers the auxiliary multiplexer core. The VREF_COM and VREF_AB supplies determine the logic levels on the corresponding DDC buses. For example, if the DDC_COM bus is using 5 V I^2C, then VREF_COM should be connected to +5 V relative to DVEE. If the DDC_AB buses are using 3.3 V I^2C, then VREF_AB should be connected to +5 V relative to DVEE.

In a typical application, connect all pins labeled AVEE or DVEE directly to ground. Likewise, connect all pins labeled AVCC, DVCC, VTTI, or VTTO to 3.3 V, and tie Pin AMUXVCC to 5 V. VREF_AB and VREF_COM can be tied to either 3.3 V or 5 V, depending on the application. The supplies can also be powered individually, but care must be taken to ensure that each stage of the AD8192 is powered correctly.

Power Supply Bypassing

The AD8192 requires minimal supply bypassing. When powering the supplies individually, place a 0.01 μF capacitor between each 3.3 V supply pin (AVCC, DVCC, VTTI, and VTTO) and ground, and place a 0.1 μF capacitor between each additional supply pin (AMUXVCC, VREF_AB, and VREF_COM) and ground to filter out supply noise. Generally, place bypass capacitors near the power pins and connect them directly to the relevant supplies (without long intervening traces). For example, to improve the parasitic inductance of the power supply decoupling capacitors, minimize the trace length between capacitor landing pads and the vias.

In applications where the AD8192 is powered by a single 3.3 V supply, it is recommended to use two reference supply planes and bypass the 3.3 V reference plane to the ground reference plane with one 220 pF, one 1000 pF, two 0.01 μF, and one 4.7 μF capacitors. If the AMUXVCC, VREF_AB, and VREF_COM connections are all powered by a single 5 V supply, it is sufficient to use a single 0.1 μF to bypass all three connections. The capacitors should via down directly to the supply planes and be placed within a few centimeters of the AD8192.