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Evaluation Board for G = 1, 2, 5, 10; 10 MHz, 20 V/µs Programmable Gain In-Amp

AD8250-EVALZ

FEATURES

Quick evaluation
On-board gain control switches
SMA connectors for high speed gain testing

GENERAL DESCRIPTION

The AD8250-EVALZ is designed to enable quick evaluation of the AD8250 programmable gain instrumentation amplifier (PGIA). The evaluation board includes on-board gain setting switches to quickly demonstrate the AD8250's software gain programmability. In addition, an external logic generator can be connected to the AD8250-EVALZ SMA ports to test the PGIA's gain control.

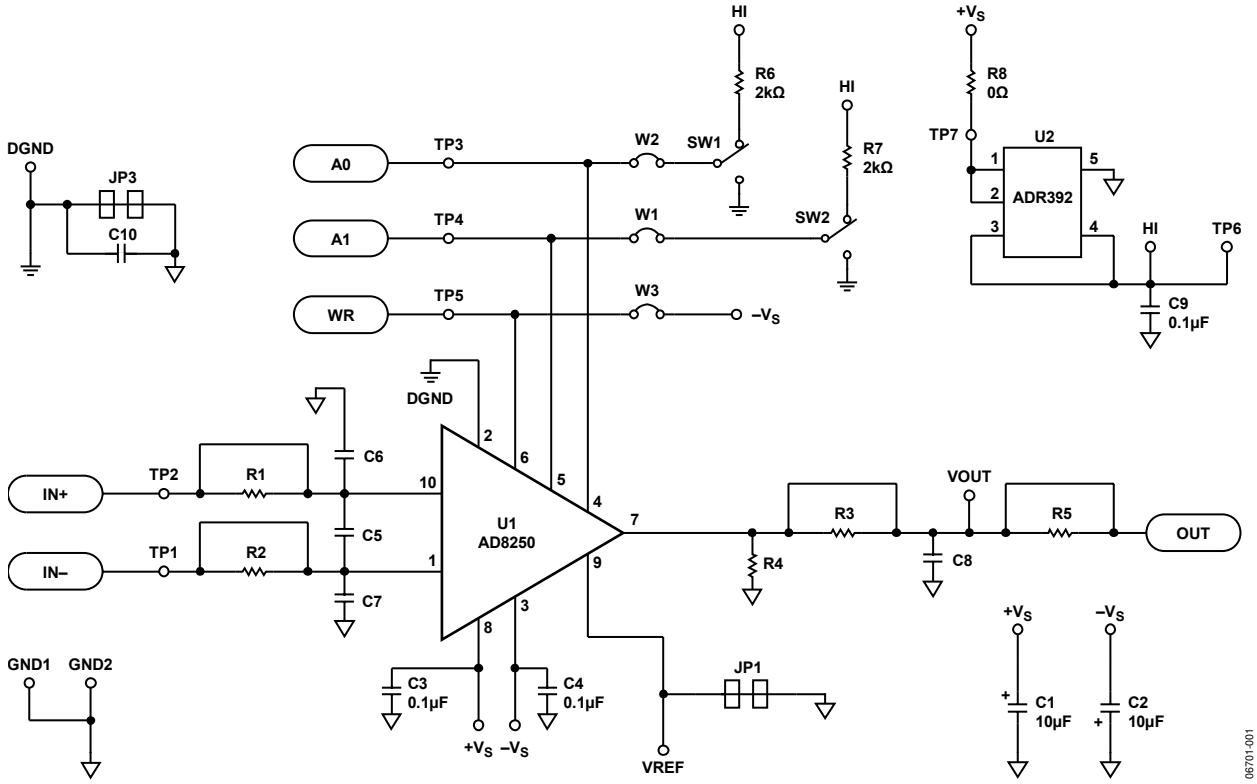

Figure 1. Schematic

Rev. 0

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EVALUATION BOARD HARDWARE

QUICK START GUIDE

By default, the AD8250-EVALZ is configured for gain change using the on-board switches, SW1 and SW2, as shown in Table 1.

Table 1. Gain Setting Using the On-Board Switches

W3 (Jumper)	SW2	SW1	Gain
In place	Low	Low	1
In place	Low	High	2
In place	High	Low	5
In place	High	High	10

Table 2. Default Settings (From the Factory)

Name	Default Status
W1, W2, W3	In place (tied)
JP1, JP3, R1, R2, R3, R5	Shorted by design (on trace)

USING EXTERNAL LOGIC TO CHANGE GAIN

The AD8250-EVALZ accepts external logic signals such as those from logic generators or FPGAs. To change gains using external logic signals, Jumpers W1, W2, and W3 must be removed. Only then will the A0, A1, and $\overline{WR}$ pins on the AD8250 be directly tied to TP3, TP4, and TP5 (and to the respective SMA connectors). External logic can be tied via the test points TP3, TP4 and TP5, or via the respective SMA connector.

TERMINATION

The AD8250-EVALZ has 50 Ω traces leading to the A0, A1, and $\overline{WR}$ pins. However, it does not have terminations to those pins. If terminations are added, remove Jumper W1, Jumper W2, and Jumper W3.

RFI FILTER

An RFI filter pattern is included at the input traces of the AD8250-EVALZ. R1 and R2 are shorted. The shorted traces must be cut before R1 and R2 are placed on the board.

OUTPUT FILTER

An output filter pattern is included at the output trace of the AD8250-EVALZ. To use R3 or R5 in a filter, cut the shorted traces prior to placing resistors in those locations.

REFERENCE

To level shift the output, a nonzero reference voltage can be applied to REF. By default, REF is tied to analog GND. Cutting the trace at JP1 opens the connection between REF and analog GND.

ANALOG AND DIGITAL GROUND

Analog and digital grounds are tied at JP3. To sever the connection between them, JP3 can be cut with a knife to open the connection between the two grounds.

GAIN SELECTION (FROM AD8250 DATA SHEET)

This section shows users how to configure the AD8250 for basic operation. Logic low and logic high voltage limits are listed in the Specifications section of the AD8250 data sheet. Typically, logic low is 0 V and logic high is 5 V; both voltages are measured with respect to DGND. Refer to the specifications table of the AD8250 for the permissible voltage range of DGND. The gain of the AD8250 can be set using two methods.

Transparent Gain Mode

The easiest way to set the gain is to program it directly via a logic high or logic low voltage applied to A0 and A1. Figure 2 shows an example of this gain setting method, referred to throughout the data sheet as transparent gain mode. Tie $\overline{WR}$ to the negative supply to engage transparent gain mode. (On the AD8250-EVALZ board, put the W3 jumper in place.) In this mode, any change in voltage applied to A0 and A1 from logic low to logic high, or vice versa, immediately results in a gain change. Table 3 is the truth table for transparent gain mode and Figure 2 shows the AD8250 configured in transparent gain mode.

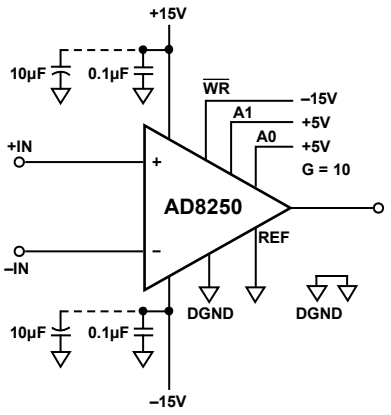

Figure 2. Transparent Gain Mode, A0 and A1 = High, G = 10

Table 3. Truth Table Logic Levels for Transparent Gain Mode

$\overline{WR}$ (W3)	A1 (SW2)	A0 (SW1)	Gain
$-V_S$ (in place)	Low	Low	1
$-V_S$ (in place)	Low	High	2
$-V_S$ (in place)	High	Low	5
$-V_S$ (in place)	High	High	10

Latched Gain Mode

Some applications have multiple programmable devices such as multiplexers or other programmable gain instrumentation amplifiers on the same PCB. In such cases, devices can share a data bus. The gain of the AD8250 can be set using $\overline{WR}$ as a latch, allowing other devices to share A0 and A1. Figure 3 shows a schematic using this method, known as latched gain mode. (On the AD8250-EVALZ, remove the W1, W2, and W3 jumpers, and drive A0, A1, and $\overline{WR}$ with external logic to test this gain setting mode.) The AD8250 is in this mode when $\overline{WR}$ is held at logic high or logic low, typically 5 V and 0 V, respectively. The voltages on A0 and A1 are read on the downward edge of the $\overline{WR}$ signal as it transitions from logic high to logic low. This latches in the logic levels on A0 and A1, resulting in a gain change. See the truth table listing in Table 4 for more information on these gain changes.

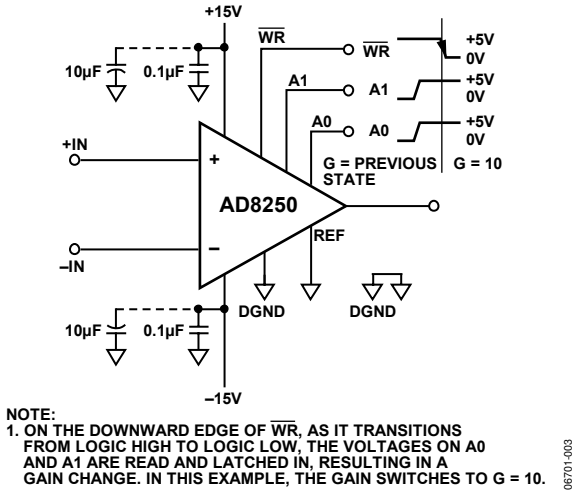

Figure 3. Latched Gain Mode, G = 10

Table 4. Truth Table Logic Levels for Latched Gain Mode

$\overline{WR}$[1]	A1[1]	A0[1]	Gain
High to low	Low	Low	Change to 1
High to low	Low	High	Change to 2
High to low	High	Low	Change to 5
High to low	High	High	Change to 10
Low to low	X[2]	X[2]	No change
Low to high	X[2]	X[2]	No change
High to high	X[2]	X[2]	No change

[1] Jumper W1, Jumper W2, and Jumper W3 must be removed and external logic must be used to test latched gain mode.
[2] X = Don't care.

On power-up, the AD8250 defaults to a gain of 1 when in latched gain mode. In contrast, if the AD8250 is configured in transparent gain mode, it starts at the gain indicated by the voltage levels on A0 and A1 upon power-up.

Timing for Latched Gain Mode

In latched gain mode, logic levels at A0 and A1 have to be held for a minimum setup time, t_{SU}, before the downward edge of $\overline{WR}$ latches in the gain. Similarly, they must be held for a minimum hold time of t_{HD} after the downward edge of $\overline{WR}$ to ensure that the gain is latched in correctly. After t_{HD}, A0 and A1 may change logic levels but the gain does not change (until the next downward edge of $\overline{WR}$). The minimum duration that $\overline{WR}$ can be held high is $t_{\overline{WR}\text{-HIGH}}$, and $t_{\overline{WR}\text{-LOW}}$ is the minimum duration that $\overline{WR}$ can be held low. Digital timing specifications are listed in the Specification section of the AD8250 data sheet. The time required for a gain change is dominated by the settling time of the amplifier. A timing diagram is shown in Figure 4.

When sharing a data bus with other devices, logic levels applied to those devices can potentially feed through to the output of the AD8250. Feedthrough can be minimized by decreasing the edge rate of the logic signals. Furthermore, careful layout of the PCB also reduces coupling between the digital and analog portions of the board.

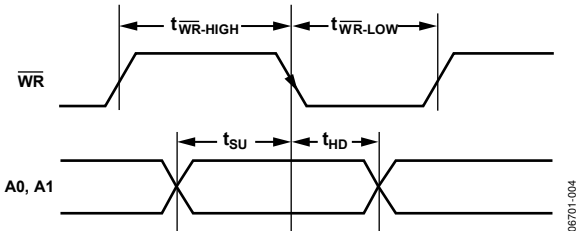

Figure 4. Timing Diagram for Latched Gain Mode

ORDERING INFORMATION

ORDERING GUIDE

Model	Package Description
AD8250-EVALZ[1]	Evaluation Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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