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Quad, 235 MHz, DC-Coupled VGA and Differential Output Amplifier

Data Sheet **AD8264**

FEATURES

- **Low noise**
  - **Voltage noise: 2.3 nV/√Hz**
  - **Current noise: 2 pA/√Hz**
- **Wide bandwidth**
  - **Small signal: 235 MHz (VGAx); 80 MHz (output amplifier)**
  - **Large signal: 80 MHz (1 V p-p)**
- **Gain range**
  - **0 to 24 dB (input to VGA output)**
  - **6 to 30 dB (input to differential output)**
- **Gain scaling: 20 dB/V**
- **DC-coupled**
- **Single-ended input and differential output**
- **Supplies: ±2.5 V to ±5 V**
- **Low power: 140 mW per channel at ±3.3 V**

APPLICATIONS

- **Multichannel data acquisition**
- **Positron emission tomography**
- **Gain trim**
- **Industrial and medical ultrasound**
- **Radar receivers**

GENERAL DESCRIPTION

The AD8264 is a quad, linear-in-dB, general-purpose variable gain amplifier (VGA) with a preamplifier (preamp), and a flexible differential output buffer. DC coupling, combined with wide bandwidth, makes this amplifier a very good pulse processor. Each channel includes a single-ended input preamp/VGA section to preserve the wide bandwidth and fast slew rate for low distortion pulse applications. A 6 dB differential output buffer with common-mode and offset adjustments enable direct coupling to most modern high speed analog-to-digital converters (ADCs), using the converter reference output for perfect dc matching levels.

The −3 dB bandwidth of the preamp/VGA is dc to 235 MHz, and the bandwidth of the differential driver is 80 MHz. The floating gain control interface provides a precise linear-in-dB scale of 20 dB/V and is easy to interface to a variety of external circuits. The gain of each channel is adjusted independently, and all channels are referenced to a single pin, GNLO. Combined with a multioutput, digital-to-analog converter (DAC), each section of the AD8264 can be used for active calibration or as a trim amplifier.

Operation from a bipolar power supply enables amplification of negative voltage pulses generated by current-sinking pulses into a grounded load, such as is typical of photodiodes or photomultiplier tubes (PMT). Delay-free processing of wideband video signals is also possible.

FUNCTIONAL BLOCK DIAGRAM

ONE CHANNEL SHOWN

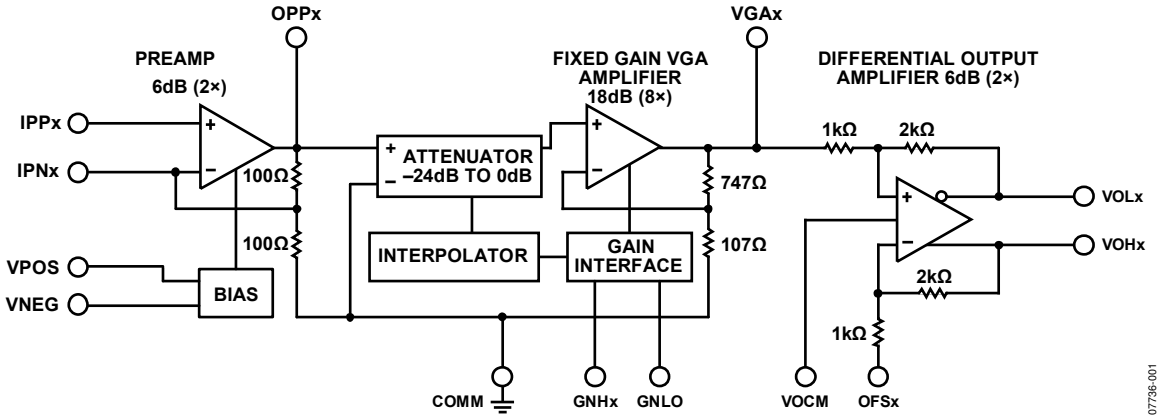

Figure 1.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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- AD8264 Evaluation Board

DOCUMENTATION

Data Sheet

- AD8264: Quad, 235 MHz, DC Coupled VGA and Differential Output Amplifier Data Sheet

DESIGN RESOURCES

- AD8264 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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Visit the product page to see pricing options.

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Submit a technical question or find your regional support number.

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5/09—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±2.5 V, T_A = 25°C, f = 10 MHz, C_L = 5 pF, R_L = 500 Ω per output (VGAx, VOHx, VOLx), V_{GAIN} = (V_{GNHx} − V_{GNLO}) = 0 V, V_{VOCM} = GND, V_{OFSx} = GND, gain range = 6 dB to 30 dB, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GENERAL PERFORMANCE					
−3 dB Small Signal Bandwidth (VGAx)	V_{OUT} = 10 mV p-p		235		MHz
−3 dB Large Signal Bandwidth (VGAx)	V_{OUT} = 1 V p-p		150		MHz
−3 dB Small Signal Bandwidth (Differential Output)[1]	V_{OUT} = 100 mV p-p		80		MHz
−3 dB Large Signal Bandwidth (Differential Output)[1]	V_{OUT} = 2 V p-p		80		MHz
Slew Rate	VGAx, V_{OUT} = 2 V p-p		380		V/µs
	VGAx, V_{OUT} = 1 V p-p		290		V/µs
	Differential output, V_{OUT} = 2 V p-p		470		V/µs
	Differential output, V_{OUT} = 1 V p-p		220		V/µs
Input Bias Current	Pins IPPx	−8	−5	−3	µA
Input Resistance	Pins IPPx at dc; $\Delta V_{IN}/\Delta I_{BIAS}$		4.2		MΩ
Input Capacitance	Pins IPPx		2		pF
Input Impedance	Pins IPPx at 10 MHz		7.9		kΩ
Input Voltage Noise			2.3		nV/√Hz
Input Current Noise			2		pA/√Hz
Noise Figure (Differential Output)	V_{GAIN} = 0.7 V, R_S = 50 Ω, unterminated		9		dB
Output-Referred Noise (Differential Output)	V_{GAIN} = 0.7 V (Gain = 30 dB)		72		nV/√Hz
	V_{GAIN} = −0.7 V (Gain = 6 dB)		45		nV/√Hz
Output Impedance	VGAx, dc to 10 MHz		3.5		Ω
	Differential output, dc to 10 MHz		<1		Ω
Output Signal Range	Preamp		$\|V_S\|$ − 1.3		V
	VGAx, R_L ≥ 500 Ω		$\|V_S\|$ − 1.3		V
	Differential amplifier, R_L ≥ 500 Ω per side		$\|V_S\|$ − 0.5		V
Output Offset Voltage	Preamp offset	−6	|<1|	+6	mV
	VGAx offset, V_{GAIN} = 0.7 V	−18	|<5|	+18	mV
	Differential output offset, V_{GAIN} = 0.7 V	−38	|<10|	+38	mV
DYNAMIC PERFORMANCE					
Harmonic Distortion	VGAx = 1 V p-p, differential output = 2 V p-p (measured at VGAx)				
HD2	f = 1 MHz		−73		dBc
HD3			−68		dBc
HD2	f = 10 MHz		−71		dBc
HD3			−61		dBc
HD2	f = 35 MHz		−60		dBc
HD3			−53		dBc
	VGAx = 1 V p-p, differential output = 2 V p-p (measured at differential output)				
HD2	f = 1 MHz		−78		dBc
HD3			−66		dBc
HD2	f = 10 MHz		−71		dBc
HD3			−43		dBc
HD2	f = 35 MHz		−56		dBc
HD3			−20		dBc
Input 1 dB Compression Point	V_{GAIN} = −0.7 V, f = 10 MHz		7		dBm[2]
	V_{GAIN} = +0.7 V, f = 10 MHz		−9.6		dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Two-Tone Intermodulation Distortion (IMD3)	VGAx = 1 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−68		dBc
	VGAx = 1 V p-p, f_1 = 35 MHz, f_2 = 36 MHz		−51		dBc
	V_{OUT} = 2 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−49		dBc
	V_{OUT} = 2 V p-p, f_1 = 35 MHz, f_2 = 36 MHz		−34		dBc
Output Third-Order Intercept	VGAx = 1 V p-p, f = 10 MHz		32		dBm
			19		dBV_{RMS}
	VGAx = 1 V p-p, f = 35 MHz		23		dBm
			10		dBV_{RMS}
	V_{OUT} = 2 V p-p, f = 10 MHz		30		dBm
			17		dBV_{RMS}
	V_{OUT} = 2 V p-p, f = 35 MHz		21		dBm
			8		dBV_{RMS}
Overload Recovery	V_{GAIN} = 0.7 V, V_{IN} stepped from 0.1 V p-p to 1 V p-p		25		ns
Group Delay Variation	1 MHz < f < 100 MHz, full gain range		±1		ns
ACCURACY					
Absolute Gain Error[3]	−0.7 V < V_{GAIN} < −0.6 V	0	0.2 to 2	3	dB
	−0.6 V < V_{GAIN} < −0.5 V	−1.25	±0.35	+1.25	dB
	−0.5 V < V_{GAIN} < +0.5 V	−1	±0.25	+1	dB
	0.5 V < V_{GAIN} < 0.6 V	−1.25	±0.35	+1.25	dB
	0.6 V < V_{GAIN} < 0.7 V	−3	−0.2 to −2	0	dB
Gain Law Conformance[4]	−0.5 V < V_{GAIN} < +0.5 V, ±2.5 V ≤ V_S ≤ ±5 V		±0.2		dB
	−0.5 V < V_{GAIN} < +0.5 V, −40°C ≤ T_A ≤ +105°C		±0.3		dB
Channel-to-Channel Matching	Single IC, −0.5 V < V_{GAIN} < +0.5 V, −40°C ≤ T_A ≤ +105°C	−0.5	±0.1 to ±0.25	+0.5	dB
	Multiple ICs, −0.5 V < V_{GAIN} < +0.5 V, −40°C ≤ T_A ≤ +105°C		±0.25		dB
GAIN CONTROL INTERFACE					
Gain Scaling Factor	−0.5 V < V_{GAIN} < +0.5 V	19.5	20.0	20.5	dB/V
Over Temperature	−40°C ≤ T_A ≤ +105°C		20 ± 0.5		dB/V
Gain Range			24		dB
Gain Intercept to VGAx		11.5	11.9	12.2	dB
Over Temperature	−40°C ≤ T_A ≤ +105°C		11.9 ± 0.4		dB
Gain Intercept to Differential Output		17.5	17.9	18.2	dB
Over Temperature	−40°C ≤ T_A ≤ +105°C		17.9 ± 0.4		dB
GNHx Input Voltage Range	GNLO = 0 V, no gain foldover	$-V_S$		$+V_S$	V
Input Resistance	$\Delta V_{IN}/\Delta I_{BIAS}$, −0.7 V < V_{GAIN} < +0.7 V		70		MΩ
GNHx Input Bias Current	−0.7 V < V_{GAIN} < 0.7 V	−0.9	−0.4	0	µA
Over Temperature	−0.7 V < V_{GAIN} < 0.7 V, −40°C ≤ T_A ≤ +105°C		−0.4 ± +0.2		µA
GNLO Input Bias Current	−0.7 V < V_{GAIN} < 0.7 V		−1.2		µA
Over Temperature	−0.7 V < V_{GAIN} < 0.7 V, −40°C ≤ T_A ≤ +105°C		−1.2 ± +0.4		µA
Response Time	24 dB gain change		200		ns
OUTPUT BUFFER					
VOCM Input Bias Current		0.3	1.5	2.5	nA
Over Temperature	−40°C ≤ T_A ≤ +105°C		1.5 ± 0.3		nA
VOCM Input Voltage Range	OFSx = 0 V, VGAx = 0 V	−1.4		+1.4	V
Gain (VGAx to Differential Output)		5.75	6	6.25	dB
Over Temperature	−40°C ≤ T_A ≤ +105°C		6 ± 0.5		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Voltage		±2.5		±5	V
Power Consumption					
Quiescent Current					
	V_S = ± 2.5 V	65	79	88	mA
	V_S = ± 2.5 V, −40°C ≤ T_A ≤ +105°C		79 ± 25		mA
	V_S = ± 3.3 V	70	85	95	mA
	V_S = ± 3.3 V, −40°C ≤ T_A ≤ +105°C		85 ± 30		mA
	V_S = ± 5 V	81	99	110	mA
	V_S = ± 5 V, −40°C ≤ T_A ≤ +85°C[5]		99 ± 30		mA
Power Dissipation	V_S = ± 2.5 V		395		mW
	V_S = ±3.3 V		560		mW
	V_S = ±5 V		990		mW
PSRR	From VPOS to differential output, V_{GAIN} = 0.7 V		−15		dB
	From VNEG to differential output, V_{GAIN} = 0.7 V		−15		dB

[1] Differential Output = (VOHx − VOLx).
[2] All dBm values are calculated with 50 Ω reference, unless otherwise noted.
[3] Conformance to theoretical gain expression (see Equation 1 in the Theory of Operation section).
[4] Conformance to best-fit dB linear curve.
[5] For supplies greater than ±3.3 V, the operating temperature range is limited to −40°C ≤ T_A ≤ +85°C.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply Voltage (VPOS, VNEG)	±6 V
Input Voltage (INPx)	VPOS, VNEG
Gain Voltage (GNHx, GNLO)	VPOS, VNEG
Power Dissipation	2.5 W
Temperature	
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Package Glass Transition Temperature (T_G)	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA} values in Table 3 assume a 4-layer JEDEC standard board with zero airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP[1]	31.0	2.3	°C/W

[1] 4-Layer JEDEC board (2S2P).

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8264 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 150°C for an extended period can cause changes in silicon devices, potentially resulting in a loss of functionality.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

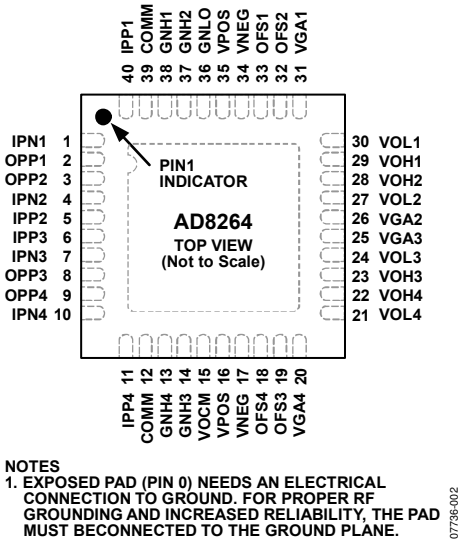

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
0 (EP), 12, 39	COMM	Ground. Exposed pad (EP, Pin 0) needs an electrical connection to ground. For proper RF grounding and increased reliability, the pad must be connected to the ground plane.
1, 4, 7, 10	IPN1, IPN2, IPN3, IPN4	Negative Preamp Inputs for Channel 1 Through Channel 4. Normally, no external connection is needed.
2, 3, 8, 9	OPP1, OPP2, OPP3, OPP4	Preamp Output for Channel 1 Through Channel 4. This pin is internally connected to the attenuator (VGA) input, and normally, no external connection is needed.
5, 6, 11, 40	IPP1, IPP2, IPP3, IPP4	Positive Preamp Input for Channel 1 Through Channel 4. High impedance.
13, 14, 37, 38	GNH1, GNH2, GNH3, GNH4	Positive Gain Control Voltage Input for Channel 1 Through Channel 4. This pin is referenced to GNLO (Pin 36).
15	VOCM	This pin sets the differential output amplifier (VOHx and VOLx) common-mode voltage.
16, 35	VPOS	Positive Supply (Internally Tied Together).
17, 34	VNEG	Negative Supply (Internally Tied Together).
18, 19, 32, 33	OFS1, OFS2, OFS3, OFS4	Voltage sets the differential output offset for Channel 1 through Channel 4. This is the noninverting input to the differential amplifier, and it has the same bandwidth as the inverting input (VGAx).
20, 25, 26, 31	VGA4, VGA3 VGA2, VGA1	VGA Output for Channel 1 Through Channel 4.
21, 24, 27, 30	VOL1, VOL2 VOL3, VOL4	Negative Differential Amplifier Output for Channel 1 Through Channel 4.
22, 23, 28, 29	VOH1, VOH2, VOH3, VOH4	Positive Differential Amplifier Output for Channel 1 Through Channel 4.
36	GNLO	Negative Gain Control Input (Reference for GNHx Pins).

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±2.5 V, T_A = 25°C, f = 10 MHz, C_L = 5 pF, R_L = 500 Ω per output (VGAx, VOHx, VOLx), V_{GAIN} = (V_{GNHx} − V_{GNLO}) = 0 V, V_{VOCM} = GND, V_{OFSx} = GND, gain range = 6 dB to 30 dB, unless otherwise specified.

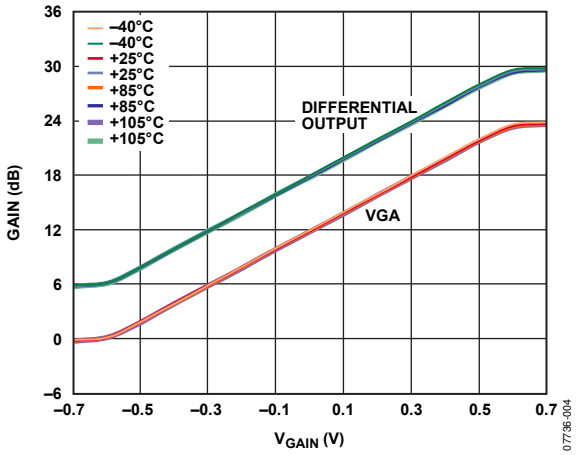

Figure 3. Gain vs. V_{GAIN} vs. Temperature

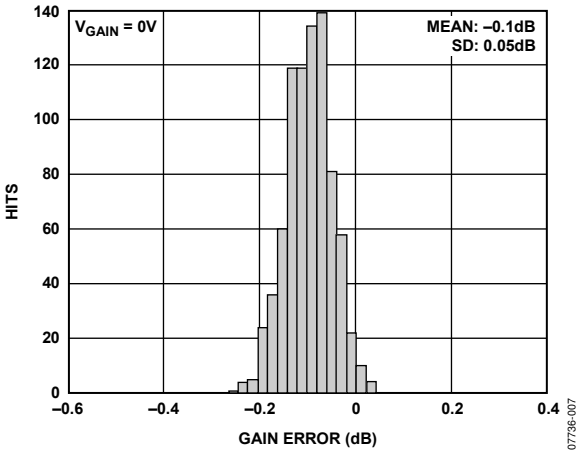

Figure 6. VGA Absolute Gain Error Histogram

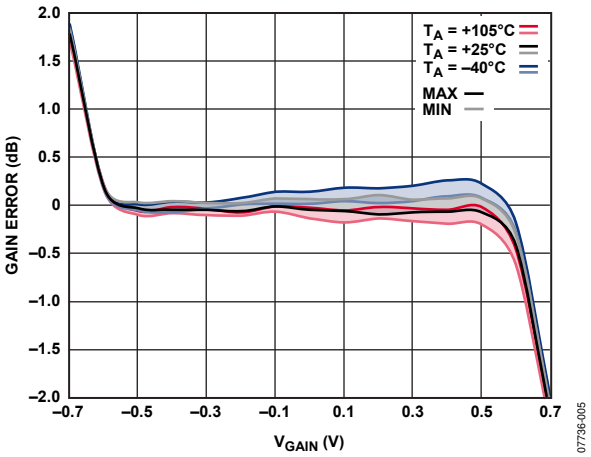

Figure 4. Gain Error vs. V_{GAIN} vs. Temperature

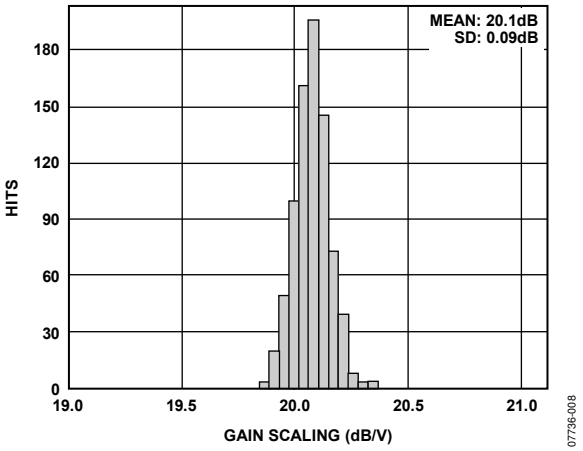

Figure 7. Gain Scale Factor Histogram (–0.4 V < V_{GAIN} < +0.4 V)

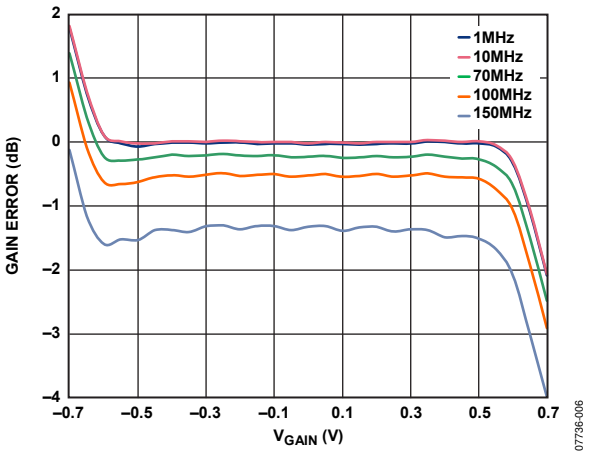

Figure 5. Gain Error vs. V_{GAIN} at Various Frequencies to VGAx

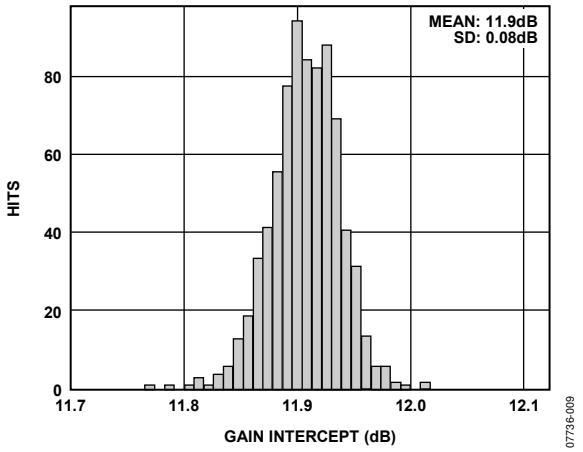

Figure 8. VGA Gain Intercept Histogram

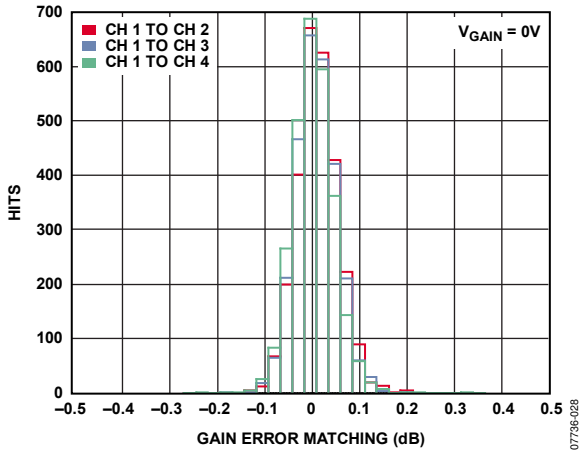

Figure 9. Channel-to-Channel Gain Match Histogram

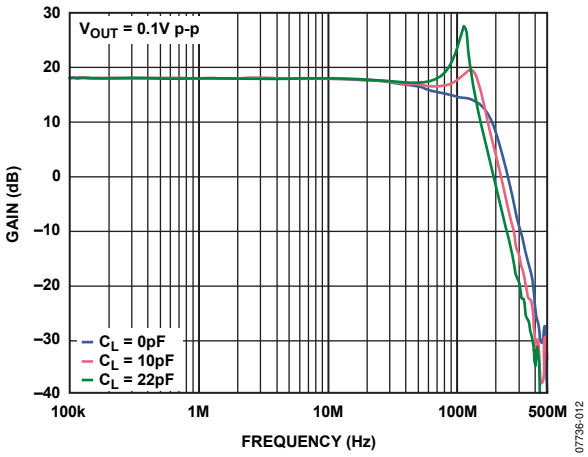

Figure 12. Frequency Response to Differential Output for Various Capacitive Loads

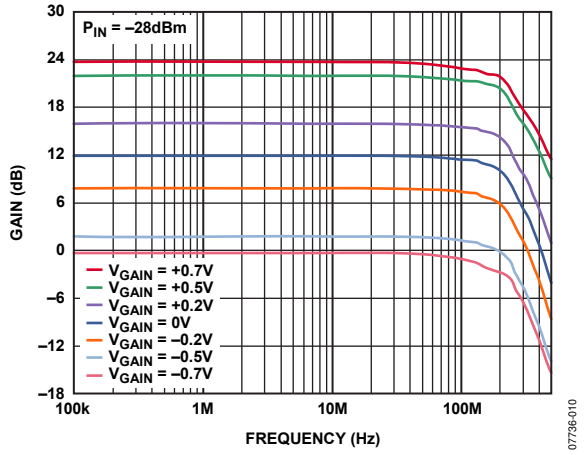

Figure 10. Frequency Response vs. Gain to VGAx for Various Values of V_{GAIN}

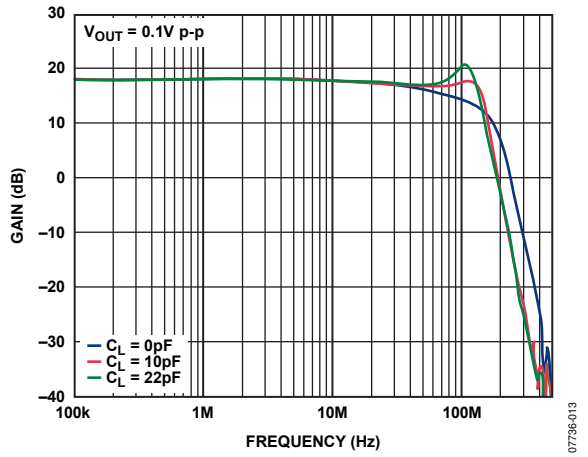

Figure 13. Frequency Response to Differential Output for Various Capacitive Loads with Series R = 10 Ω

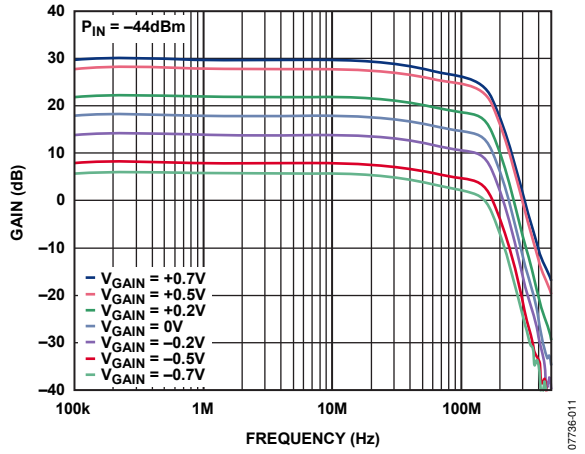

Figure 11. Frequency Response vs. Gain to Differential Output for Various Values of V_{GAIN}

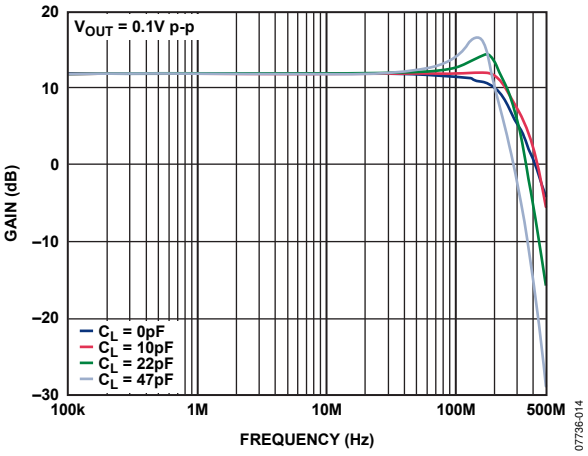

Figure 14. Small Signal Frequency Response to VGAx for Various Capacitive Loads

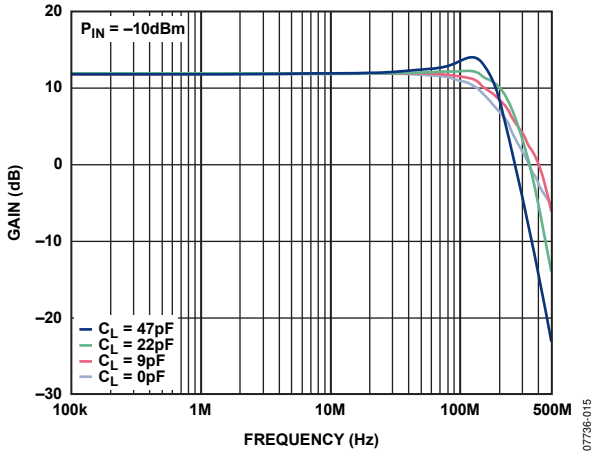

Figure 15. Large Signal Frequency Response to VGAx for Various Capacitive Loads

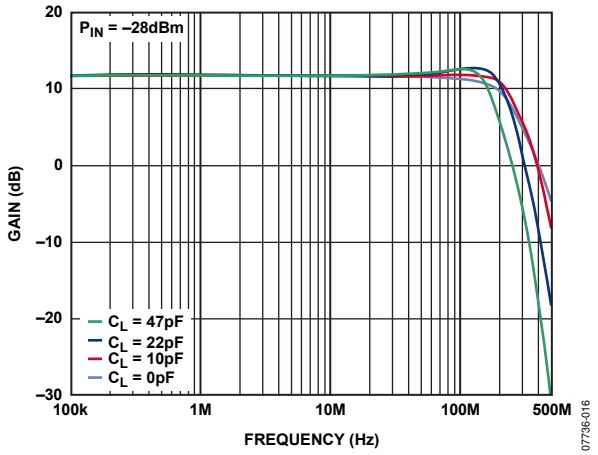

Figure 16. Small Signal Frequency Response to VGAx for Various Capacitive Loads with Series R = 10 Ω

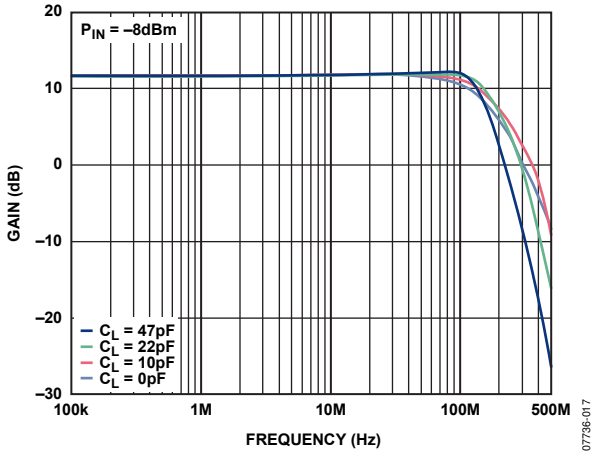

Figure 17. Large Signal Frequency Response to VGAx for Various Capacitive Loads with Series R = 10 Ω

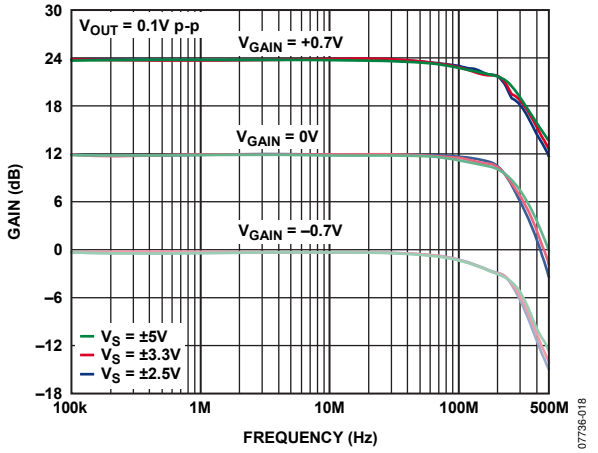

Figure 18. Small Signal Frequency Response vs. Gain to VGAx for Various Supply Voltages

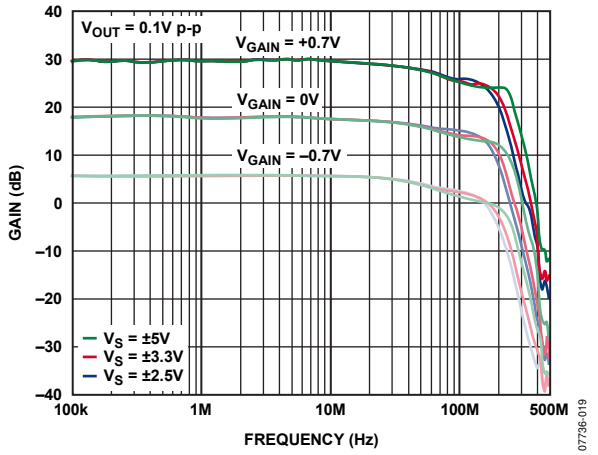

Figure 19. Small Signal Frequency Response vs. Gain to Differential Output for Various Supply Voltages

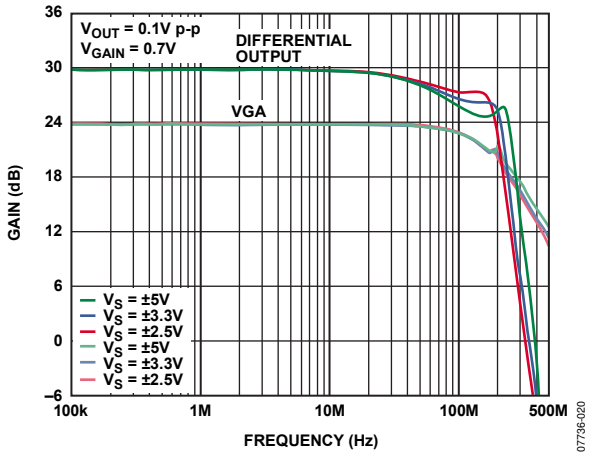

Figure 20. Large Signal Frequency Response to VGAx and Differential Output for Various Supply Voltages

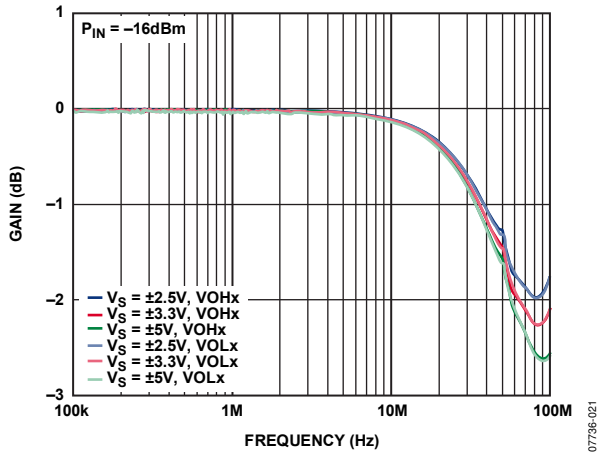

Figure 21. Frequency Response from VOCM to VOHx and VOLx for Various Supplies

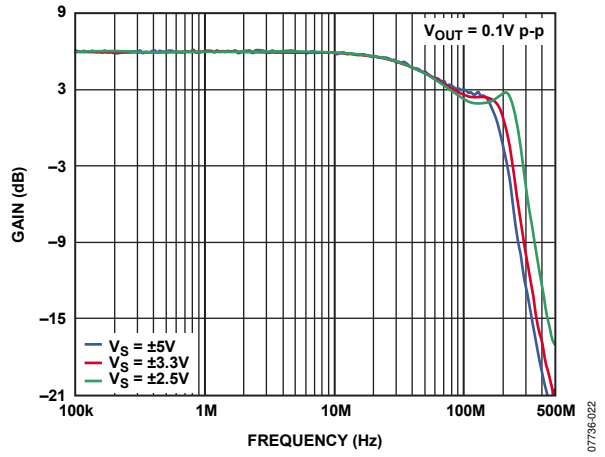

Figure 22. Frequency Response from OFSx to Differential Output for Various Supply Voltages

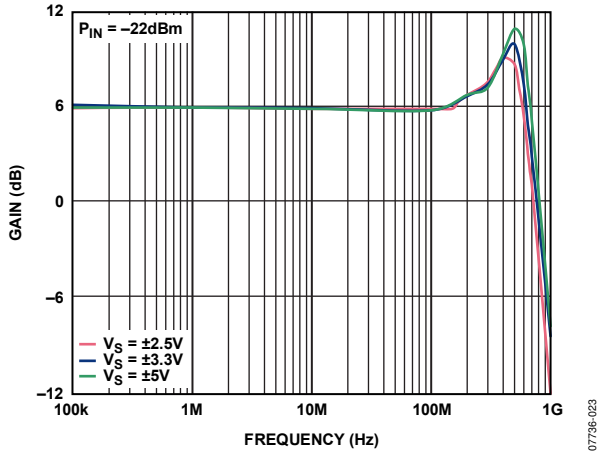

Figure 23. Preamp Frequency Response to OPPx

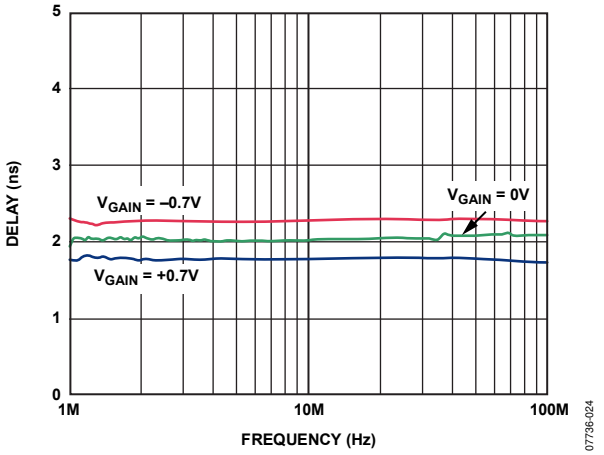

Figure 24. Group Delay vs. Frequency to VGAx

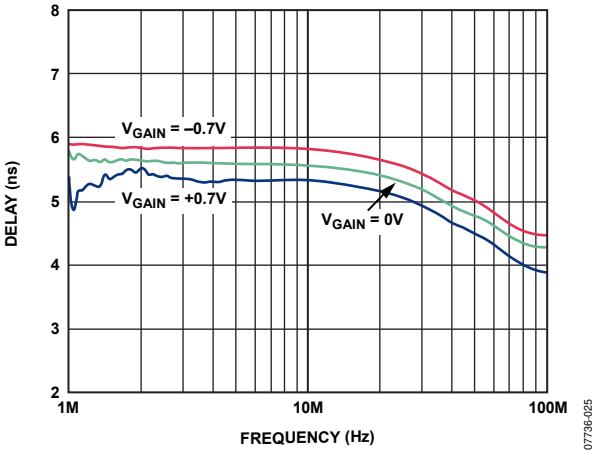

Figure 25. Group Delay vs. Frequency to Differential Output

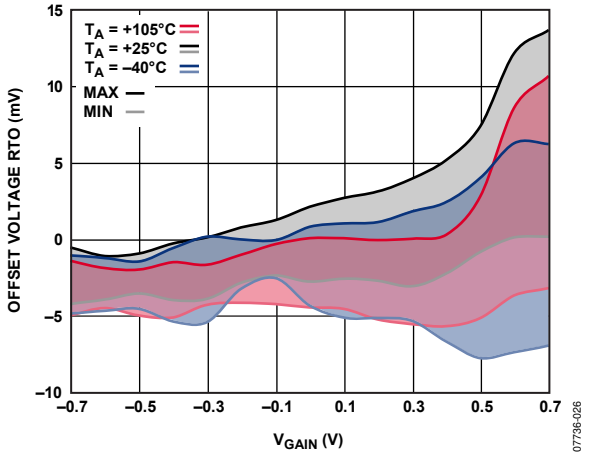

Figure 26. Differential Output Offset Voltage vs. V_{GAIN} vs. Temperature

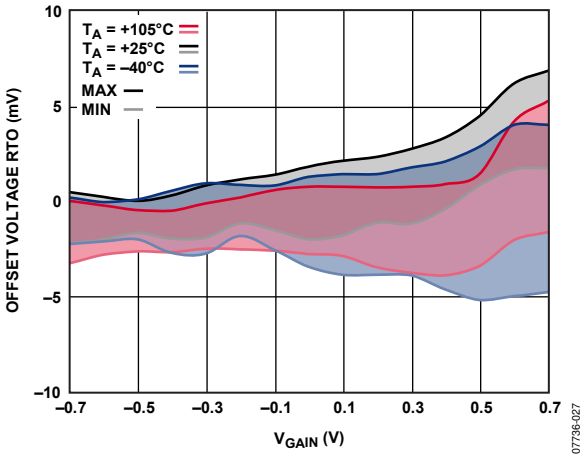

Figure 27. VGAx Output Offset Voltage vs. V_{GAIN} vs. Temperature

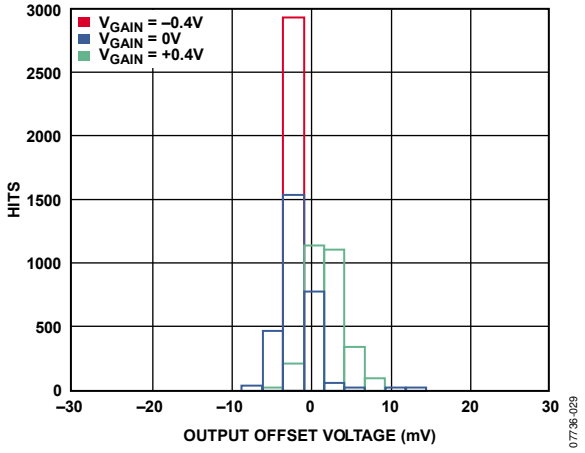

Figure 28. Output Offset Histogram to VGAx

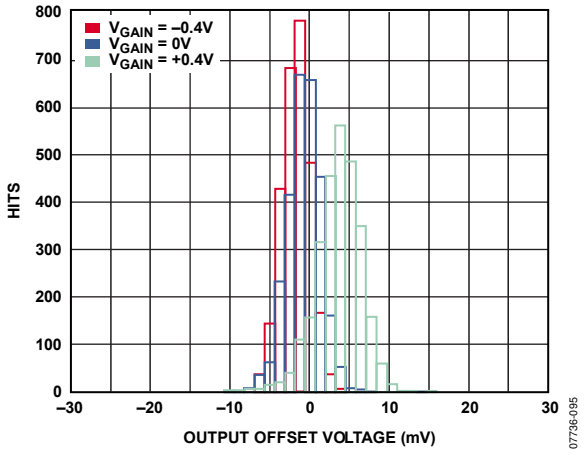

Figure 29. Output Offset Histogram to Differential Output

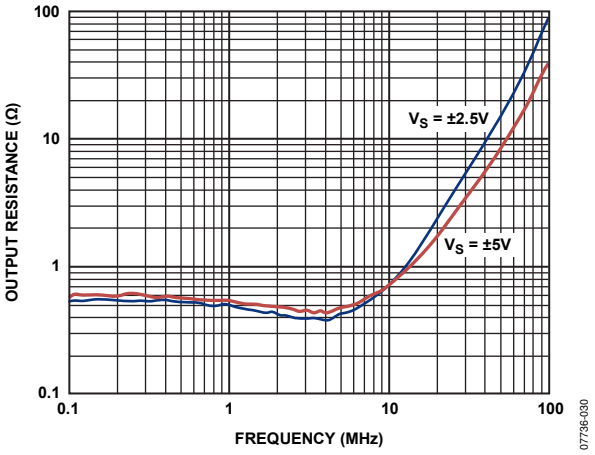

Figure 30. Output Resistance (VOHx, VOLx) vs. Frequency

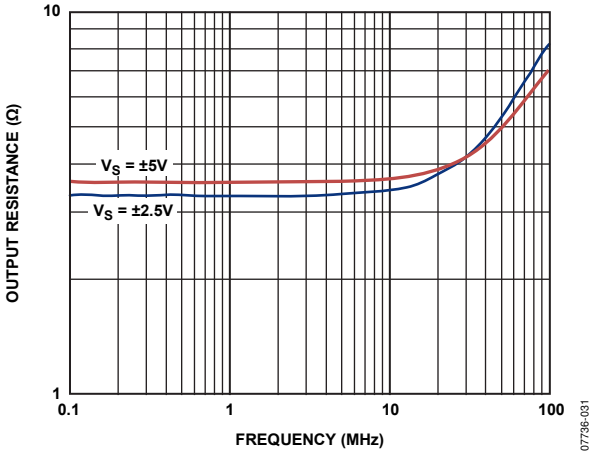

Figure 31. Output Resistance (VGAx) vs. Frequency

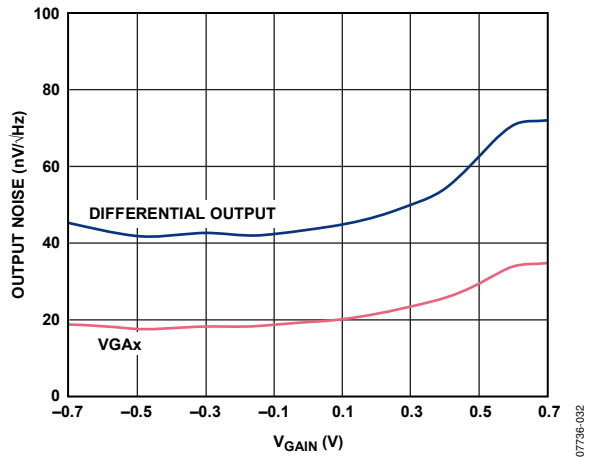

Figure 32. Output Referred Noise to VGAx and Differential Output vs. V_{GAIN}

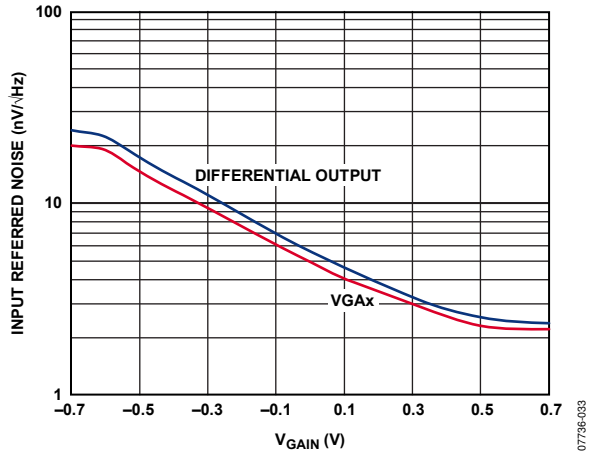

Figure 33. Input Referred Noise from VGAx and Differential Output vs. V_{GAIN}

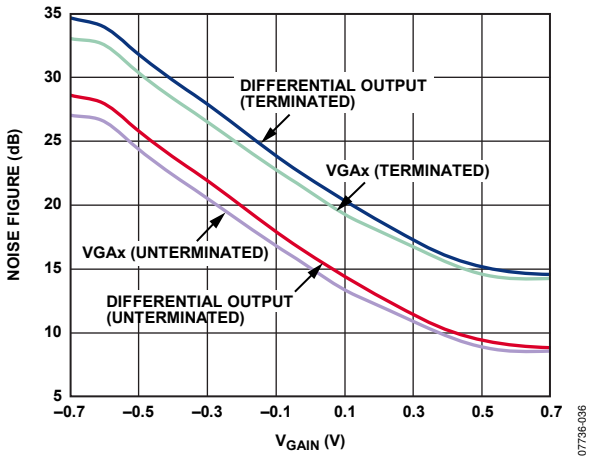

Figure 36. Noise Figure vs. V_{GAIN}

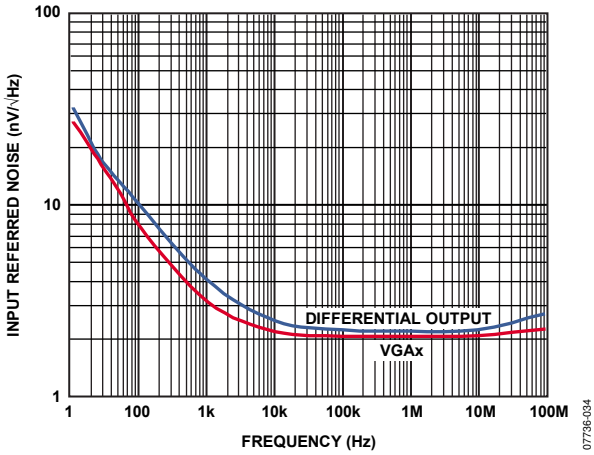

Figure 34. Input Referred Noise vs. Frequency at Maximum Gain

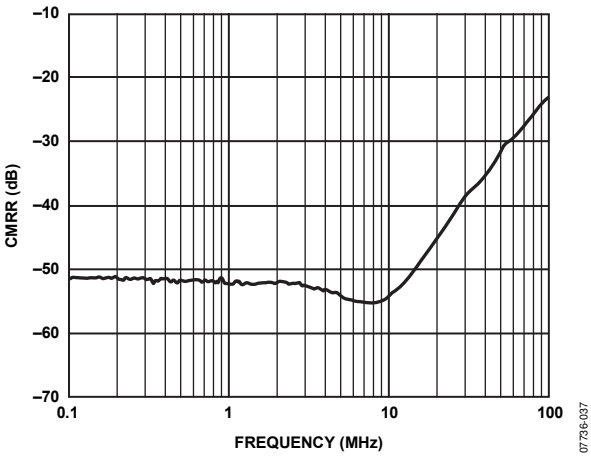

Figure 37. VOCM Common-Mode Rejection Ratio vs. Frequency

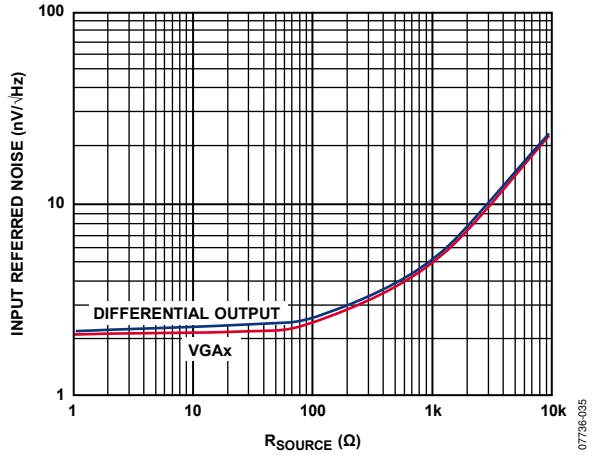

Figure 35. Input Referred Noise vs. R_{SOURCE}

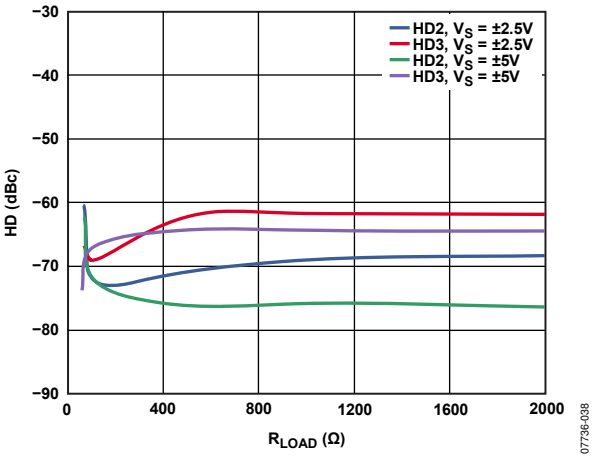

Figure 38. Harmonic Distortion to VGAx vs. R_{LOAD} and Various Supplies

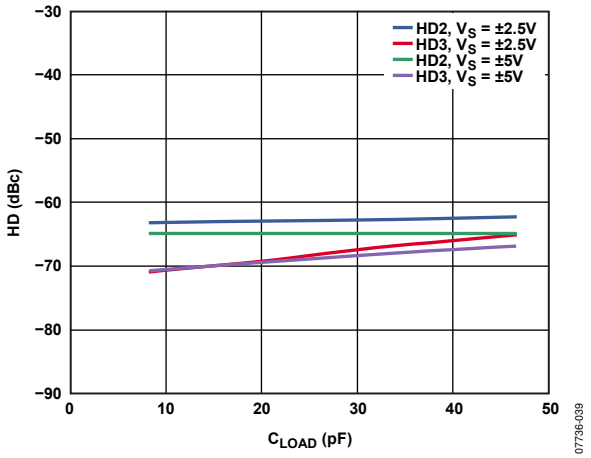

Figure 39. Harmonic Distortion to VGAx vs. C_{LOAD}

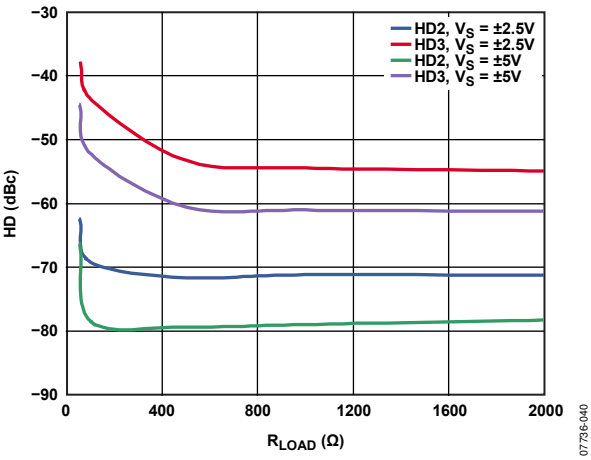

Figure 40. Harmonic Distortion to Differential Output vs. R_{LOAD} and Various Supplies

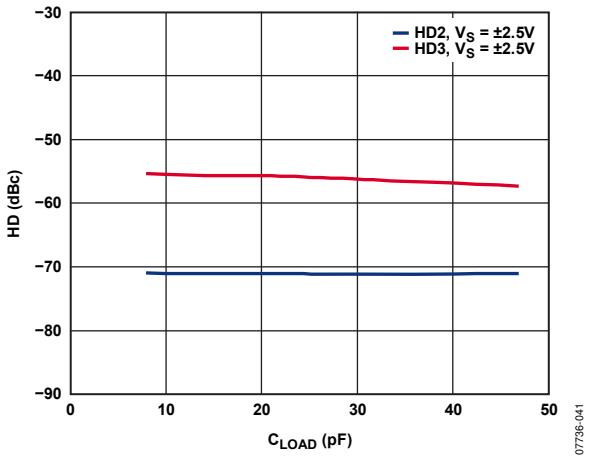

Figure 41. Harmonic Distortion to Differential Output vs. C_{LOAD}

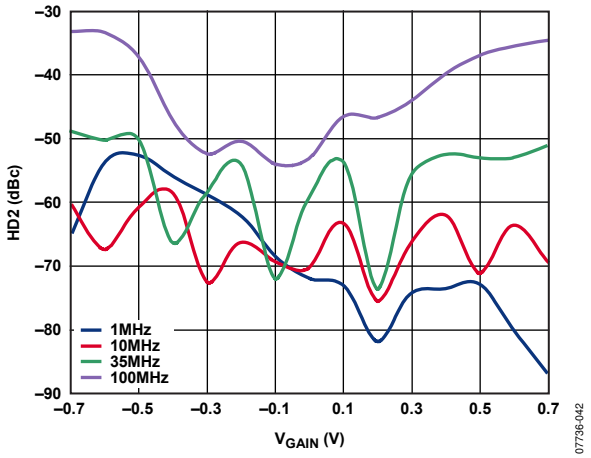

Figure 42. HD2 vs. V_{GAIN} vs. Frequency to VGAx

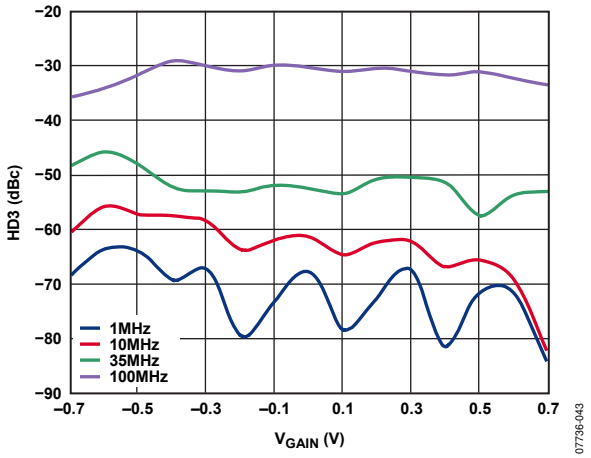

Figure 43. HD3 vs. V_{GAIN} vs. Frequency to VGAx

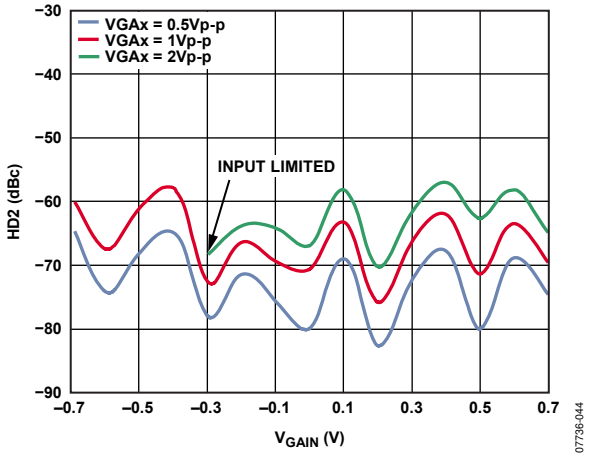

Figure 44. HD2 vs. Amplitude to VGAx

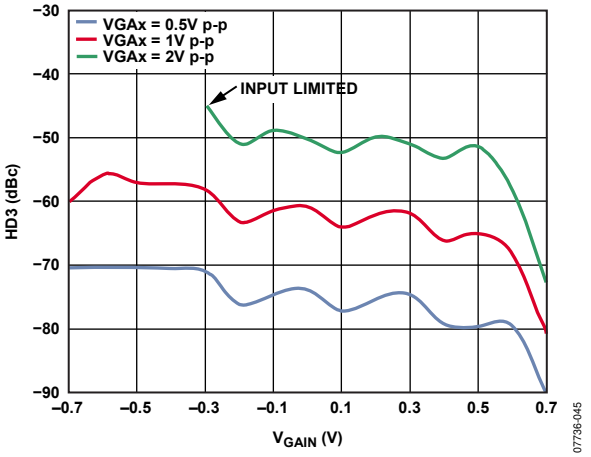

Figure 45. HD3 vs. Amplitude to VGAx

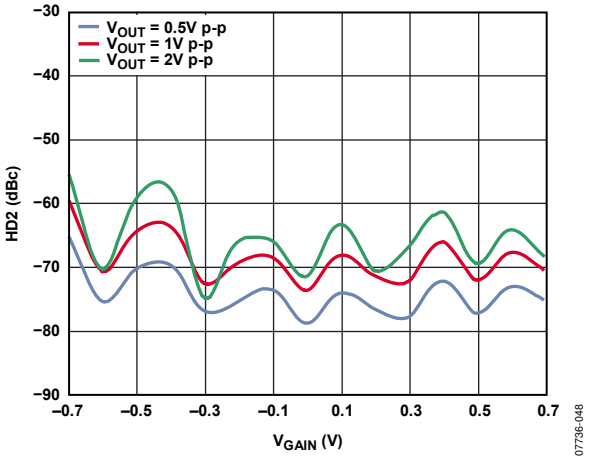

Figure 48. HD2 vs. Amplitude to Differential Output

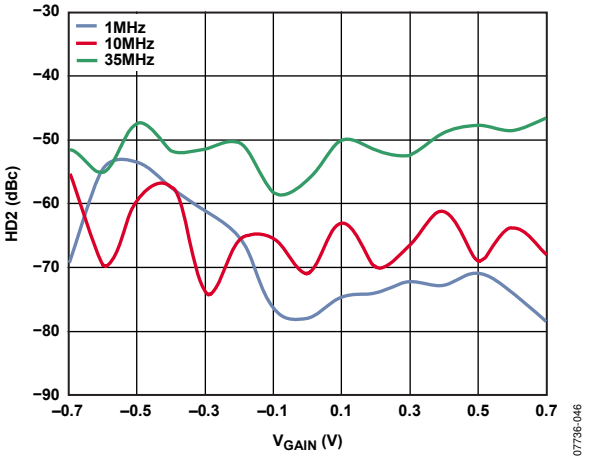

Figure 46. HD2 vs. V_{GAIN} vs. Frequency to Differential Output

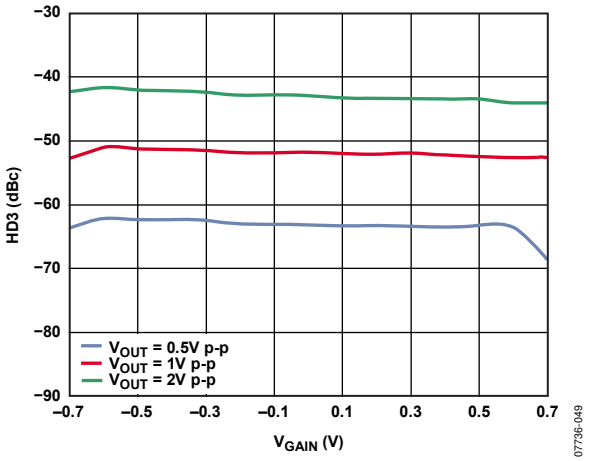

Figure 49. HD3 vs. Amplitude to Differential Output

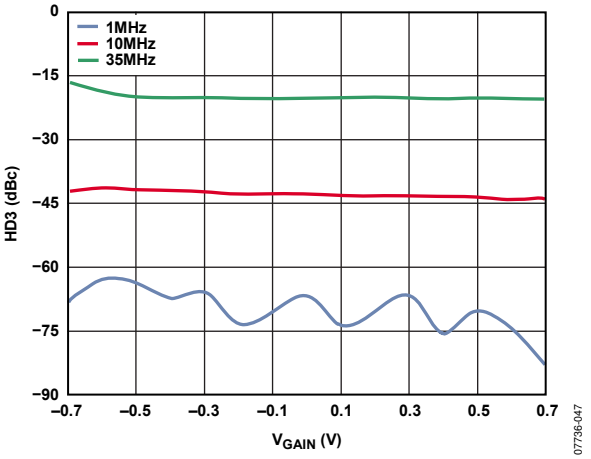

Figure 47. HD3 vs. V_{GAIN} vs. Frequency to Differential Output

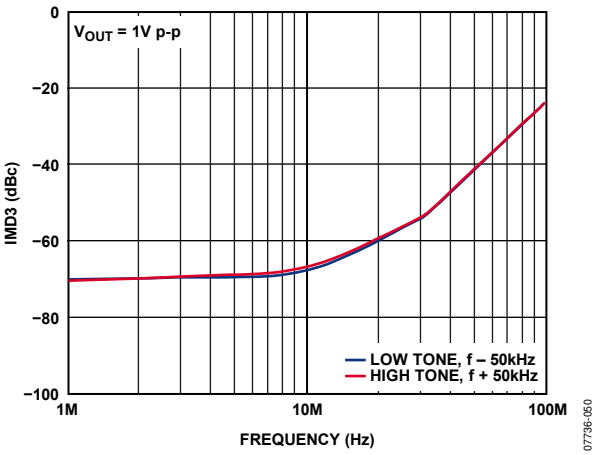

Figure 50. IMD3 vs. Frequency to VGAx

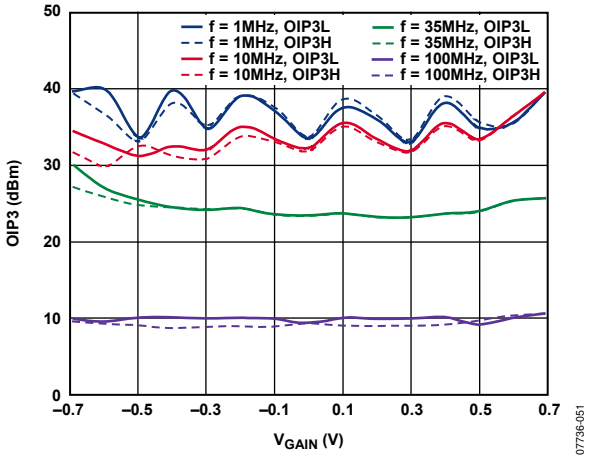

Figure 51. OIP3 vs. V_{GAIN} vs. Frequency to VGAx

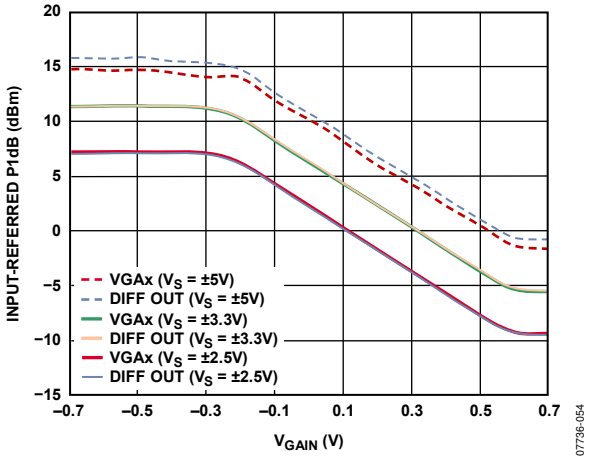

Figure 54. Input P1dB vs. V_{GAIN}

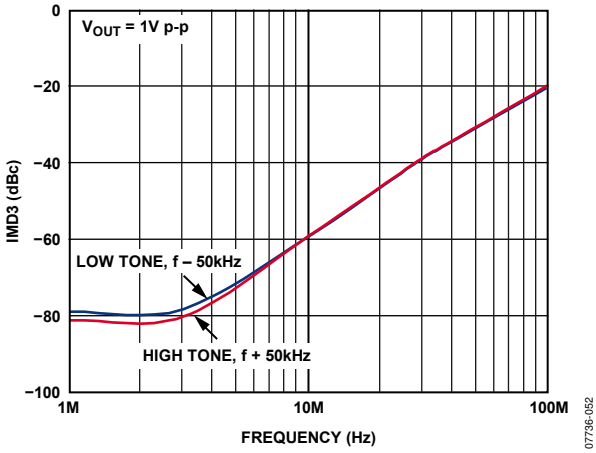

Figure 52. IMD3 vs. Frequency to Differential Output

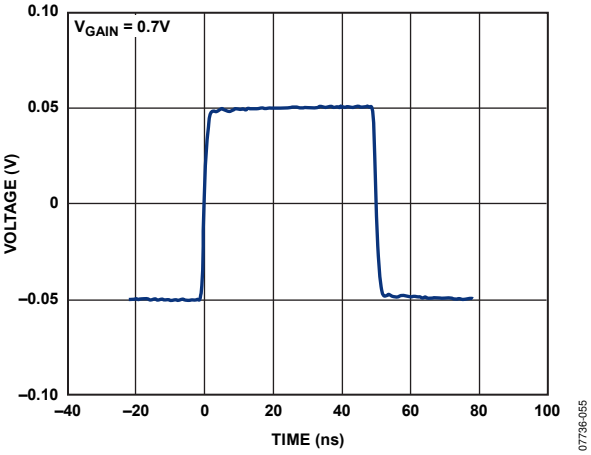

Figure 55. Small Signal Pulse Response to VGAx

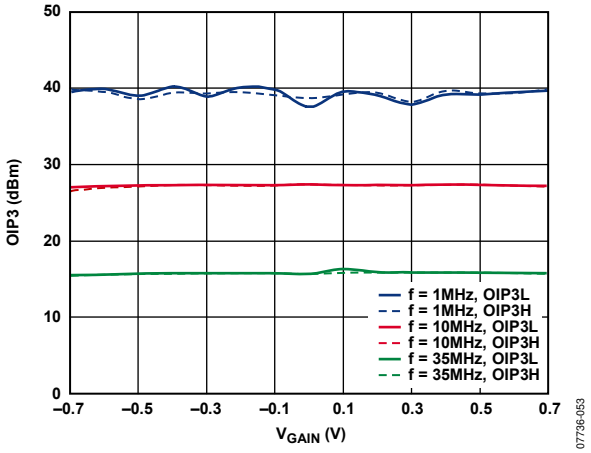

Figure 53. OIP3 vs. Frequency to Differential Output

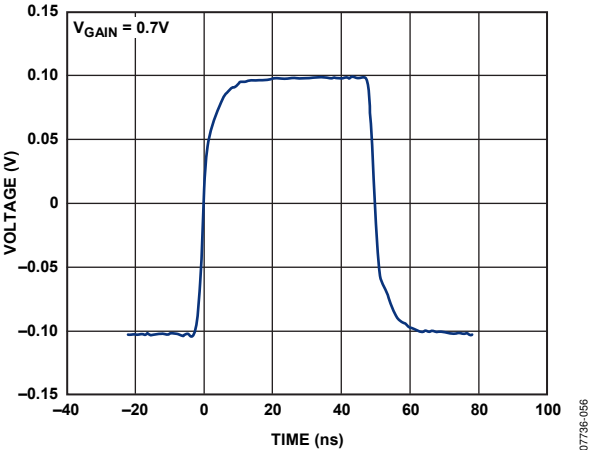

Figure 56. Small Signal Pulse Response to Differential Output

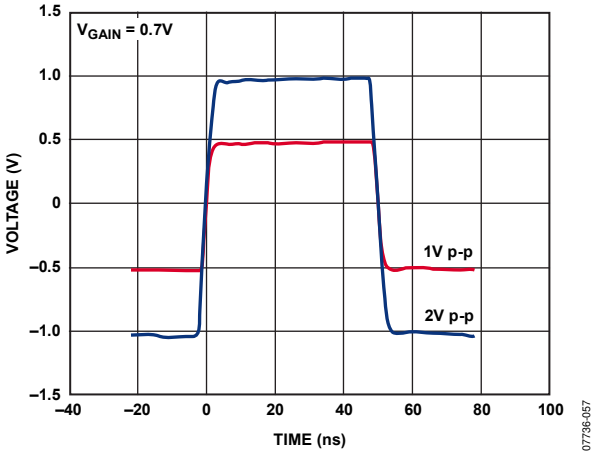

Figure 57. Large Signal Pulse Response to VGAx

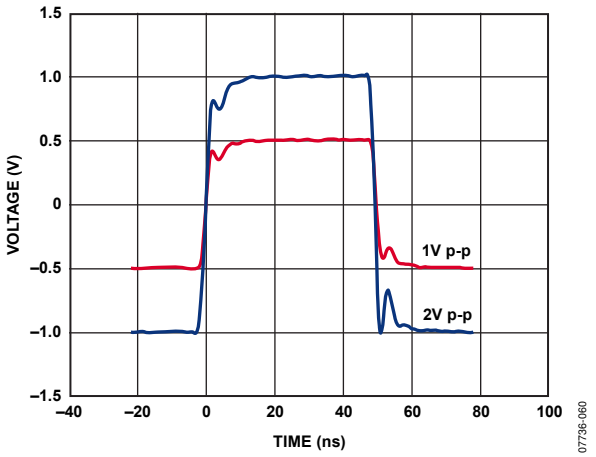

Figure 60. OFSx Large Signal Pulse Response

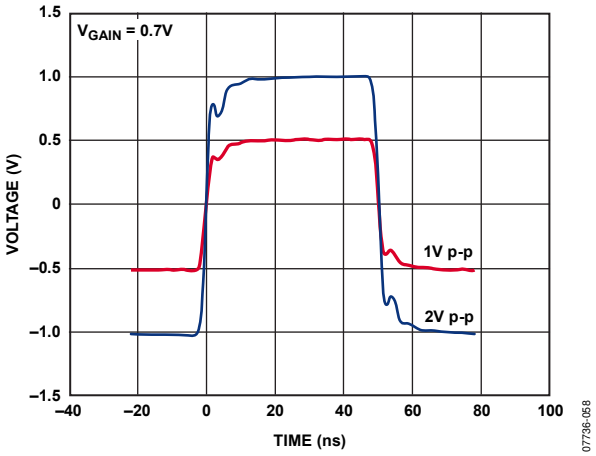

Figure 58. Large Signal Pulse Response to Differential Output

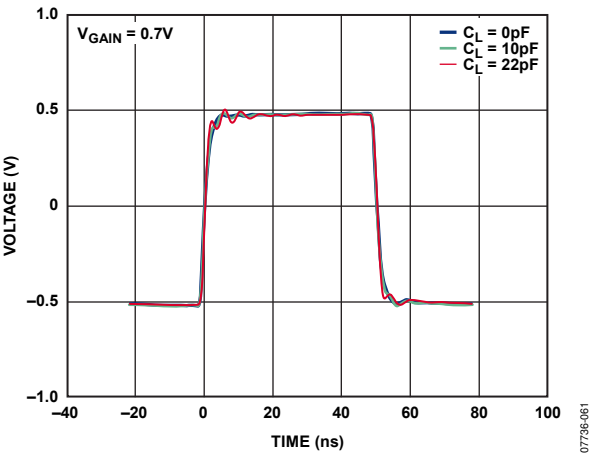

Figure 61. Large Signal Pulse Response to VGAx for Various Capacitive Loads

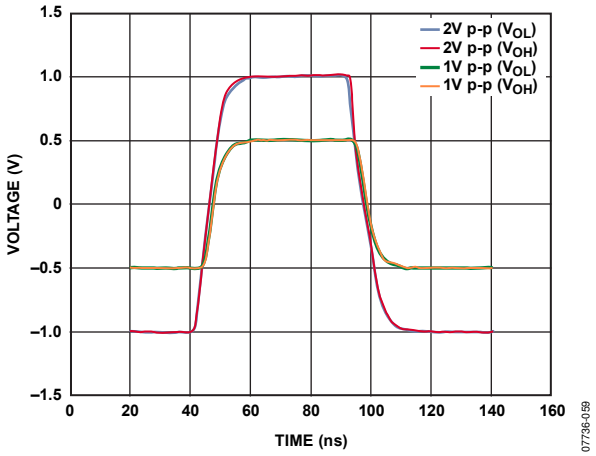

Figure 59. VOCM Large Signal Pulse Response

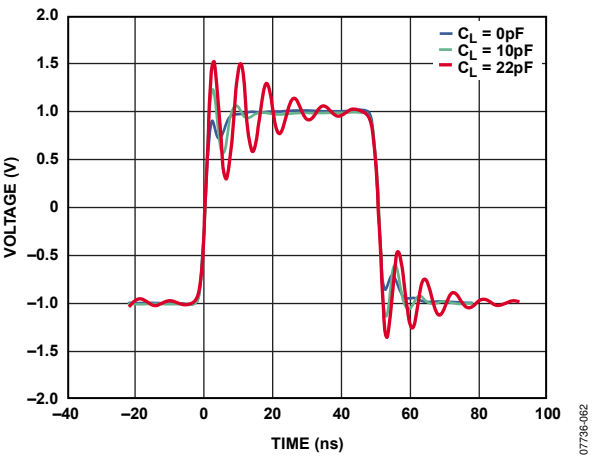

Figure 62. Large Signal Pulse Response to Differential Output for Various Capacitive Loads

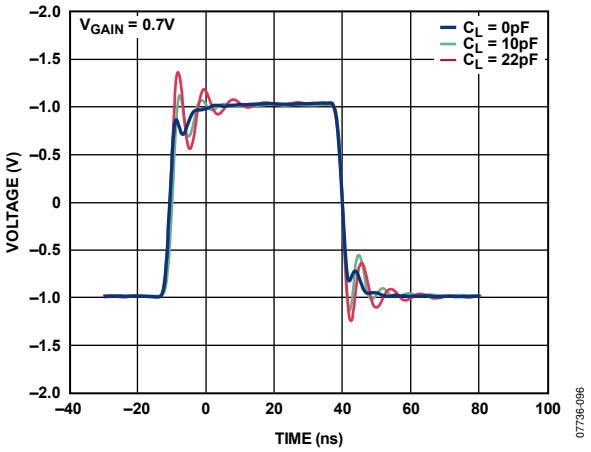

Figure 63. Large Signal Pulse Response to Differential Output for Various Capacitive Loads with Series R = 10 Ω

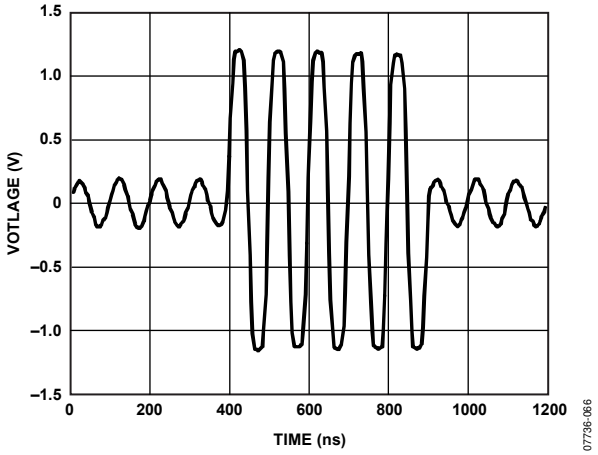

Figure 66. Preamp Overdrive Recovery

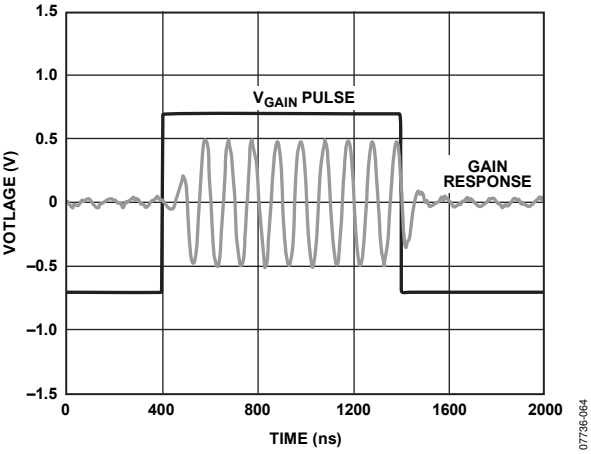

Figure 64. VGAx Response to Change in V_{GAIN}

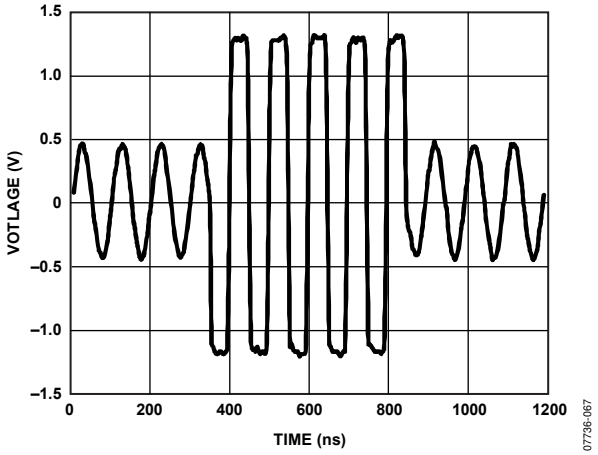

Figure 67. VGA Overdrive Recovery

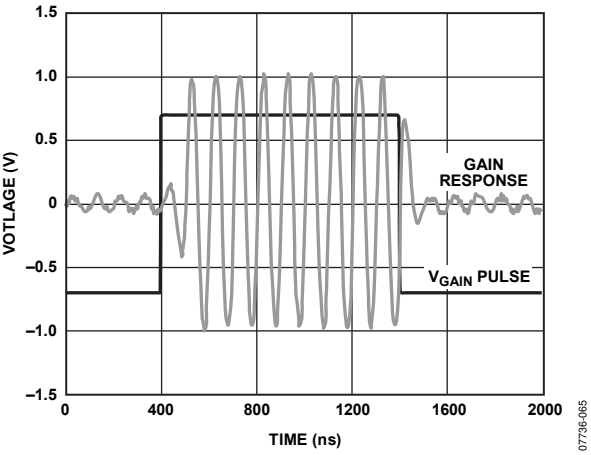

Figure 65. Differential Output Response to Change in V_{GAIN}

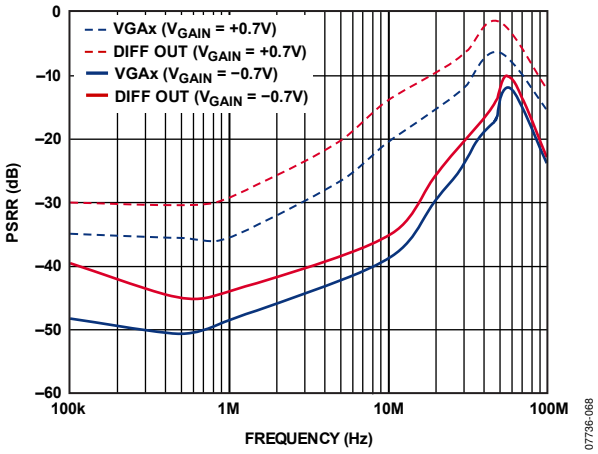

Figure 68. Power Supply Rejection vs. Frequency (VPOS)

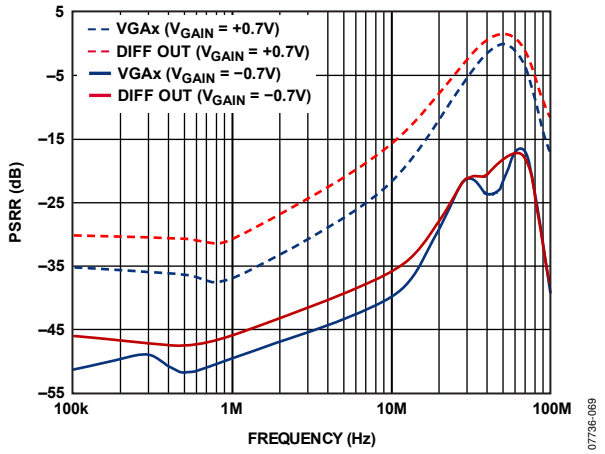

Figure 69. Power Supply Rejection vs. Frequency (VNEG)

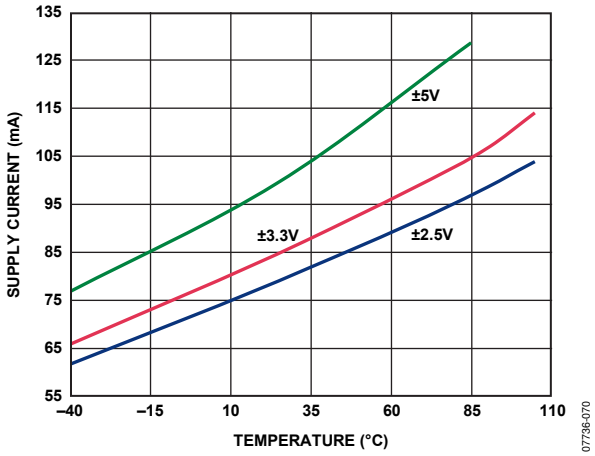

Figure 70. Quiescent Supply Current vs. Temperature

TEST CIRCUITS

V_S = ±2.5 V, T_A = 25°C, f = 10 MHz, C_L = 5 pF, R_L = 500 Ω per output (VGAx, VOHx, VOLx), V_{GAIN} = (V_{GNHx} − V_{GNLO}) = 0 V, V_{VOCM} = GND, V_{OFSx} = GND, gain range = 6 dB to 30 dB, unless otherwise specified.

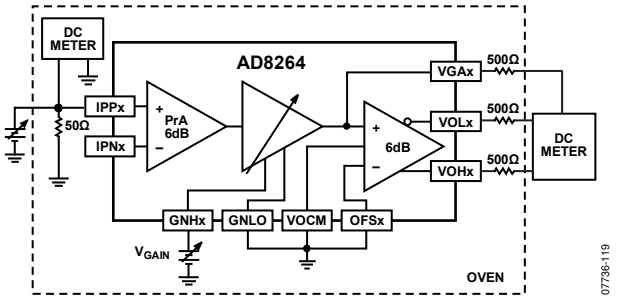

Figure 71. Gain vs. V_{GAIN} vs. Temperature (See Figure 3 and Figure 4)

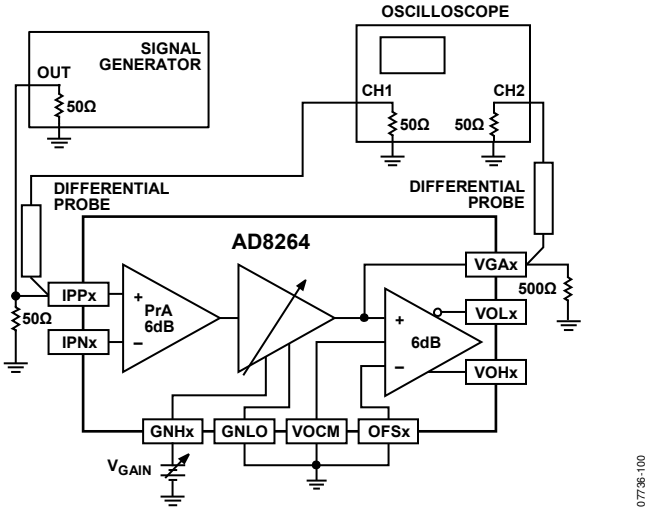

Figure 72. Gain Error vs. V_{GAIN} at Various Frequencies to VGAx (See Figure 5)

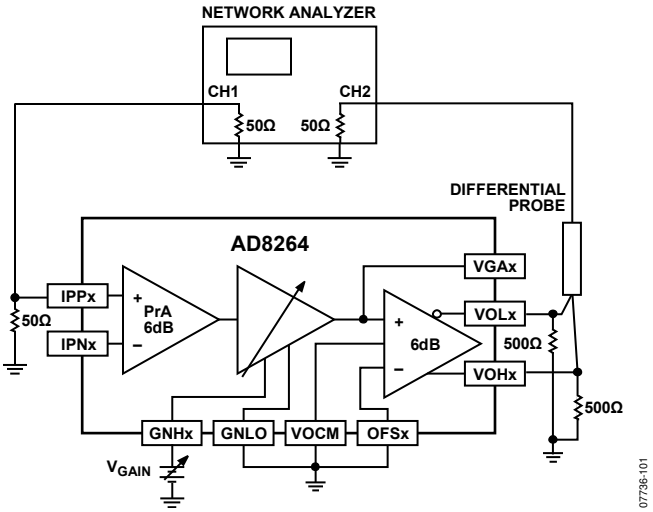

Figure 74. Frequency Response vs. Gain to Differential Output for Various Values of V_{GAIN} (See Figure 11)

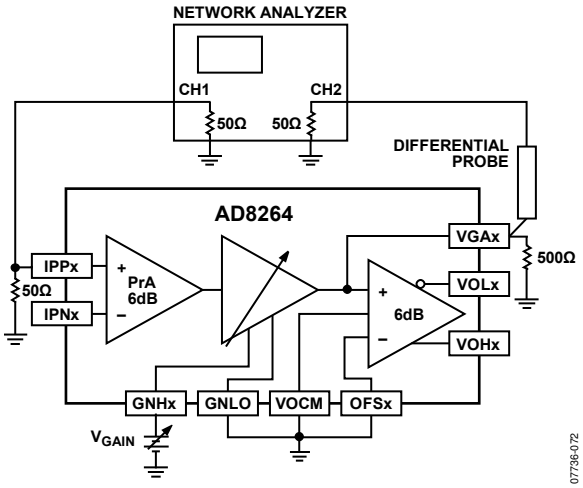

Figure 73. Frequency Response vs. Gain to VGAx for Various Values of V_{GAIN}, V_{GAIN} = GNHx − GNLO (See Figure 10)

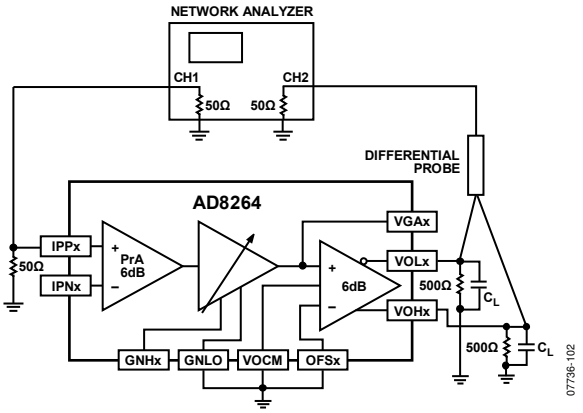

Figure 75. Frequency Response to Differential Output for Various Capacitive Loads (See Figure 12)

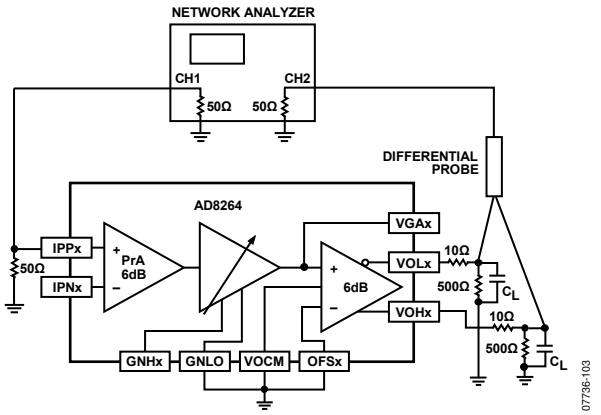

Figure 76. Frequency Response to Differential Output for Various Capacitive Loads with Series R = 10 Ω (See Figure 13)

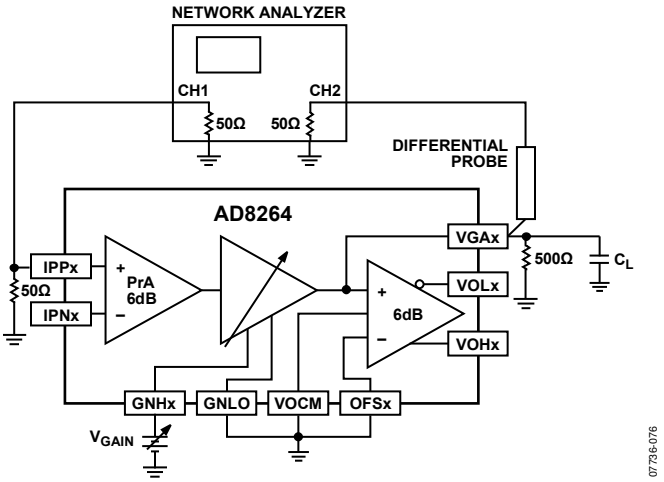

Figure 77. Frequency Response to VGAx for Various Capacitive Loads (See Figure 14)

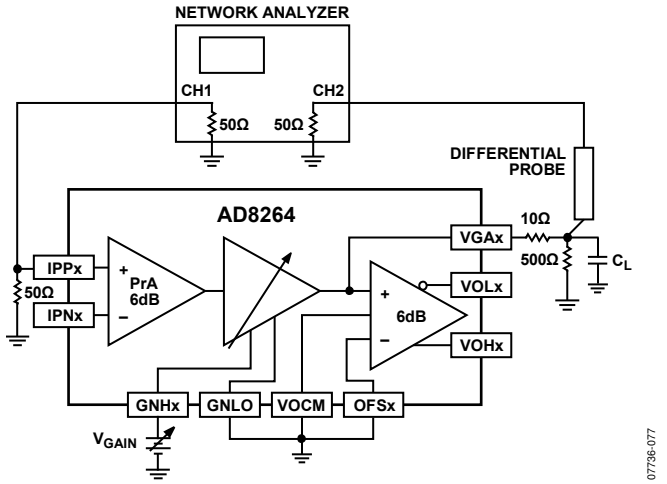

Figure 78. Frequency Response to VGAx for Various Capacitive Loads with Series R =10 Ω (See Figure 16)

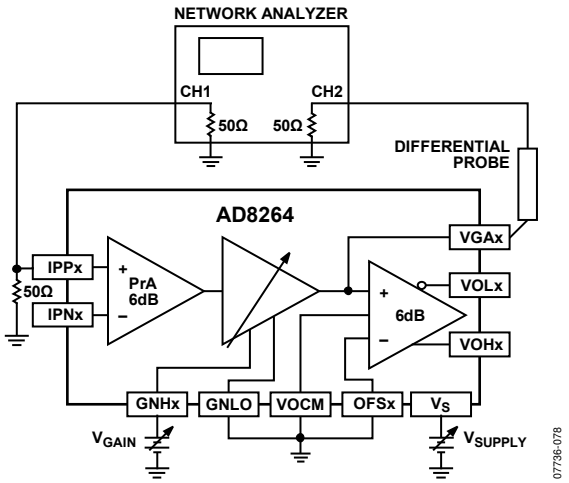

Figure 79. Frequency Response vs. Gain to VGAx for Various Supply Voltages (See Figure 18)

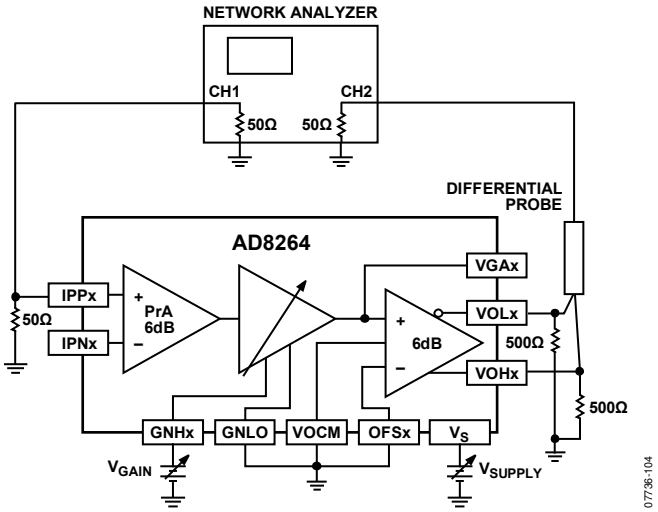

Figure 80. Frequency Response vs. Gain to Differential Output for Various Supply Voltages (See Figure 19)

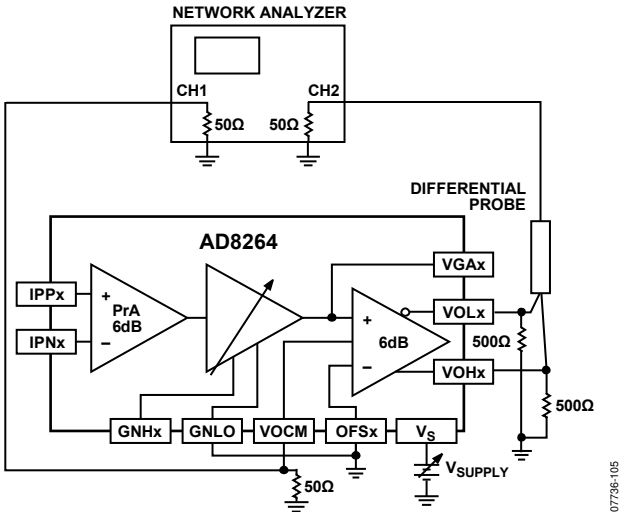

Figure 81. VOCM Frequency Response to Differential Output (See Figure 21)

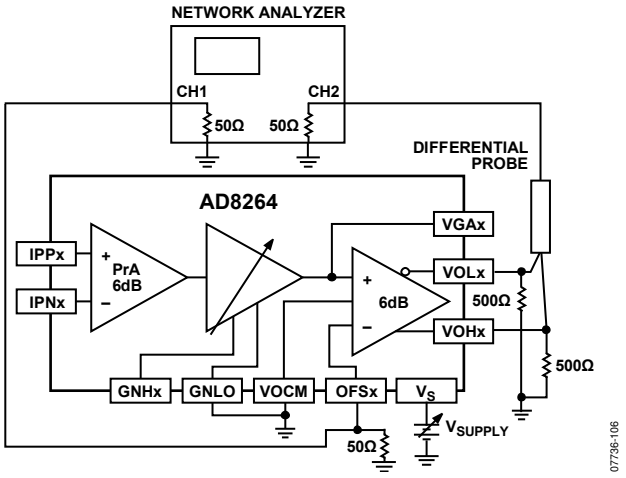

Figure 82. OFSx Frequency Response to Differential Output (See Figure 22)

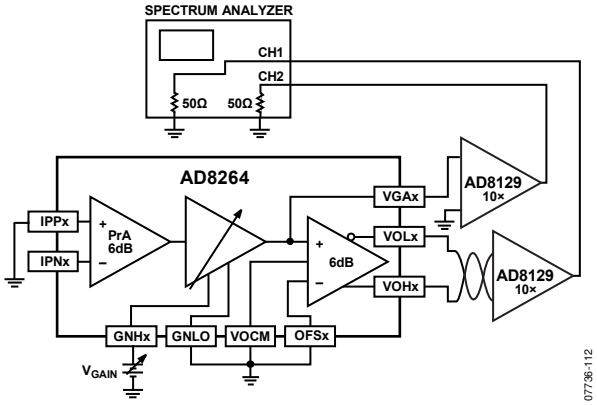

Figure 85. Output Referred Noise vs. V_{GAIN} (See Figure 32)

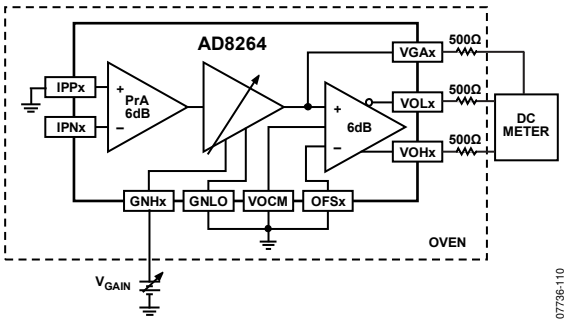

Figure 83. Output Offset Voltage vs. V_{GAIN} vs. Temperature (See Figure 26 and Figure 27)

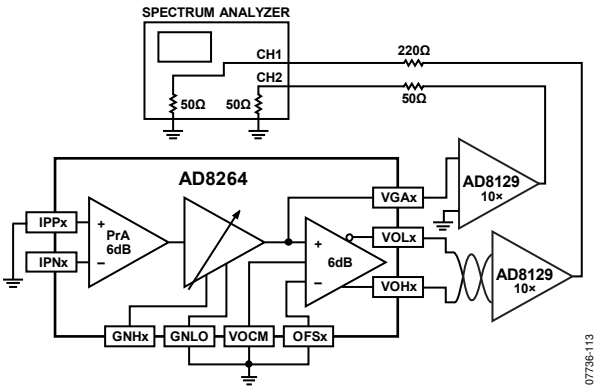

Figure 86. Input Referred Noise vs. Frequency (See Figure 34)

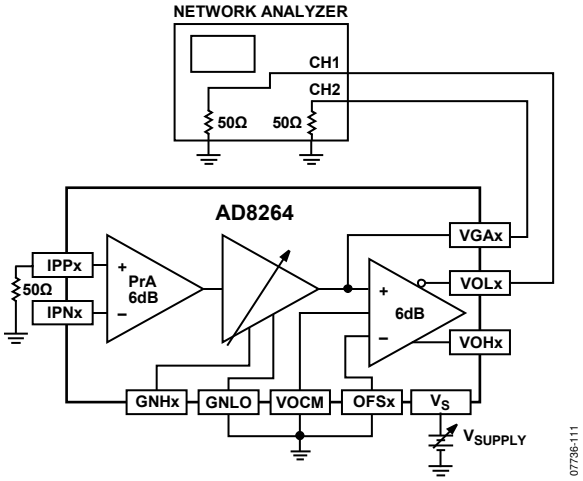

Figure 84. Output Resistance vs. Frequency (See Figure 30 and Figure 31)

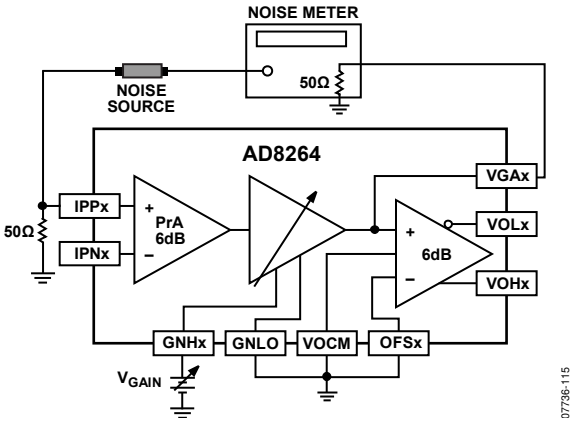

Figure 87. Noise Figure vs. V_{GAIN} (See Figure 36)

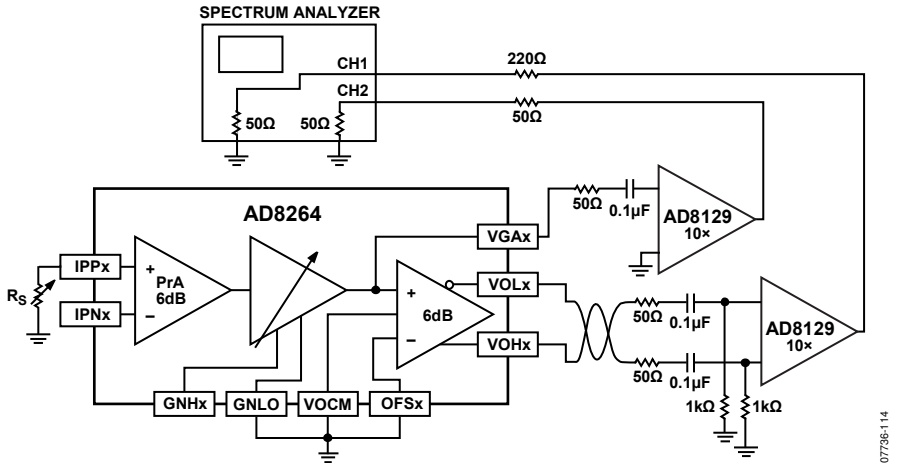

Figure 88. Input Referred Noise vs. R_{SOURCE} (See Figure 35)

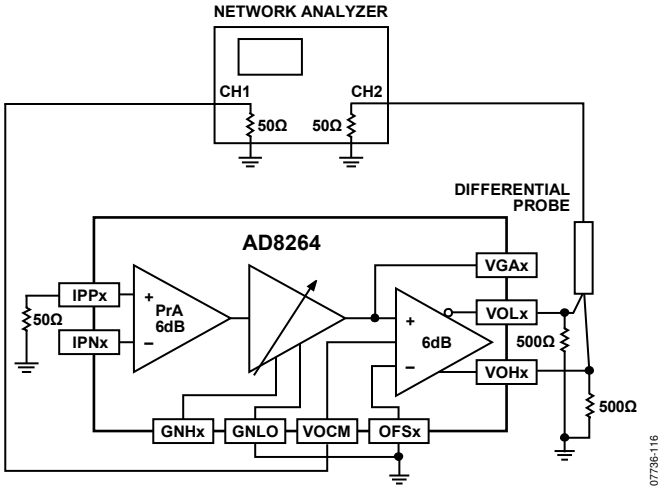

Figure 89. VOCM Common-Mode Rejection vs. Frequency (See Figure 37)

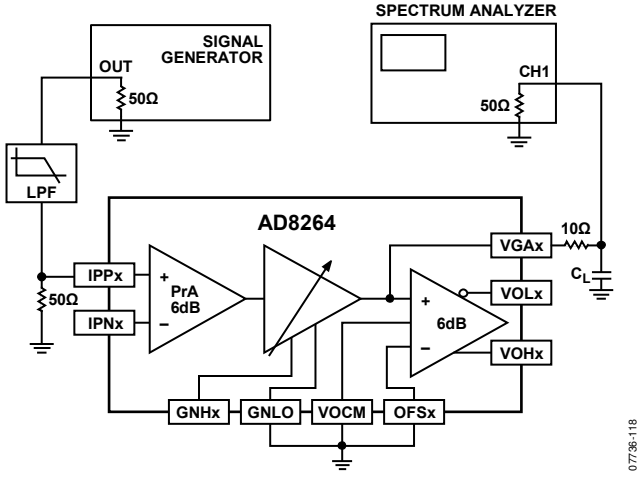

Figure 91. Harmonic Distortion to VGAx vs. C_{LOAD} (Figure 39)

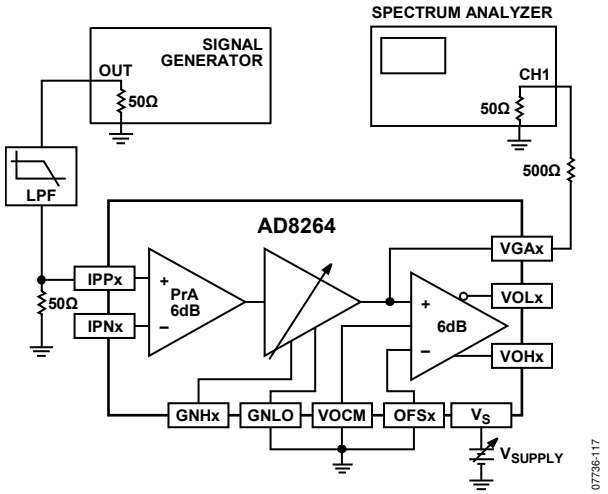

Figure 90. Test Circuit Harmonic Distortion to VGAx vs. R_{LOAD} and Various Supplies (See Figure 38)

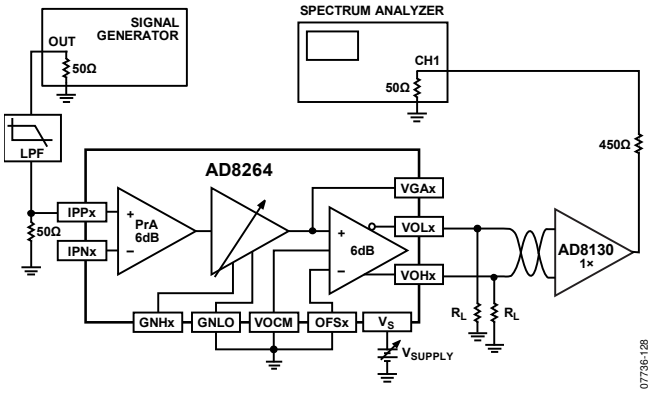

Figure 92. Harmonic Distortion to Differential Output vs. R_{LOAD} and Various Supplies (See Figure 40)

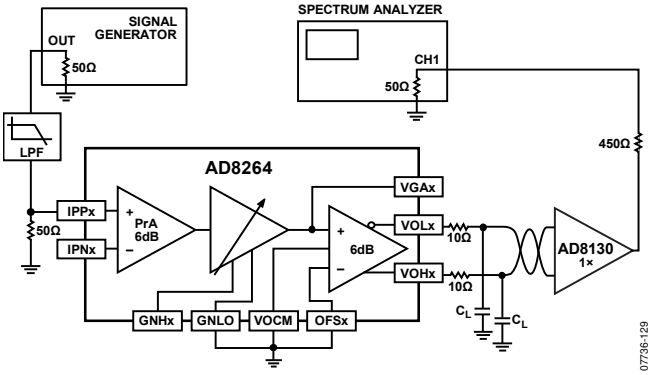

Figure 93. Harmonic Distortion to Differential Output vs. C_{LOAD} (See Figure 41)

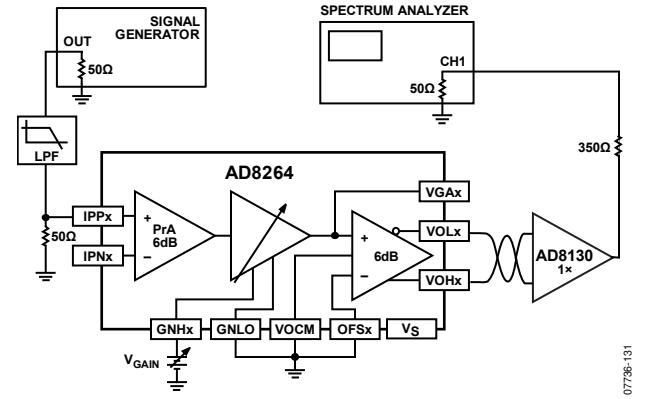

Figure 95. HD2 and HD3 to Differential Output (See Figure 46 through Figure 49)

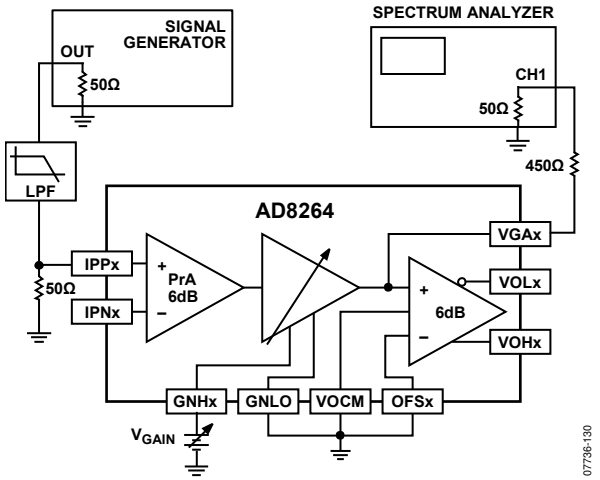

Figure 94. HD2 and HD3 to VGAx (See Figure 42 Through Figure 45)

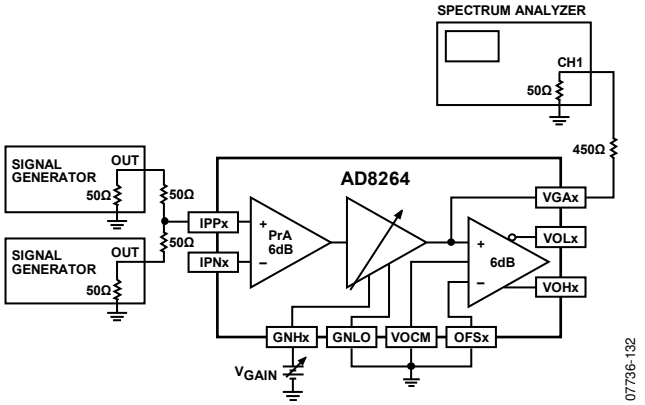

Figure 96. IMD3 and OIP3 to VGAx (See Figure 50 and Figure 51)

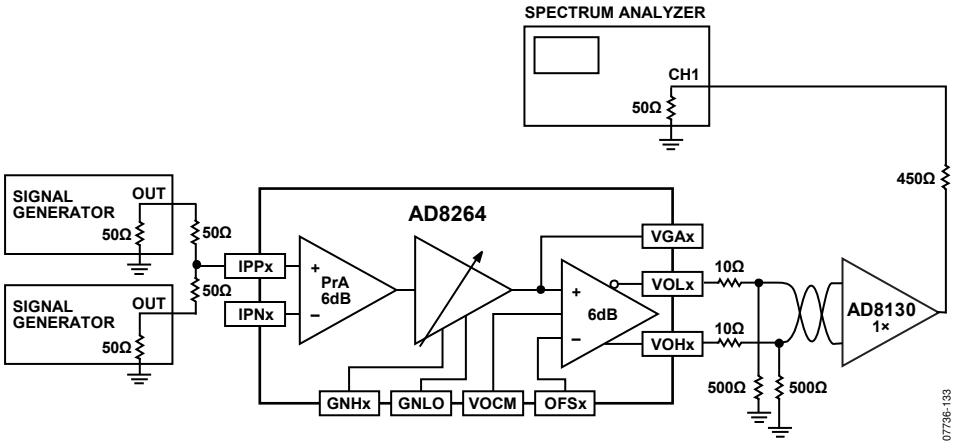

Figure 97. IMD3 and OIP3 to Differential Output (See Figure 52 and Figure 53)