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Ultralow Noise VGAs with Preamplifier and Programmable R_{IN}

Data Sheet

AD8331/AD8332/AD8334

FEATURES

- Ultralow noise preamplifier (preamp)
  - Voltage noise = 0.74 nV/√Hz
  - Current noise = 2.5 pA/√Hz
- 3 dB bandwidth
  - AD8331: 120 MHz
  - AD8332, AD8334: 100 MHz
- Low power
  - AD8331: 125 mW/channel
  - AD8332, AD8334: 145 mW/channel
- Wide gain range with programmable postamp
  - −4.5 dB to +43.5 dB in LO gain mode
  - 7.5 dB to 55.5 dB in HI gain mode
- Low output-referred noise: 48 nV/√Hz typical
- Active input impedance matching
- Optimized for 10-bit/12-bit ADCs
- Selectable output clamping level
- Single 5 V supply operation
- AD8332 and AD8334 available in lead frame chip scale package

APPLICATIONS

- Ultrasound and sonar time-gain controls
- High performance automatic gain control (AGC) systems
- I/Q signal processing
- High speed, dual ADC drivers

GENERAL DESCRIPTION

The AD8331/AD8332/AD8334 are single-, dual-, and quad-channel, ultralow noise linear-in-dB, variable gain amplifiers (VGAs). Optimized for ultrasound systems, they are usable as a low noise variable gain element at frequencies up to 120 MHz.

Included in each channel are an ultralow noise preamp (LNA), an X-AMP® VGA with 48 dB of gain range, and a selectable gain postamp with adjustable output limiting. The LNA gain is 19 dB with a single-ended input and differential outputs. Using a single resistor, the LNA input impedance can be adjusted to match a signal source without compromising noise performance.

The 48 dB gain range of the VGA makes these devices suitable for a variety of applications. Excellent bandwidth uniformity is maintained across the entire range. The gain control interface provides precise linear-in-dB scaling of 50 dB/V for control voltages between 40 mV and 1 V. Factory trim ensures excellent part-to-part and channel-to-channel gain matching.

FUNCTIONAL BLOCK DIAGRAM

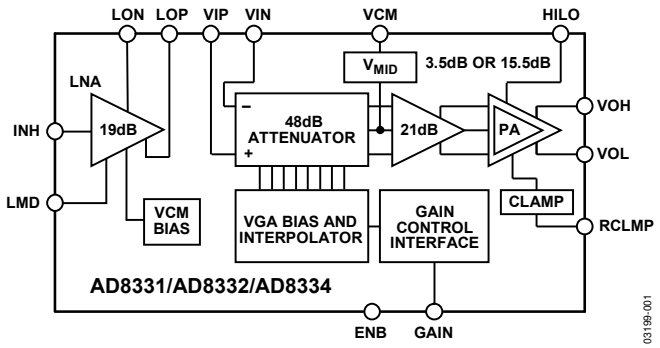

Figure 1. Signal Path Block Diagram

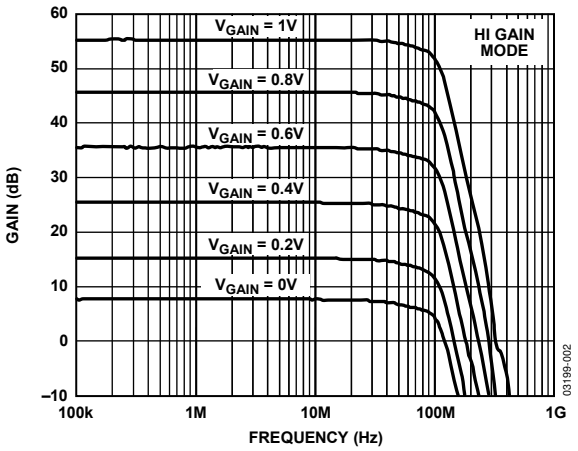

Figure 2. Frequency Response vs. Gain

Differential signal paths result in superb second- and third-order distortion performance and low crosstalk.

The low output-referred noise of the VGA is advantageous in driving high speed differential ADCs. The gain of the postamp can be pin selected to 3.5 dB or 15.5 dB to optimize gain range and output noise for 12-bit or 10-bit converter applications. The output can be limited to a user-selected clamping level, preventing input overload to a subsequent ADC. An external resistor adjusts the clamping level.

The operating temperature range is −40°C to +85°C. The AD8331 is available in a 20-lead QSOP package, the AD8332 is available in 28-lead TSSOP and 32-lead LFCSP packages, and the AD8334 is available in a 64-lead LFCSP package.

Rev. I

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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SPECIFICATIONS

T_A = 25°C, V_S = 5 V, R_L = 500 Ω, R_S = R_{IN} = 50 Ω, R_{IZ} = 280 Ω, C_{SH} = 22 pF, f = 10 MHz, R_{CLMP} = ∞, C_L = 1 pF, VCM pin floating, −4.5 dB to +43.5 dB gain (HILO = LO), and differential output voltage, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
LNA CHARACTERISTICS					
Gain	Single-ended input to differential output		19		dB
	Input to output (single-ended)		13		dB
Input Voltage Range	AC-coupled		±275		mV
Input Resistance	R_{IZ} = 280 Ω		50		Ω
	R_{IZ} = 412 Ω		75		Ω
	R_{IZ} = 562 Ω		100		Ω
	R_{IZ} = 1.13 kΩ		200		Ω
	R_{IZ} = ∞		6		kΩ
Input Capacitance			13		pF
Output Impedance	Single-ended, either output		5		Ω
−3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		130		MHz
Slew Rate			650		V/µs
Input Voltage Noise	R_S = 0 Ω, HI or LO gain, R_{IZ} = ∞, f = 5 MHz		0.74		nV/√Hz
Input Current Noise	R_{IZ} = ∞, HI or LO gain, f = 5 MHz		2.5		pA/√Hz
Noise Figure	f = 10 MHz, LOP output				
Active Termination Match	R_S = R_{IN} = 50 Ω		3.7		dB
Unterminated	R_S = 50 Ω, R_{IZ} = ∞		2.5		dB
Harmonic Distortion at LOP1 or LOP2	V_{OUT} = 0.5 V p-p, single-ended, f = 10 MHz				
HD2			−56		dBc
HD3			−70		dBc
Output Short-Circuit Current	Pin LON, Pin LOP		165		mA
LNA AND VGA CHARACTERISTICS					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p				
AD8331			120		MHz
AD8332, AD8334			100		MHz
−3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p				
AD8331			110		MHz
AD8332, AD8334			90		MHz
Slew Rate					
AD8331	LO gain		300		V/µs
	HI gain		1200		V/µs
AD8332, AD8334	LO gain		275		V/µs
	HI gain		1100		V/µs
Input Voltage Noise	R_S = 0 Ω, HI or LO gain, R_{IZ} = ∞, f = 5 MHz		0.82		nV/√Hz
Noise Figure	V_{GAIN} = 1.0 V				
Active Termination Match	R_S = R_{IN} = 50 Ω, f = 10 MHz, measured		4.15		dB
	R_S = R_{IN} = 200 Ω, f = 5 MHz, simulated		2.0		dB
Unterminated	R_S = 50 Ω, R_{IZ} = ∞, f = 10 MHz, measured		2.5		dB
	R_S = 200 Ω, R_{IZ} = ∞, f = 5 MHz, simulated		1.0		dB
Output-Referred Noise					
AD8331	V_{GAIN} = 0.5 V, LO gain		48		nV/√Hz
	V_{GAIN} = 0.5 V, HI gain		178		nV/√Hz
AD8332, AD8334	V_{GAIN} = 0.5 V, LO gain		40		nV/√Hz
	V_{GAIN} = 0.5 V, HI gain		150		nV/√Hz
Output Impedance, Postamplifier	DC to 1 MHz		1		Ω
Output Signal Range, Postamplifier	R_L ≥ 500 Ω, unclamped, either pin		V_{CM} ± 1.125		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
Differential			4.5		V p-p
Output Offset Voltage					
AD8331	Differential, V_{GAIN} = 0.5 V	−50	±5	+50	mV
	Common mode	−125	−25	+100	mV
AD8332, AD8334	Differential, 0.05 V ≤ V_{GAIN} ≤ 1.0 V	−20	±5	+20	mV
	Common mode	−125	−25	+100	mV
Output Short-Circuit Current			45		mA
Harmonic Distortion	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, HI gain				
AD8331					
HD2	f = 1 MHz		−88		dBc
HD3			−85		dBc
HD2	f = 10 MHz		−68		dBc
HD3			−65		dBc
AD8332, AD8334					
HD2	f = 1 MHz		−82		dBc
HD3			−85		dBc
HD2	f = 10 MHz		−62		dBc
HD3			−66		dBc
Input 1 dB Compression Point	V_{GAIN} = 0.25 V, V_{OUT} = 1 V p-p, f = 1 MHz to 10 MHz		1		dBm
Two-Tone Intermodulation Distortion (IMD3)					
AD8331	V_{GAIN} = 0.72 V, V_{OUT} = 1 V p-p, f = 1 MHz		−80		dBc
	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, f = 10 MHz		−72		dBc
AD8332, AD8334	V_{GAIN} = 0.72 V, V_{OUT} = 1 V p-p, f = 1 MHz		−78		dBc
	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, f = 10 MHz		−74		dBc
Output Third-Order Intercept					
AD8331	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, f = 1 MHz		38		dBm
	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, f = 10 MHz		33		dBm
AD8332, AD8334	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, f = 1 MHz		35		dBm
	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, f = 10 MHz		32		dBm
Channel-to-Channel Crosstalk (AD8332, AD8334)	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, f = 1 MHz		−98		dB
Overload Recovery	V_{GAIN} = 1.0 V, V_{IN} = 50 mV p-p/1 V p-p, f = 10 MHz		5		ns
Group Delay Variation	5 MHz < f < 50 MHz, full gain range		±2		ns
ACCURACY					
Absolute Gain Error[2]	0.05 V < V_{GAIN} < 0.10 V	−1	+0.5	+2	dB
	0.10 V < V_{GAIN} < 0.95 V	−1	±0.3	+1	dB
	0.95 V < V_{GAIN} < 1.0 V	−2	−1	+1	dB
Gain Law Conformance[3]	0.1 V < V_{GAIN} < 0.95 V		±0.2		dB
Channel-to-Channel Gain Matching	0.1 V < V_{GAIN} < 0.95 V		±0.1		dB
GAIN CONTROL INTERFACE (Pin GAIN)					
Gain Scaling Factor	0.10 V < V_{GAIN} < 0.95 V	48.5	50	51.5	dB/V
Gain Range	LO gain		−4.5 to +43.5		dB
	HI gain		7.5 to 55.5		dB
Input Voltage (V_{GAIN}) Range			0 to 1.0		V
Input Impedance			10		MΩ
Response Time	48 dB gain change to 90% full scale		500		ns
COMMON-MODE INTERFACE (PIN VCMx)					
Input Resistance[4]	Current limited to ±1 mA		30		Ω
Output CM Offset Voltage	V_{CM} = 2.5 V	−125	−25	+100	mV
Voltage Range	V_{OUT} = 2.0 V p-p		1.5 to 3.5		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
ENABLE INTERFACE (PIN ENB, PIN ENBL, PIN ENBV)					
Logic Level to Enable Power		2.25		5	V
Logic Level to Disable Power		0		1.0	V
Input Resistance	Pin ENB		25		kΩ
	Pin ENBL		40		kΩ
	Pin ENBV		70		kΩ
Power-Up Response Time	V_{INH} = 30 mV p-p		300		µs
	V_{INH} = 150 mV p-p		4		ms
HILO GAIN RANGE INTERFACE (PIN HILO)					
Logic Level to Select HI Gain Range		2.25		5	V
Logic Level to Select LO Gain Range		0		1.0	V
Input Resistance			50		kΩ
OUTPUT CLAMP INTERFACE (PIN RCLMP; HI OR LO GAIN)					
Accuracy					
HILO = LO	R_{CLMP} = 2.74 kΩ, V_{OUT} = 1 V p-p (clamped)		±50		mV
HILO = HI	R_{CLMP} = 2.21 kΩ, V_{OUT} = 1 V p-p (clamped)		±75		mV
MODE INTERFACE (PIN MODE)					
Logic Level for Positive Gain Slope		0		1.0	V
Logic Level for Negative Gain Slope		2.25		5	V
Input Resistance			200		kΩ
POWER SUPPLY (PIN VPS1, PIN VPS2, PIN VPSV, PIN VPSL, PIN VPOS)					
Supply Voltage		4.5	5.0	5.5	V
Quiescent Current per Channel					
AD8331		20	25		mA
AD8332		22	27.5	32	mA
AD8334		24	29.5	34	
Power Dissipation per Channel	No signal				
AD8331			125		mW
AD8332, AD8334			138		mW
Power-Down Current	VGA and LNA disabled				
AD8331		50	240	400	µA
AD8332		50	300	600	µA
AD8334		50	600	1200	µA
LNA Current					
AD8331 (ENBL)	Each channel	7.5	11	15	mA
AD8332, AD8334 (ENBL)	Each channel	7.5	12	15	mA
VGA Current					
AD8331 (ENBV)		7.5	14	20	mA
AD8332, AD8334 (ENBV)		7.5	17	20	mA
PSRR	V_{GAIN} = 0 V, f = 100 kHz		−68		dB

[1] All dBm values are referred to 50 Ω.
[2] The absolute gain refers to the theoretical gain expression in Equation 1.
[3] Best-fit to linear-in-dB curve.
[4] The current is limited to ±1 mA typical.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply Voltage (VPSn, VPSV, VPSL, VPOS)	5.5 V
Input Voltage (INHx)	V_S + 200 mV
ENB, ENBL, ENBV, HILO Voltage	V_S + 200 mV
GAIN Voltage	2.5 V
Power Dissipation	
RU Package[1] (AD8332)	0.96 W
CP-32 Package (AD8332)	1.97 W
RQ Package[1] (AD8331)	0.78 W
CP-64 Package (AD8334)	0.91 W
Temperature	
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C
θ_{JA}	
RU Package[1] (AD8332)	68°C/W
CP-32 Package2[2] (AD8332)	33°C/W
RQ Package[1] (AD8331)	83°C/W
CP-64 Package[3] (AD8334)	24.2°C/W

[1] 4-layer JEDEC board (2S2P).
[2] Exposed pad soldered to board, nine thermal vias in pad—JEDEC, 4-layer board J-STD-51-9.
[3] Exposed pad soldered to board, 25 thermal vias in pad—JEDEC, 4-layer board J-STD-51-9.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

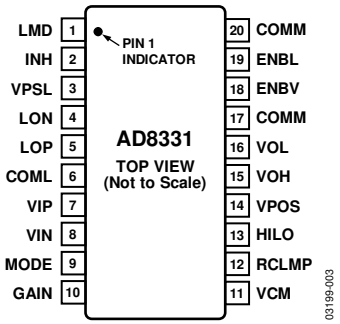

Figure 3. 20-Lead QSOP Pin Configuration (AD8331)

Table 3. 20-Lead QSOP Pin Function Description (AD8331)

Pin No.	Mnemonic	Description
1	LMD	LNA Midsupply Bypass Pin; Connect a Capacitor for Midsupply HF Bypass
2	INH	LNA Input
3	VPSL	LNA 5 V Supply
4	LON	LNA Inverting Output
5	LOP	LNA Noninverting Output
6	COML	LNA Ground
7	VIP	VGA Noninverting Input
8	VIN	VGA Inverting Input
9	MODE	Gain Slope Logic Input
10	GAIN	Gain Control Voltage
11	VCM	Common-Mode Voltage
12	RCLMP	Output Clamping Level
13	HILO	Gain Range Select (HI or LO)
14	VPOS	VGA 5 V Supply
15	VOH	Noninverting VGA Output
16	VOL	Inverting VGA Output
17	COMM	VGA Ground
18	ENBV	VGA Enable
19	ENBL	LNA Enable
20	COMM	VGA Ground

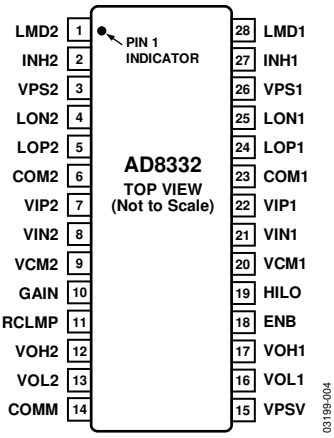

Figure 4. 28-Lead TSSOP Pin Configuration (AD8332)

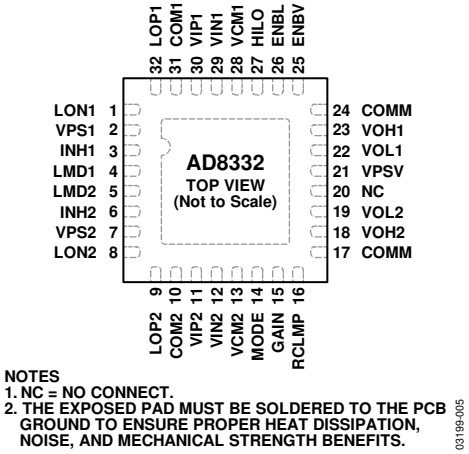

Figure 5. 32-Lead LFCSP Pin Configuration (AD8332)

Table 4. 28-Lead TSSOP Pin Function Description (AD8332)

Pin No.	Mnemonic	Description
1	LMD2	CH 2 LNA Midsupply Pin; Connect a Capacitor for Midsupply HF Bypass
2	INH2	CH2 LNA Input
3	VPS2	CH2 Supply LNA 5 V
4	LON2	CH2 LNA Inverting Output
5	LOP2	CH2 LNA Noninverting Output
6	COM2	CH2 LNA Ground
7	VIP2	CH2 VGA Noninverting Input
8	VIN2	CH2 VGA Inverting Input
9	VCM2	CH2 Common-Mode Voltage
10	GAIN	Gain Control Voltage
11	RCLMP	Output Clamping Resistor
12	VOH2	CH2 Noninverting VGA Output
13	VOL2	CH2 Inverting VGA Output
14	COMM	VGA Ground (Both Channels)
15	VPSV	VGA Supply 5 V (Both Channels)
16	VOL1	CH1 Inverting VGA Output
17	VOH1	CH1 Noninverting VGA Output
18	ENB	Enable—VGA/LNA
19	HILO	VGA Gain Range Select (HI or LO)
20	VCM1	CH1 Common-Mode Voltage
21	VIN1	CH1 VGA Inverting Input
22	VIP1	CH1 VGA Noninverting Input
23	COM1	CH1 LNA Ground
24	LOP1	CH1 LNA Noninverting Output
25	LON1	CH1 LNA Inverting Output
26	VPS1	CH1 LNA Supply 5 V
27	INH1	CH1 LNA Input
28	LMD1	CH 1 LNA Midsupply Pin; Connect a Capacitor for Midsupply HF Bypass

Table 5. 32-Lead LFCSP Pin Function Description (AD8332)

Pin No.	Mnemonic	Description
1	LON1	CH1 LNA Inverting Output
2	VPS1	CH1 LNA Supply 5 V
3	INH1	CH1 LNA Input
4	LMD1	CH 1 LNA Midsupply Pin; Connect a Capacitor for Midsupply HF Bypass
5	LMD2	CH 2 LNA Midsupply Pin; Connect a Capacitor for Midsupply HF Bypass
6	INH2	CH2 LNA Input
7	VPS2	CH2 LNA Supply 5 V
8	LON2	CH2 LNA Inverting Output
9	LOP2	CH2 LNA Noninverting Output
10	COM2	CH2 LNA Ground
11	VIP2	CH2 VGA Noninverting Input
12	VIN2	CH2 VGA Inverting Input
13	VCM2	CH2 Common-Mode Voltage
14	MODE	Gain Slope Logic Input
15	GAIN	Gain Control Voltage
16	RCLMP	Output Clamping Level Input
17	COMM	VGA Ground
18	VOH2	CH2 Noninverting VGA Output
19	VOL2	CH2 Inverting VGA Output
20	NC	No Connect
21	VPSV	VGA Supply 5 V
22	VOL1	CH1 Inverting VGA Output
23	VOH1	CH1 Noninverting VGA Output
24	COMM	VGA Ground
25	ENBV	VGA Enable
26	ENBL	LNA Enable
27	HILO	VGA Gain Range Select (HI or LO)
28	VCM1	CH1 Common-Mode Voltage
29	VIN1	CH1 VGA Inverting Input
30	VIP1	CH1 VGA Noninverting Input
31	COM1	CH1 LNA Ground
32	LOP1	CH1 LNA Noninverting Output
	EPAD	Exposed Pad. The exposed pad must be soldered to the PCB ground to ensure proper heat dissipation, noise, and mechanical strength benefits.

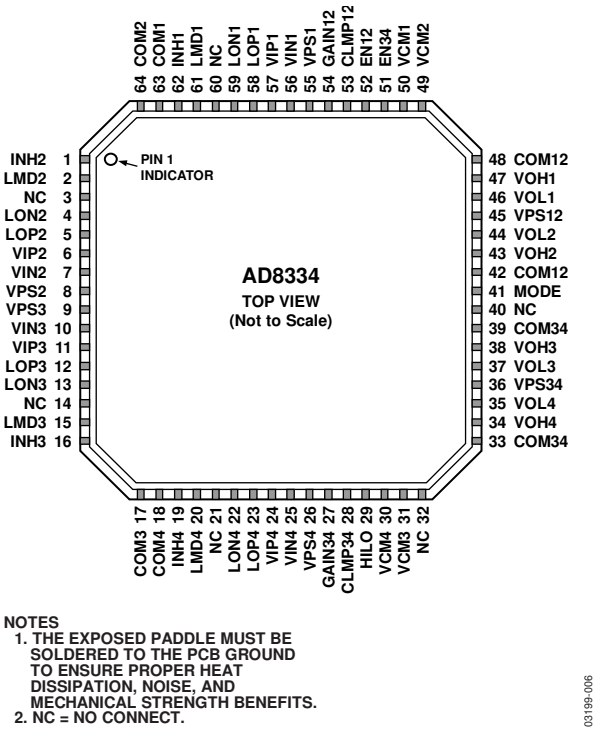

Figure 6. 64-Lead LFCSP Pin Configuration (AD8334)

Table 6. 64-Lead LFCSP Pin Function Description (AD8334)

Pin No.	Mnemonic	Description
1	INH2	CH2 LNA Input.
2	LMD2	CH 2 LNA Midsupply Pin; Connect a Capacitor for Midsupply HF Bypass.
3	NC	Not Connected.
4	LON2	CH2 LNA Feedback Output (for R_{IZ}).
5	LOP2	CH2 LNA Output.
6	VIP2	CH2 VGA Positive Input.
7	VIN2	CH2 VGA Negative Input.
8	VPS2	CH2 LNA Supply 5 V.
9	VPS3	CH3 LNA Supply 5 V.
10	VIN3	CH3 VGA Negative Input.
11	VIP3	CH3 VGA Positive Input.
12	LOP3	CH3 LNA Positive Output.
13	LON3	CH3 LNA Feedback Output (for R_{IZ}).
14	NC	Not Connected.
15	LMD3	CH 3 LNA Midsupply Pin; Connect a Capacitor for Midsupply HF Bypass.
16	INH3	CH3 LNA Input.
17	COM3	CH3 LNA Ground.
18	COM4	CH4 LNA Ground.
19	INH4	CH4 LNA Input.
20	LMD4	CH 4 LNA Midsupply Pin; Connect a Capacitor for Midsupply HF Bypass.
21	NC	Not Connected.
22	LON4	CH4 LNA Feedback Output (for R_{IZ}).
23	LOP4	CH4 LNA Positive Output.
24	VIP4	CH4 VGA Positive Input.
25	VIN4	CH4 VGA Negative Input.
26	VPS4	CH4 LNA Supply 5 V.

Pin No.	Mnemonic	Description
27	GAIN34	Gain Control Voltage for CH3 and CH4.
28	CLMP34	Output Clamping Level Input for CH3 and CH4.
29	HILO	VGA Gain Range Select (HI or LO).
30	VCM4	CH4 Common-Mode Voltage—AC Bypass.
31	VCM3	CH3 Common-Mode Voltage—AC Bypass.
32	NC	No Connect.
33	COM34	VGA Ground CH3 and CH4.
34	VOH4	CH4 Positive VGA Output.
35	VOL4	CH4 Negative VGA Output.
36	VPS34	VGA Supply 5 V CH3 and CH4.
37	VOL3	CH3 Negative VGA Output.
38	VOH3	CH3 Positive VGA Output.
39	COM34	VGA Ground CH3 and CH4.
40	NC	No Connect.
41	MODE	Gain Control Slope, Logic Input, 0 = Positive.
42	COM12	VGA Ground CH1 and CH2.
43	VOH2	CH2 Positive VGA Output.
44	VOL2	CH2 Negative VGA Output.
45	VPS12	CH2 VGA Supply 5 V CH1 and CH2.
46	VOL1	CH1 Negative VGA Output.
47	VOH1	CH1 Positive VGA Output.
48	COM12	VGA Ground CH1 and CH2.
49	VCM2	CH2 Common-Mode Voltage—AC Bypass.
50	VCM1	CH1 Common-Mode Voltage—AC Bypass.
51	EN34	Shared LNA/VGA Enable CH3 and CH4.
52	EN12	Shared LNA/VGA Enable CH1 and CH2.
53	CLMP12	Output Clamping Level Input CH1 and CH2.
54	GAIN12	Gain Control Voltage CH1 and CH2.
55	VPS1	CH1 LNA Supply 5 V.
56	VIN1	CH1 VGA Negative Input.
57	VIP1	CH1 VGA Positive Input.
58	LOP1	CH1 LNA Positive Output.
59	LON1	CH1 LNA Feedback Output (for R_{IZ}).
60	NC	Not Connected.
61	LMD1	CH 1 LNA Midsupply Pin; Connect a Capacitor for Midsupply HF Bypass.
62	INH1	CH1 LNA Input.
63	COM1	CH1 LNA Ground.
64	COM2	CH2 LNA Ground.
	EPAD	The exposed paddle must be soldered to the PCB ground to ensure proper heat dissipation, noise, and mechanical strength benefits.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5 V, R_L = 500 Ω, R_S = R_{IN} = 50 Ω, R_{IZ} = 280 Ω, C_{SH} = 22 pF, f = 10 MHz, R_{CLMP} = ∞, C_L = 1 pF, VCM pin floating, −4.5 dB to +43.5 dB gain (HILO = LO), and differential output voltage, unless otherwise specified.

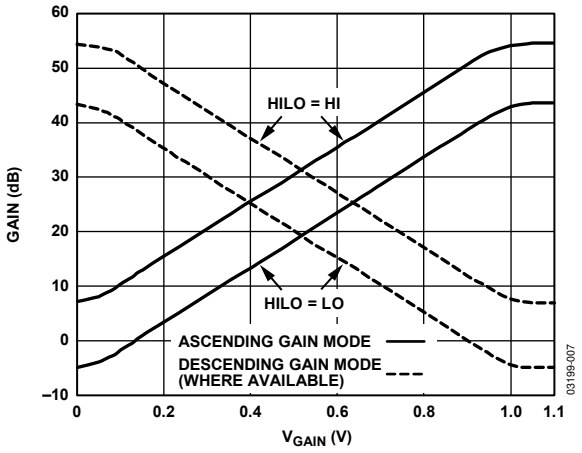

Figure 7. Gain vs. V_{GAIN} and MODE (MODE Available on RU Package)

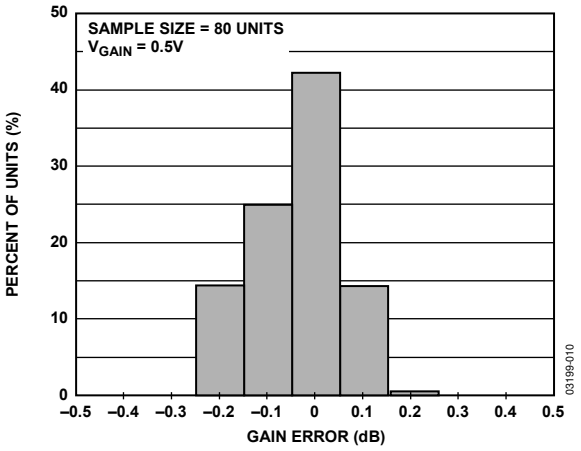

Figure 10. Gain Error Histogram

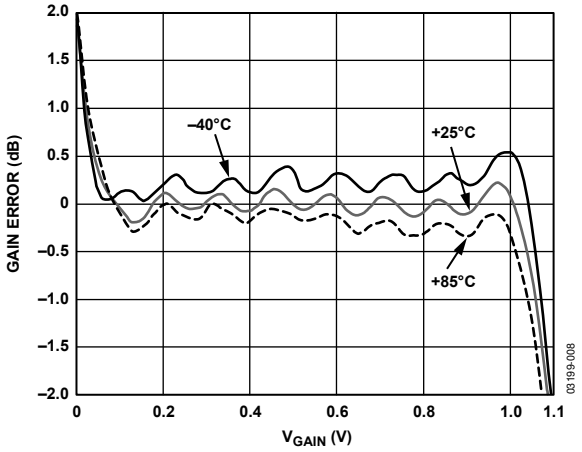

Figure 8. Absolute Gain Error vs. V_{GAIN} at Three Temperatures

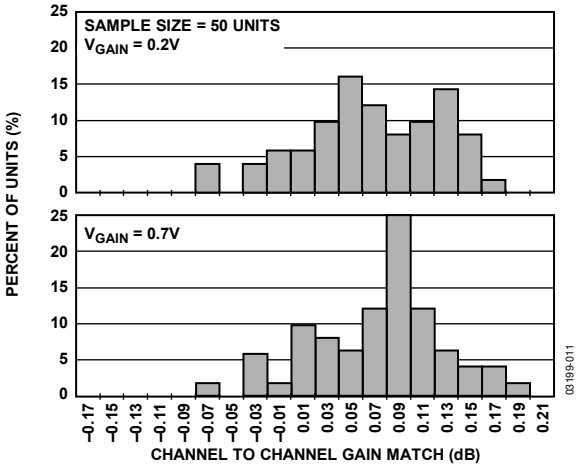

Figure 11. Gain Match Histogram for V_{GAIN} = 0.2 V and 0.7 V

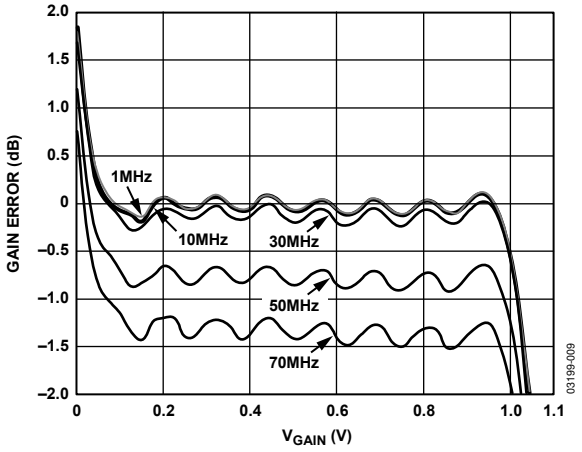

Figure 9. Absolute Gain Error vs. V_{GAIN} at Various Frequencies

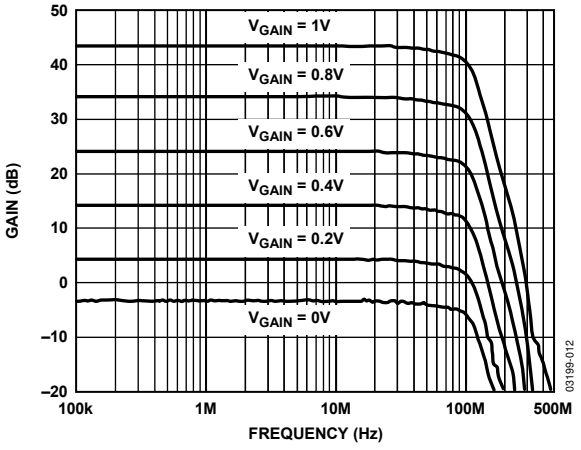

Figure 12. Frequency Response for Various Values of V_{GAIN}

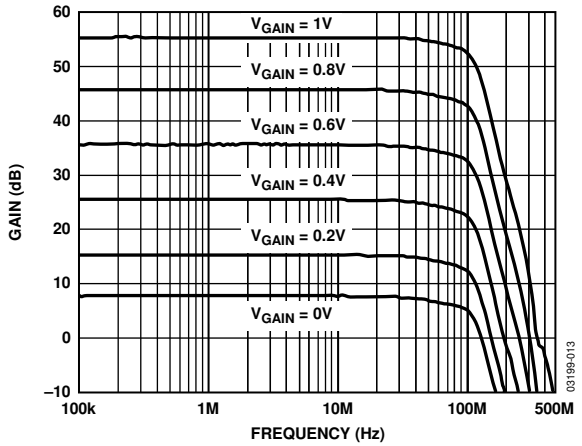

Figure 13. Frequency Response for Various Values of V_{GAIN}, HILO = HI

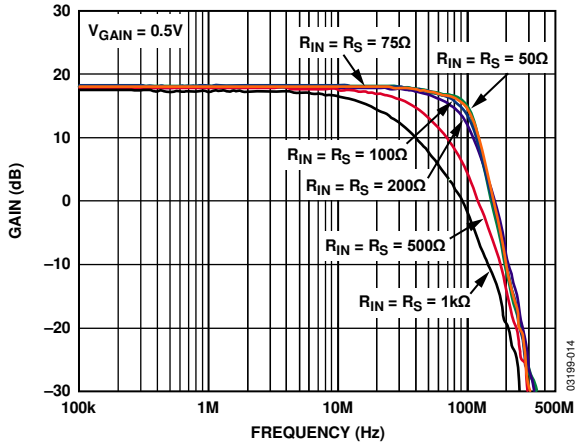

Figure 14. Frequency Response for Various Matched Source Impedances

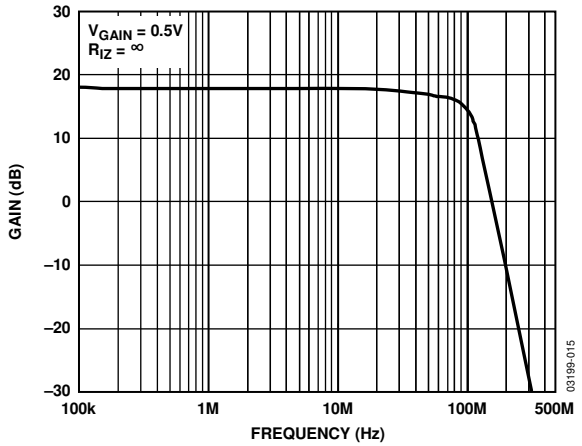

Figure 15. Frequency Response, Unterminated LNA, R_S = 50 Ω

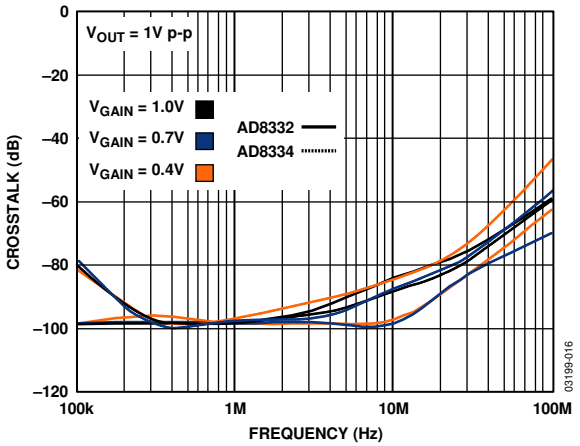

Figure 16. Channel-to-Channel Crosstalk vs. Frequency for Various Values of V_{GAIN}

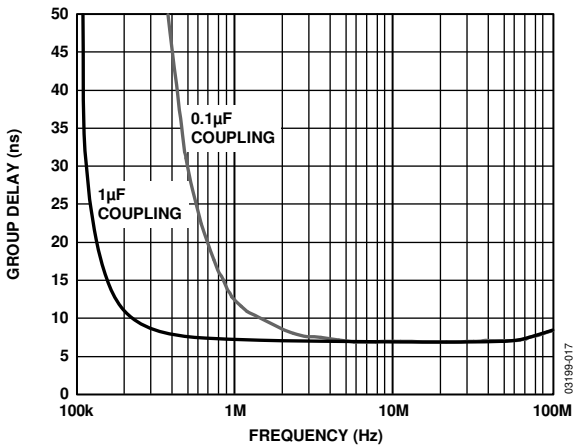

Figure 17. Group Delay vs. Frequency for Two Values of AC Coupling

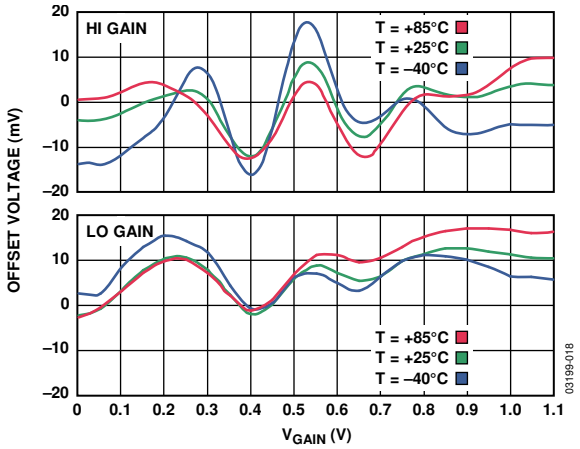

Figure 18. Representative Differential Output Offset Voltage vs. V_{GAIN} at Three Temperatures

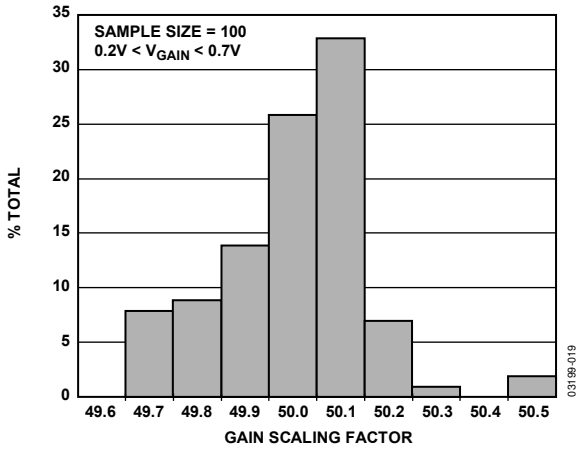

Figure 19. Gain Scaling Factor Histogram

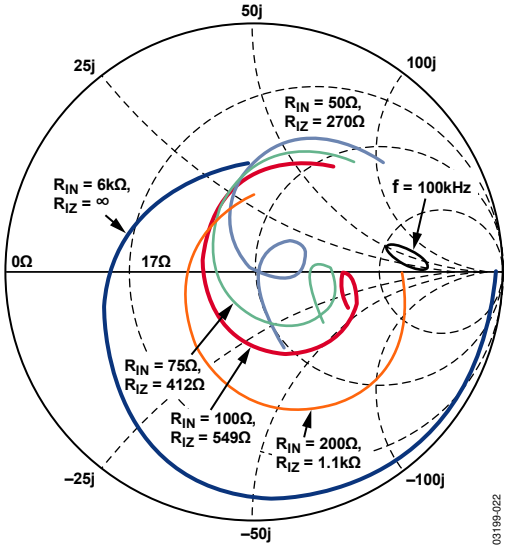

Figure 22. Smith Chart, S11 vs. Frequency, 0.1 MHz to 200 MHz for Various Values of R_{IZ}

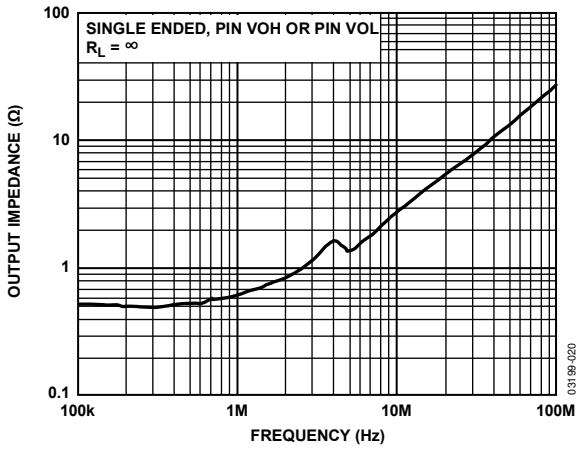

Figure 20. Output Impedance vs. Frequency

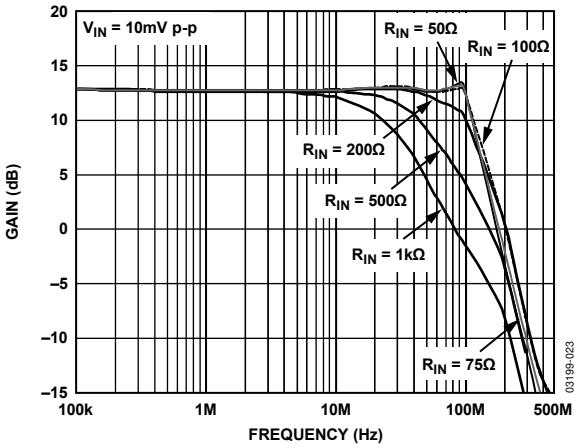

Figure 23. LNA Frequency Response, Single-Ended, for Various Values of R_{IN}

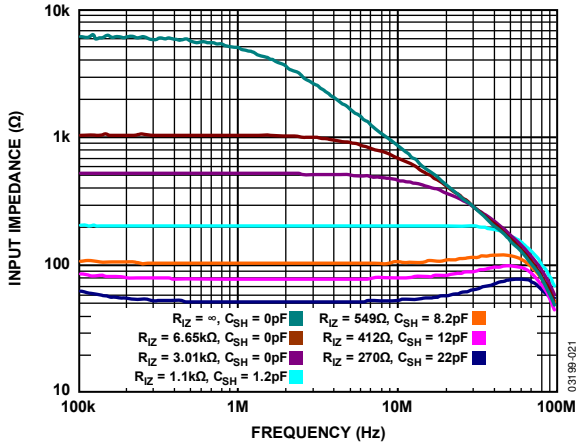

Figure 21. LNA Input Impedance vs. Frequency for Various Values of R_{IZ} and C_{SH}

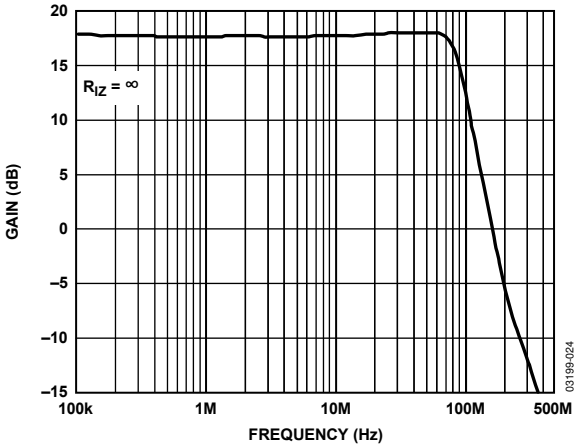

Figure 24. Frequency Response for Unterminated LNA, Single-Ended

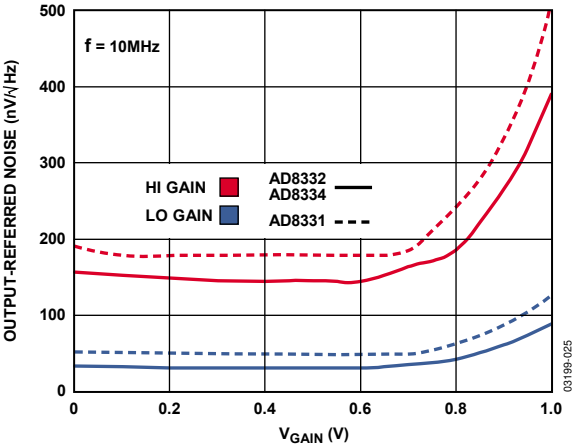

Figure 25. Output-Referred Noise vs. V_{GAIN}

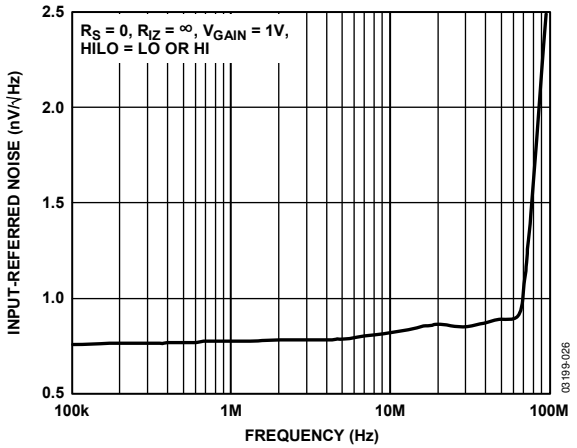

Figure 26. Short-Circuit, Input-Referred Noise vs. Frequency

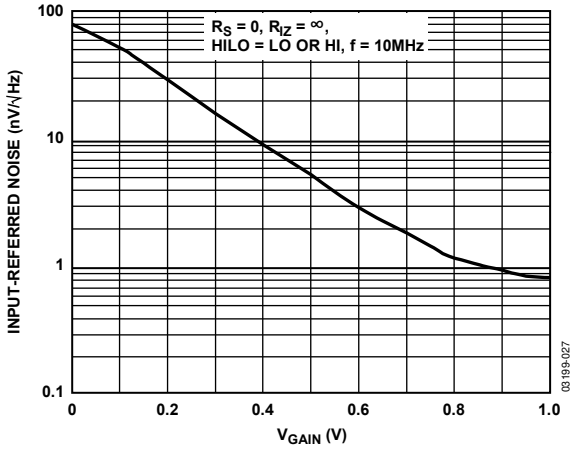

Figure 27. Short-Circuit, Input-Referred Noise vs. V_{GAIN}

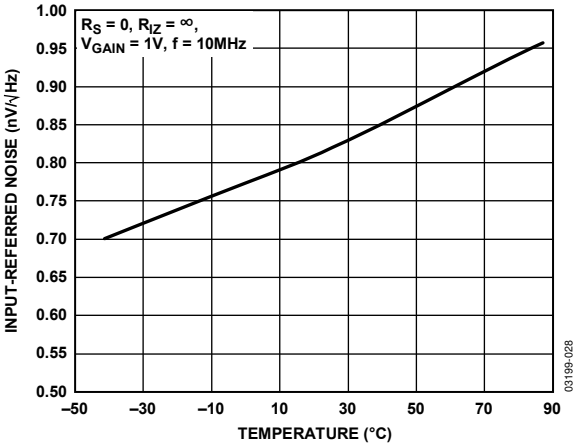

Figure 28. Short-Circuit, Input-Referred Noise vs. Temperature

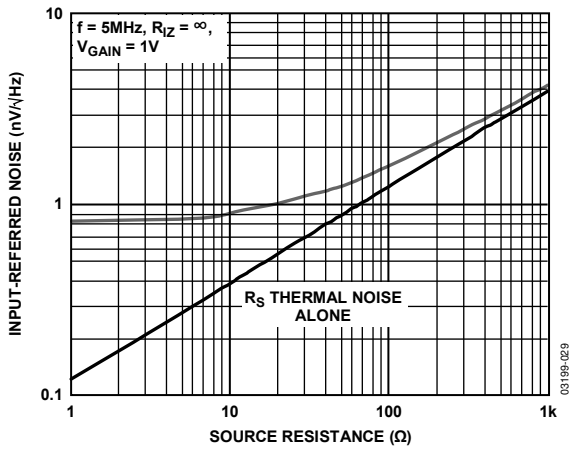

Figure 29. Input-Referred Noise vs. R_S

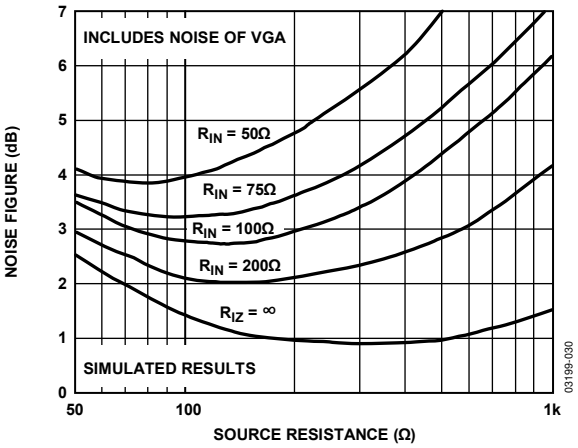

Figure 30. Noise Figure vs. R_S for Various Values of R_{IN}

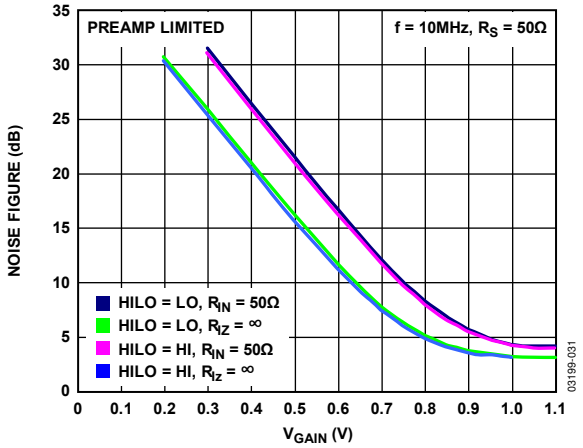

Figure 31. Noise Figure vs. V_{GAIN}

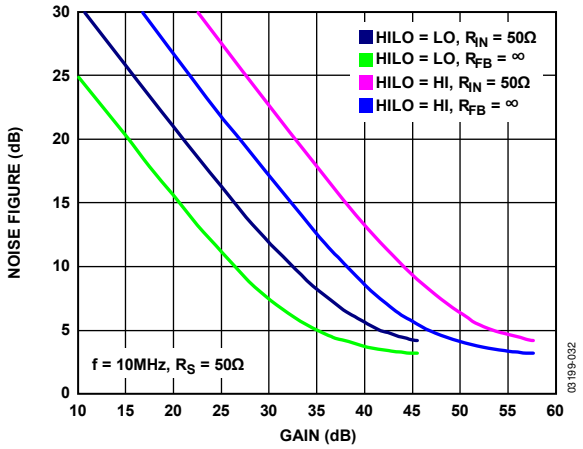

Figure 32. Noise Figure vs. Gain

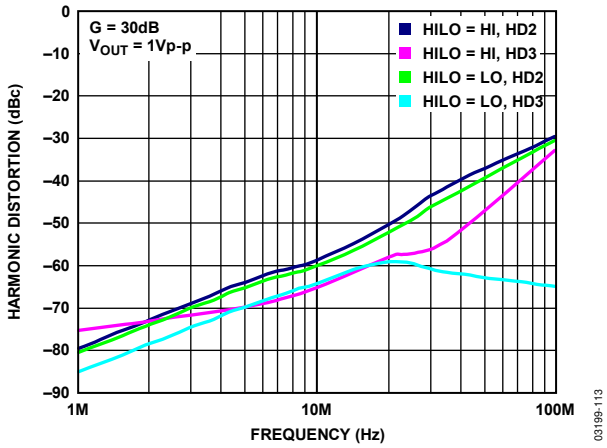

Figure 33. Harmonic Distortion vs. Frequency

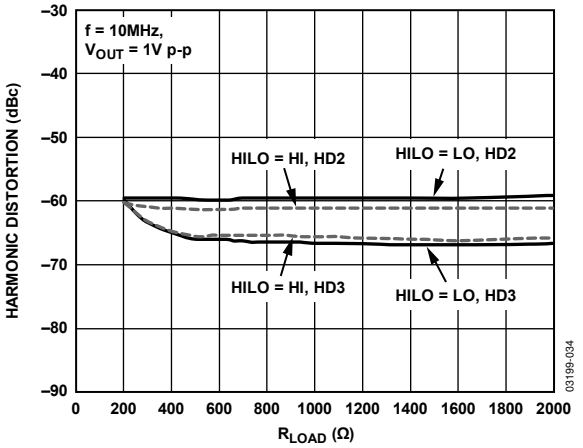

Figure 34. Harmonic Distortion vs. R_{LOAD}

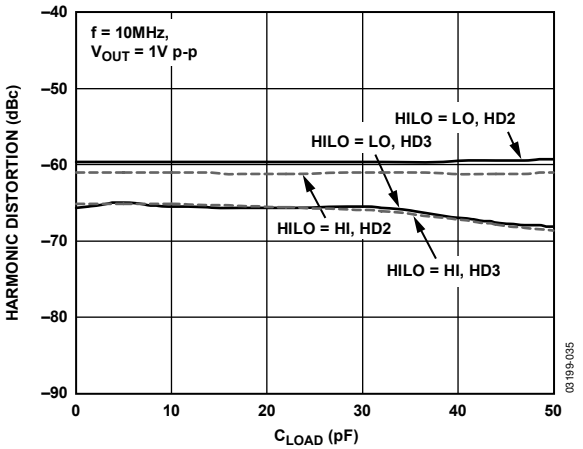

Figure 35. Harmonic Distortion vs. C_{LOAD}

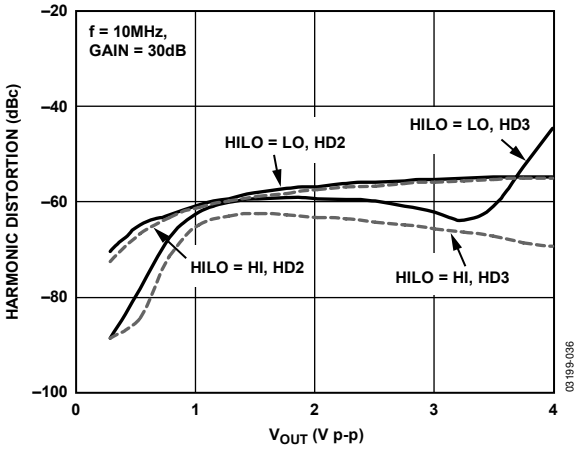

Figure 36. Harmonic Distortion vs. Differential Output Voltage

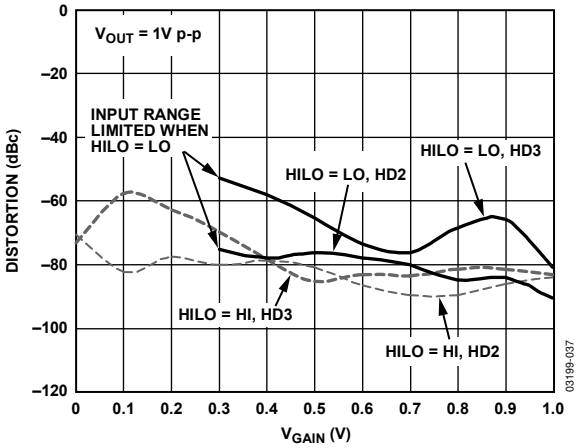

Figure 37. Harmonic Distortion vs. V_{GAIN}, f = 1 MHz

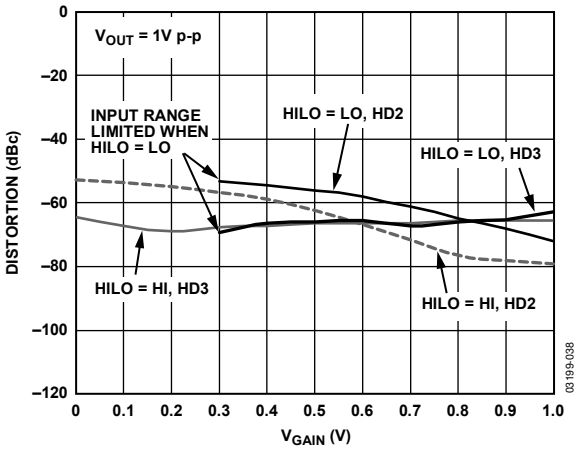

Figure 38. Harmonic Distortion vs. V_{GAIN}, f = 10 MHz

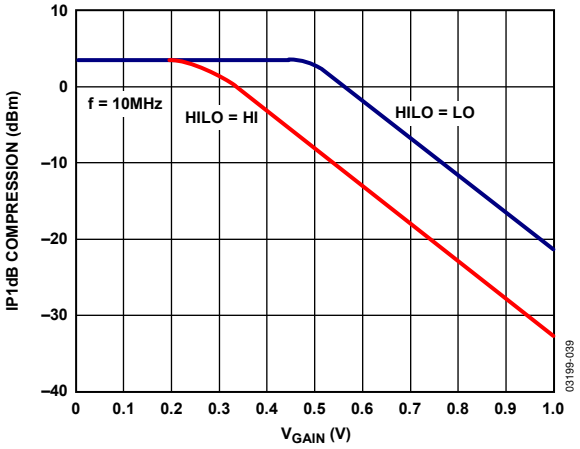

Figure 39. IP1dB Compression vs. V_{GAIN}

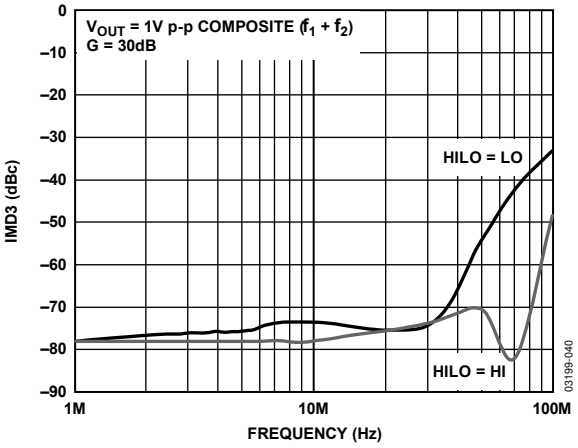

Figure 40. IMD3 vs. Frequency

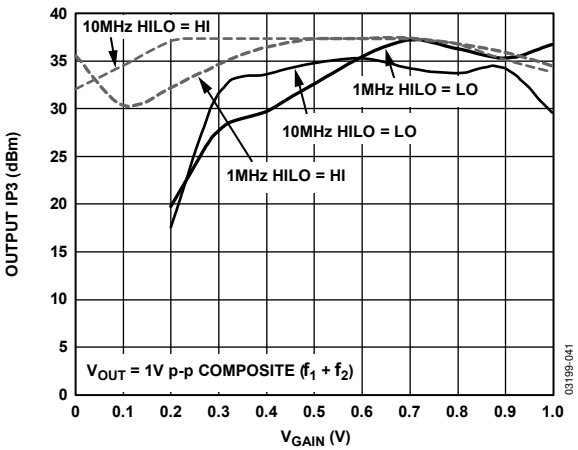

Figure 41. Output Third-Order Intercept (IP3) vs. V_{GAIN}

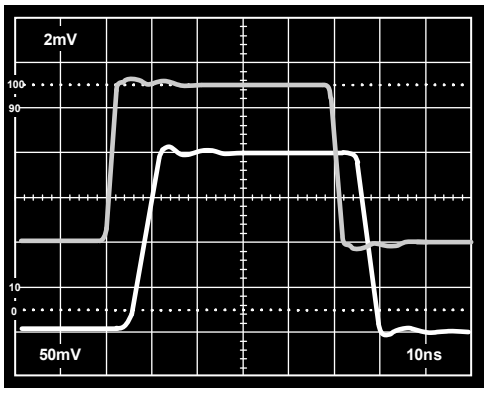

Figure 42. Small Signal Pulse Response, G = 30 dB, Top: Input, Bottom: Output Voltage, HILO = HI or LO

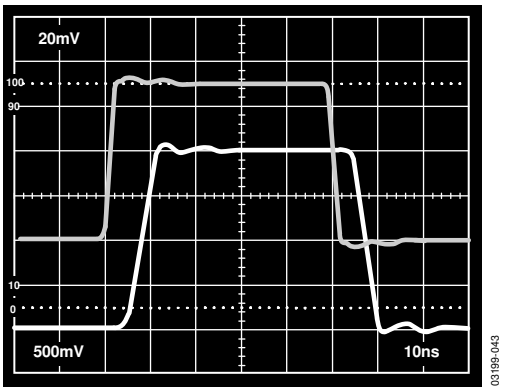

Figure 43. Large Signal Pulse Response, G = 30 dB, HILO = HI or LO, Top: Input, Bottom: Output Voltage

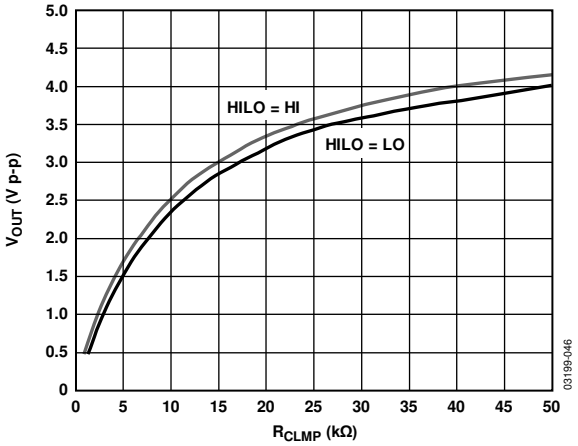

Figure 46. Clamp Level vs. R_{CLMP}

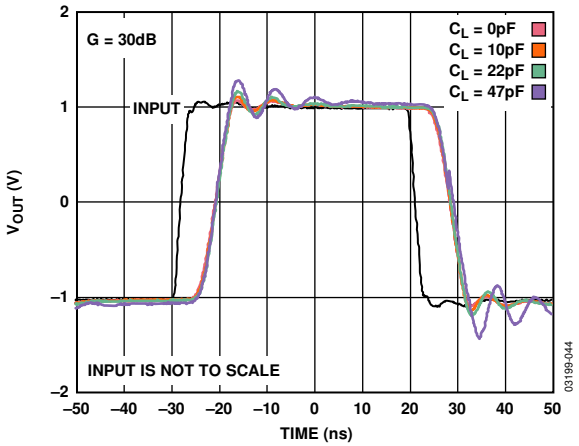

Figure 44. Large Signal Pulse Response for Various Capacitive Loads, C_L = 0 pF, 10 pF, 20 pF, 50 pF

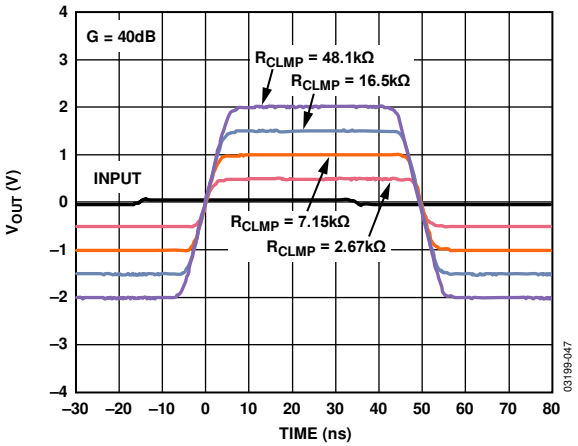

Figure 47. Clamp Level Pulse Response for Four Values of R_{CLMP}

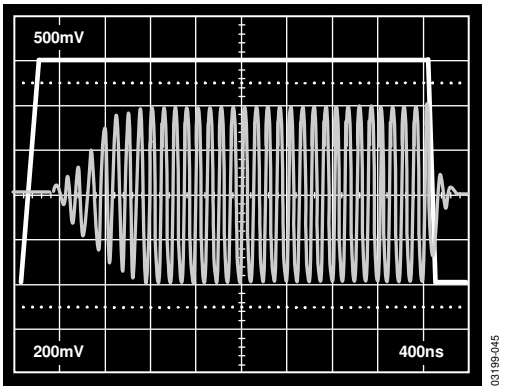

Figure 45. Pin GAIN Transient Response, Top: V_{GAIN}, Bottom: Output Voltage

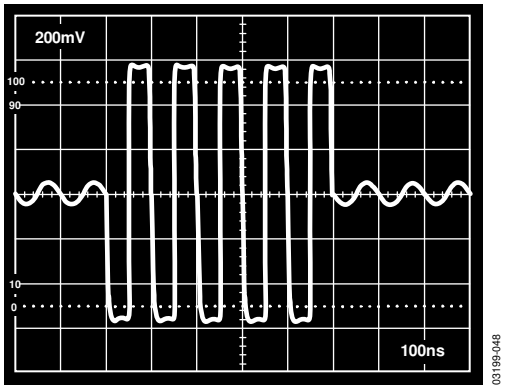

Figure 48. LNA Overdrive Recovery, V_{INH} 0.05 V p-p to 1 V p-p Burst, V_{GAIN} = 0.27 V VGA Output Shown

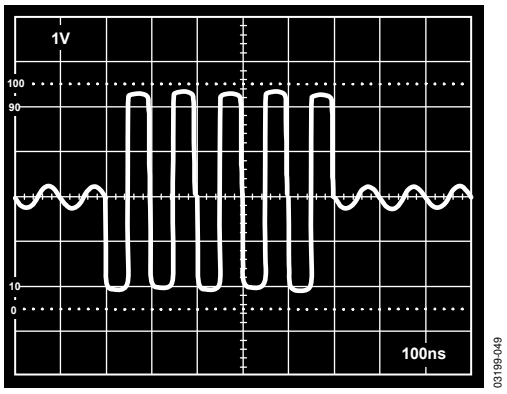

Figure 49. VGA Overdrive Recovery, V_{INH} 4 mV p-p to 70 mV p-p Burst, V_{GAIN} = 1 V VGA Output Shown Attenuated by 24 dB

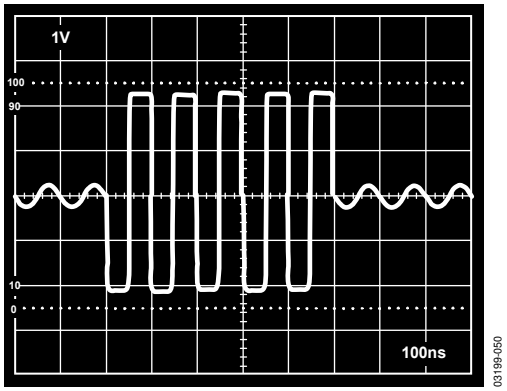

Figure 50. VGA Overdrive Recovery, V_{INH} 4 mV p-p to 275 mV p-p Burst, V_{GAIN} = 1 V VGA Output Shown Attenuated by 24 dB

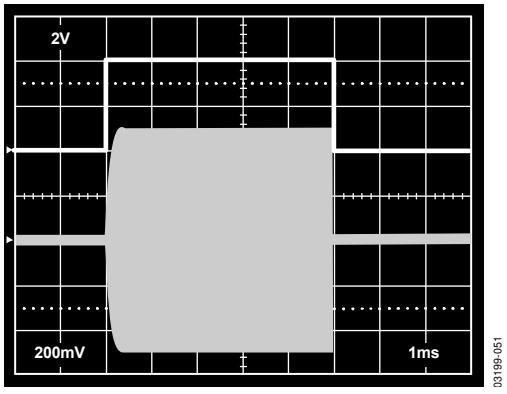

Figure 51. Enable Response, Top: V_{ENB}, Bottom: V_{OUT}, V_{INH} = 30 mV p-p

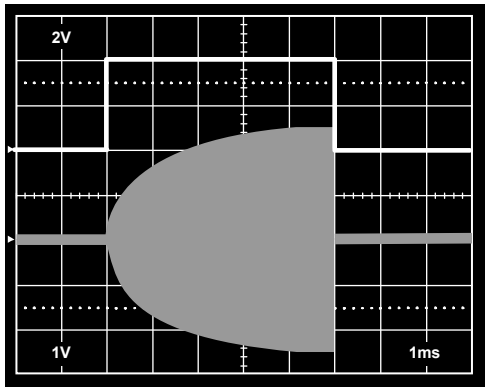

Figure 52. Enable Response, Large Signal, Top: V_{ENB}, Bottom: V_{OUT}, V_{INH} = 150 mV p-p

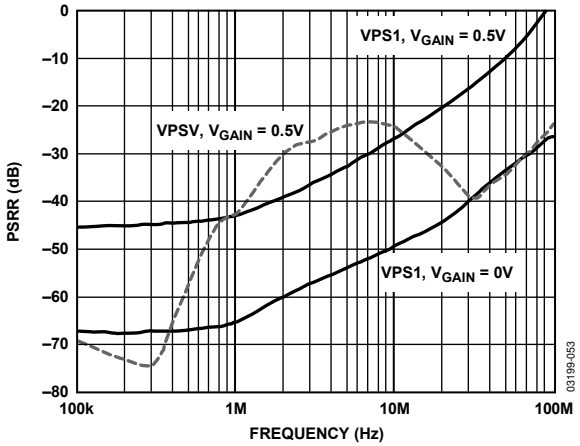

Figure 53. PSRR vs. Frequency (No Bypass Capacitor)

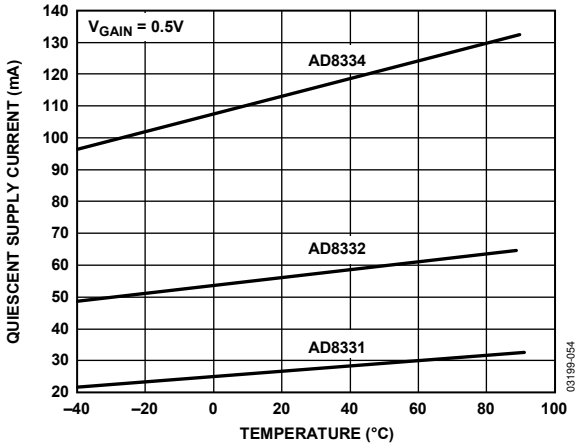

Figure 54. Quiescent Supply Current vs. Temperature

TEST CIRCUITS

MEASUREMENT CONSIDERATIONS

Figure 55 through Figure 68 show typical measurement configurations and proper interface values for measurements with 50 Ω conditions.

Short-circuit input noise measurements are made as shown in Figure 62. The input-referred noise level is determined by dividing the output noise by the numerical gain between Point A and Point B and accounting for the noise floor of the spectrum analyzer. The gain should be measured at each frequency of interest and with low signal levels because a 50 Ω load is driven directly. The generator is removed when noise measurements are made.

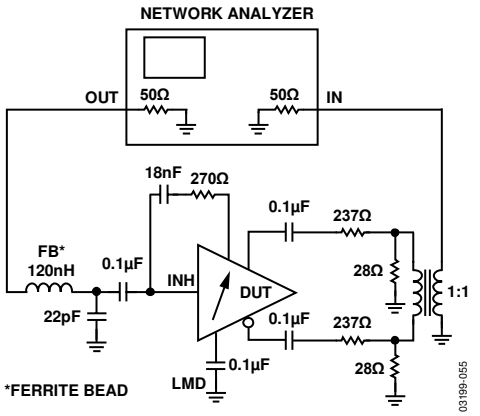

Figure 55. Test Circuit—Gain and Bandwidth Measurements

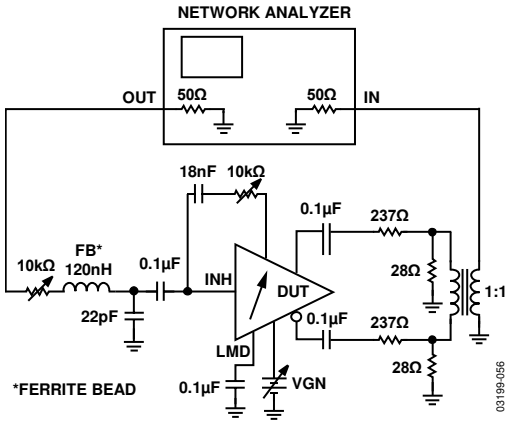

Figure 56. Test Circuit—Frequency Response for Various Matched Source Impedances

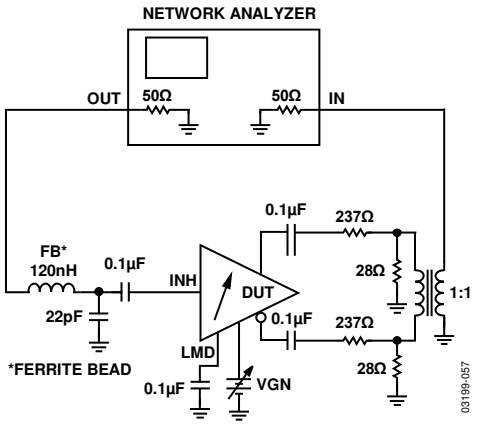

Figure 57. Test Circuit—Frequency Response for Unterminated LNA, R_S = 50 Ω

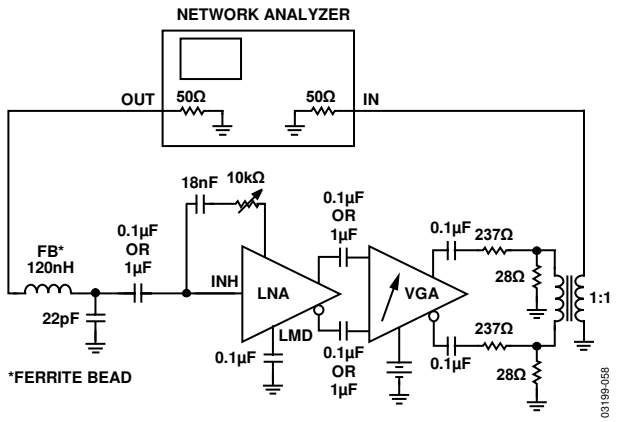

Figure 58. Test Circuit—Group Delay vs. Frequency for Two Values of AC Coupling

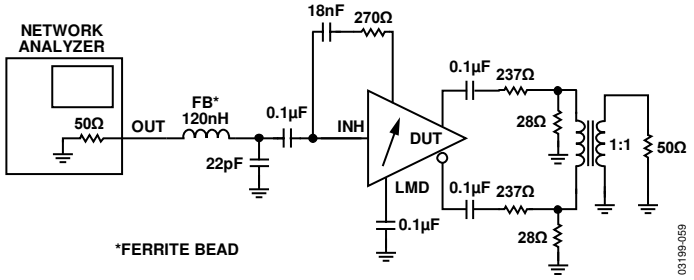

Figure 59. Test Circuit—LNA Input Impedance vs. Frequency in Standard and Smith Chart (S11) Formats

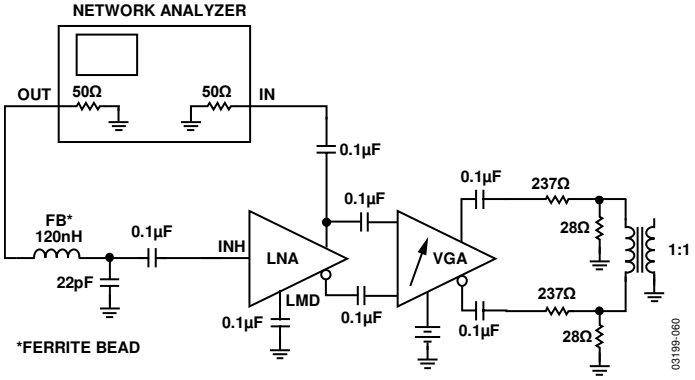

Figure 60. Test Circuit—Frequency Response for Unterminated LNA, Single-Ended

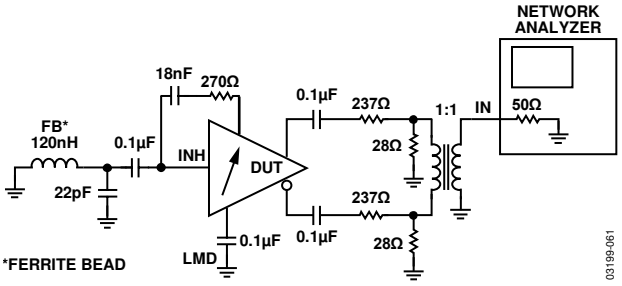

Figure 61. Test Circuit—Short-Circuit, Input-Referred Noise

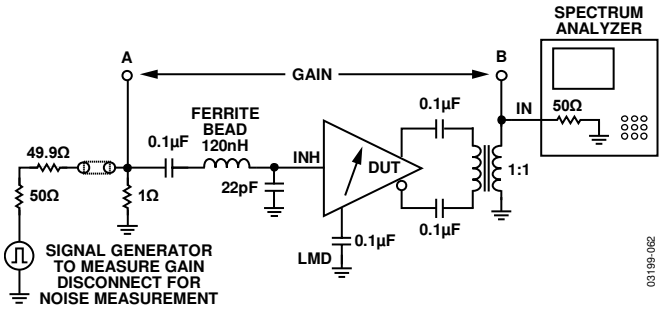

Figure 62. Test Circuit—Noise Figure

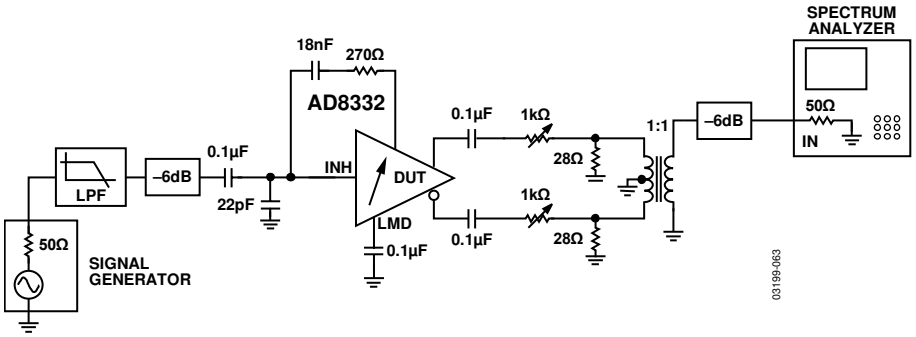

Figure 63. Test Circuit—Harmonic Distortion vs. Load Resistance

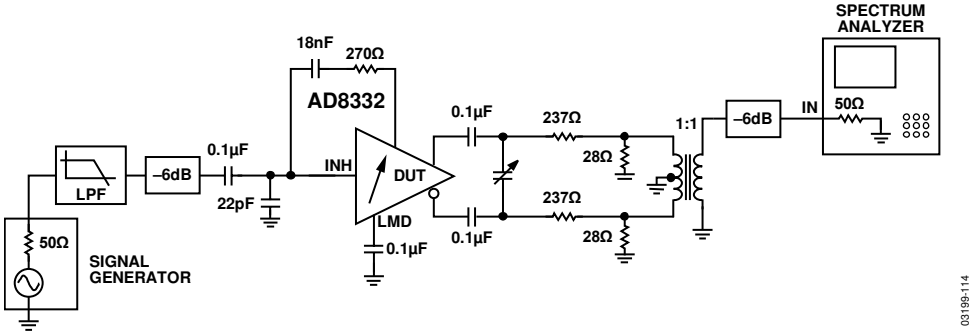

Figure 64. Test Circuit—Harmonic Distortion vs. Load Capacitance

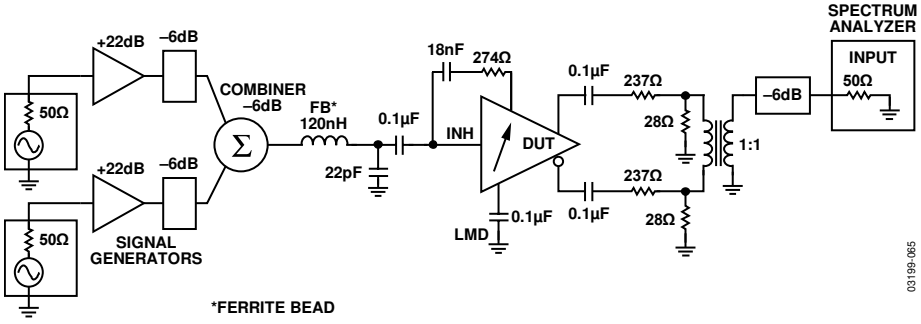

Figure 65.Test Circuit—IMD3 vs. Frequency

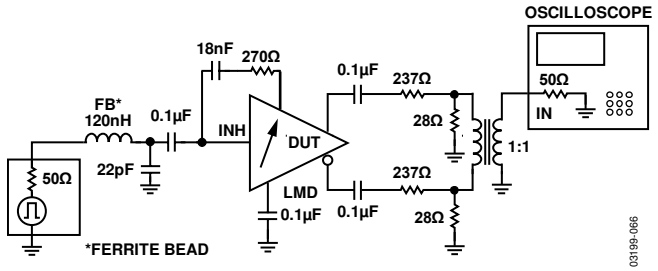

Figure 66. Test Circuit—Pulse Response Measurements

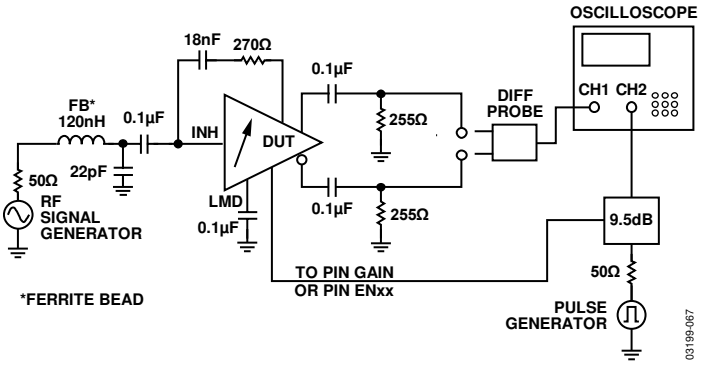

Figure 67. Test Circuit—Gain and Enable Transient Response

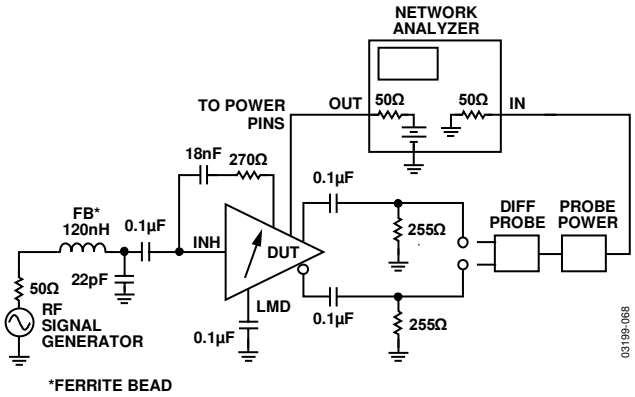

Figure 68. Test Circuit—PSRR vs. Frequency

THEORY OF OPERATION

OVERVIEW

The AD8331/AD8332/AD8334 operate in the same way. Figure 69, Figure 70, and Figure 71 are functional block diagrams of the three devices

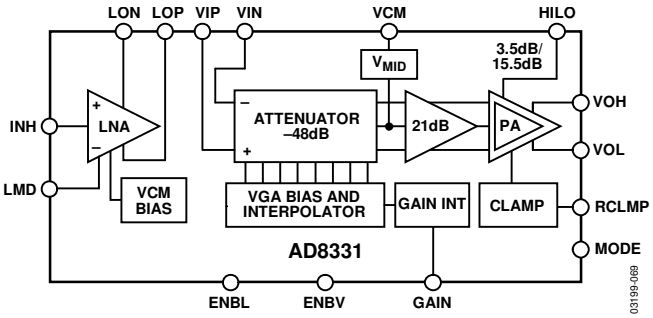

Figure 69. AD8331 Functional Block Diagram

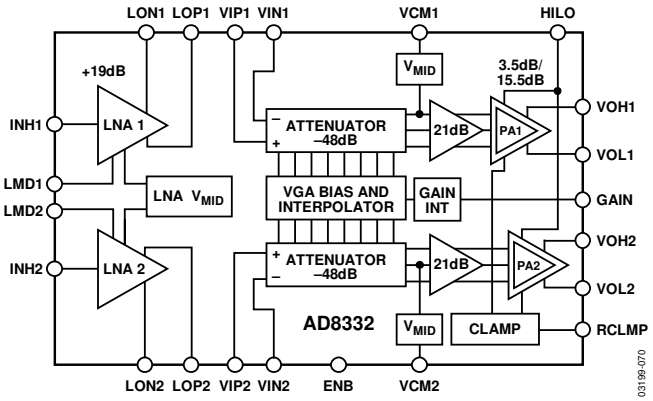

Figure 70. AD8332 Functional Block Diagram

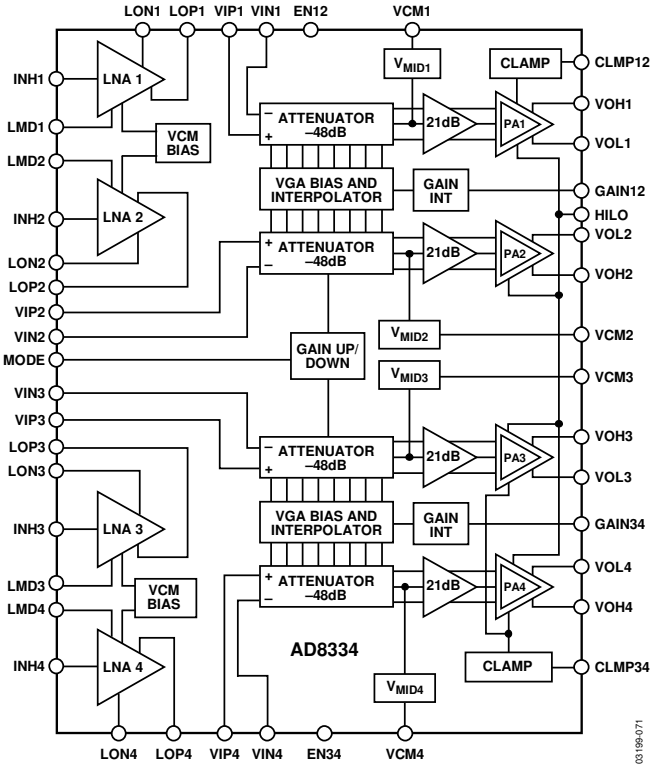

Figure 71. AD8334 Functional Block Diagram

Each channel contains an LNA that provides user-adjustable input impedance termination, a differential X-AMP VGA, and a programmable gain postamp with adjustable output voltage limiting. Figure 72 shows a simplified block diagram with external components.

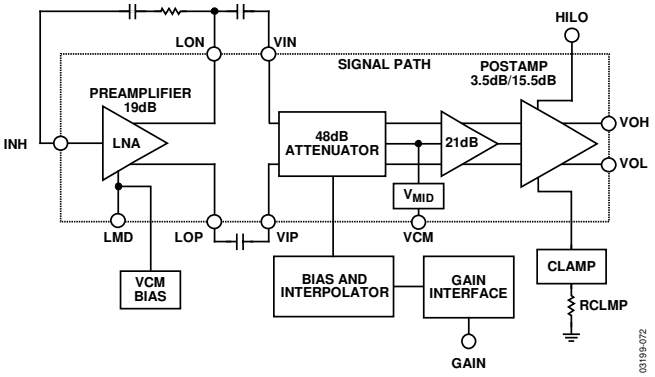

Figure 72. Simplified Block Diagram

The linear-in-dB, gain control interface is trimmed for slope and absolute accuracy. The gain range is +48 dB, extending from −4.5 dB to +43.5 dB in LO gain and +7.5 dB to +55.5 dB in HI gain mode. The slope of the gain control interface is 50 dB/V, and the gain control range is 40 mV to 1 V. Equation 1 and Equation 2 are the expressions for gain.

$$GAIN\ (\text{dB}) = 50\ (\text{dB/V}) \times V_{GAIN} - 6.5\ \text{dB},\ (HILO = LO) \quad (1)$$

or

$$GAIN\ (\text{dB}) = 50\ (\text{dB/V}) \times V_{GAIN} + 5.5\ \text{dB},\ (HILO = HI) \quad (2)$$

The ideal gain characteristics are shown in Figure 73.

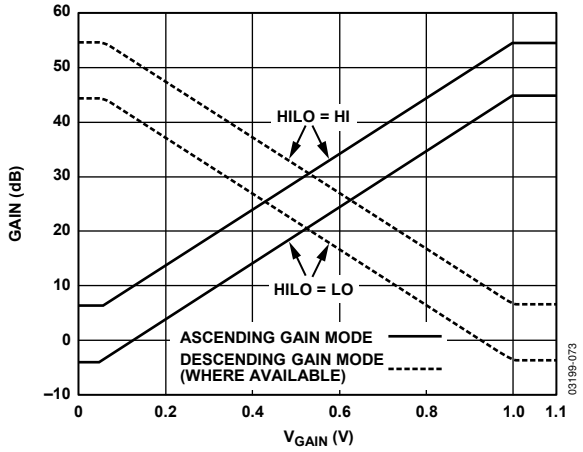

Figure 73. Ideal Gain Control Characteristics

The gain slope is negative with MODE pulled high (where available), as follows:

$$GAIN\ (\text{dB}) = -50\ (\text{dB/V}) \times V_{GAIN} + 45.5\ \text{dB},\ (HILO = LO) \quad (3)$$

or

$$GAIN\ (\text{dB}) = -50\ (\text{dB/V}) \times V_{GAIN} + 57.5\ \text{dB},\ (HILO = HI) \quad (4)$$

The LNA converts a single-ended input to a differential output with a voltage gain of 19 dB. If only one output is used, the gain is 13 dB. The inverting output is used for active input impedance termination. Each of the LNA outputs is capacitively coupled to a VGA input. The VGA consists of an attenuator with a range of 48 dB followed by an amplifier with 21 dB of gain for a net gain range of −27 dB to +21 dB. The X-AMP, gain interpolation technique results in low gain error and uniform bandwidth, and differential signal paths minimize distortion.

The final stage is a logic programmable amplifier with gains of 3.5 dB or 15.5 dB. The LO and HI gain modes are optimized for 12-bit and 10-bit ADC applications, in terms of output-referred noise and absolute gain range. Output voltage limiting can be programmed by the user.

LOW NOISE AMPLIFIER (LNA)

Good noise performance in the AD8331/AD8332/AD8334 relies on a proprietary ultralow noise preamplifier at the beginning of the signal chain, which minimizes the noise contribution in the following VGA. Active impedance control optimizes noise performance for applications that benefit from input matching.

A simplified schematic of the LNA is shown in Figure 74. INH is capacitively coupled to the source. A bias generator establishes dc input bias voltages of 3.25 V and centers the output common-mode levels at 2.5 V. A capacitor C_{LMD} (can be the same value as the input coupling capacitor C_{INH}) is connected from the LMD pin to ground to decouple the LMD bus. The LMD pin is not useable for configuring the LNA as a differential input amplifier.

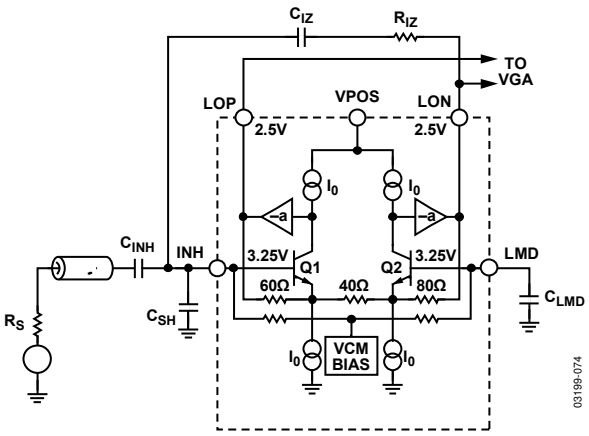

Figure 74. Simplified LNA Schematic

The LNA supports differential output voltages as high as 5 V p-p, with positive and negative excursions of ±1.25 V, about a common-mode voltage of 2.5 V. Because the differential gain magnitude is 9, the maximum input signal before saturation is ±275 mV or +550 mV p-p. Overload protection ensures quick recovery time from large input voltages. Because the inputs are capacitively coupled to a bias voltage near midsupply, very large inputs can be handled without interacting with the ESD protection.

Low value feedback resistors and the current-driving capability of the output stage allow the LNA to achieve a low input-referred voltage noise of 0.74 nV/√Hz. This is achieved with a current consumption of only 11 mA per channel (55 mW). On-chip resistor matching results in precise single-ended gains of 4.5× (9× differential), critical for accurate impedance control. The use of a fully differential topology and negative feedback minimizes distortion. Low HD2 is particularly important in second harmonic ultrasound imaging applications. Differential signaling enables smaller swings at each output, further reducing third-order distortion.