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0.8 GHz to 2.7 GHz Direct Conversion Quadrature Demodulator

AD8347

FEATURES

Integrated RF and baseband AGC amplifiers
Quadrature phase accuracy 1° typ
I/Q amplitude balance 0.3 dB typ
Third-order intercept (IIP3) +11.5 dBm @ min gain
Noise figure 11 dB @ max gain
AGC range 69.5 dB
Baseband level control circuit
Low LO drive −8 dBm
ADC-compatible I/Q outputs
Single supply 2.7 V to 5.5 V
Power-down mode
28-lead TSSOP package

APPLICATIONS

Cellular base stations
Radio links
Wireless local loop
IF broadband demodulators
RF instrumentation
Satellite modems

FUNCTIONAL BLOCK DIAGRAM

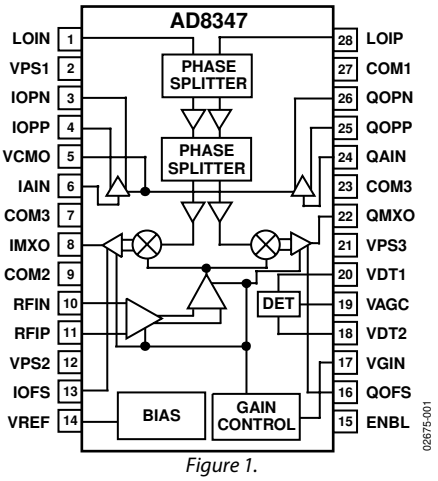

Figure 1.

GENERAL DESCRIPTION

The AD8347[1] is a broadband direct quadrature demodulator with RF and baseband automatic gain control (AGC) amplifiers. It is suitable for use in many communications receivers, performing quadrature demodulation directly to baseband frequencies. The input frequency range is 800 MHz to 2.7 GHz. The outputs can be connected directly to popular A-to-D converters such as the AD9201 and AD9283.

The RF input signal goes through two stages of variable gain amplifiers prior to two Gilbert-cell mixers. The LO quadrature phase splitter employs polyphase filters to achieve high quadrature accuracy and amplitude balance over the entire operating frequency range. Separate I and Q channel variable gain amplifiers follow the baseband outputs of the mixers. The RF and baseband amplifiers together provide 69.5 dB of gain control. A precision control circuit sets the linear-in-dB RF gain response to the gain control voltage.

Baseband level detectors are included for use in an AGC loop to maintain the output level. The demodulator dc offsets are minimized by an internal loop, whose time constant is controlled by external capacitor values. The offset control can also be overridden by forcing an external voltage at the offset nulling pins.

The baseband variable gain amplifier outputs are brought off-chip for filtering before final amplification. By inserting a channel selection filter before each output amplifier, high level out-of-channel interferers are eliminated. Additional internal circuitry also allows the user to set the dc common-mode level at the baseband outputs.

[1] U.S. patents issued and pending.

Rev. A

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AD8347* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD8347 Evaluation Board

DOCUMENTATION

Application Notes

- AN-924: Digital Quadrature Modulator Gain

Data Sheet

- AD8347: 0.8 GHz to 2.7 GHz Direct Conversion Quadrature Demodulator Data Sheet

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- Simplifying Direct-Conversion Tx Paths in Wireless Designs
- Single Chip Realizes Direct-Conversion Rx
- Techniques Simplify Wireless Transmission

DESIGN RESOURCES

- AD8347 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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SAMPLE AND BUY

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TABLE OF CONTENTS

REVISION HISTORY

10/05—Rev. 0 to Rev. A

Updated Format ... Universal
Change V_{GIN} to V_{VGIN} ... Universal
Changes to Figure 46 ... 19
Changes to Figure 48 ... 21
Changes to Figure 49 and Figure 50 ... 22
Changes to Ordering Guide ... 27

10/01—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V; T_A = 25°C; F_{LO} = 1.9 GHz; V_{VCMO} = 1 V; F_{RF} = 1.905 GHz; P_{LO} = −8 dBm, R_{LOAD} = 10 kΩ, dBm with respect to 50 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO/RF Frequency Range		0.8		2.7	GHz
LO Input Level		−10		0	dBm
VGIN Input Level		0.2		1.2	V
V_{SUPPLY} (V_S)		2.7		5.5	V
Temperature Range		−40		+85	°C
RF AMPLIFIER/DEMODULATOR	From RFIP/RFIN to IMXO and QMXO (IMXO/QMXO load > 1 kΩ)				
AGC Gain Range			69.5		dB
Conversion Gain (Max)	V_{VGIN} = 0.2 V (max gain)		39.5		dB
Conversion Gain (Min)	V_{VGIN} = 1.2 V (min gain)		−30		dB
Gain Linearity	V_{VGIN} = 0.3 V to 1 V		±2		dB
Gain Flatness	F_{LO} = 0.8 GHz to 2.7 GHz, F_{BB} = 1 MHz		+0.7		dB p-p
Input P1 dB	V_{VGIN} = 0.2 V		−30		dBm
	V_{VGIN} = 1.2 V		−2		dBm
Third-Order Input Intercept (IIP3)	F_{RF1} = 1.905 GHz,		+11.5		dBm
	F_{RF2} = 1.906 GHz, −10 dBm each tone, (min gain)				
Second-Order Input Intercept (IIP2)	F_{RF1} = 1.905 GHz,		+25.5		dBm
	F_{RF2} = 1.906 GHz, −10 dBm each tone, (min gain)				
LO Leakage (RF)	At RFIP		−60		dBm
LO Leakage (MXO)	At IMXO/QMXO		−42		dBm
Demodulation Bandwidth	−3 dB		+90		MHz
Quadrature Phase Error	F_{RF} = 1.9 GHz	−3	±1	+3	degree
I/Q Amplitude Imbalance	F_{RF} = 1.9 GHz		+0.3		dB
Noise Figure	Max Gain		11		dB
Mixer AGC Output Level	See Figure 34		24		mV p-p
Baseband DC Offset	At IMXO/QMXO, max gain (corrected, REF to VREF)		2		mV
Mixer Output Swing	Level at which IMD3 = 45 dBc				
	R_{LOAD} = 200 Ω		65		mV p-p
	R_{LOAD} = 1 kΩ		65		mV p-p
Mixer Output Impedance			3		Ω
BASEBAND OUTPUT AMPLIFIER	From IAIN to IOPP/IOPN and QAIN to QOPP/QOPN				
	R_{LOAD} = 10 kΩ				
Gain			30		dB
Bandwidth	−3 dB (see Figure 22)		65		MHz
Output DC Offset (Differential)	(V_{IOPP} − V_{IOPN})	−200	±50	+200	mV
Common-Mode Offset	(V_{IOPP} + V_{IOPN})/2 − V_{VCMO}	−40	±5	+40	mV
Group Delay Flatness	0 MHz to 50 MHz		+1.8		ns p-p
Second-Order Intermod. Distortion	$F_{IN}1$ = 5 MHz, $F_{IN}2$ = 6 MHz, $V_{IN}1$ = $V_{IN}2$ = 8 mV p-p		−49		dBc
Third-Order Intermod. Distortion	$F_{IN}1$ = 5 MHz, $F_{IN}2$ = 6 MHz, $V_{IN}1$ = $V_{IN}2$ = 8 mV p-p		−67		dBc
Input Bias Current			+2		µA
Input Impedance			1||3		MΩ||pF
Output Swing Limit (Upper)		V_S − 1.3			V
Output Swing Limit (Lower)				0.4	V

Parameter	Conditions	Min	Typ	Max	Unit
CONTROL INPUT/OUTPUTS					
VCMO Input	@ V_S = 2.7 V		1		V
	@ V_S = 5 V	0.5	1	2.5	V
Gain Control Input Bias Current	VGIN		<1		µA
Offset Input Overriding Current	IOFS, QOFS		10		µA
VREF Output	R_{LOAD} = 10 kΩ	0.95	1.00	1.05	V
RESPONSE FROM RF INPUT TO FINAL BB AMP	IMXO and QMXO connected directly to IAIN and QAIN, respectively				
Gain @ V_{VGIN} = 0.2 V		65.5	69.5	72.5	dB
Gain @ V_{VGIN} = 1.2 V		−3	+0.5	+4	dB
Gain Slope		−96.5	−89	−82.5	dB/V
Gain Intercept	Linear extrapolation back to theoretical value at VGIN = 0	88	94	101	dB
LO/RF INPUT	(See Figure 30 through Figure 33 for more detail)				
LOIP Input Return Loss	Measuring LOIP LOIN, ac-coupled to ground with 100 pF.		−4		dB
	Measuring through evaluation board balun with termination		−9.5		dB
RFIP Input Return Loss	RFIP input pin		−10		dB
ENABLE					
Power-Up Control	Low = standby	0		0.5	V
Power-Up Control	High = enabled	$+V_S$ − 1		$+V_S$	V
Power-Up Time	Time for final BB amps to be within 90% of final amplitude				
	@ V_S = 5 V		20		µs
	@ V_S = 2.7 V		10		µs
Power-Down Time	Time for supply current to be <4 mA				
	@ V_S = 5 V		30		µs
	@ V_S = 2.7 V		1.5		ms
POWER SUPPLIES	VPS1, VPS2, VPS3				
Voltage		2.7		5.5	V
Current (Enabled)	@ 5 V	48	64	80	mA
Current (Standby)	@ 5 V		400		µA
Current (Standby)	@ 3.3 V		80		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPS1, VPS2, VPS3	5.5 V
LO and RF Input Power	10 dBm
Internal Power Dissipation	500 mW
θ_{JA}	68°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

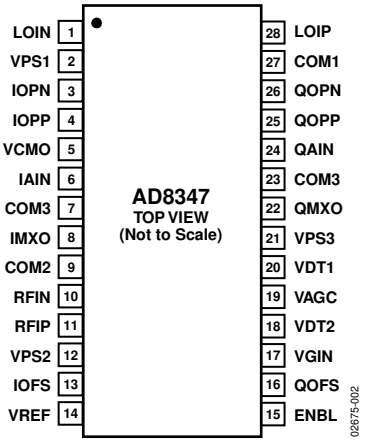

Figure 2. 28-Lead TSSOP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Equiv. Circuit	Description
1, 28	LOIN, LOIP	A	LO Input. For optimum performance, these inputs are differentially driven. Typical input drive level is equal to −8 dBm. To improve the match to a 50 Ω source, connect a 200 Ω shunt resistor between LOIP and LOIN. A single-ended drive is possible, but slightly increases LO leakage.
2	VPS1		Positive Supply for LO Section. Decouple VPS1 with 0.1 µF and 100 pF capacitors.
3, 4	IOPN, IOPP	B	I-Channel Differential Baseband Output. Typical output swing is equal to 760 mV p-p differential in AGC mode. The common-mode level on these pins is programmed by the voltage on VCMO.
5	VCMO	C	Baseband Amplifier Common-Mode Voltage. The voltage applied to this pin sets the output common-mode level of the baseband amplifiers. This pin can either be connected to VREF (Pin 14) or to a reference voltage from another device (typically an ADC).
6	IAIN	D	I-Channel Baseband Amplifier Input. This pin, which has a high input impedance, should be biased to VREF (approximately 1 V). If IAIN is connected directly to IMXO, biasing is provided by IMXO. If an ac-coupled filter is placed between IMXO and IAIN, this pin can be biased from VREF through a 1 kΩ resistor. The gain from IAIN to the differential outputs IOPN/IOPP is 30 dB.
7, 23	COM3		Ground for Biasing and Baseband Sections.
8, 22	IMXO, QMXO	B	I-Channel and Q-Channel Baseband Mixer/VGA Outputs. Low impedance outputs with bias levels equal to VREF. IMXO and QMXO are typically connected to IAIN and QAIN, respectively, either directly or through filters. These outputs have a maximum current limit of about 1.5 mA. This allows for a 600 mV p-p swing into a 200 Ω load. This corresponds to an input level of −40 dBm @ a maximum gain of 39.5 dB. At lower output levels, IMXO and QMXO can drive a lower load resistance, subject to the same current limit.
9	COM2		RF Section Ground.
10, 11	RFIN, RFIP	E	RF Input. RFIN must be ac-coupled to ground. The RF input signal should be ac-coupled into RFIP. For a broadband 50 Ω input impedance, connect a 200 Ω resistor from the signal side of the RFIP coupling capacitor to ground. Note that RFIN and RFIP are not interchangeable differential inputs. RFIN is the ground reference for the input system.
12	VPS2		Positive Supply for RF Section. Decouple VPS2 with 0.1 µF and 100 pF capacitors.
13, 16	IOFS, QOFS	F	I-Channel and Q-Channel Offset Nulling Inputs. To null the dc offset on the I-channel and Q-channel mixer outputs (IMXO, QMXO), connect a 0.1 µF capacitor from these pins to ground. Alternately, a forced voltage of approximately 1 V on these pins disables the offset compensation circuit.
14	VREF	G	Reference Voltage Output. This output voltage (1 V) is the main bias level for the device and can be used to externally bias the inputs and outputs of the baseband amplifiers. The VREF pin should be decoupled with a 0.1 µF capacitor to ground.
15	ENBL	H	Chip Enable Input. Active high.
17	VGIN	C	Gain Control Input. The voltage on this pin controls the gain on the RF and baseband VGAs. The gain control is applied in parallel to all VGAs. The gain control voltage range is from 0.2 V to 1.2 V and corresponds to a gain range from +39.5 dB to −30 dB. This is the gain to the output of the baseband VGAs (that is, QMXO and IMXO). There is an additional 30 dB of gain in the baseband amplifiers. Note that the gain control function has a negative sense (that is, increasing control voltage decreases gain). In AGC mode, connect this pin directly to VAGC.

Pin No.	Mnemonic	Equiv. Circuit	Description
18, 20	VDT2, VDT1	D	Detector Inputs. These pins are the inputs to the on-board detector. VDT2 and VDT1, which have high input impedances, are normally connected to IMXO and QMXO, respectively.
19	VAGC	I	AGC Output. This pin provides the output voltage from the on-board detector. In AGC mode, connect this pin directly to VGIN.
21	VPS3		Positive Supply for Biasing and Baseband Sections. Decouple VPS3 with 0.1 µF and 100 pF capacitors.
24	QAIN	D	Q-Channel Baseband Amplifier Input. Bias this high input impedance pin to VREF (approximately 1 V). If QAIN is directly connected to QMXO, biasing is provided by QMXO. If an ac-coupled filter is placed between QMXO and QAIN, this pin can be biased from VREF through a 1 kΩ resistor. The gain from QAIN to the QOPN/QOPP differential outputs is 30 dB.
25, 26	QOPP, QOPN	B	Q-Channel Differential Baseband Output. Typical output swing is equal to 760 mV p-p differential. The common-mode level on these pins is programmed by the voltage on VCMO.
27	COM1		LO Section Ground.

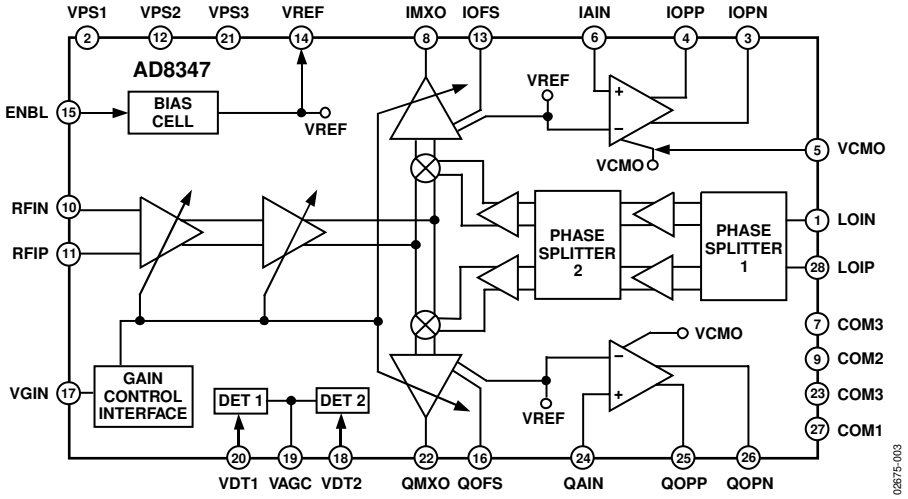

Figure 3. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

RF AMP AND DEMODULATOR

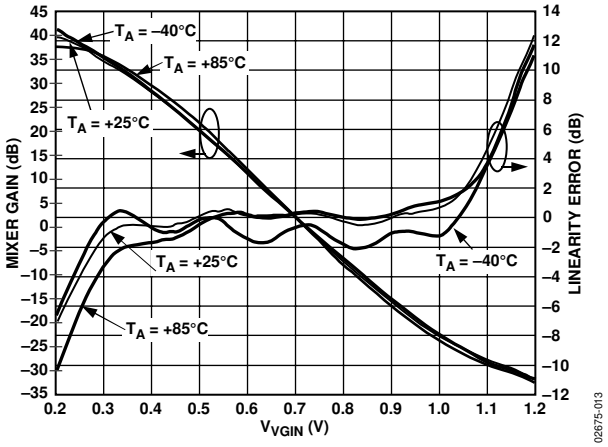

Figure 4. Gain and Linearity Error vs. V_{VGIN}, V_S = 5 V, F_{LO} = 1900 MHz, F_{BB} = 1 MHz

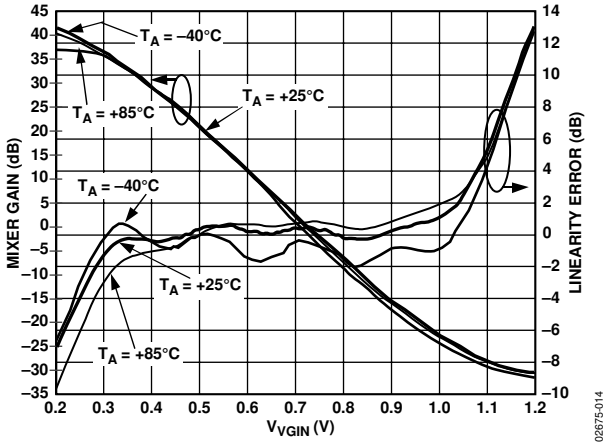

Figure 5. Gain and Linearity Error vs. V_{VGIN}, V_S = 2.7 V, F_{LO} = 1900 MHz, F_{BB} = 1 MHz

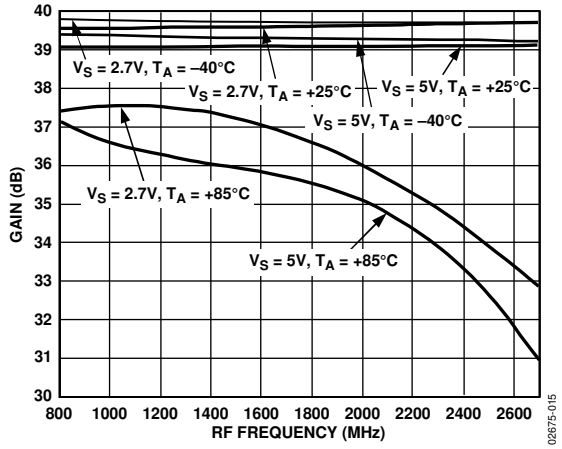

Figure 6. Gain vs. F_{LO}, V_{VGIN} = 0.2 V, F_{BB} = 1 MHz

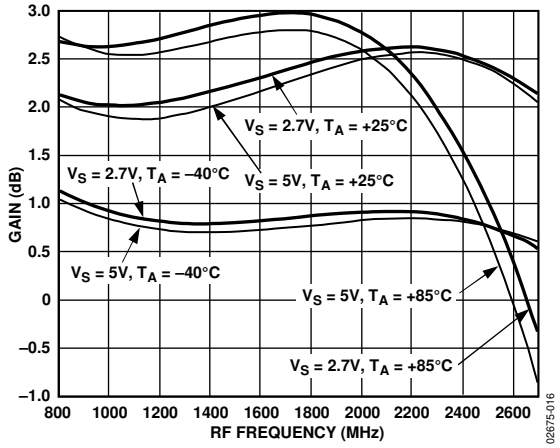

Figure 7. Gain vs. F_{LO}, V_{VGIN} = 0.7 V, F_{BB} = 1 MHz

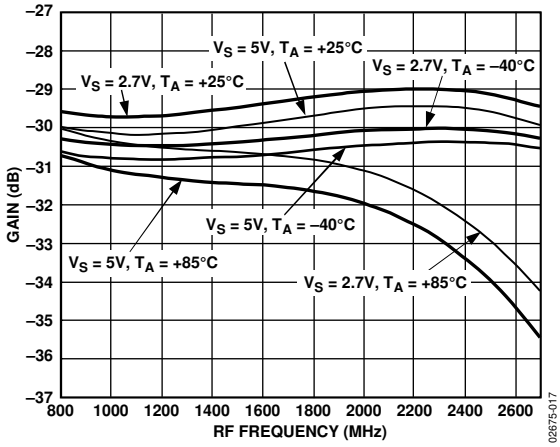

Figure 8. Gain vs. F_{LO}, V_{VGIN} = 1.2 V, F_{BB} = 1 MHz

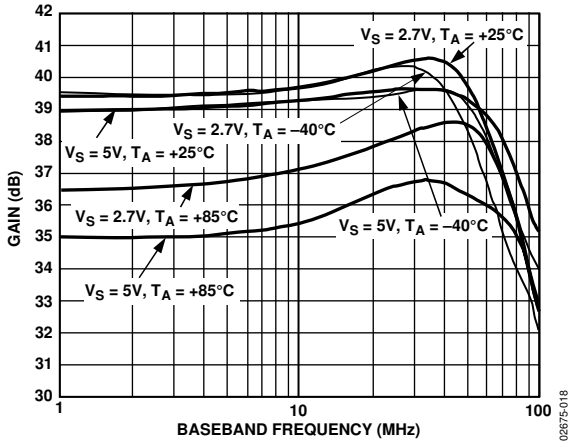

Figure 9. Gain vs. F_{BB}, V_{VGIN} = 0.2 V, F_{LO} = 1900 MHz

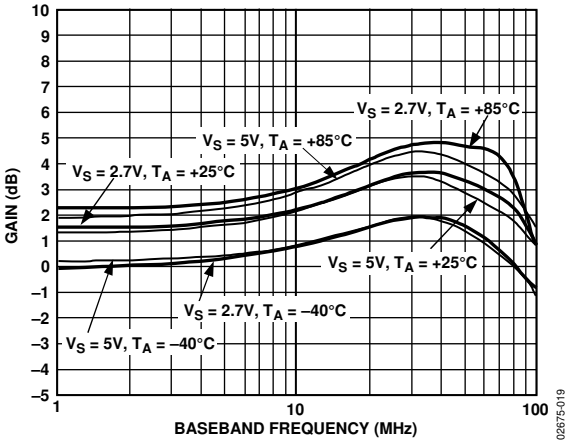

Figure 10. Gain vs. F_{BB}, V_{VGIN} = 0.7 V, F_{LO} = 1900 MHz

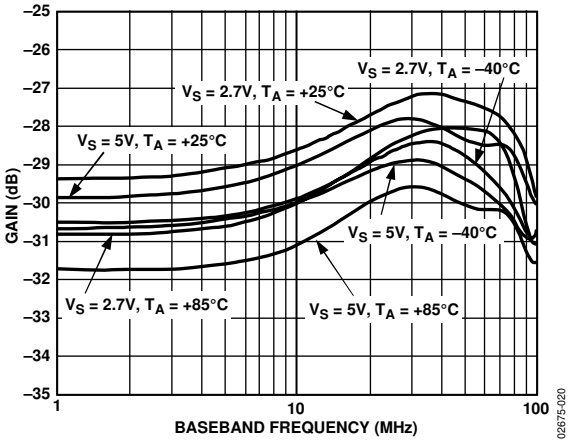

Figure 11. Gain vs. F_{BB}, V_{VGIN} = 1.2 V, F_{LO} = 1900 MHz

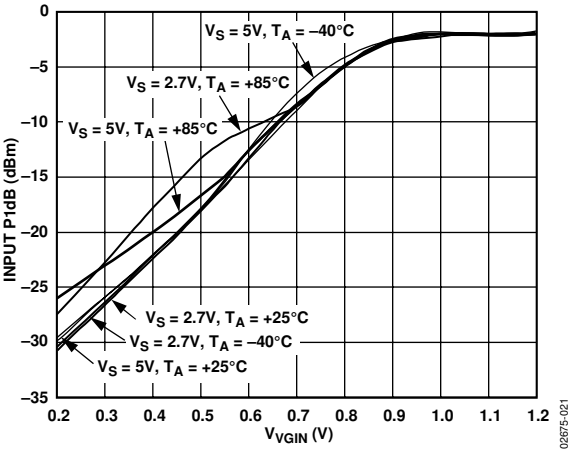

Figure 12. Input 1 dB Compression Point (OP1 dB) vs. V_{VGIN}, F_{LO} = 1900 MHz, F_{BB} = 1 MHz

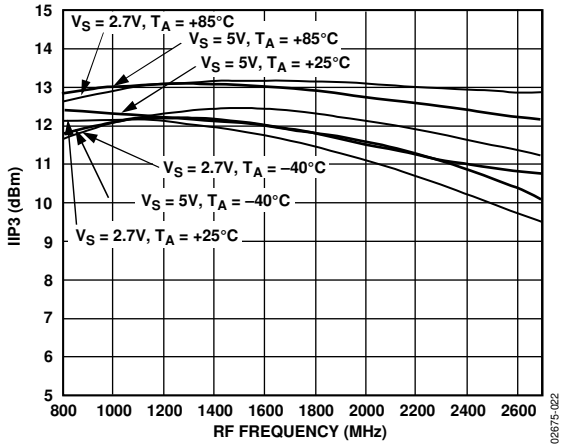

Figure 13. IIP3 vs. F_{LO}, V_{VGIN} = 1.2 V, F_{BB} = 1 MHz

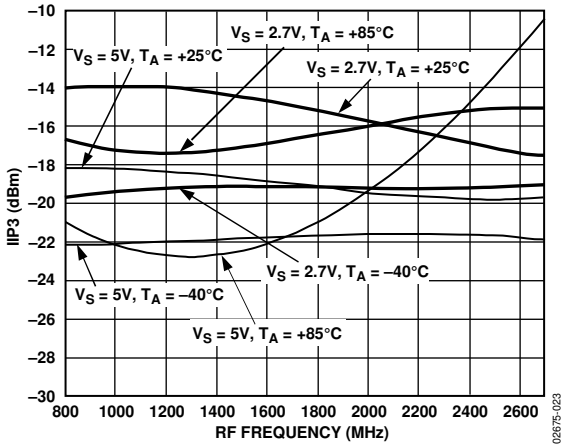

Figure 14. IIP3 vs. F_{LO}, V_{VGIN} = 0.2 V, F_{BB} = 1 MHz

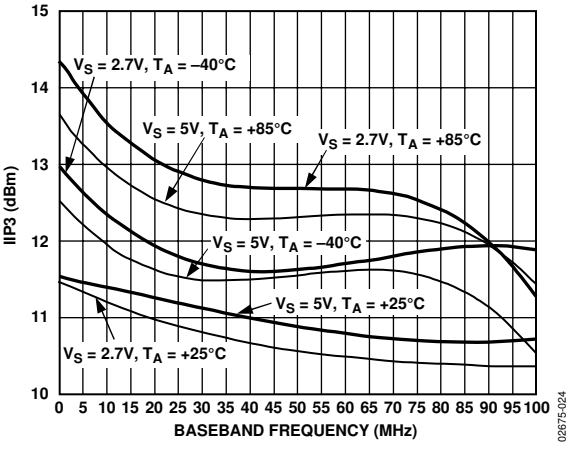

Figure 15. IIP3 vs. F_{BB}, V_{VGIN} = 1.2 V, F_{LO} = 1900 MHz

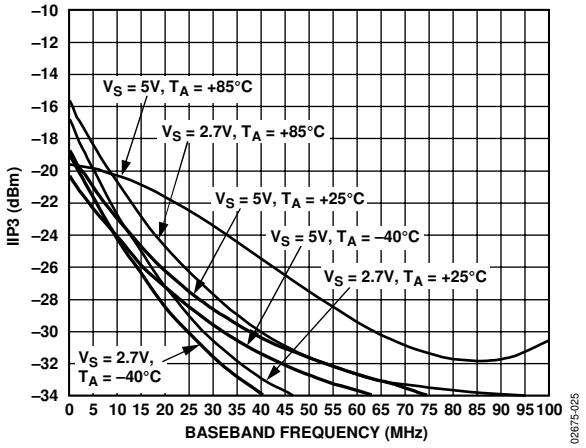

Figure 16. IIP3 vs. F_{BB}, V_{VGIN} = 0.2 V, F_{LO} = 1900 MHz

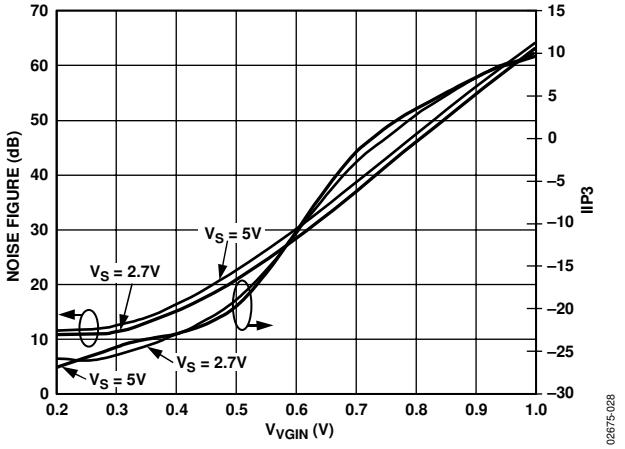

Figure 19. Noise Figure and IIP3 vs. V_{VGIN}, Temperature = 25°C, F_{LO} = 1900 MHz, F_{BB} = 1 MHz

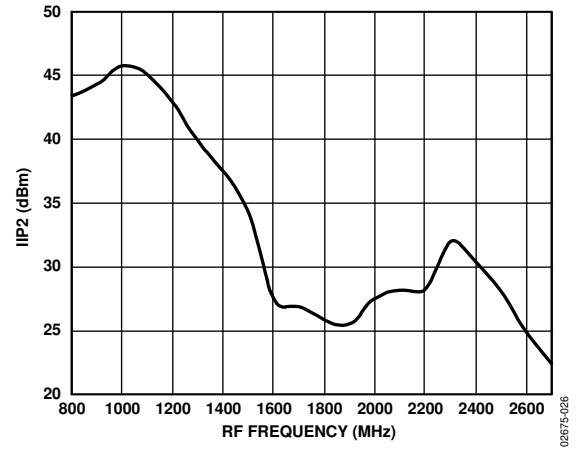

Figure 17. IIP2 vs. F_{LO}, V_{VGIN} = 1.2 V, Baseband Tone1 = 5 MHz, −10 dBm, Baseband Tone2 = 6 MHz, −10 dBm, Temperature = 25°C, V_S = 5 V

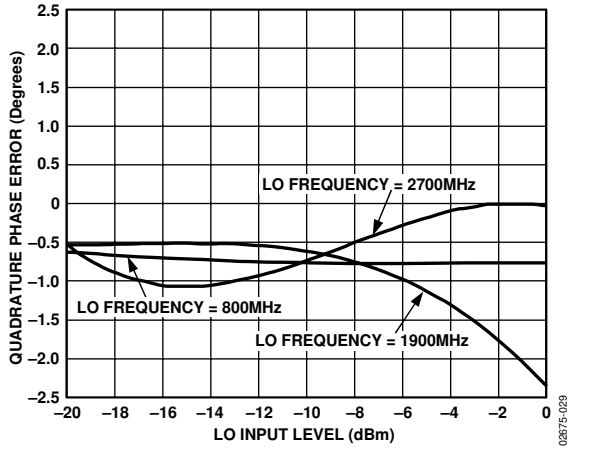

Figure 20. Quadrature Error vs. LO Power Level, Temperature = 25°C, V_{VGIN} = 0.2 V, V_S = 5 V

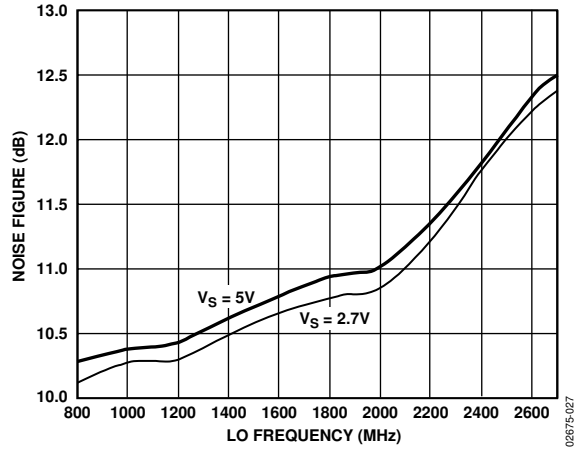

Figure 18. Noise Figure vs. LO Frequency (F_{LO}), Temperature = 25°C, V_{VGIN} = 0.2 V, F_{BB} = 1 MHz

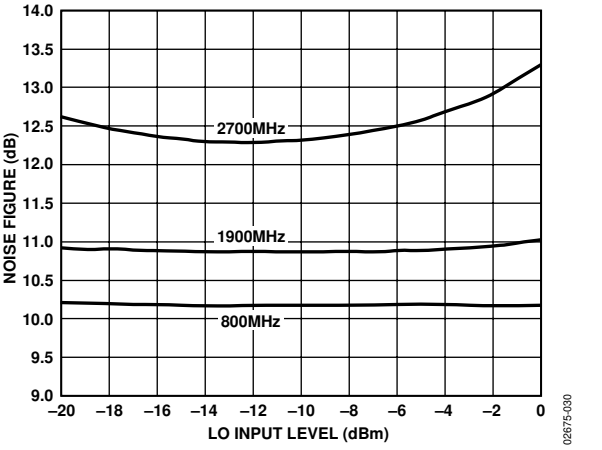

Figure 21. Noise Figure vs. LO Input Level, Temperature = 25°C, V_{VGIN} = 0.2 V, V_S = 5 V

BASEBAND OUTPUT AMPLIFIERS

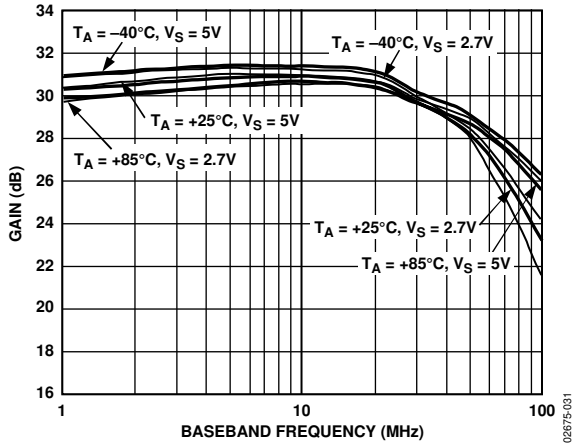

Figure 22. Gain vs. F_{BB}, V_{VCMO} = 1 V

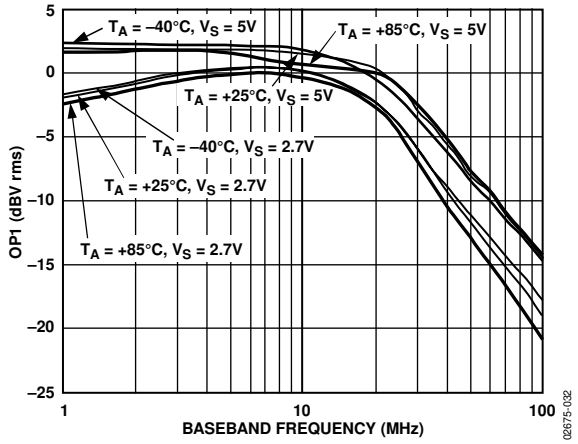

Figure 23. OP1 vs. F_{BB}, V_{VCMO} = 1 V

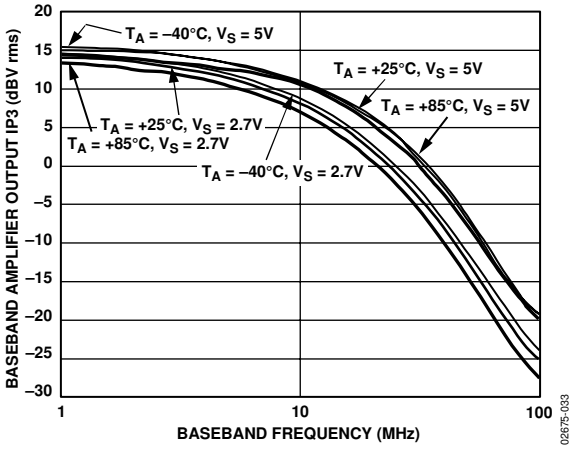

Figure 24. OIP3 vs. F_{BB}, V_{VCMO} = 1 V

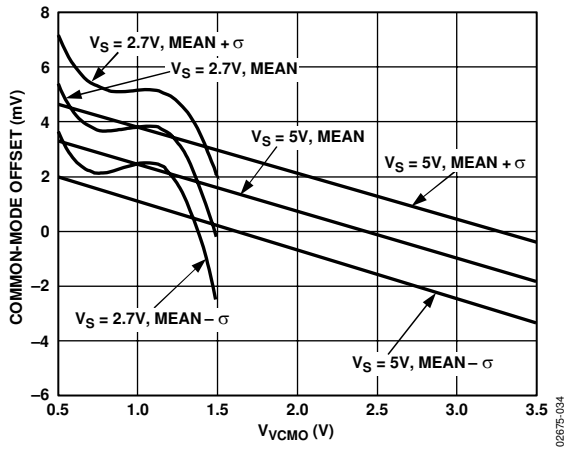

Figure 25. Common-Mode Output Offset Voltage vs. V_{VCMO}, Temperature = 25°C (σ = 1 Standard Deviation)

RF AMP/DEMOD AND BASEBAND OUTPUT AMPLIFIERS

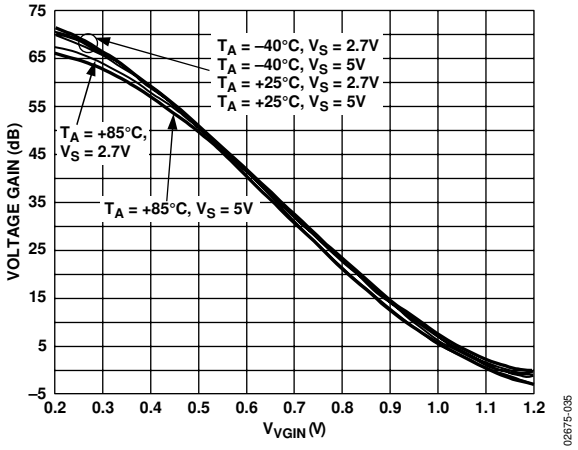

Figure 26. Voltage Gain vs. V_{VGIN}, F_{LO} = 1900 MHz, F_{BB} = 1 MHz

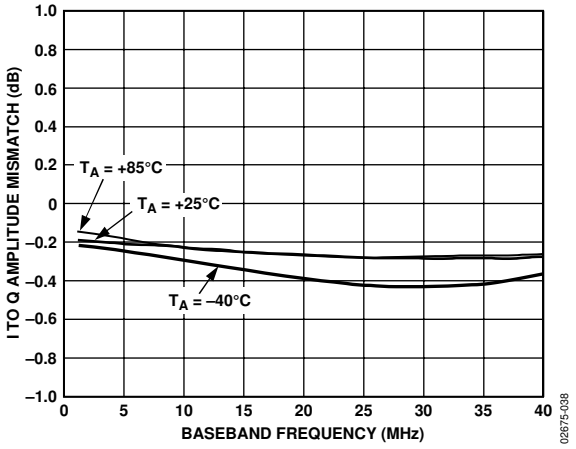

Figure 29. I/Q Amplitude Imbalance vs. F_{BB}, Temperature = 25°C, V_S = 5 V

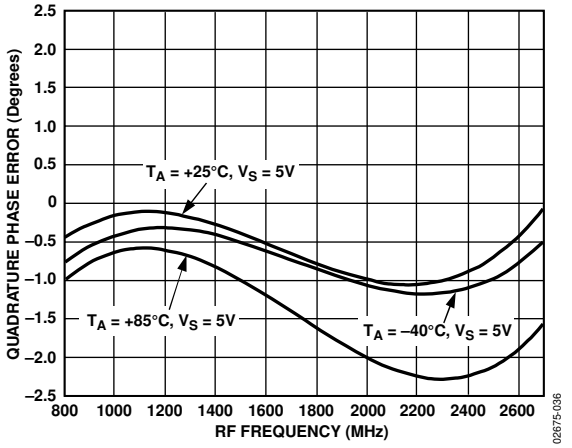

Figure 27. Quadrature Phase Error vs. F_{LO}, V_{VGIN} = 0.7 V, V_S = 5 V

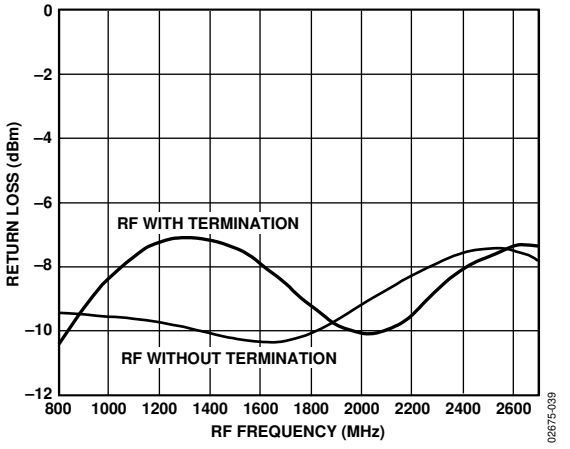

Figure 30. Return Loss of RFIP vs. F_{RF}, V_{VGIN} = 0.7 V, V_S = 5 V

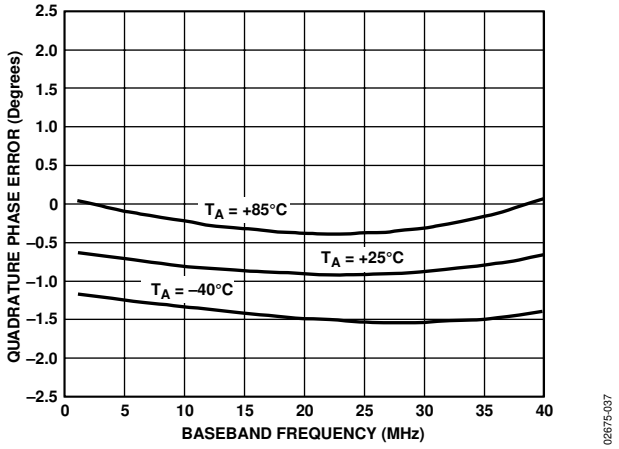

Figure 28. Quadrature Phase Error vs. F_{BB}, V_{VGIN} = 0.7 V, V_S = 5 V

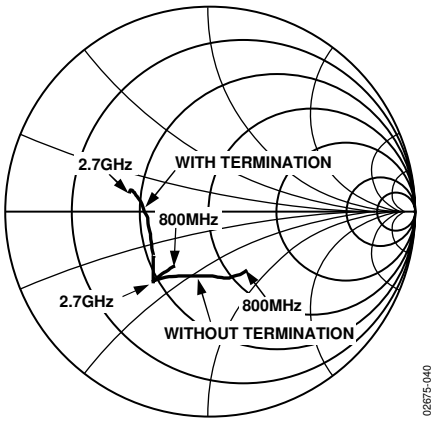

Figure 31. S11 of RFIN vs. F_{RF}, V_{VGIN} = 0.7 V, V_S = 5 V

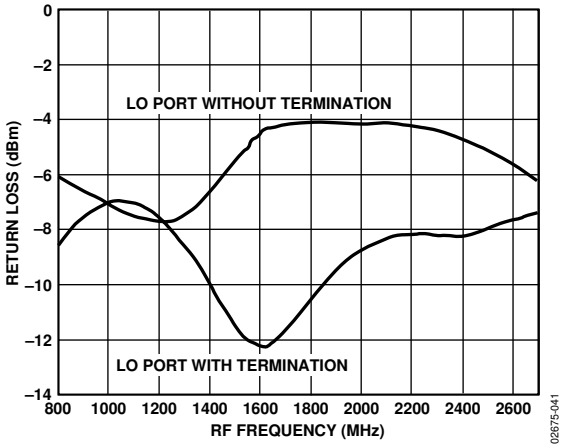

Figure 32. Return Loss of LOIP vs. F_{LO}, V_{VGIN} = 0.7 V, V_P = 5 V

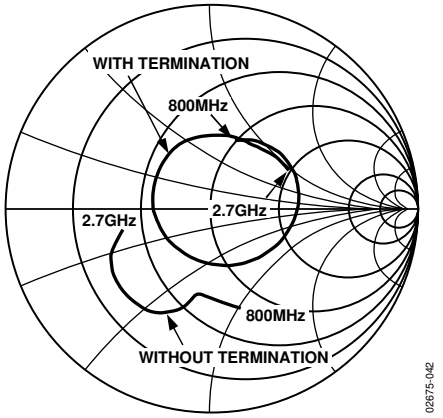

Figure 33. S11 of LOIN vs. F_{LO}, V_{VGIN} = 0.7 V, V_S = 5 V

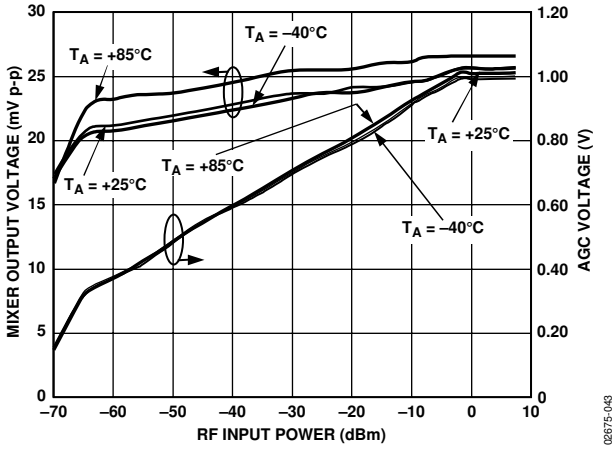

Figure 34. AGC Voltage and Mixer Output Level vs. RF Input Power, F_{LO} = 1900 MHz, F_{BB} = 1 MHz, V_S = 5 V

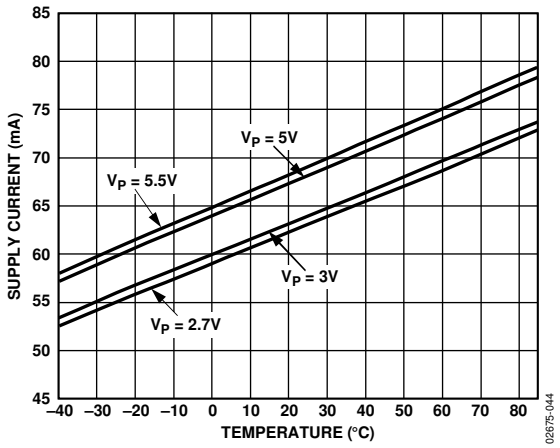

Figure 35. Supply Current vs. Temperature, V_{VGIN} = 0.7 V, V_{VCMO} = 1 V

EQUIVALENT CIRCUITS

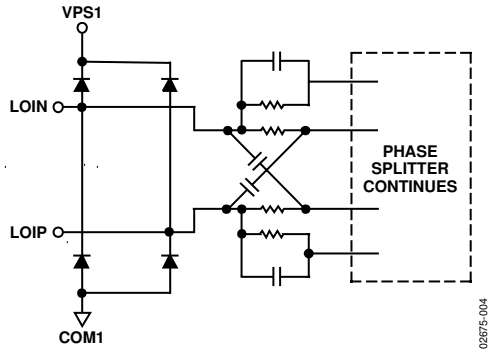

Figure 36. Circuit A

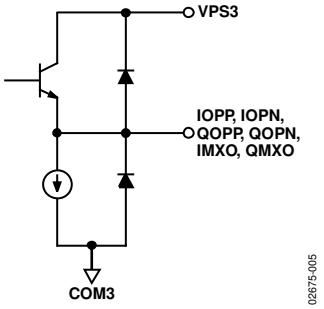

Figure 37. Circuit B

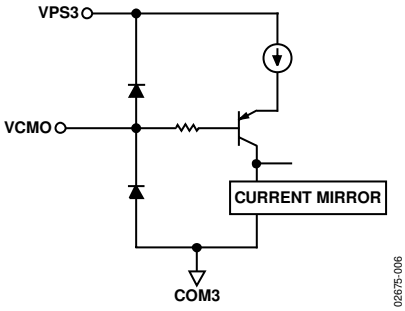

Figure 38. Circuit C

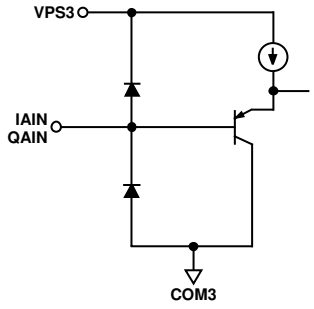

Figure 39. Circuit D

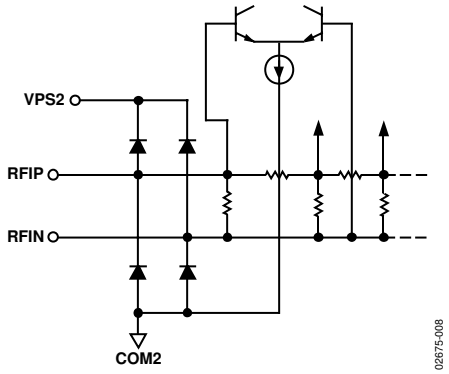

Figure 40. Circuit E

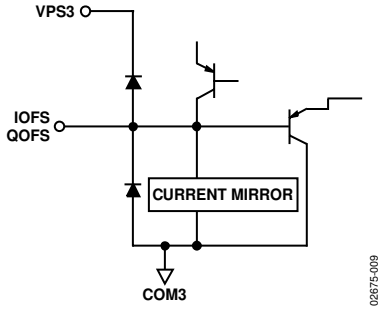

Figure 41. Circuit F

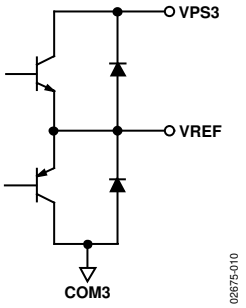

Figure 42. Circuit G

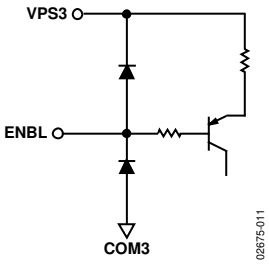

Figure 43. Circuit H

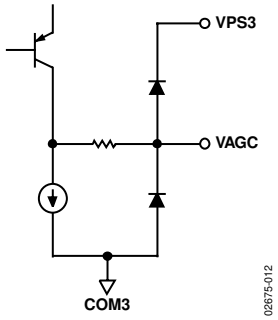

Figure 44. Circuit I

THEORY OF OPERATION

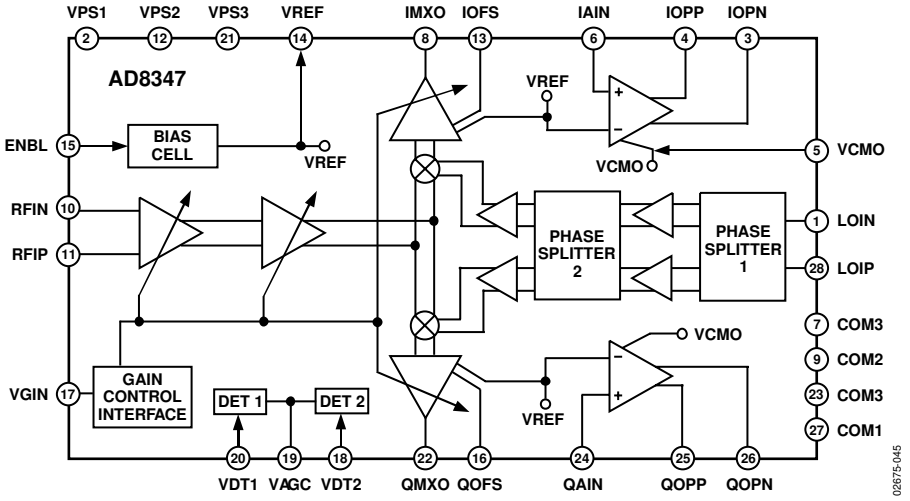

Figure 45. Block Diagram

The AD8347 is a direct I/Q demodulator usable in digital wireless communication systems including cellular, PCS, and digital video receivers. An RF signal in the frequency range of 800 MHz to 2,700 MHz is directly downconverted to the I and Q components at baseband using a local oscillator (LO) signal at the same frequency as the RF signal.

The RF input signal goes through two stages of variable gain amplifiers before splitting up to reach two Gilbert-cell mixers. The mixers are driven by a pair of LO signals which are in quadrature (90 degrees of phase difference). The outputs of the mixers are applied to baseband I-channel and Q-channel variable gain amplifiers. The outputs from these baseband variable gain amplifiers are brought out to pins for external filtering. The filter outputs are then applied to a pair of on-chip, fixed gain, baseband amplifiers. These amplifiers gain up the outputs from the external filters to a level compatible with most A-to-D converters. A sum of squares detector is available for use in an automatic gain control (AGC) loop to set the output level. The RF and baseband amplifiers provide approximately 69.5 dB of gain control range. Additional on-chip circuits allow the setting of the dc level at the I-channel and Q-channel baseband outputs, as well as nulling the dc offset at each channel.

RF VARIABLE GAIN AMPLIFIERS (VGA)

These amplifiers use the patented X-AMP® approach with NPN differential pairs separated by sections of resistive attenuators. The gain control is achieved through a gaussian interpolator where the control voltage sets the tail currents supplied to the various differential pairs according to the gain desired. In the first amplifier, the combined output currents from the transconductance cells go through a cascode stage to resistive loads with inductive peaking. In the second amplifier, the differential currents are split and fed to the two Gilbert-cell mixers through separate cascode stages.

MIXERS

Two double balanced Gilbert-cell mixers, one for each channel, perform the in-phase (I) and quadrature (Q) down conversion. Each mixer has four cross-connected transistor pairs that are terminated in resistive loads and feed the differential baseband variable gain amplifiers for each channel. The quadrature LO signals drive the bases of the mixer transistors.

BASEBAND VARIABLE GAIN AMPLIFIERS

The baseband VGAs also use the X-AMP approach with NPN differential pairs separated by sections of resistive attenuators. The same interpolator controlling the RF amplifiers controls the tail currents of the differential pairs. The outputs of these amplifiers are provided off chip for external filtering. Automatic offset nulling minimizes the dc offsets at both I- and Q-channels. The common-mode output voltage is set to the same level as the reference voltage (1.0 V) generated in the Bias cell, also made available at the VREF pin (see Figure 45).

OUTPUT AMPLIFIERS

The output amplifiers gain up the signal coming back from each of the external filters to a level compatible with most high speed A-to-D converters. These amplifiers are based on an active feedback design to achieve high gain bandwidth with low distortion.

LO AND PHASE SPLITTERS

The incoming LO signal is applied to a polyphase phase splitter to generate the LO signals for the I-channel and Q-channel mixers. The polyphase phase splitters are RC networks connected in a cyclical manner to achieve gain balance and phase quadrature. The wide operating frequency range of these phase splitters is achieved by cascading multiple sections of

these networks with staggered RC constants. Each branch goes through a buffer to make up for the loss and high frequency roll-off. The output from the buffers then goes into another polyphase phase splitter to enhance the accuracy of phase quadrature. Each LO signal is buffered again to drive the mixers.

OUTPUT LEVEL DETECTOR

To create an AGC voltage (VAGC), two signals proportional to the square of each output channel are summed together and compared to a built-in threshold. The inputs to this rms detector are referenced to VREF.

BIAS

An accurate reference circuit generates the reference currents used by the different sections. The reference circuit is controlled by an external power-up (ENBL) logic signal that, when set low, puts the whole chip into a sleep mode typically requiring less than 400 μA of supply current. The reference voltage (VREF) of 1.0 V, that serves as the common-mode reference for the baseband circuits, is made available for external use. The VREF pin should be decoupled with a 0.1 μF capacitor to ground.

APPLICATIONS

BASIC CONNECTIONS

The basic connections for operating the AD8347 are shown in Figure 46. The device is powered through three power supply pins: VPS1, VPS2, and VPS3. These pins supply current to different parts of the overall circuit. VPS1 and VPS2 power the local oscillator (LO) and RF sections, respectively, while VPS3 powers the baseband amplifiers. Connect all of these pins to the same supply voltage; however, separately decouple each pin using two capacitors. 100 pF and 0.1 μF capacitors are recommended, though values close to these can be used.

Use a supply voltage in the range 2.7 V to 5.5 V. The quiescent current is 64 mA when operating from a 5 V supply. By pulling the ENBL pin low, the device goes into its power-down mode. The power-down current is 400 μA when operating on a 5 V supply and 80 μA on a 2.7 V supply.

Like the supply pins, the individual sections of the circuit are separately grounded. COM1, COM2, and COM3 provide ground for the LO, RF, and baseband sections, respectively. Connect all of these pins to the same low impedance ground.

RF INPUT AND MATCHING

The RF input signal should be ac-coupled into the RFIP pin and RFIN should be ac-coupled to ground. To improve broadband matching to a 50 Ω source, a 200 Ω resistor can be connected from the signal side of the RFIP coupling capacitor to ground.

LO DRIVE INTERFACE

For optimum performance, the LO inputs, LOIN and LOIP, should be driven differentially; the M/A-COM balun, ETC1-1-13 is recommended. Unless an ac-coupled transformer is used to generate the differential LO, the inputs must be ac-coupled, as shown in Figure 46. To improve broadband matching to a 50 Ω source, connect a 200 Ω shunt resistor between LOIP and LOIN.

A LO drive level of −8 dBm is recommended. Figure 20 shows the relationship between LO drive level, LO frequency, and quadrature error for a typical device.

A single-ended drive is also possible as shown in Figure 47, but this slightly increases LO leakage. Apply the LO signal through a coupling capacitor to LOIP, and ac-couple LOIN to ground. Because the inputs are fully differential, the drive orientation can be reversed. As in the case of the differential drive, a 200 Ω resistor connected across LOIP and LOIN improves the match to a 50 Ω source.

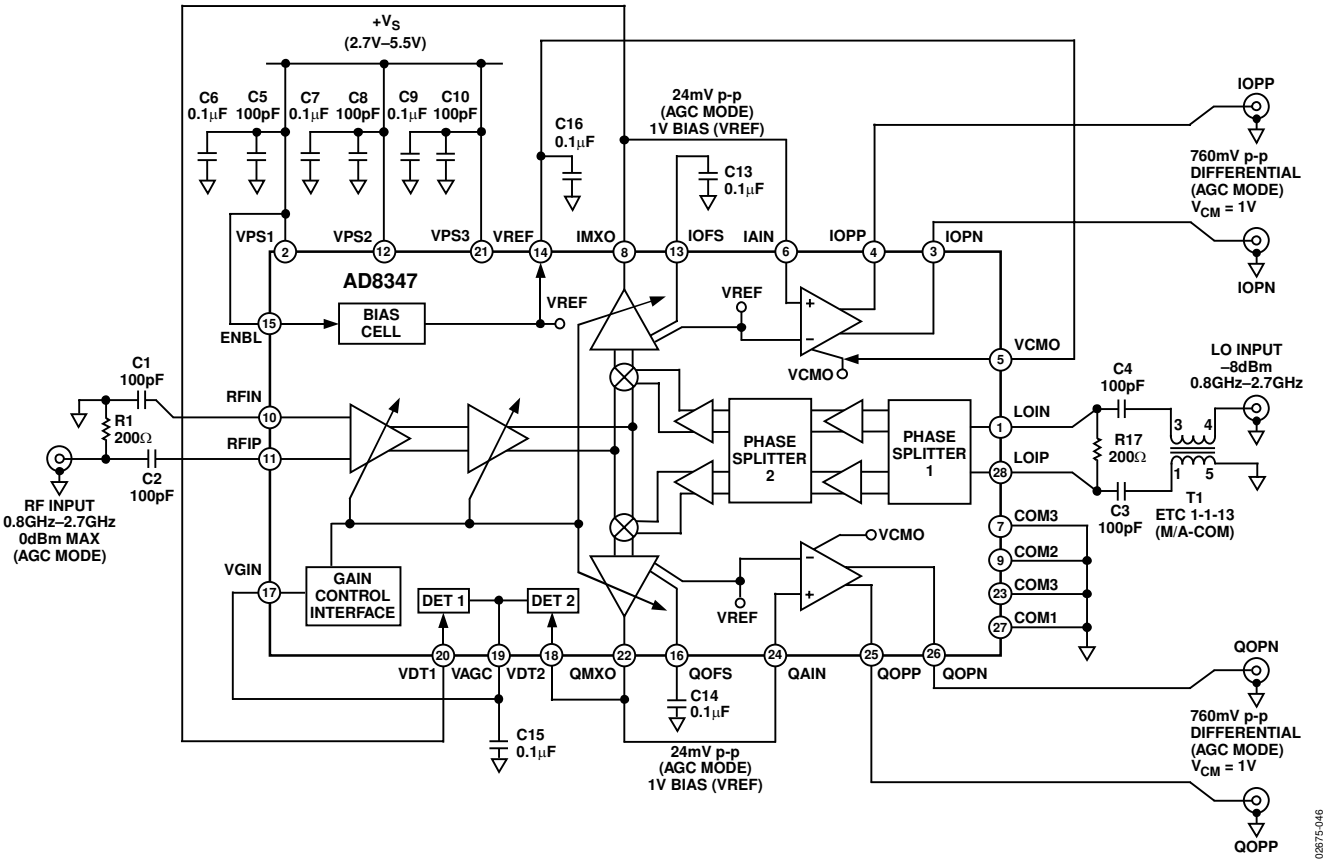

Figure 46. Basic Connections

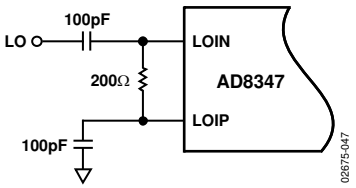

Figure 47. Single-Ended LO Drive

OPERATING THE VGA

A three-stage VGA sets the gain in the RF section. Two of the three stages come before the mixer while the third amplifies the mixer output. All three stages are driven in parallel. The gain range of the first RF VGA and that of the second RF VGA combined with the mixer are both −13 dB to +10 dB. The gain range of the baseband VGA is −4 dB to +19.5 dB. Therefore, the overall gain range from the RF input to the IMXO and QMXO pins is −30 dB to approximately +39.5 dB.

The gain of the VGA is set by the voltage on the VGIN pin, which is a high impedance input. The gain control function (which is linear-in-dB) and linearity are shown in Figure 4 and Figure 5 at 1.9 GHz. Note that the sense of the gain control voltage is negative because as the gain control voltage ranges from 0.2 V to 1.2 V, the gain decreases from +39.5 dB to −30 dB.

MIXER OUTPUT LEVEL AND DRIVE CAPABILITY

I- and Q-channel baseband outputs, IMXO and QMXO, are low impedance outputs (R_{OUT} @ 3 Ω) with bias levels equal to V_{VREF}, the voltage on Pin 14. The achievable output levels on IMXO/QMXO are limited by their current drive capability of 1.5 mA maximum. This allows for a 600 mV p-p swing into a 200 Ω load. At lower output levels, IMXO and QMXO can drive smaller load resistances, subject to the same current limit. These output stages are not, however, designed to directly drive 50 Ω loads.

OPERATING THE VGA IN AGC MODE

Although the VGA can be driven by an external source such as a DAC, the AD8347 has an on-board sum of squares detector to allow the AD8347 to operate in an automatic leveling mode. Due to the nature of the detector, an input signal with a higher peak-to-average ratio causes the AGC loop to settle with a higher mixer output peak-to-peak voltage. In this data sheet, peak-to-peak calculations assume a sine wave input when referencing AGC operation.

The connections for operating in this mode are shown in Figure 46. The two mixer outputs are connected to Detector Input VDT1 and Detector Input VDT2. The summed detector output drives an internal integrator which, in turn, delivers a gain correction voltage to the VAGC pin. A 0.1 μF capacitor from VAGC to ground sets the dominant pole of the integrator circuit. VAGC, which should be connected to VGIN, adjusts gain until an internal threshold is reached. This threshold corresponds to a level at the IMXO and QMXO pins of approximately 8.5 mV rms. This level changes slightly as a function of RF input power (see Figure 34). For a CW (sine wave) input, this corresponds to approximately 24 mV p-p. If this signal is applied directly to the subsequent baseband amplifier stage, the final baseband output is 760 mV p-p differential. See the Baseband Amplifiers section.

If the VGA gain is set from an external source, VDT1 and VDT2 (the on-board detector inputs) are not used and are tied to VREF.

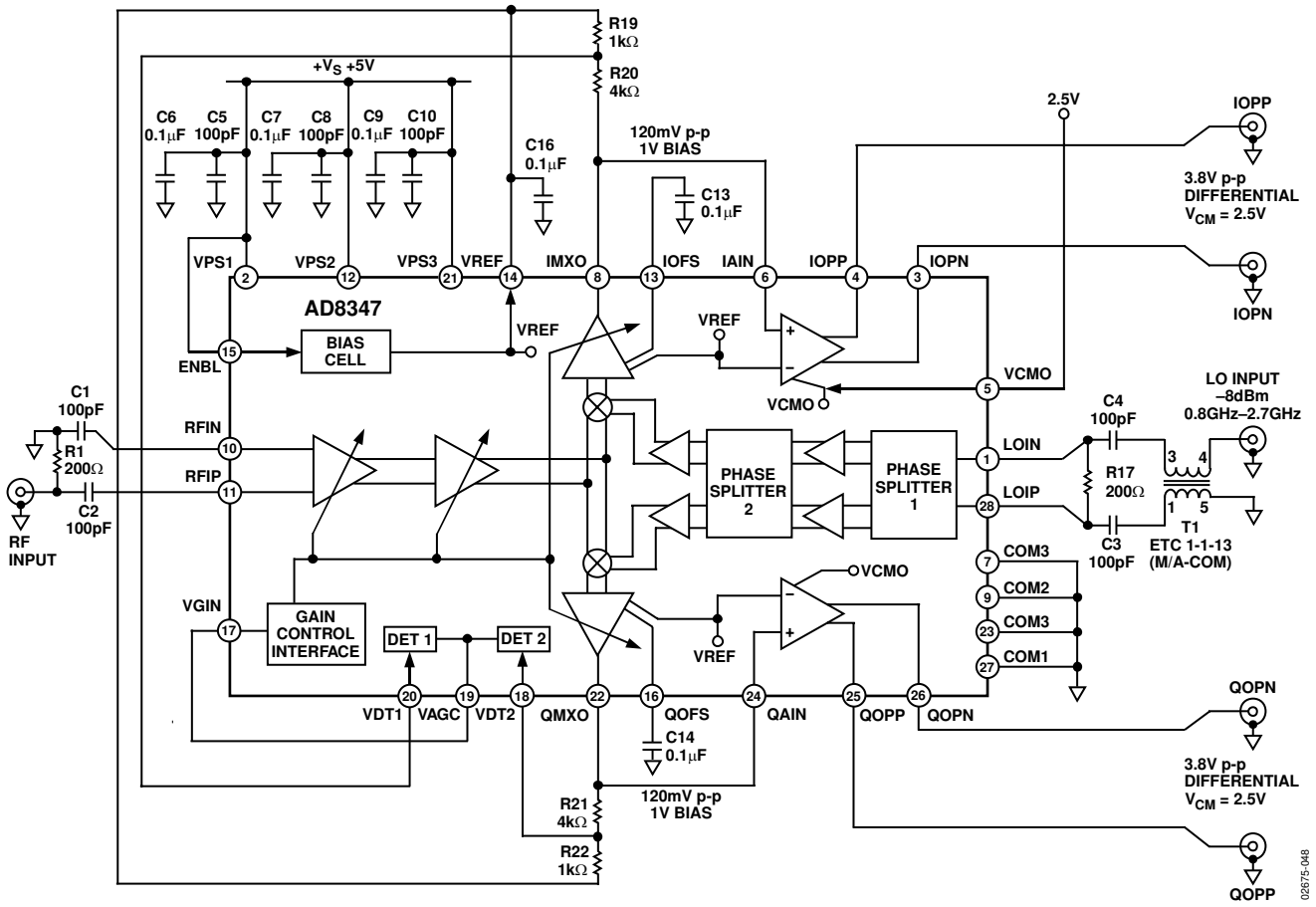

Figure 48. Adjusting AGC Level to Increase Baseband Amplifier Output Swing

CHANGING THE AGC SETPOINT

The AGC circuit can be easily set up to level at voltages higher than the nominal 24 mV p-p, as shown in Figure 48. The voltages on Pin IMXO and Pin QMXO are attenuated before being applied to the detector inputs. In the example shown, an attenuation factor of 0.2 (−14 dB) between IMXO and QMXO and the detector inputs causes the VGA to level at approximately 120 mV p-p (note that the resistor divider network must be referenced to V_{VREF}). This results in a peak-to-peak output swing at the baseband amplifier outputs of 3.8 V differential, that is, 1.6 V to 3.4 V on each side. Note that V_{VCMO} has been increased to 2.5 V to avoid signal clipping at the baseband outputs. Due to the attenuation between the mixer output and the detector input, the variation in the settled mixer output level vs. RF input power will be greater than the variation shown in Figure 34. The variation will be greater by a factor equal to the inverse of the attenuation factor.

BASEBAND AMPLIFIERS

The final baseband amplifier stage takes the signals from IMXO and QMXO and amplifies them by 30 dB, or a factor of 31.6. This results in a maximum system gain of 69.5 dB. When the VGA is in AGC mode, the baseband I and Q outputs (IOPN, IOPP, QOPN, and QOPP) deliver a differential voltage of approximately 760 mV p-p (380 mV p-p on each side).

The single-ended input signal to the baseband amplifiers is applied at IAIN and QAIN, the high impedance inputs. As shown in Figure 46, the baseband amplifier operates internally as a differential amplifier, with the second input driven by V_{VREF}. Therefore, bias the input signal to the baseband amplifier at V_{VREF}.

The output common-mode level of the baseband amplifiers is set by the voltage on Pin 5, VCMO. Connect this pin to VREF (Pin 14) or to an external reference voltage from a device such as an analog-to-digital converter (ADC). V_{VCMO} has a nominal range from 0.5 V to 2.5 V. However, since the baseband amplifiers can only swing down to 0.4 V, higher values of V_{VCMO} are generally required to avoid low end signal clipping. Alternatively, the positive swing at each output is limited to 1.3 V below the supply voltage; therefore, the maximum p-p swing is given by $2 \times (V_{PS} - 1.3 - 0.4)$ V differentially.

For example, for the baseband output amplifier to deliver an output swing of 2 V p-p (1 V p-p on each side), V_{VCMO} must be in a range from 0.9 V to 2.5 V.

The differential output offset voltages of the baseband amplifiers are typically ±50 mV. This offset voltage results from both input and output effects.

The overall signal-to-noise ratio can be improved by increasing the VGA gain by driving it with an external voltage or by changing the setpoint of the AGC circuit. See the Changing the AGC Setpoint section.

DRIVING CAPACITIVE LOADS

In applications where the baseband amplifiers are driving unbalanced capacitive loads, place some series resistance between the amplifier and the capacitive load. For example, for a 10 pF load, use four 200 Ω series resistors, one in each baseband output.

EXTERNAL BASEBAND AMPLIFICATION

Reduce baseband output offset voltage and noise by bypassing the internal baseband amplifiers and amplifying the mixer output signal using a high quality differential amplifier. In the example shown in Figure 49, two AD8132 differential amplifiers are used to gain up the mixer output signals by 20 dB. In this example, the setpoint of the AGC circuit was increased to give an approximate 72 mV p-p input to the external amplifiers. This resulted in final baseband output signals of 720 mV p-p.

The closed-loop bandwidth of the amplifiers in Figure 49 is equal to approximately 20 MHz. Higher bandwidths are achievable, but at the cost of lower closed-loop gain. In Figure 49, the output common-mode levels at Pin 2 (V_{OCM} pin) of the AD8132s are set by the AD8347's VREF (approximately 1 V). The output common-mode levels can also be externally set, using, for example, the reference voltage from an ADC.

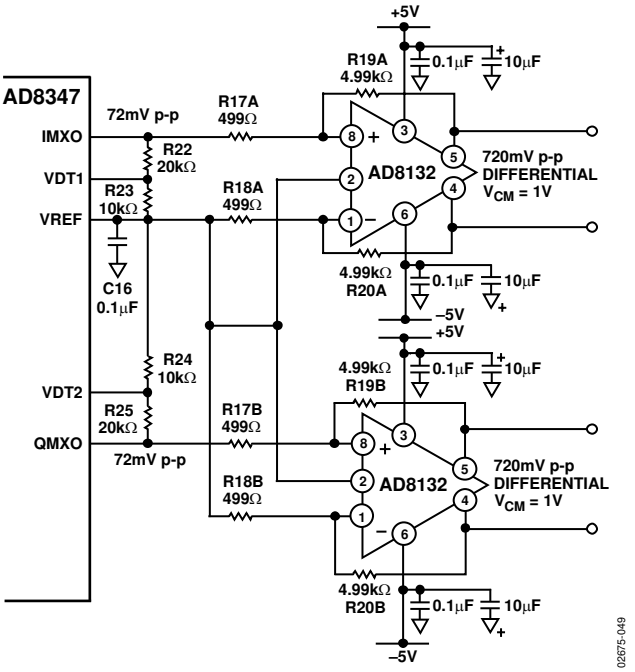

Figure 49. External Baseband Amplification Example

FILTER DESIGN CONSIDERATIONS

Baseband low-pass or band-pass filtering can be conveniently performed between the mixer outputs (IMXO and QMXO) and the input to the baseband amplifiers. Because the output impedance of the mixer is low (approximately 3 Ω) and the input impedance of the baseband amplifier is high, it is not practical to design a filter that is reactively matched to these impedances. An LC filter can be matched by placing a series resistor at the mixer output and a shunt resistor (terminated to V_{VREF}) at the input to the baseband amplifier.

Because the mixer output drive level is limited to a maximum current of 1.5 mA, the characteristic impedance of the filter should be greater than 50 Ω, especially to achieve larger signal swings.

Figure 50 shows the schematic for a 100 Ω, fourth-order elliptic low-pass filter with a 3 dB cutoff frequency of 20 MHz. Source and load impedances of approximately 100 Ω ensure that the filter sees a matched source and load. This also ensures that the mixer output is driving an overall load of 200 Ω. Note that the shunt termination resistor is tied to VREF and not to ground. The frequency response and group delay of this filter are shown in Figure 51 and Figure 52.

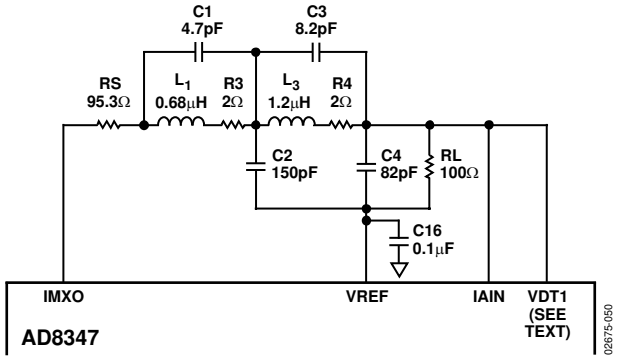

Figure 50. Typical Baseband Low-Pass Filter

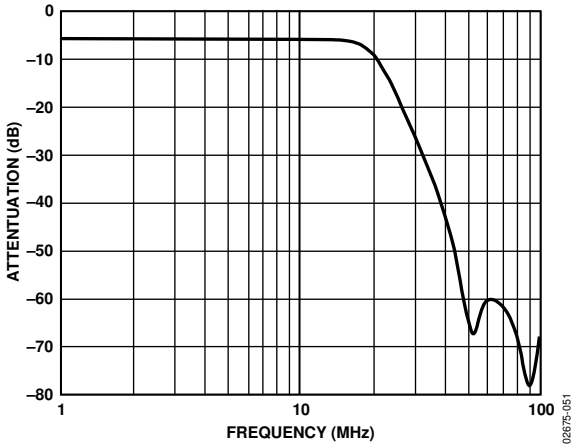

Figure 51. Frequency Response of 20 MHz Baseband Low-Pass Filter

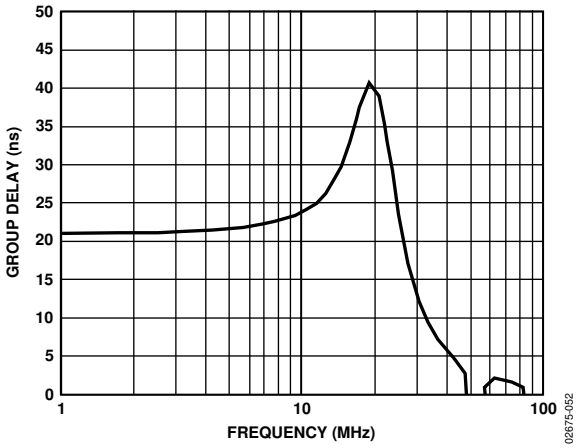

Figure 52. Group Delay of 20 MHz Baseband Low-Pass Filter

If the VGA is operating in AGC mode, the detector inputs (VDT1 and VDT2) can be tied either to the inputs or outputs of the filter. Connecting the detector inputs to the inputs of the filter (IMXO and QMXO) causes the VGA leveling point to be determined by the composite of the wanted signal and any unfiltered components, such as blockers or signal harmonics. Alternatively, connecting VDT1 and VDT2 to the outputs of the filters ensures that the leveling point of the AGC circuit is based upon the amplitude of the filtered output only. The latter option is more desirable as it results in a more constant baseband output. However, when using this method, set the leveling point of the AGC so that the out-of-band blockers do not overdrive the mixer output.

DC OFFSET COMPENSATION

Feedthrough of the LO signal to the RF input port results in self-mixing of the LO signal. This produces a dc component at the mixer output that is frequency dependent.

The AD8347 includes an internal circuit that actively nulls any dc offsets that appear at the mixer output. The dc bias level of the mixer output (which should ideally equal V_{VREF}, the bias level for the baseband sections of the chip) is continually compared to V_{VREF}. Any differences between the mixer output level and V_{VREF} forces a compensating voltage on to the mixer output. The time constant of this correction loop is set by the capacitors that are connected to Pin IOFS and Pin QOFS (each output can be separately compensated). For normal operation, 0.1 µF capacitors are recommended. The corner frequency of the compensation loop is given approximately by

$$f_{3dB} = \frac{40}{C_{OFS}}\left(C_{OFS} \text{ in } \mu\text{F}\right)$$

The corner frequency must be set to a frequency that is much lower than the symbol rate of the demodulated data. This prevents the compensation loop from falsely interpreting the data stream as a changing offset voltage.

To disable the offset compensation circuits, tie IOFS and QOFS to VREF.

EVALUATION BOARD

Figure 53 shows the schematic of the AD8347 evaluation board. Note that uninstalled components are indicated with the open designation. The board is powered by a single supply in the range of 2.7 V to 5.5 V. Table 4 details the various configuration options of the evaluation board.

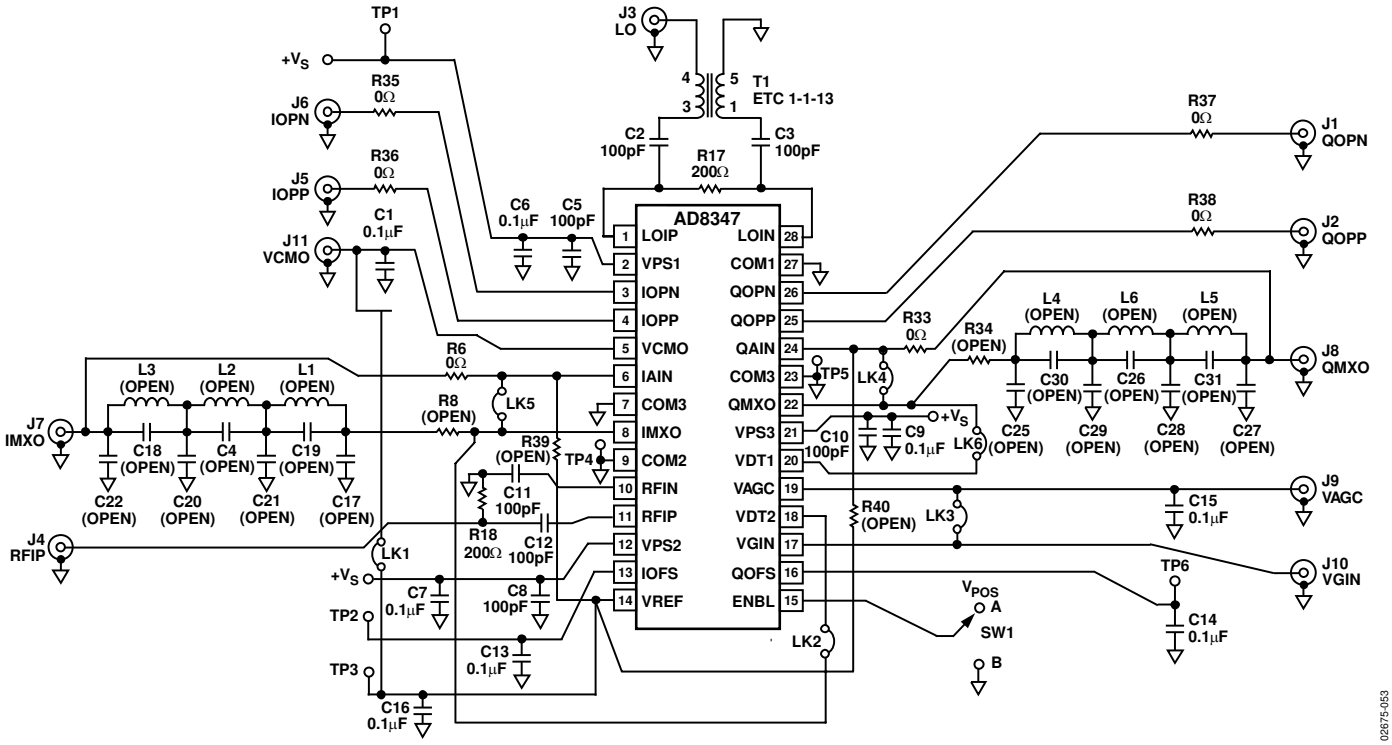

Figure 53. Evaluation Board Schematic

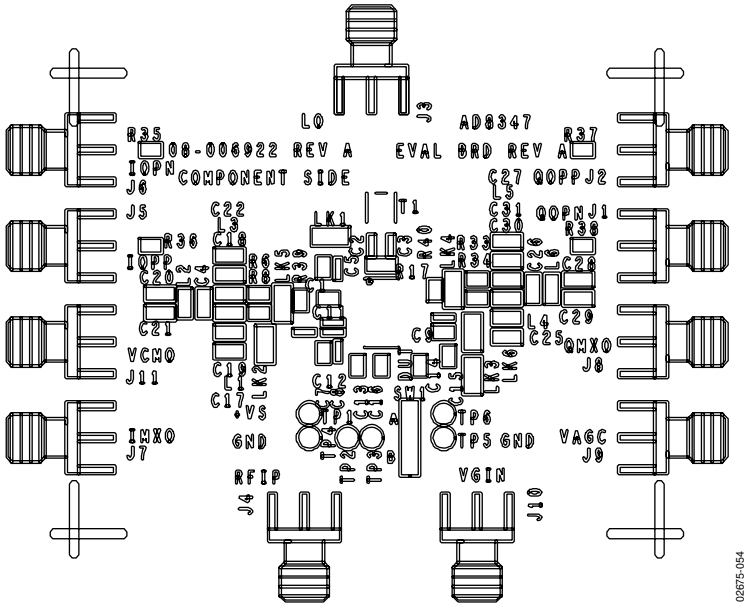

Figure 54. Silkscreen of Component Side

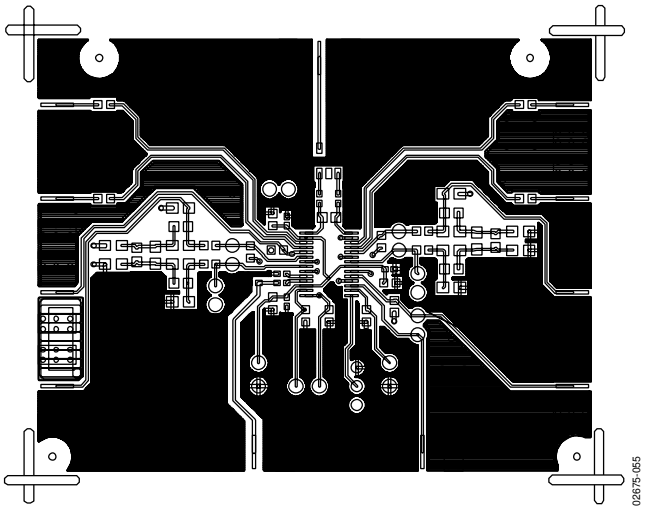

Figure 55. Layout of Component Side

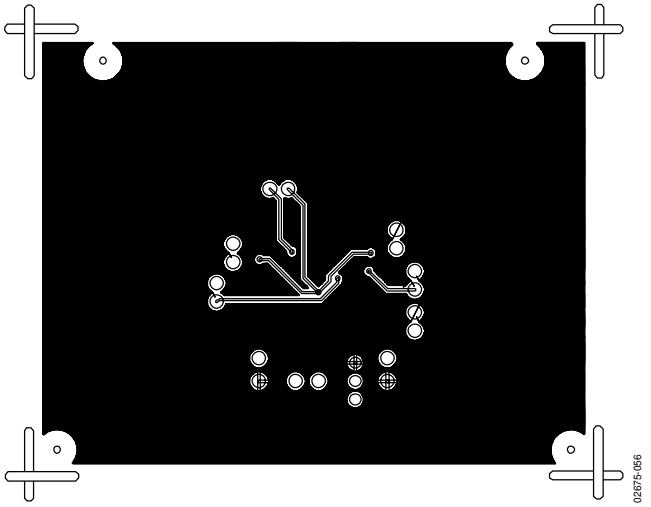

Figure 56. Layout of Circuit Side