Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

50 MHz to 1000 MHz Quadrature Demodulator

AD8348

FEATURES

Integrated I/Q demodulator with IF VGA amplifier
Operating IF frequency 50 MHz to 1000 MHz
(3 dB IF BW of 500 MHz driven from R_S = 200 Ω)
Demodulation bandwidth 75 MHz
Linear-in-decibel AGC range 44 dB
Third-order intercept
IIP3 +28 dBm @ minimum gain (F_{IF} = 380 MHz)
IIP3 −8 dBm @ maximum gain (F_{IF} = 380 MHz)
Quadrature demodulation accuracy
Phase accuracy 0.5°
Amplitude balance 0.25 dB
Noise figure 11 dB @ maximum gain (F_{IF} = 380 MHz)
LO input −10 dBm
Single supply 2.7 V to 5.5 V
Power-down mode
Compact, 28-lead TSSOP package

APPLICATIONS

QAM/QPSK demodulator
W-CDMA/CDMA/GSM/NADC
Wireless local loop
LMDS

FUNCTIONAL BLOCK DIAGRAM

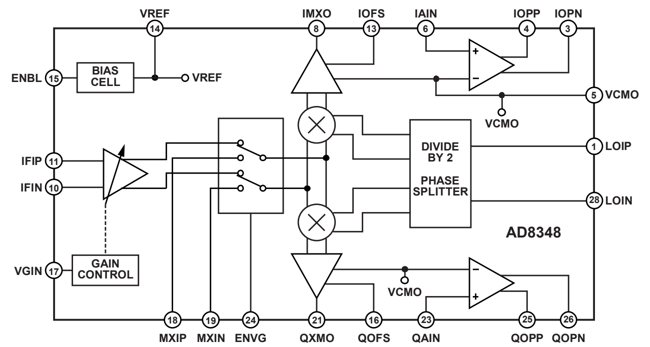

Figure 1.

GENERAL DESCRIPTION

The AD8348 is a broadband quadrature demodulator with an integrated intermediate frequency (IF), variable gain amplifier (VGA), and integrated baseband amplifiers. It is suitable for use in communications receivers, performing quadrature demodulation from IF directly to baseband frequencies. The baseband amplifiers are designed to interface directly with dual-channel ADCs, such as the AD9201, AD9283, and AD9218, for digitizing and post-processing.

The IF input signal is fed into two Gilbert cell mixers through an X-AMP® VGA. The IF VGA provides 44 dB of gain control. A precision gain control circuit sets a linear-in-decibel gain characteristic for the VGA and provides temperature compensation. The LO quadrature phase splitter employs a divide-by-2 frequency divider to achieve high quadrature accuracy and amplitude balance over the entire operating frequency range.

Optionally, the IF VGA can be disabled and bypassed. In this mode, the IF signal is applied directly to the quadrature mixer inputs via the MXIP and MXIN pins.

Separate I- and Q-channel baseband amplifiers follow the baseband outputs of the mixers. The voltage applied to the VCMO pin sets the dc common-mode voltage level at the baseband outputs. Typically, VCMO is connected to the internal VREF voltage, but it can also be connected to an external voltage. This flexibility allows the user to maximize the input dynamic range to the ADC. Connecting a bypass capacitor at each offset compensation input (IOFS and QOFS) nulls dc offsets produced in the mixer. Offset compensation can be overridden by applying an external voltage at the offset compensation inputs.

The mixers' outputs are brought off-chip for optional filtering before final amplification. Inserting a channel selection filter before each baseband amplifier increases the baseband amplifiers' signal handling range by reducing the amplitude of high level, out-of-channel interferers before the baseband signal is fed into the I/Q baseband amplifiers. The single-ended mixer output is amplified and converted to a differential signal for driving ADCs.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

AD8348* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD8348 Evaluation Board

DOCUMENTATION

Application Notes

- AN-924: Digital Quadrature Modulator Gain

Data Sheet

- AD8348: 50-1000 MHz Quadrature Demodulator Data Sheet

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- Simplifying Direct-Conversion Tx Paths in Wireless Designs

DESIGN RESOURCES

- AD8348 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD8348 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

4/06—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Specifications ... 3
Changes to IF Inputs Section ... 20
Changes to Evaluation Board Section ... 23
Changes to Table 6 ... 27
Changes to Ordering Guide ... 28

8/03—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, F_{LO} = 380 MHz, F_{IF} = 381 MHz, P_{LO} = −10 dBm, R_S (LO) = 50 Ω, R_S (IFIP and MXIP/MXIN) = 200 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO Frequency Range	External input = 2 × LO frequency	100		2000	MHz
IF Frequency Range		50		1000	MHz
Baseband Bandwidth			75		MHz
LO Input Level	50 Ω source	−12	−10	0	dBm
V_{SUPPLY} (V_S)		2.7		5.5	V
Temperature Range		−40		+85	°C
IF FRONT END WITH VGA	IFIP to IMXO (QMXO),				
	ENVG = 5 V, IMXO/QMXO load = 1.5 kΩ				
Input Impedance	Measured differentially across MXIP/MXIN		200‖1.1		Ω‖pF
Gain Control Range			44		dB
Maximum Conversion Voltage Gain	VGIN = 0.2 V (maximum voltage gain)		25.5		dB
Minimum Conversion Voltage Gain	VGIN = 1.2 V (minimum voltage gain)		−18.5		dB
3 dB Bandwidth			500		MHz
Gain Control Linearity	VGIN = 0.4 V (+21 dB) to 1.1 V (−14 dB)		±0.5		dB
IF Gain Flatness	F_{IF} = 380 MHz ± 5% (VGIN = 1.2 V)		0.1		dB p-p
	F_{IF} = 900 MHz ± 5% (VGIN = 1.2 V)		1.3		dB p-p
Input 1 dB Compression Point (P1dB)	VGIN = 0.2 V (maximum gain)		−22		dBm
	VGIN = 1.2 V (maximum gain)		+13		dBm
Second-Order Input Intercept (IIP2)	IF1 = 385 MHz, IF2 = 386 MHz				
	+3 dBm each tone from 200 Ω source,		65		dBm
	VGIN = 1.2 V (minimum gain)				
	−42 dBm each tone from 200 Ω source,		18		dBm
	VGIN = 0.2 V (maximum gain)				
Third-Order Input Intercept (IIP3)	IF1 = 381 MHz, IF2 = 381.02 MHz				
	Each tone 10 dB below P1dB from 200 Ω source,		28		dBm
	VGIN = 1.2 V (minimum gain)				
	Each tone 10 dB below P1dB from 200 Ω source,		−8		dBm
	VGIN = 0.2 V (maximum gain)				
LO Leakage	Measured at IFIP, IFIN		−80		dBm
	Measured at IMXO/QMXO (LO = 50 MHz)		−60		dBm
Demodulation Bandwidth	Small signal 3 dB bandwidth		75		MHz
Quadrature Phase Error[1]	LO = 380 MHz (LOIP/LOIN 760 MHz)	−0.7	±0.1	+0.7	Degrees
	vs. temperature		−0.0032		°/°C
	vs. baseband frequency (dc to 30 MHz)		+0.01		°/MHz
I/Q Amplitude Imbalance[1]		−0.3	±0.05	+0.3	dB
	vs. temperature		0		dB/°C
	vs. baseband frequency (dc to 30 MHz)		±0.0125		dB
Noise Figure (Double Sideband)	Maximum gain, from 200 Ω source, F_{IF} = 380 MHz		10.75		dB
Mixer Output Impedance			40		Ω
Capacitive Load	Shunt from IMXO, QMXO to VCMO	0		10	pF
Resistive Load	Shunt from IMXO, QMXO to VCMO	200	1.5		kΩ
Mixer Peak Output Current			2.5		mA

Parameter	Conditions	Min	Typ	Max	Unit
IF FRONT END WITHOUT VGA	From MXIP, MXIN to IMXO (QMXO), ENVG = 0 V, IMXO/QMXO load = 1.5 kΩ				
Input Impedance	Measured differentially across MXIP/MXIN		200||1.5		Ω||pF
Conversion voltage Gain			10.5		dB
3 dB Output Bandwidth			75		MHz
IF Gain Flatness	F_{IF} = 380 MHZ ± 5%		0.1		dB p-p
	F_{IF} = 900 MHZ ± 5%		0.15		dB p-p
Input 1 dB Compression Point (P1dB)			−4		dBm
Third-Order Input Intercept (IIP3)	IF1 = 381 MHz, IF2 = 381.02 MHz		14		dBm
	Each tone 10 dB below P1dB from 200 Ω source				
LO Leakage	Measured at MXIP/MXIN		−70		dBm
	Measured at IMXO, QMXO		−60		dBm
Demodulation Bandwidth	Small signal 3 dB bandwidth		75		MHz
Quadrature Phase Error	LO = 380 MHz (LOIP/LOIN 760 MHz, single-ended)	−2	±0.5	+2	Degrees
I/Q Amplitude Imbalance			0.25		dB
Noise Figure (Double Sideband)	From 200 Ω source, F_{IF} = 380 MHz		21		dB
I/Q BASEBAND AMPLIFIER	From IAIN to IOPP/IOPN and QAIN to QOPP/QOPN, R_{LOAD} = 2 kΩ, single-ended to ground				
Gain			20		dB
Bandwidth	10 pF differential load		125		MHz
Output DC Offset (Differential)	LO leakage offset corrected using 500 pF capacitor on IOFS, QOFS ($V_{IOPP} − V_{IOPN}$)	−50	±12	+50	mV
Output Common-Mode Offset	($V_{IOPP} + V_{IOPN}$)/2 − VCMO	−75	±35	+75	mV
Group Delay Flatness	0 MHz to 50 MHz		3		ns p-p
Input-Referred Noise Voltage	Frequency = 1 MHz		8		nV/√Hz
Output Swing Limit (Upper)		V_S −1			V
Output Swing Limit (Lower)				0.5	V
Peak Output Current			1		mA
Input Impedance			50||1		kΩ||pF
Input Bias Current			2		μA
RESPONSE FROM IF AND MX INPUTS TO BASEBAND AMPLIFIER OUTPUT	IMXO and QMXO connected directly to IAIN and QAIN, respectively				
Gain	From MXIP/MXIN		30.5		dB
	From IFIP/IFIN, VGIN = 0.2 V		45.5		dB
	From IFIP/IFIN, VGIN = 1.2 V		1.5		dB
CONTROL INPUT/OUTPUTS					
VCMO Input Range	V_S = 5 V	0.5	1	4	V
	V_S = 2.7 V	0.5	1	1.7	V
VREF Output Voltage		0.95	1	1.05	V
Gain Control Voltage Range	VGIN	0.2		1.2	V
Gain Slope		−55	−50	−45	dB/V
Gain Intercept	Linear extrapolation back to theoretical gain at VGIN = 0 V	55	61	67	dB
Gain Control Input Bias Current			1		μA
LO INPUTS					
LOIP Input Return Loss	LOIN ac-coupled to ground (760 MHz applied to LOIP)		−6		dB

Parameter	Conditions	Min	Typ	Max	Unit
POWER-UP CONTROL					
ENBL Threshold Low	Low = standby	0	$V_S/2$	1	V
ENBL Threshold High	High = enable	$V_S - 1$	$V_S/2$	V_S	V
Input Bias Current			2		µA
Power-Up Time	Time for final baseband amplifiers to be within 90% of final amplitude		45		µs
Power-Down Time	Time for supply current to be <10% of enabled value		700		ns
POWER SUPPLIES	VPOS1, VPOS2, VPOS3				
Voltage		2.7		5.5	V
Current (Enabled)	$V_S = 5$ V, $V_{ENBL} = 5$ V	38	48	58	mA
Current (Standby)	$V_S = 5$ V, $V_{ENBL} = 0$ V		75		µA

[1] These parameters are guaranteed but not tested in production. Limits are ±6 Σ from the mean.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage on VPOS1, VPOS2, VPOS3 Pins	5.5 V
LO Input Power	10 dBm (re: 50 Ω)
IF Input Power	18 dBm (re: 200 Ω)
Internal Power Dissipation	450 mW
θ_{JA}	68°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

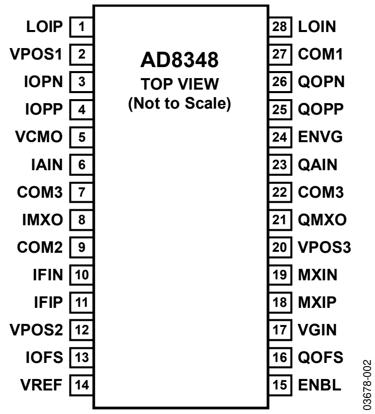

Figure 2. 28-Lead TSSOP Pin Configuration

Table 3. Pin Function Descriptions—28-Lead TSSOP

Pin No.	Mnemonic	Description	Equivalent Circuit
1, 28	LOIP, LOIN	LO Inputs. For optimum performance, these inputs should be ac-coupled and driven differentially. Differential drive from single-ended sources can be achieved via a balun. To obtain a broadband 50 Ω input impedance, connect a 60.4 Ω shunt resistor between LOIP and LOIN. Typical input drive level is equal to −10 dBm.	A
2, 12, 20	VPOS1, VPOS2, VPOS3	Positive Supply for LO, IF, and Biasing and Baseband Sections, Respectively. These pins should be decoupled with 0.1 µF and 100 pF capacitors.	
3, 4, 25, 26	IOPN, IOPP, QOPP, QOPN	I- and Q-Channel Differential Baseband Outputs. Typical output swing is equal to 2 V p-p differential. The dc common-mode voltage level on these pins is set by the voltage on VCMO.	B
5	VCMO	Baseband DC Common-Mode Voltage. The voltage applied to this pin sets the dc common-mode levels for all the baseband outputs and inputs (IMXO, QMXO, IOPP, IOPN, QOPP, QOPN, IAIN, and QAIN). This pin can be connected either to VREF or to a reference voltage from another device (typically an ADC).	C
6, 23	IAIN, QAIN	I- and Q-Channel Baseband Amplifier Inputs. The single-ended signals on these pins are referenced to VCMO and must have a dc bias equal to the dc voltage on the VCMO pin. If IMXO (QMXO) is dc-coupled to IAIN (QAIN), biasing will be provided by IMXO (QMXO). If an ac-coupled filter is placed between IMXO and IAIN, these pins can be biased from the source driving VCMO through a 1 kΩ resistor. The gain from IAIN/QAIN to the differential outputs (IOPP/IOPN and QOPP/QOPN) is 20 dB.	D
7, 22	COM3	Ground for Biasing and Baseband Sections.	
8, 21	IMXO, QMXO	I- and Q-Channel Mixer Baseband Outputs. These are low impedance (40 Ω) outputs whose bias levels are set by the voltage applied to the VCMO pin. These pins are typically connected to IAIN and QAIN, respectively, either directly or through a filter. Each output can drive a maximum current of 2.5 mA.	H
9	COM2	IF Section Ground.	
10, 11	IFIN, IFIP	IF Inputs. IFIN should be ac-coupled to ground. The single-ended IF input signal should be ac-coupled into IFIP. The nominal differential input impedance of these pins is 200 Ω. For a broadband 50 Ω input impedance, a minimum-loss L pad should be used; R_{SERIES} = 174 Ω, R_{SHUNT} = 57.6 Ω. This provides a 200 Ω source impedance to the IF input. However, the AD8348 does not necessarily require a 200 Ω source impedance, and a single shunt 66.7 Ω resistor can be placed between IFIP and IFIN.	E
13, 16	IOFS, QOFS	I- and Q-Channel Offset Nulling Inputs. DC offsets on the I-channel mixer output (IMXO) can be nulled by connecting a 0.1 µF capacitor from IOFS to ground. Driving IOFS with a fixed voltage (typically a DAC calibrated such that the offset at IOPP/IOPN is nulled) can extend the operating frequency range to include dc. The QOFS pin can likewise be used to null offsets on the Q-channel mixer output (QMXO).	F
14	VREF	Reference Voltage Output. This output voltage (1 V) is the main bias level for the device and can be used to externally bias the inputs and outputs of the baseband amplifiers. The typical maximum drive current for this output is 2 mA.	G

Pin No.	Mnemonic	Description	Equivalent Circuit
15	ENBL	Chip Enable Input. Active high. Threshold is equal to $V_S/2$.	D
17	VGIN	Gain Control Input. The voltage on this pin controls the gain on the IF VGA. The gain control voltage range is from 0.2 V to 1.2 V and corresponds to a conversion gain range from +25.5 dB to −18.5 dB. This is the gain to the output of the mixers (that is, IMXO and QMXO). There is an additional 20 dB of fixed gain in the final baseband amplifiers (IAIN to IOPP/IOPN and QAIN to QOPP/QOPN). Note that the gain control function has a negative sense (that is, increasing voltage decreases gain).	D
18, 19	MXIP, MXIN	Auxiliary Mixer Inputs. If ENVG is low, the IFIP and IFIN inputs are disabled and MXIP and MXIN are enabled, allowing the VGA to be bypassed. The auxiliary mixer inputs are fully differential inputs that should be ac-coupled to the signal source.	I
24	ENVG	Active High VGA Enable. When ENVG is high, IFIP and IFIN inputs are enabled and MXIP and MXIN inputs are disabled. When ENVG is low, MXIP and MXIN inputs are enabled and IFIP and IFIN inputs are disabled.	D
27	COM1	LO Section Ground.	

EQUIVALENT CIRCUITS

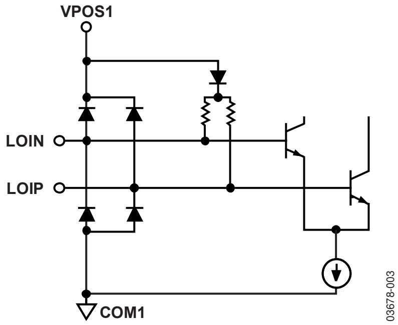

Figure 3. Circuit A

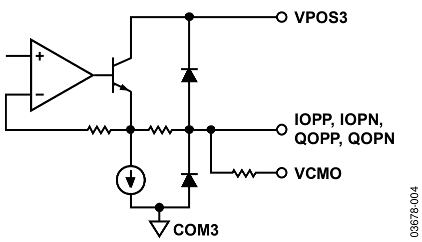

Figure 4. Circuit B

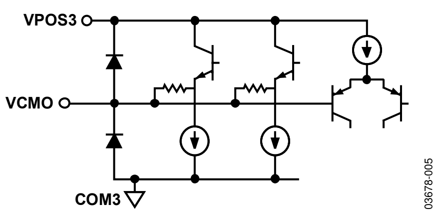

Figure 5. Circuit C

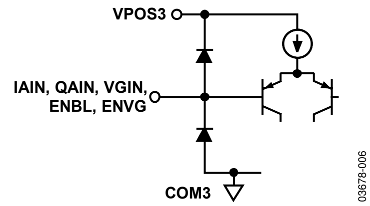

Figure 6. Circuit D

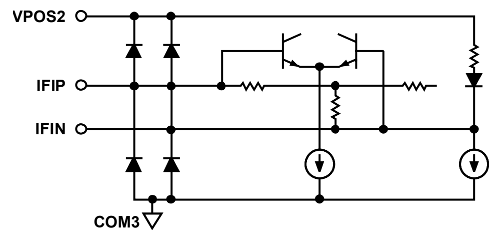

Figure 7. Circuit E

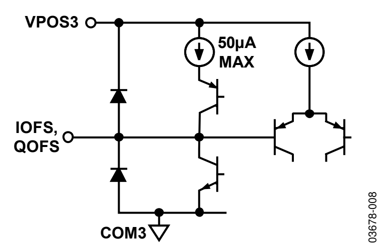

Figure 8. Circuit F

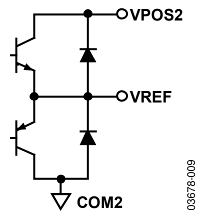

Figure 9. Circuit G

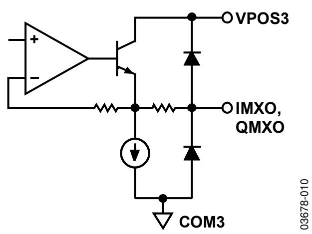

Figure 10. Circuit H

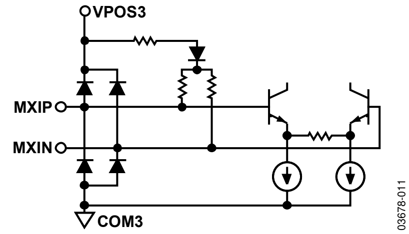

Figure 11. Circuit I

TYPICAL PERFORMANCE CHARACTERISTICS

VGA AND DEMODULATOR

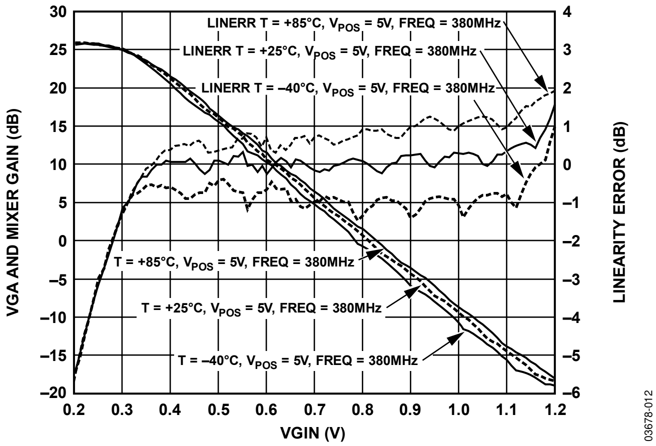

Figure 12. Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 5 V, F_{IF} = 380 MHz, F_{BB} = 1 MHz, Temperature = −40°C, +25°C, +85°C

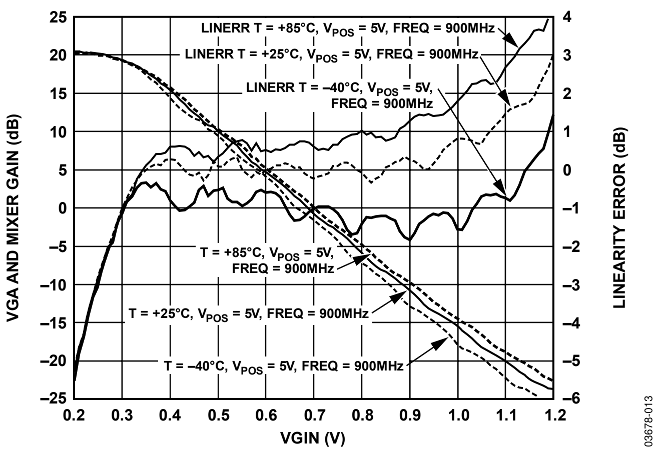

Figure 13. Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 5 V, F_{IF} = 900 MHz, F_{BB} = 1 MHz, Temperature = −40°C, +25°C, +85°C

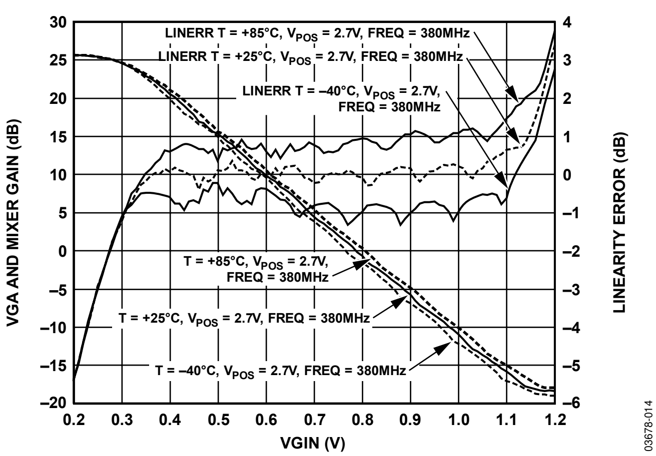

Figure 14. Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 2.7 V, F_{IF} = 380 MHz, F_{BB} = 1 MHz, Temperature = −40°C, +25°C, +85°C

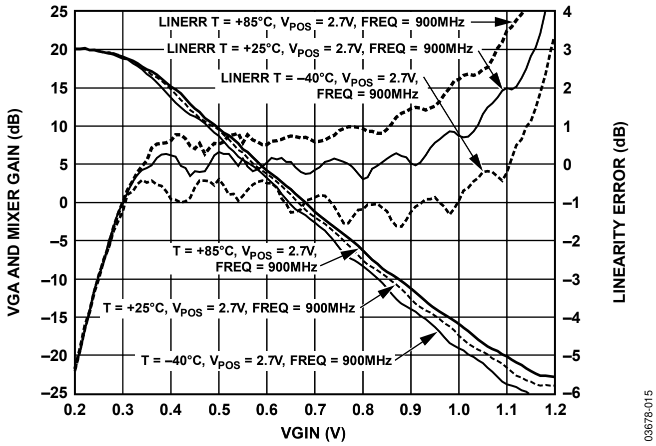

Figure 15. Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 2.7 V, F_{IF} = 900 MHz, F_{BB} = 1 MHz, Temperature = −40°C, +25°C, +85°C

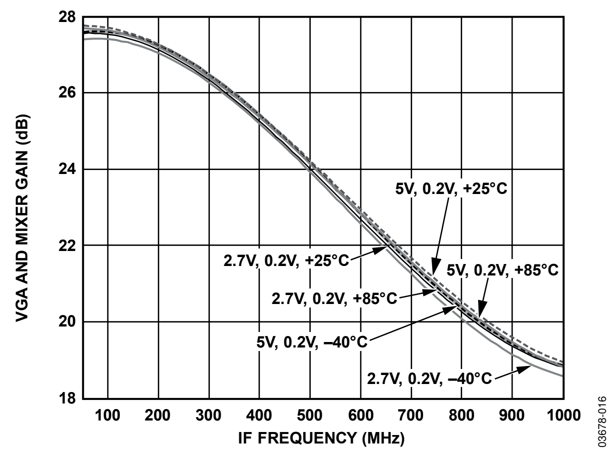

Figure 16. Gain vs. F_{IF}, VGIN = 0.2 V, F_{BB} = 1 MHz, Temperature = −40°C, +25°C, +85°C

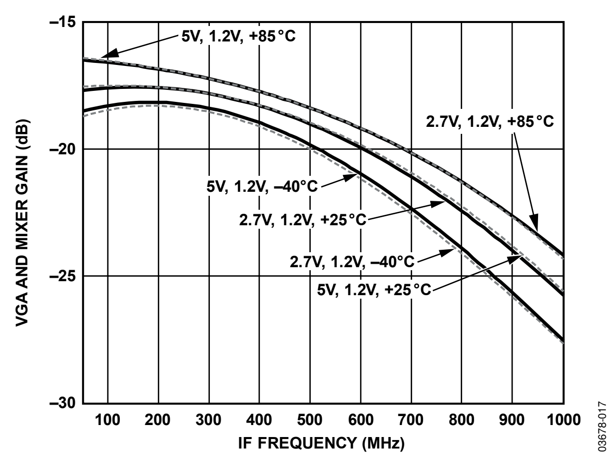

Figure 17. Gain vs. F_{IF}, VGIN = 1.2 V, F_{BB} = 1 MHz, Temperature = −40°C, +25°C, +85°C

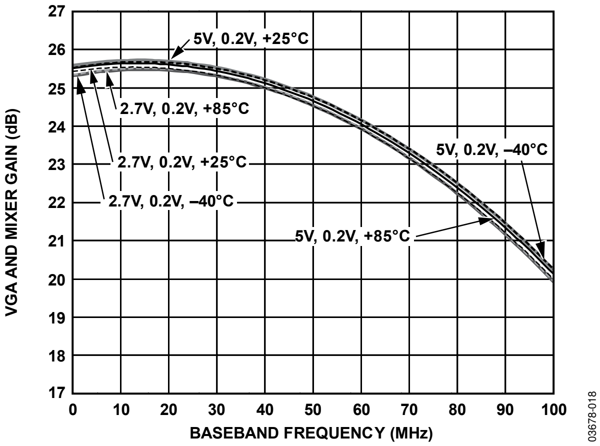

Figure 18. Gain vs. F_{BB}, VGIN = 0.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

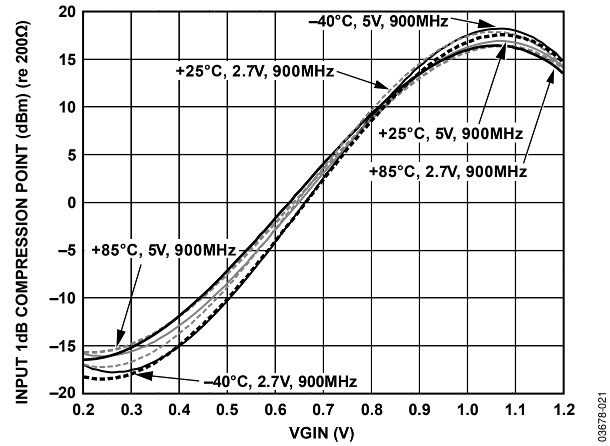

Figure 21. Input 1 dB Compression Point (IP1dB) vs. VGIN, F_{IF} = 900 MHz, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

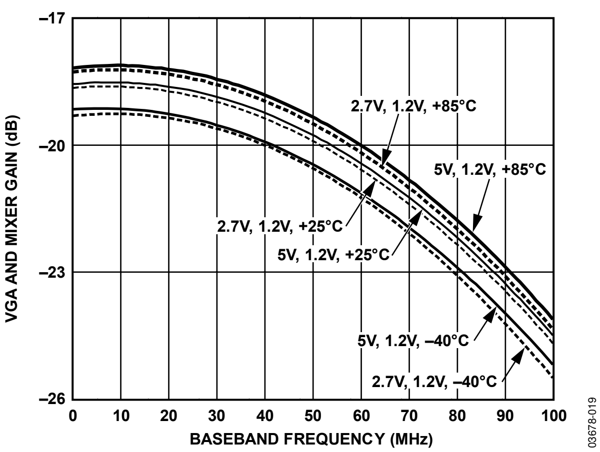

Figure 19. Gain vs. F_{BB}, VGIN = 1.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

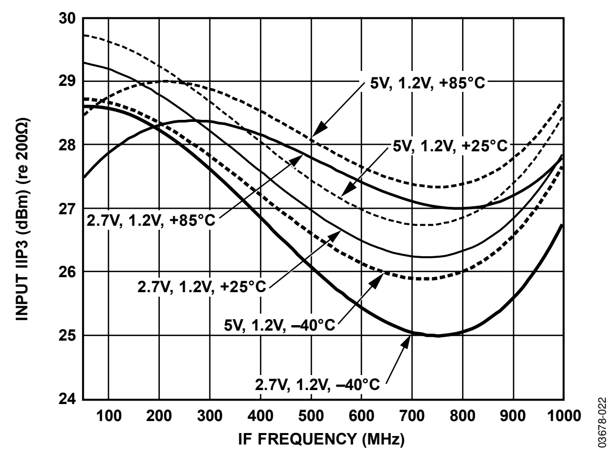

Figure 22. IIP3 vs. F_{IF}, VGIN = 1.2 V, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C, Tone Spacing = 20 kHz

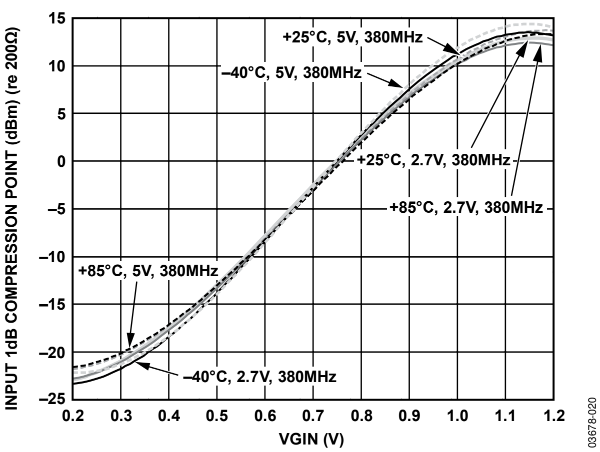

Figure 20. Input 1 dB Compression Point (IP1dB) vs. VGIN, F_{IF} = 380 MHz, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

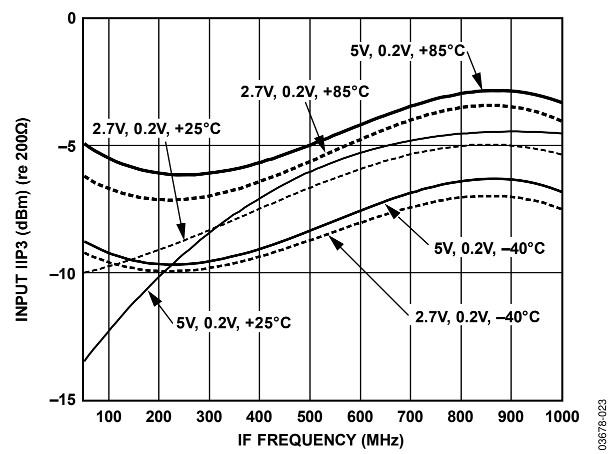

Figure 23. IIP3 vs. F_{IF}, VGIN = 0.2 V, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

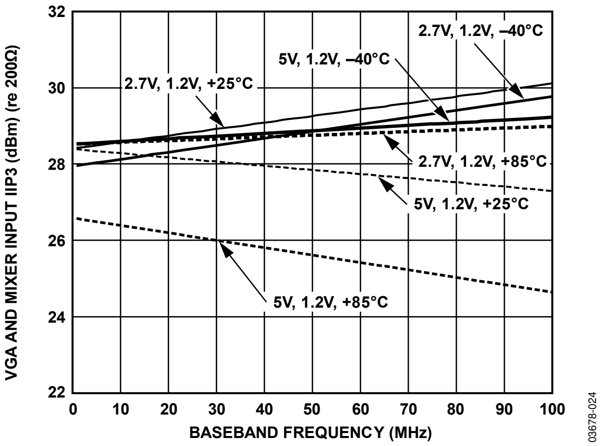

Figure 24. IIP3 vs. F_{BB}, VGIN = 1.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

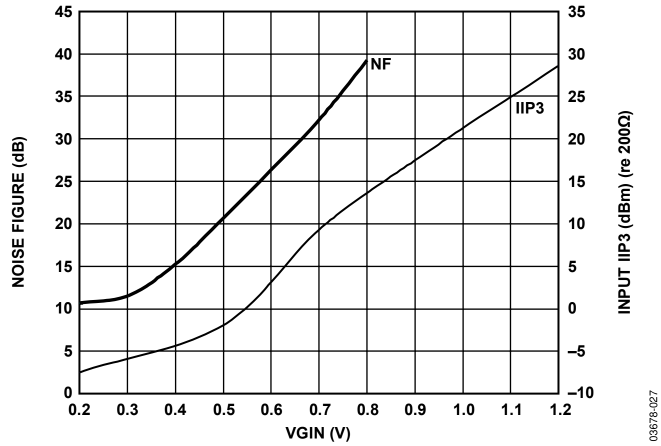

Figure 27. Noise Figure and IIP3 vs. VGIN, Temperature = 25°C, F_{IF} = 380 MHz, F_{BB} = 1 MHz, V_{POS} = 2.7 V

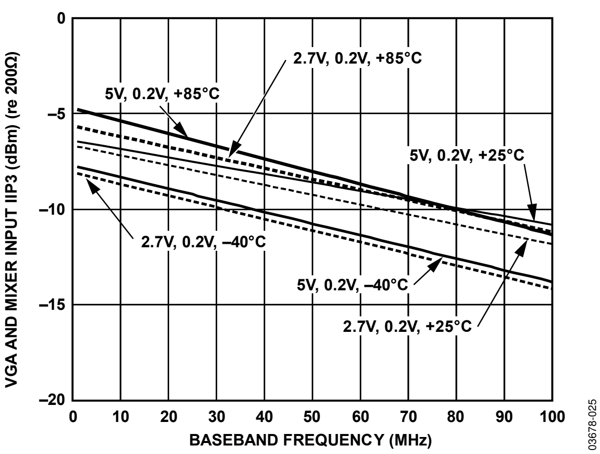

Figure 25. IIP3 vs. F_{BB}, VGIN = 0.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

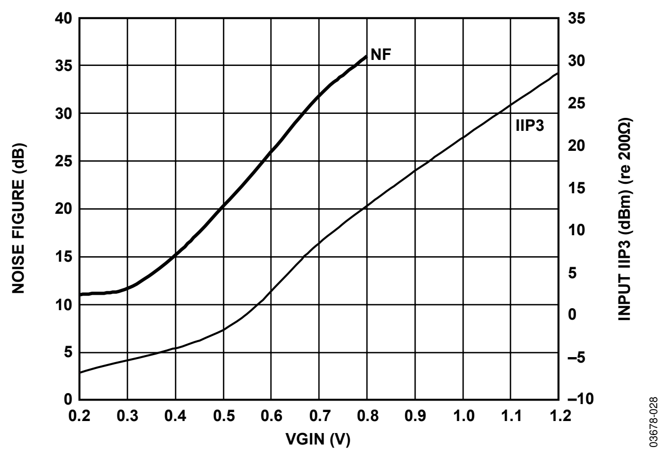

Figure 28. Noise Figure and IIP3 vs. VGIN, Temperature = 25°C, F_{IF} = 380 MHz, F_{BB} = 1 MHz, V_{POS} = 5 V

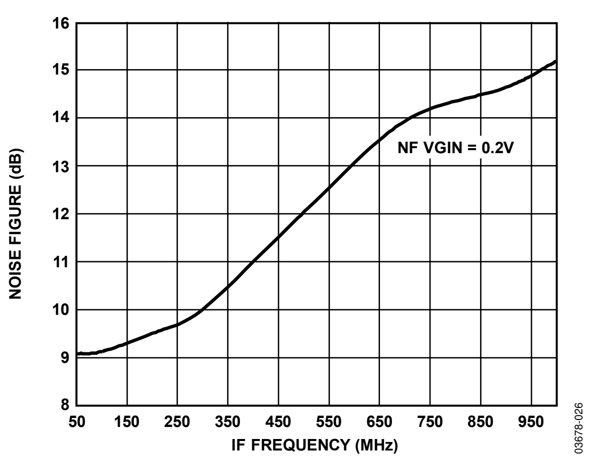

Figure 26. Noise Figure vs. F_{IF}, T = 25°C, VGIN = 0.2 V, F_{BB} = 1 MHz

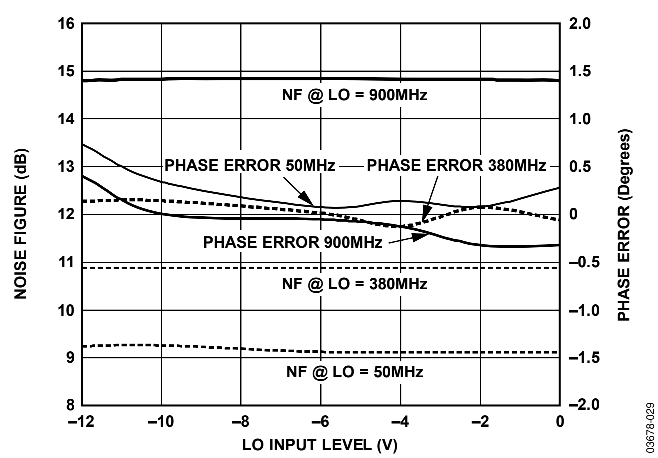

Figure 29. Noise Figure and Quadrature Phase Error IMXO/QMXO vs. LO Input Level, Temperature = 25°C, VGIN = 0.2 V, V_{POS} = 5 V for F_{IF} = 50 MHz, 380 MHz, and 900 MHz

DEMODULATOR USING MXIP AND MXIN

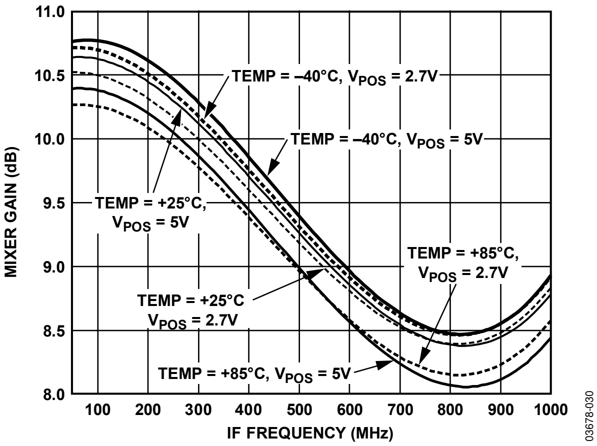

Figure 30. Mixer Gain vs. F_{IF}, V_{POS} = 2.7 V, 5 V, F_{BB} = 1 MHz, Temperature = −40°C, +25°C, +85°C

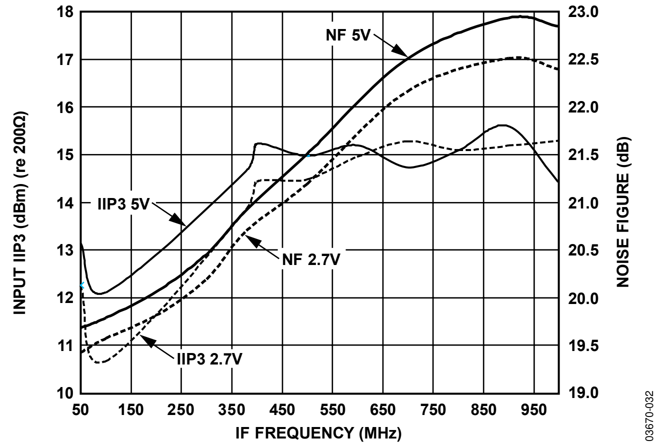

Figure 32. IIP3 and Noise Figure vs. F_{IF}, V_{POS} = 2.7 V, 5 V, Temperature = 25°C

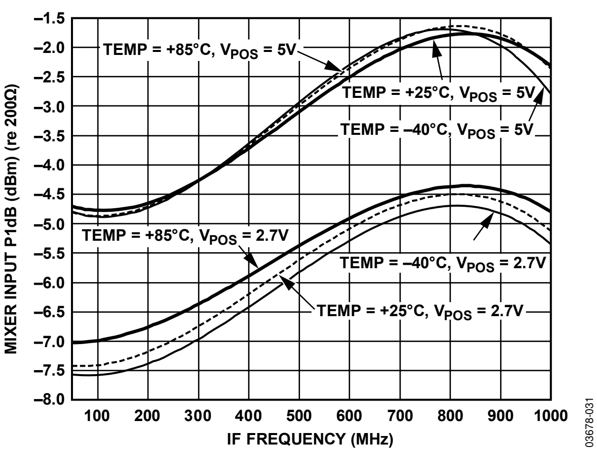

Figure 31. Input 1 dB Compression Point vs. F_{IF}, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

FINAL BASEBAND AMPLIFIERS

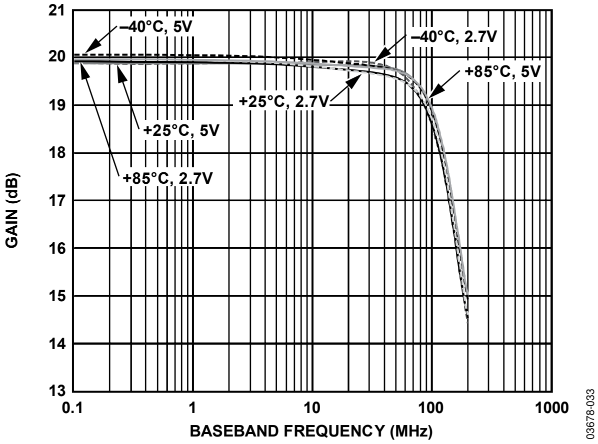

Figure 33. Gain vs. F_{BB}, V_{VCMO} = VREF = 1 V, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

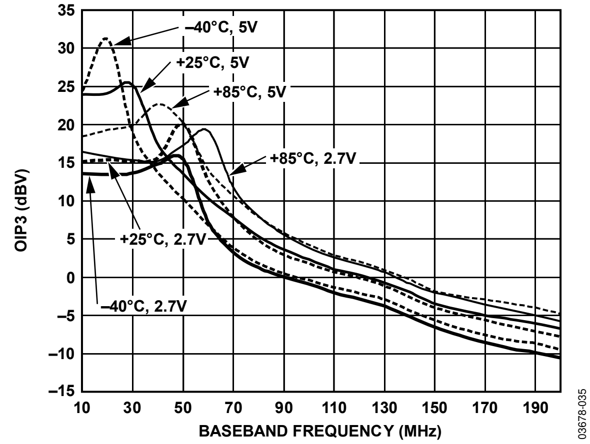

Figure 35. OIP3 vs. F_{BB}, V_{VCMO} = VREF = 1 V, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

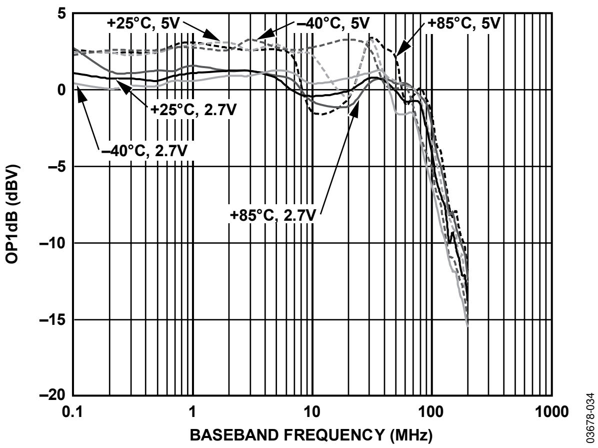

Figure 34. OP1dB Compression vs. F_{BB}, V_{VCMO} = VREF = 1 V, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

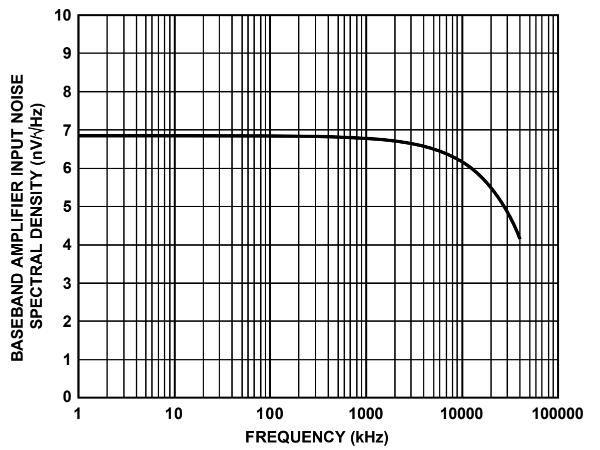

Figure 36. Noise Spectral Density

VGA/DEMODULATOR AND BASEBAND AMPLIFIER

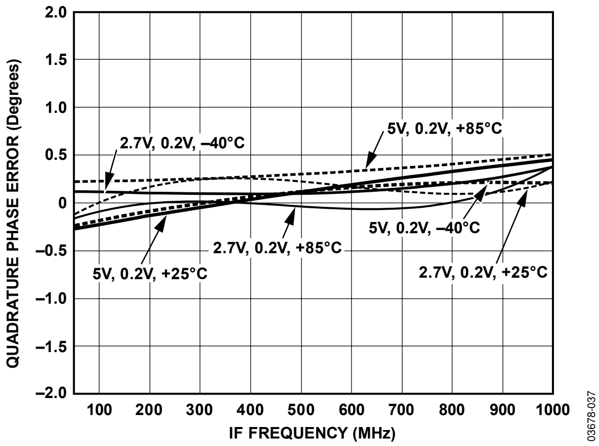

Figure 37. Quadrature Phase Error vs. F_{IF}, VGIN = 0.7 V, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

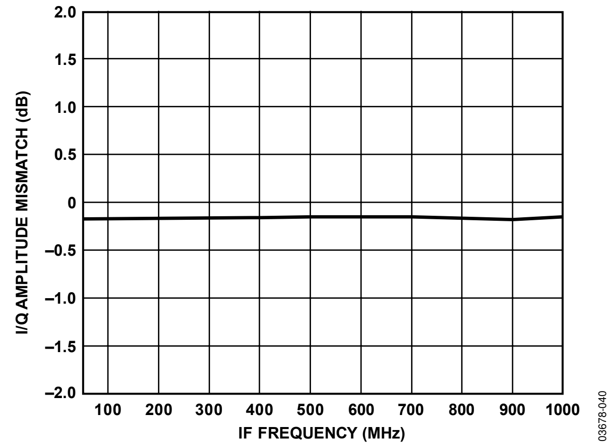

Figure 40. I/Q Amplitude Imbalance vs. F_{IF}, Temperature = 25°C, V_{POS} = 5 V

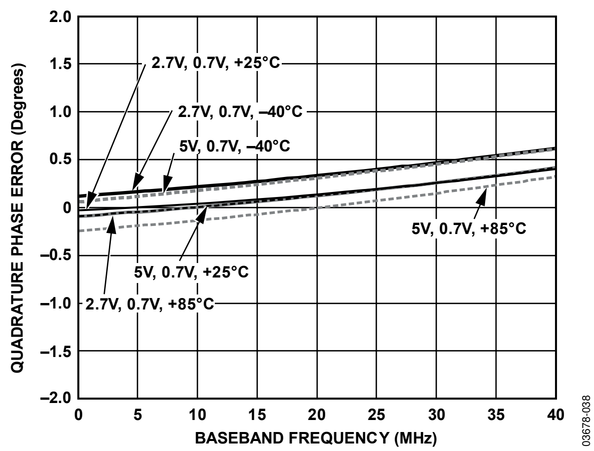

Figure 38. Quadrature Phase Error vs. F_{BB}, VGIN = 0.7 V, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C, F_{IF} = 380 MHz

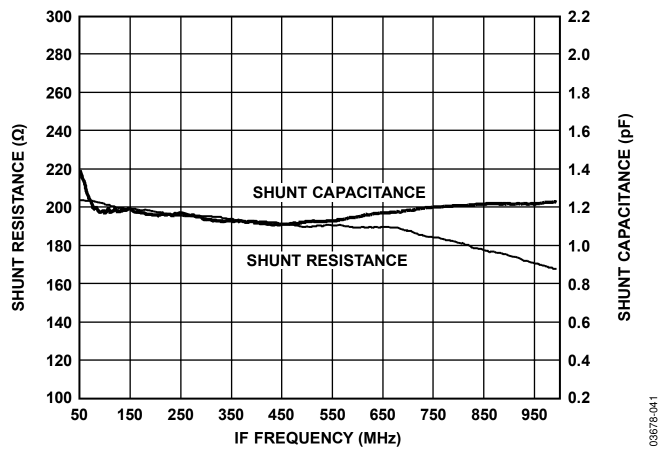

Figure 41. Input Impedance of IF Input vs. F_{IF}, VGIN = 0.7 V, V_{POS} = 5 V

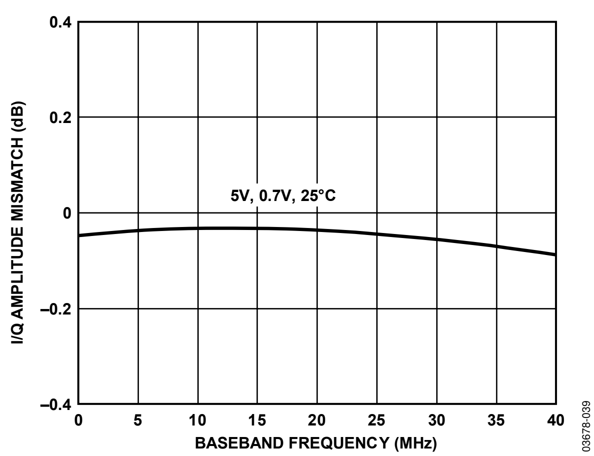

Figure 39. I/Q Amplitude Imbalance vs. F_{BB}, Temperature = 25°C, V_{POS} = 5 V

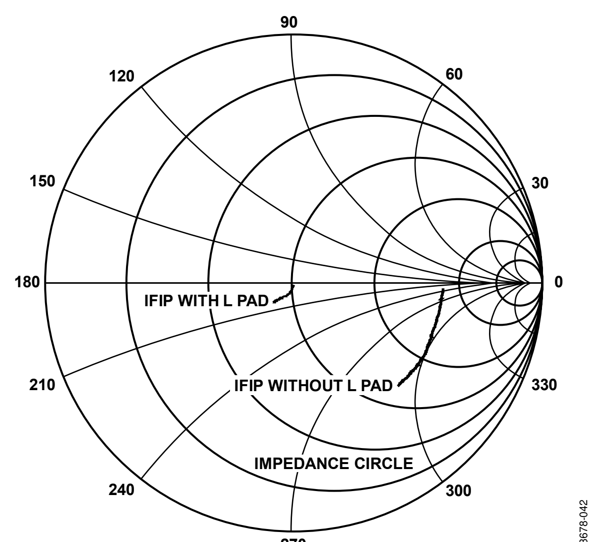

Figure 42. S11 of IF Input vs. F_{IF}, F_{IF} = 50 MHz to 1 GHz, VGIN = 0.7 V, V_{POS} = 5 V (with L Pad, with No Pad, Normalized to 50 Ω)

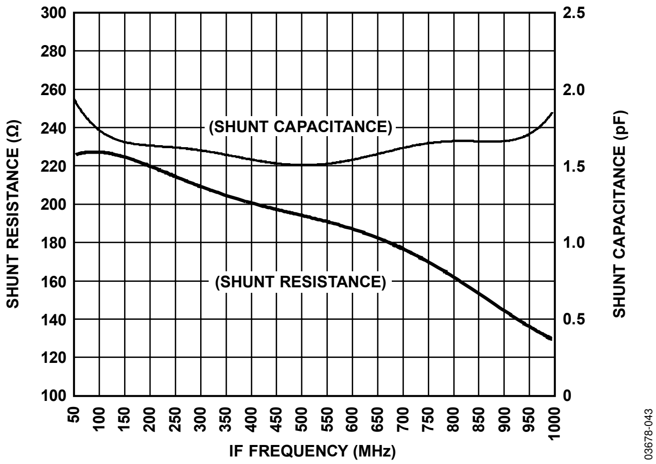

Figure 43. Input Impedance of Mixer Input vs. F_{IF}, VGIN = 0.7 V, V_{POS} = 5 V

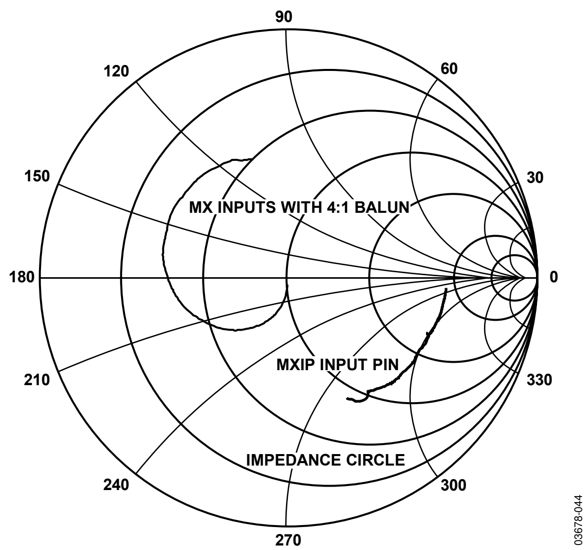

Figure 44. S11 of Mixer Input vs. F_{IF}, F_{IF} = 50 MHz to 1 GHz, VGIN = 0.7 V, V_{POS} = 5 V (With and Without Balun)

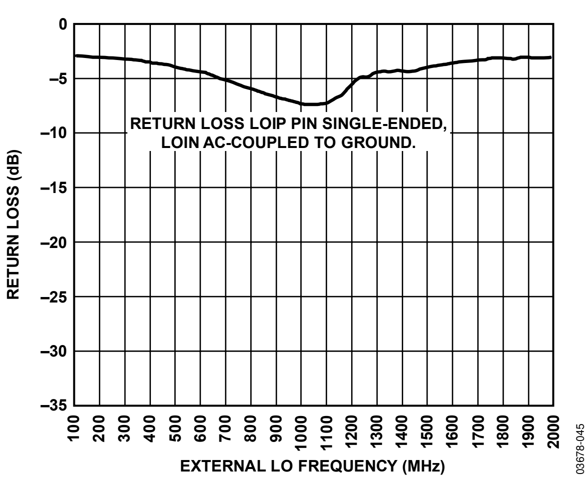

Figure 45. Return Loss of LOIP Input vs. External LO Frequency

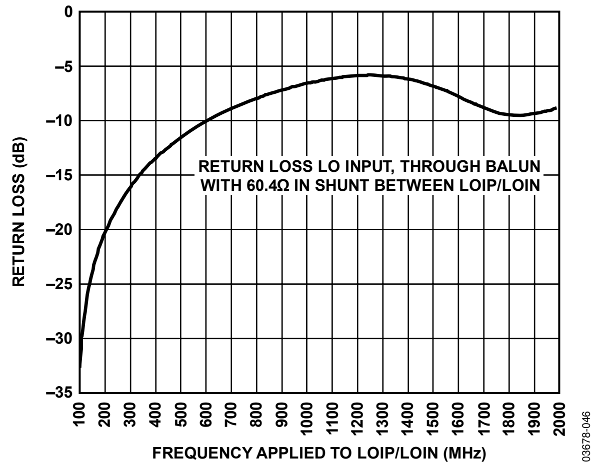

Figure 46. Return Loss of LO Input vs. External LO Frequency Through Balun, with Termination Resistor

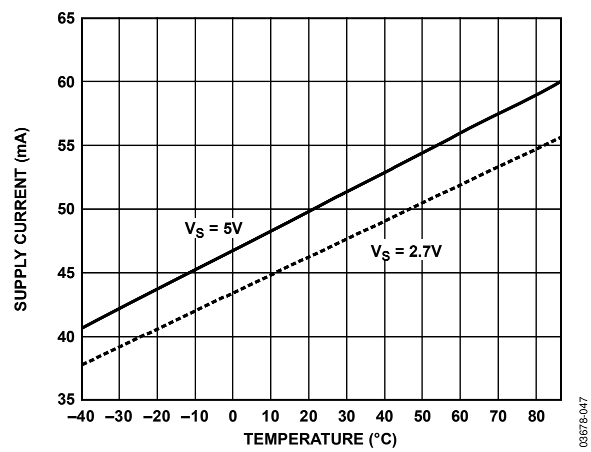

Figure 47. Supply Current vs. Temperature

THEORY OF OPERATION

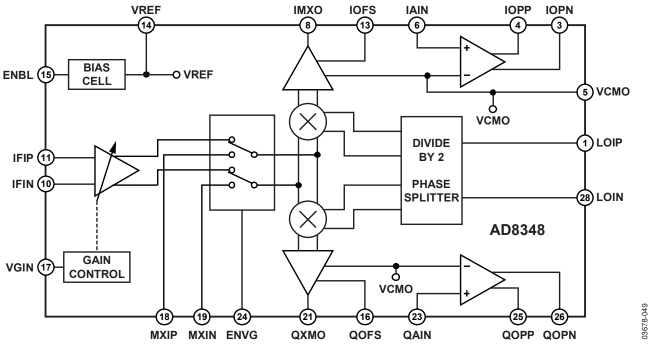

Figure 48. Functional Block Diagram

VGA

The VGA is implemented using the patented X-AMP architecture. The single-ended IF signal is attenuated in eight discrete 6 dB steps by a passive R-2R ladder. Each discrete attenuated version of the IF signal is applied to the input of a transconductance stage. The current outputs of all transconductance stages are summed together and drive a resistive load at the output of the VGA. Gain control is achieved by smoothly turning on and off the relevant transconductance stages with a temperature-compensated interpolation circuit. This scheme allows the gain to continuously vary over a 44 dB range with linear-in-decibel gain control. This configuration also keeps the relative dynamic range constant (for example, IIP3 – NF in dB) over the gain setting; however, the absolute intermodulation intercepts and noise figure vary directly with gain. The analog voltage VGIN sets the gain. VGIN = 0.2 V is the maximum gain setting, and VGIN = 1.2 V is the minimum voltage gain setting.

DOWNCONVERSION MIXERS

The output of the VGA drives two (I and Q) double-balanced Gilbert cell downconversion mixers. Alternatively, driving the ENVG pin low can disable the VGA, and the mixers can be externally driven directly via the MXIP and MXIN ports. At the input of the mixer, a degenerated differential pair performs linear voltage-to-current conversions. The differential output current feeds into the mixer core where it is downconverted by the mixing action of the Gilbert cell. The phase splitter provides quadrature LO signals that drive the LO ports of the in-phase and quadrature mixers.

Buffers at the output of each mixer drive the IMXO and QMXO pins. These linear, low output impedance buffers drive 40 Ω, temperature-stable, passive resistors in series with each output pin (IMXO and QMXO). This 40 Ω should be considered when calculating the reverse termination if an external filter is inserted between IMXO (QMXO) and IAIN (QAIN). The VCMO pin sets the dc output level of the buffer. This can be set externally or connected to the on-chip 1.0 V reference, VREF.

PHASE SPLITTER

Quadrature generation is achieved using a divide-by-2 frequency divider. Unlike a polyphase filter that achieves quadrature over a limited frequency range, the divide-by-2 approach maintains quadrature over a broad frequency range and does not attenuate the LO. The user, however, must provide an external signal XLO that is twice the frequency of the desired LO frequency. XLO drives the clock inputs of two flip-flops that divide down the frequency by a factor of 2. The outputs of the two flip-flops are one-half period of XLO out of phase. Equivalently, the outputs are one-quarter period (90°) of the desired LO frequency out of phase. Because the transitions on XLO define the phase difference at the outputs, deviation from 50% duty cycle translates directly to quadrature phase errors.

If the user generates XLO from a 1× frequency (f_{REF}) and a frequency-doubling circuit (XLO = 2 × f_{REF}), fundamentally there is a 180° phase uncertainty between f_{REF} and the AD8348 internal quadrature LO. The phase relationship between I and Q LO, however, is always 90°.

I/Q BASEBAND AMPLIFIERS

Two (I and Q) fixed gain (20 dB), single-ended-to-differential amplifiers are provided to amplify the demodulated signal after off-chip filtering. The amplifiers use voltage feedback to linearize the gain over the demodulation bandwidth. These amplifiers can be used to maximize the dynamic range at the input of an ADC following the AD8348.

The input to the baseband amplifiers, IAIN (QAIN), feeds into the base of a bipolar transistor with an input impedance of roughly 50 kΩ. The baseband amplifiers sense the single-ended difference between IAIN (QAIN) and VCMO. IAIN (QAIN) can be dc biased by terminating it with a shunt resistor to VCMO, such as when an external filter is inserted between IMXO (QMXO) and IAIN (QAIN). Alternatively, any dc connection to IMXO (QXMO) can provide appropriate bias via the offset-nulling loop.

ENABLE

A master biasing cell that can be disabled using the ENBL pin controls the biasing for the chip. If the ENBL pin is held low, the entire chip powers down to a low power sleep mode, typically consuming 75 μA at 5 V.

BASEBAND OFFSET CANCELLATION

A low output current integrator senses the output voltage offset at IOPP and IOPN (QOPP and QOPN) and injects a nulling current into the signal path. The integration time constant of the offset-nulling loop is set by Capacitor COFS from IOFS (QOFS) to

VCMO. This forms a high-pass response for the baseband signal path with a lower 3 dB frequency of

$$f_{PASS} = \frac{1}{2\pi \times 2650\ \Omega\ \times COFS}$$

Alternatively, the user can externally adjust the dc offset by driving IOFS (QOFS) with a digital-to-analog converter or other voltage source. In this case, the baseband circuit operates all the way down to dc (f_{PASS} = 0 Hz). The integrator output current is only 50 μA and can be easily overridden with an external voltage source. The nominal voltage level applied to IOFS (QOFS) to produce a 0 V differential offset at the baseband outputs is 900 mV.

The IOFS (QOFS) pin must be connected to either a bypass capacitor (>0.1 μF) or an external voltage source to prevent the feedback loop from oscillating.

The feedback loop will be broken at dc if an ac-coupled baseband filter is placed between the mixer outputs and the baseband amplifier inputs. If an ac-coupled filter is implemented, the user must handle the offset compensation via some external means.

APPLICATIONS

BASIC CONNECTIONS

Figure 49 shows the basic connections schematic for the AD8348.

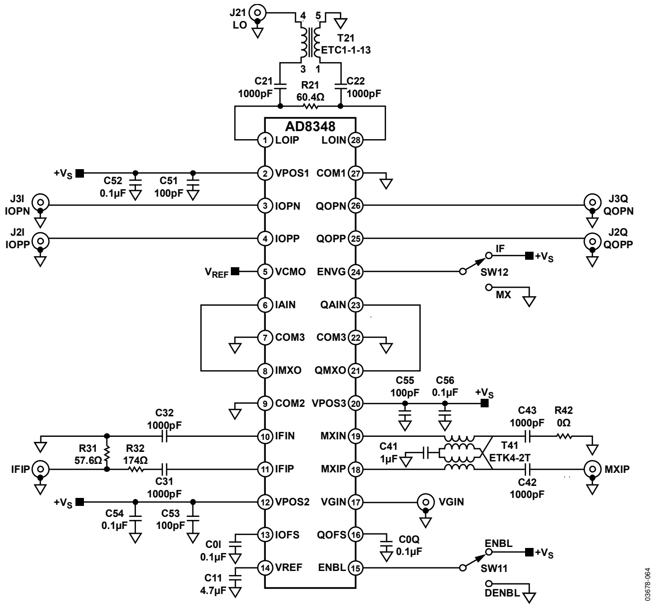

Figure 49. Basic Connections Schematic

POWER SUPPLY

The voltage supply for the AD8348, between 2.7 V and 5 V, should be provided to the +VPOSx pins, and ground should be connected to the COMx pins. Each supply pin should be decoupled separately using two capacitors whose recommended values are 100 pF and 0.1 µF (values close to these can also be used).

DEVICE ENABLE

To enable the device, the ENBL pin should be driven to V_S. Grounding the ENBL pin disables the device.

VGA ENABLE

Driving the voltage on the ENVG pin to V_S enables the VGA. In this mode, the MX inputs are disabled and the IF inputs are used. Grounding the ENVG pin disables the VGA and the IF inputs. When the VGA is disabled, the MX inputs should be used.

GAIN CONTROL

When the VGA is enabled, the voltage applied to the VGIN pin sets the gain. The gain control voltage range is between 0.2 V and 1.2 V. This corresponds to a gain range between +25.5 dB and −18.5 dB.

LO INPUTS

For optimum performance, the local oscillator port should be driven differentially through a balun. The recommended balun is M/A-COM ETC1-1-13. The LO inputs to the device should be ac-coupled, unless an ac-coupled transformer is being used. For a broadband match to a 50 Ω source, a 60.4 Ω resistor should be placed between the LOIP and LION pins.

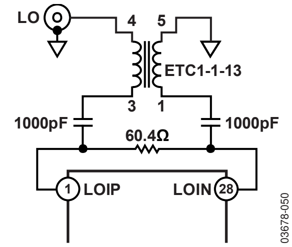

Figure 50. Differential LO Drive with Balun

Alternatively, the LO port can be driven from a single-ended source without a balun (Figure 51). The LO signal is ac-coupled directly into the LOIP pin via an ac-coupling capacitor, and the LOIN pin is ac-coupled to ground. Driving the LO port from a single-ended source results in an increase in both quadrature phase error and LO leakage.

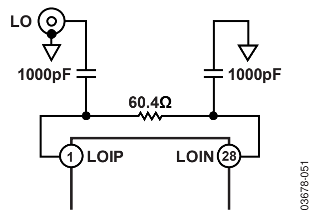

Figure 51. Single-Ended LO Drive

The recommended LO drive level is between −12 dBm and 0 dBm. The LO frequency at the input to the device should be twice that of the desired LO frequency at the mixer core. The applied LO frequency range is between 100 MHz and 2 GHz.

IF INPUTS

The IF inputs have an input impedance of 200 Ω. A broadband 50 Ω match can be presented to the driving source through the use of a minimum-loss L pad. This minimum-loss pad introduces an 11.46 dB loss in the input path and must be taken into account when calculating metrics such as gain and noise figure. Figure 42 shows the S11 of the IF input with and without the L pad.

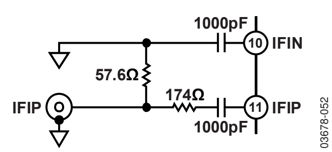

Figure 52. Minimum-Loss L Pad for 50 Ω IF Input

MX INPUTS

The mixer inputs, MXIP and MXIN, have a nominal impedance of 200 Ω and should be driven differentially. When driven from a differential source, the input should be ac-coupled to the source via capacitors, as shown in Figure 53.

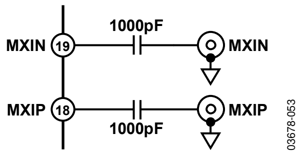

Figure 53. Driving the MX Inputs from a Differential Source

If the MX inputs are to be driven from a single-ended 50 Ω source, a 4:1 balun can be used to transform the 200 Ω impedance of the inputs to 50 Ω while performing the required single-ended-to-differential conversion. The recommended transformer is the M/A-COM ETK4-2T.

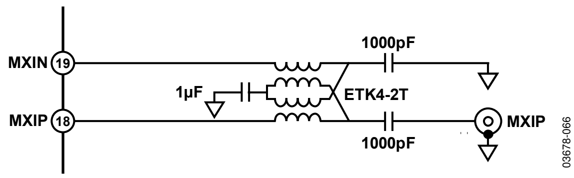

Figure 54. Driving the MX Inputs from a Single-Ended 50 Ω Source

BASEBAND OUTPUTS

The baseband amplifier outputs, IOPP, IOPN, QOPP, and QOPN, should be presented with loads of at least 2 kΩ (single-ended to ground). They are not designed to drive 50 Ω loads directly. The typical swing for these outputs is 2 V p-p differential (1 V p-p single-ended), but larger swings are possible as long as care is taken to ensure that the signals remain within the lower limit of 0.5 V and the upper limit of V_S – 1 V of the output swing. To achieve a larger swing, it is necessary to adjust the common-mode bias of the baseband output signals. Increasing the swing can have the benefit of improving the signal-to-noise ratio of the baseband amplifier output.

When connecting the baseband outputs to other devices, care should be taken to ensure that the outputs are not capacitively loaded by approximately 20 pF or more. Such loads could potentially overload the output or induce oscillations. The effect of capacitive loading on the baseband amplifier outputs can be mitigated by inserting series resistors of approximately 200 Ω.

OUTPUT DC BIAS LEVEL

The dc bias of the mixer outputs and the baseband amplifier inputs and outputs is determined by the voltage that is driven onto the VCMO pin. The range of this voltage is typically between 500 mV and 4 V when operating with a 5 V supply.

To achieve maximum voltage swing from the baseband amplifiers, VCMO should be driven at 2.25 V; this allows a swing of up to 7 V p-p differential (3.5 V p-p single-ended).

INTERFACING TO DETECTOR FOR AGC OPERATION

The AD8348 can be interfaced with a detector such as the AD8362 rms-to-dc converter to provide an automatic signal-leveling function for the baseband outputs.

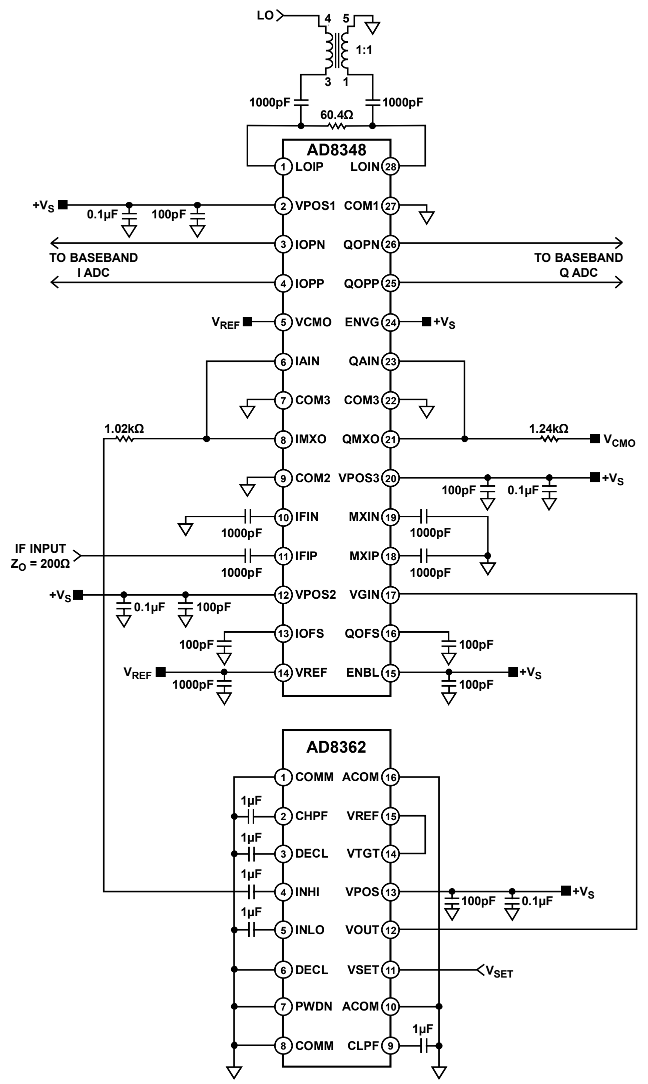

Figure 55. AD8362 Configuration for AGC Operation

Assuming the I and Q channels have the same rms power, the mixer output (or the output of the baseband filter) of one channel can be used as the input of the AD8362. The AD8362 should be operated in a region where its linearity error is small. Also, a voltage divider should be implemented with an external resistor in series with the 200 Ω input impedance of the AD8362 input. This attenuates the AD8348 mixer output so that the AD8362 input is not overdriven. The size of the resistor between the mixer output and the AD8362 input should be chosen so that the peak signal level at the input of the AD8362 is about 10 dB less than the approximately 10 dBm maximum of the AD8362 dynamic range.

The other side of the AD8348 baseband output should be loaded with a resistance equal to the series resistance of the attenuating resistor in series with the AD8362's 200 Ω input impedance. This resistor should be tied to the source driving VCMO so that there is no dc drawn from the mixer output.

The level of the mixer output (or the output of the baseband filter) can then be set by varying the setpoint voltage fed to Pin 11 (VSET) of the AD8362.

Care should be taken to ensure that blockers—unwanted signals in the band of interest that are demodulated along with the desired signal—do not dominate the rms power of the AD8362 input. This can cause an undesired reduction in the level of the mixer output. To overcome this, baseband filtering can be implemented to filter out undesired signals before the signal is presented to the AD8362.

Figure 56 shows the effectiveness of the AGC loop in maintaining a baseband amplifier output amplitude with less than 0.5 dB of amplitude error over an IF input range of 40 dB while demodulating a QPSK-modulated signal at 380 MHz. The AD8362 is insensitive to crest factor variations and therefore provides similar performance regardless of the modulation of the incoming signal.

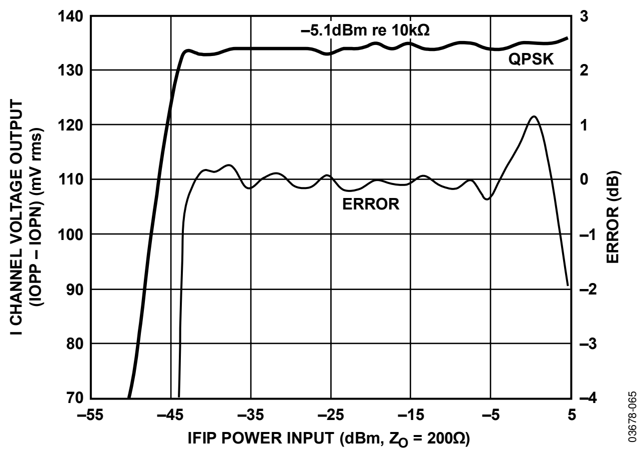

Figure 56. AD8348 Baseband Amplifier Output vs. IF Input Power with AD8362 AGC Loop

BASEBAND FILTERS

Baseband low-pass or band-pass filtering can be conveniently performed between the mixer outputs (IMXO and QMXO) and the input to the baseband amplifiers. Consideration should be given to the output impedance of the mixers (40 Ω).

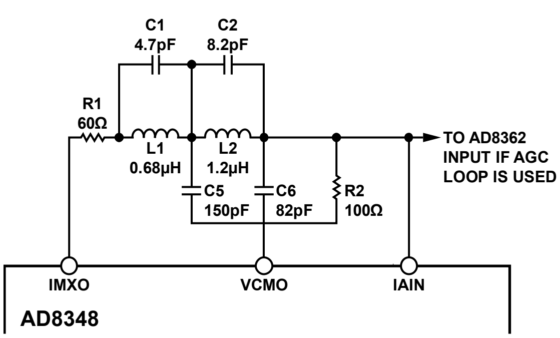

Figure 57. Baseband Filter Schematic

Figure 57 shows the schematic for a 100 Ω, fourth-order elliptic low-pass filter with a 3 dB cutoff frequency of 20 MHz. Source and load impedances of approximately 100 Ω ensure that the filter sees a matched source and load. This also ensures that the mixer output is driving an overall load of 200 Ω. Note that the shunt termination resistor is tied to the source driving VCMO and not to ground. This ensures that the input to the baseband amplifier is biased to the proper reference level. VCMO is not an output pin and must be biased by a low impedance source.

The frequency response and group delay of this filter are shown in Figure 58 and Figure 59.

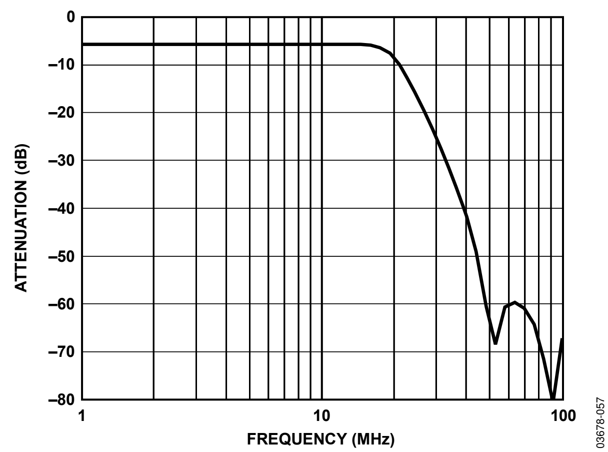

Figure 58. Baseband Filter Response

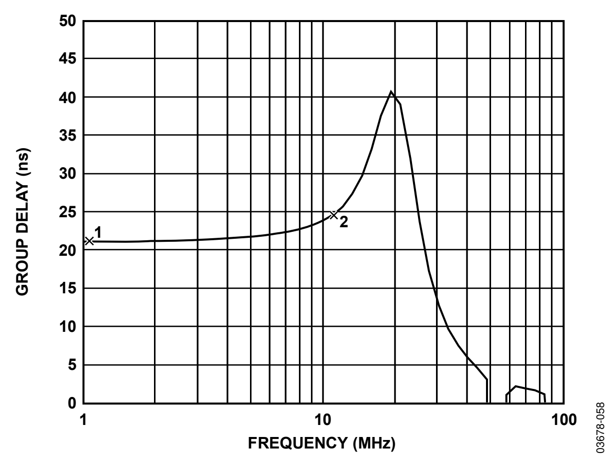

Figure 59. Baseband Filter Group Delay

LO GENERATION

Analog Devices has a line of PLLs that can be used for generating the LO signal. Table 4 lists the PLLs and their maximum frequency and phase noise performance.

Table 4. ADI PLL Selection Table

ADI Model	Frequency F_{IN} (MHz)	@ 1 kHz ΦN dBc/Hz, 200 kHz PFD
ADF4001BRU	165	−99
ADF4001BCP	165	−99
ADF4110BRU	550	−91
ADF4110BCP	550	−91
ADF4111BRU	1200	−78
ADF4111BCP	1200	−78
ADF4112BRU	3000	−86
ADF4112BCP	3000	−86
ADF4116BRU	550	−89
ADF4117BRU	1200	−87
ADF4118BRU	3000	−90

ADI also offers the ADF4360 fully integrated synthesizer and VCO on a single chip that offers differential outputs for driving the local oscillator input of the AD8348. This means that the user can eliminate the use of a balun for single-ended-to-differential conversions. The ADF4360 comes as a family of chips with six operating frequency ranges. One can be chosen depending on the local oscillator frequency required. Table 5 shows the options available.

Table 5. ADF4360 Family Operating Frequencies

ADI Model	Output Frequency Range (MHz)
ADF4360-1	2150 to 2450
ADF4360-2	1800 to 2150
ADF4360-3	1550 to 1950
ADF4360-4	1400 to 1800
ADF4360-5	1150 to 1400
ADF4360-6	1000 to 1250
ADF4360-7	Lower frequencies set by external L

EVALUATION BOARD

Figure 60 shows the schematic for the AD8348 evaluation board. Note that uninstalled components are indicated with the OPEN designation. The board is powered by a single supply in the range of 2.7 V to 5.5 V. Table 6 details the various configuration options of the evaluation board. Table 7 shows the various jumper configurations for operating the evaluation board with different signal paths.

Power to operate the board can be fed to a single V_S test point located near the LO input port at the top of the evaluation board. A GND test point is conveniently provided next to the V_S test point for the return path.

The device is enabled by moving Switch SW11 (at the bottom left of the evaluation board) to the ENBL position. The device is disabled by moving SW11 to the DENBL position. If desired, the device can be enabled and disabled from an external source that can be fed into the ENBL SMA connector or the VENB test point, in which case SW11 should be placed in the DENBL position.

The IF and MX inputs are selected via SW12. The switch should be moved in the direction of the desired input.

Gain Control

For convenience, a potentiometer, R15, is provided to allow for changes in gain without the need for an additional dc voltage source. To use the potentiometer, the SW13 switch must be set to the POT position. Alternatively, an external voltage applied to either the test point or SMA connector labeled VGIN can set the gain. SW13 must be set to the EXT position when an external gain control voltage is used.

LO Input

The local oscillator signal should be fed to the SMA Connector J21. This port is terminated in 50 Ω. The acceptable LO power input range is from −12 dBm to 0 dBm and must be at a frequency double that of the IF/MX frequency. Remember that the AD8348 uses a 2:1 frequency divider in the LO path to generate the internally required quadrature-phase-related LO signals.

IF Input

The IF input should be fed into the SMA connector IFIP. The VGA must be enabled when this port is used (SW12 in the IF position). When this IF input is chosen, the signal path includes a minimum-loss attenuator to transform a 50 Ω input source to the 200 Ω source impedance level for which the VGA was designed. This pad provides a very broadband input match at the expense of an 11.46 dB power attenuation in the input path. It is very important to take this into account when measuring the noise and distortion performance of the unmodified board using the IFIP input; the apparent noise figure will be degraded by 11.46 dB, and the apparent IIP3 will be 11.46 dB higher than actual. If full weak-signal performance is desired from the evaluation board, the attenuator (comprising R31 and R32) should be removed and replaced with a low-loss RF transformer providing the desired 4:1 impedance ratio. When a transformer is used, IFIN should be ac-coupled to ground and not driven differentially with IFIP.

MX Input

The evaluation board is by default set for a differential MX drive through a balun (T41) from a single-ended source fed into the MXIP SMA connector. When the MX inputs are used, the internal VGA is bypassed. To change to a differential driving source, T41 should be removed along with Resistor R42. The 0 Ω R43 and R44 resistors should be installed in place of T41 to bridge the gap between the input traces. This presents a nominal differential impedance of 200 Ω (100 Ω per side). The differential inputs should then be fed into SMA connectors MXIP and MXIN.

Mixer Outputs

The I and Q mixer outputs are available through the IMXO and QMXO SMA connectors. These outputs are biased to VCMO and are not designed to drive loads smaller than 200 Ω. To prevent damage to test equipment that cannot tolerate dc biases, pads for series dc-blocking capacitors are provided. These pads are populated with 0 Ω by default.

Baseband Outputs

The baseband outputs are made available at the IOPP, IOPN, QOPP, and QOPN test points and SMA connectors. These outputs are not designed to be connected directly to 50 Ω loads and should be presented with loads of approximately 2 kΩ or greater.

The dc bias level of the baseband amplifier outputs are by default tied to VREF through LK11. If desired, the dc bias level can be changed by removing LK11 and driving a dc voltage onto the VCMO test point.

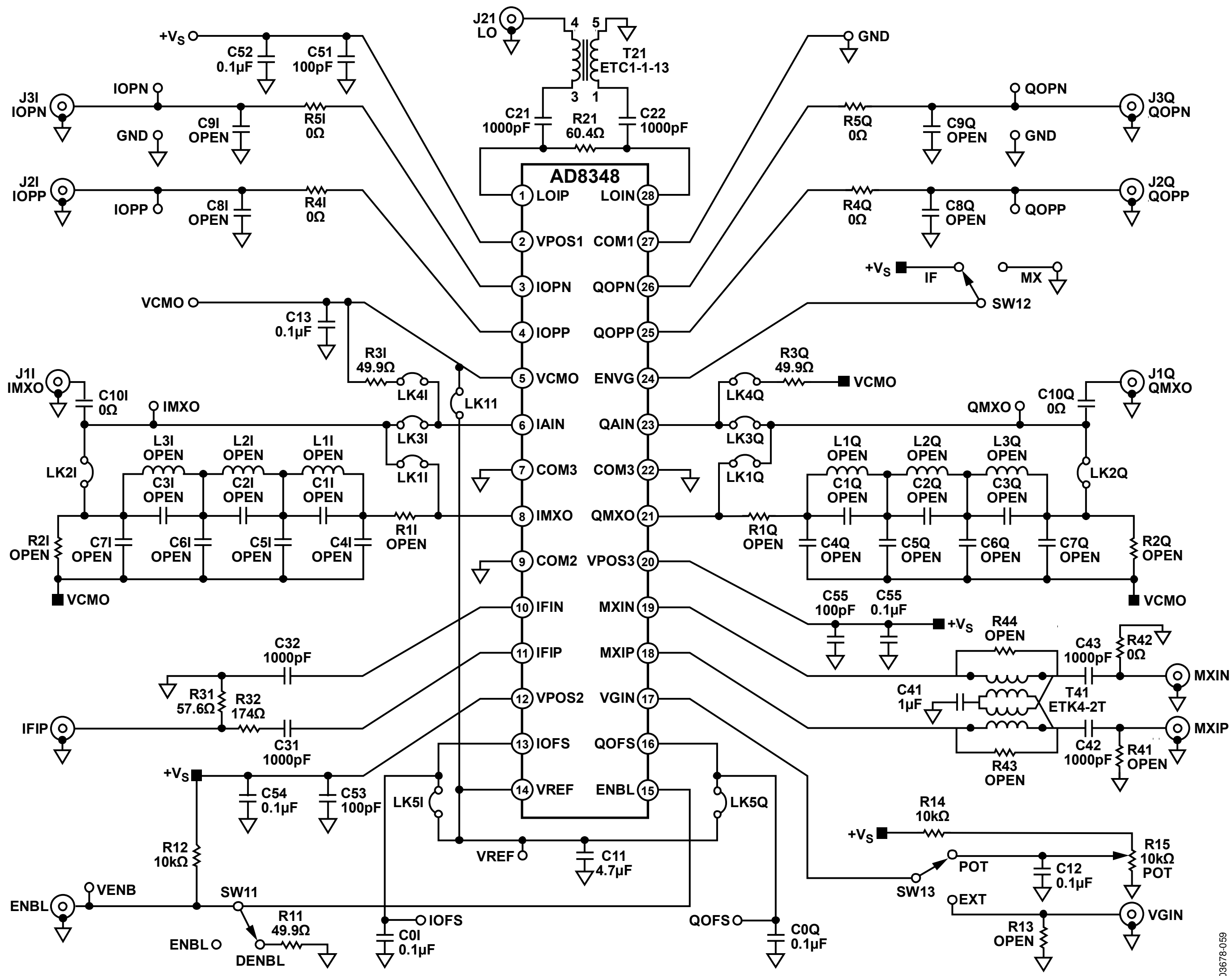

Figure 60. Evaluation Board Schematic