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LF to 2.7 GHz Dual 60 dB TruPwr™ Detector

Data Sheet

AD8364

FEATURES

RMS measurement of high crest-factor signals
Dual-channel and channel difference outputs ports
Integrated accurately scaled temperature sensor
Wide dynamic range ±1 dB over 60 dB
±0.5 dB temperature-stable linear-in-dB response
Low log conformance ripple
+5 V operation at 70 mA, –40°C to +85°C
Small footprint, 5 mm × 5 mm, LFCSP

APPLICATIONS

Wireless infrastructure power amplifier linearization/control
Antenna VSWR monitor
Gain and power control and measurement
Transmitter signal strength indication (TSSI)
Dual-channel wireless infrastructure radios

FUNCTIONAL BLOCK DIAGRAM

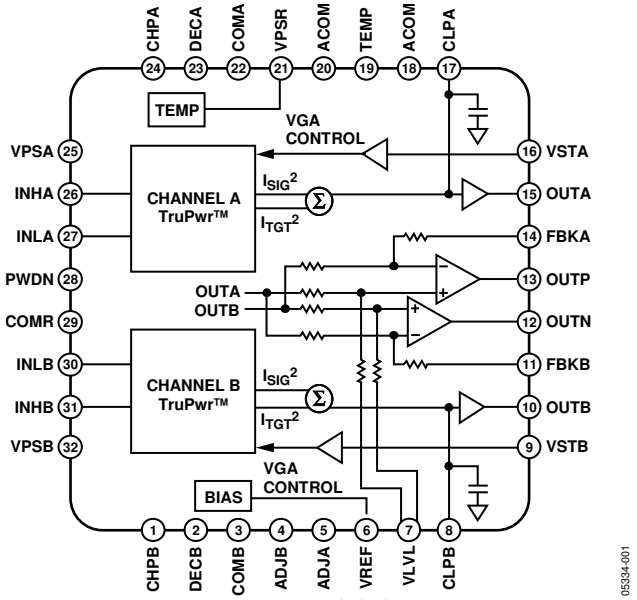

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD8364 is a true rms, responding, dual-channel RF power measurement subsystem for the precise measurement and control of signal power. The flexibility of the AD8364 allows communications systems, such as RF power amplifiers and radio transceiver AGC circuits, to be monitored and controlled with ease. Operating on a single 5 V supply, each channel is fully specified for operation up to 2.7 GHz over a dynamic range of 60 dB. The AD8364 provides accurately scaled, independent, rms outputs of both RF measurement channels. Difference output ports, which measure the difference between the two channels, are also available. The on-chip channel matching makes the rms channel difference outputs extremely stable with temperature and process variations. The device also includes a useful temperature sensor with an accurately scaled voltage proportional to temperature, specified over the device operating temperature range. The AD8364 can be used with input signals having rms values from −55 dBm to +5 dBm referred to 50 Ω and large crest factors with no accuracy degradation.

Integrated in the AD8364 are two matched AD8362 channels (see the AD8362 data sheet for more information) with improved temperature performance and reduced log conformance ripple. Enhancements include improved temperature performance and reduced log-conformance ripple compared to the AD8362. On-chip wide bandwidth output op amps are connected to accommodate flexible configurations that support many system solutions.

The device can easily be configured to provide four rms measurements simultaneously. Linear-in-dB rms measurements are supplied at OUTA and OUTB, with conveniently scaled slopes of 50 mV/dB. The rms difference between OUTA and OUTB is available as differential or single-ended signals at OUTP and OUTN. An optional voltage applied to VLVL provides a common mode reference level to offset OUTP and OUTN above ground.

The AD8364 is supplied in a 32-lead, 5 mm × 5 mm LFCSP, for the operating temperature of –40°C to +85°C.

Rev. B

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TABLE OF CONTENTS

REVISION HISTORY

1/12—Rev. A to Rev. B

Change to Figure 84 ... 40

11/11—Rev. 0 to Rev. A

Changes to Figure 2 ... 8
Changes to Automatic Power Control Section ... 24
Replaced Evaluation and Characterization Circuit Board Layouts Section with Evaluation Board Section ... 40
Changes to Figure 84 ... 40
Deleted Figure 85 and Figure 86; Renumbered Sequentially ... 41
Updated Outline Dimensions ... 41
Changes to Ordering Guide ... 41
Deleted Table 7, AD8364-EVAL-500 Evaluation Board Configuration Options and AD8364-EVAL-2140 Evaluation Board Configuration Options; Renumbered Sequentially ... 42
Deleted Evaluation Boards Section and Figure 87 ... 44
Deleted Figure 88 ... 45
Deleted Assembly Drawings Section, Figure 89, and Figure 90 ... 46

4/05—Revision 0: Initial Version

SPECIFICATIONS

V_S = VPSA = VPSB = VPSR = 5 V, T_A = 25°C, Channel A frequency = Channel B frequency, VLVL = VREF, VST[A, B] = OUT[A, B], OUT[P, N] = FBK[A, B], differential input via Balun, CW input $f \leq 2.7$ GHz, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION	Channel A and Channel B, CW sine wave input				
Signal Input Interface	INH[A, B] (Pins 26, 31) INL[A, B] (Pins 27, 30)				
Specified Frequency Range		LF		2.7	GHz
DC Common-Mode Voltage			2.5		V
Signal Output Interface	OUT[A, B] (Pins 15, 10)				
Wideband Noise	CLP[A, B] = 0.1µF, f_{SPOT} = 100 kHz, RF input = 2140 MHz, ≥−40 dBm		40		nV/√Hz
MEASUREMENT MODE, 450 MHz OPERATION	ADJA = ADJB = 0 V, error referred to best fit line using linear regression @ $P_{INH[A, B]}$ = −40 dBm and −20 dBm, T_A = 25°C, balun = M/A-Com ETK4-2T				
±1 dB Dynamic Range[1]	Pins OUT[A, B]		69		dB
	−40°C < T_A < +85°C		65		dB
±0.5 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		62/59		dB
	−40°C < T_A < +85°C, (Channel A/Channel B)		50/52		dB
Maximum Input Level	±1 dB error		12		dBm
Minimum Input Level	±1 dB error		−58		dBm
Slope			51.6		mV/dB
Intercept			−59		dBm
Output Voltage—High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		2.53		V
Output Voltage—Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		0.99		V
Temperature Sensitivity	Deviation from OUT[A, B] @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm		−0.1, +0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm		−0.2, +0.3		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm		−0.3, +0.4		dB
	Deviation from OUTP to OUTN @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm, −25 dBm		±0.25		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm, −25 dBm		±0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm, −25 dBm		±0.2		dB
Input A to Input B Isolation	Baluns = Macom ETC1.6-4-2-3 (both channels)		71		dB
Input A to OUTB Isolation	Freq separation = 1 kHz				
Input B to OUTA Isolation[2]	P_{INHB} = −50 dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		54		dB
	P_{INHA} = −50 dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB		54		dB
Input Impedance	INHA/INLA, INHB/INLB differential drive		210||0.1		Ω||pF
Input Return Loss	With recommended balun		−12		dB
MEASUREMENT MODE, 880 MHz OPERATION	ADJA = ADJB = 0 V, error referred to best fit line using linear regression @ $P_{INH[A, B]}$ = −40 dBm and −20 dBm, T_A = 25°C, balun = Mini-Circuits® JTX-4-10T				
±1 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		66/57		dB
	−40°C < T_A < +85°C		58/40		dB
±0.5 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		62/54		dB
	−40°C < T_A < +85°C		20/20		dB
Maximum Input Level	±1 dB error, (Channel A/Channel B)		8/0		dBm
Minimum Input Level	±1 dB error, (Channel A/Channel B)		−58/−57		dBm
Slope			51.6		mV/dB
Intercept			−59.2		dBm
Output Voltage—High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		2.54		V
Output Voltage—Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		0.99		V

Parameter	Conditions	Min	Typ	Max	Unit
Temperature Sensitivity	Deviation from OUT[A, B] @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm		+0.5		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm		+0.5		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm		+0.5		dB
	Deviation from OUTP to OUTN @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm, −25 dBm		+0.1, −0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm, −25 dBm		+0.1, −0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm, −25 dBm		+0.1, −0.2		dB
Input A to Input B Isolation	Baluns = Macom ETC1.6-4-2-3 (both channels)		64		dB
Input A to OUTB Isolation	P_{INHB} = −50 dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		35		dB
Input B to OUTA Isolation[2]	P_{INHA} = −50 dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB		35		dB
Input Impedance	INHA/INLA, INHB/INLB differential drive		200||0.3		Ω||pF
Input Return Loss	With recommended balun		−9		dB
MEASUREMENT MODE, 1880 MHz OPERATION	ADJA = ADJB = 0.75 V, error referred to best fit line using linear regression @ $P_{INH[A, B]}$ = −40 dBm and −20 dBm, T_A = 25°C, balun = Murata LDB181G8820C-110				
±1 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		69/61		dB
	−40°C < T_A < +85°C		60/50		dB
±0.5 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		62/51		dB
	−40°C < T_A < +85°C		58/51		dB
Maximum Input Level	±1 dB error, (Channel A/Channel B)		11/3		dBm
Minimum Input Level	±1 dB error		−58		dBm
Slope			50		mV/dB
Intercept			−62		dBm
Output Voltage—High Power In	Pins OUT[A, B] @ $P_{INH[A,B]}$ = −10 dBm		2.49		V
Output Voltage—Low Power In	Pins OUT[A, B] @ $P_{INH[A,B]}$ = −40 dBm		0.98		V
Temperature Sensitivity	Deviation from OUT[A, B] @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm		+0.5, −0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm		+0.5, −0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm		+0.5, −0.2		dB
	Deviation from OUTP to OUTN @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm, −25 dBm		±0.3		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm, −25 dBm		±0.3		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm, −25 dBm		±0.3		dB
Input A to Input B Isolation	Baluns = Macom ETC1.6-4-2-3 (both channels)		61		dB
Input A to OUTB Isolation	P_{INHB} = −50 dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		33		dB
Input B to OUTA Isolation[2]	P_{INHA} = −50 dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB		33		dB
Input Impedance	INHA/INLA, INHB/INLB differential drive		167||0.14		Ω||pF
Input Return Loss	With recommended balun		−8		dB
MEASUREMENT MODE, 2.14 GHz OPERATION	ADJA = ADJB = 1.02 V, error referred to best fit line using linear regression @ $P_{INH[A, B]}$ = −40 dBm and −20 dBm, T_A = 25°C, balun = Murata LDB212G1020C-001				
±1 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		66/57		dB
	−40°C < T_A < +85°C		58/40		dB
±0.5 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		62/54		dB
	−40°C < T_A < +85°C		30/30		dB
Maximum Input Level	±1 dB Error, (Channel A/Channel B)		−2/−4		dBm
Minimum Input Level	±1 dB Error, (Channel A/Channel B)		−57−51		dBm
Slope	Channel A/Channel B		49.5/52.1		mV/dB
Intercept	Channel A/Channel B		−58.3/−57.1		dBm
Output Voltage—High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		2.42		V
Output Voltage—Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		0.90		V

Parameter	Conditions	Min	Typ	Max	Unit
Temperature Sensitivity	Deviation from OUT[A, B] @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm		+0.1, −0.4		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm		+0.1, −0.4		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm		+0.1, −0.4		dB
	Deviation from OUTP to OUTN @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm, −25 dBm		+0.1, −0.4		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm, −25 dBm		+0.2, −0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm, −25 dBm		+0.1, −0.2		dB
Deviation from CW Response	5.5 dB peak-to-rms ratio (WCDMA one channel)		0.2		dB
	12 dB peak-to-rms ratio (WCDMA three channels)		0.3		dB
	18 dB peak-to-rms ratio (WCDMA four channels)		0.3		dB
Input A to Input B Isolation	Baluns = Macom ETC1.6-4-2-3 (both channels)		58		dB
Input A to OUTB Isolation	P_{INHB} = −50 dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		33		dB
Input B to OUTA Isolation[2]	P_{INHA} = −50 dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB		33		dB
Input Impedance	INHA/INLA, INHB/INLB differential drive		150‖1.9		Ω‖pF
Input Return Loss	With recommended balun		−10		dB
MEASUREMENT MODE, 2.5 GHz OPERATION	ADJA = ADJB = 1.14 V, error referred to best fit line using linear regression @ $P_{INH[A, B]}$ = −40 dBm and −20 dBm, T_A = 25°C, balun = Murata LDB182G4520C-110				
± 1 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		69/63		dB
	−40°C < T_A < +85°C		58		dB
±0.5 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		55/50		dB
	−40°C < T_A < +85°C		25		dB
Maximum Input Level	±1 dB error, (Channel A/Channel B)		17/11		dBm
Minimum Input Level	±1 dB error		−52		dBm
Slope			50		mV/dB
Intercept			−52.7		dBm
Output Voltage—High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		2.14		V
Output Voltage—Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		0.65		V
Temperature Sensitivity	Deviation from OUT[A, B] @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm		±0.5		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm		±0.5		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm		±0.5		dB
	Deviation from OUTP to OUTN @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm, −25 dBm		±0.3		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm, −25 dBm		±0.3		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm, −25 dBm		±0.3		dB
Input A to Input B Isolation	Baluns = Macom ETC1.6-4-2-3 (both channels)		54		dB
Input A to OUTB Isolation	P_{INHB} = −50 dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		31		dB
Input B to OUTA Isolation[2]	P_{INHA} = −50 dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB		31		
Input Impedance	INHA/INLA, INHB/INLB differential drive		150‖1.7		Ω‖pF
Input Return Loss	With recommended balun		−11.5		dB
OUTPUT INTERFACE	Pin OUTA and OUTB				
Voltage Range Min	R_L ≥ 200 Ω to ground		0.09		V
Voltage Range Max	R_L ≥ 200 Ω to ground		V_S − 0.15		V
Source/Sink Current	OUTA and OUTB held at V_S/2, to 1% change		70		mA

Parameter	Conditions	Min	Typ	Max	Unit
SETPOINT INPUT	Pin VSTA and VSTB				
Voltage Range	Law conformance error ≤1 dB	0.5		3.75	V
Input Resistance			68		kΩ
Logarithmic Scale Factor	f = 450 MHz, −40°C ≤ T_A ≤ +85°C		50		mV/dB
Logarithmic Intercept	f = 450 MHz, −40°C ≤ T_A ≤ +85°C, referred to 50 Ω		−55		dBm
CHANNEL DIFFERENCE OUTPUT	Pin OUTP and OUTN				
Voltage Range Min	R_L ≥ 200 Ω to ground		0.1		V
Voltage Range Max	R_L ≥ 200 Ω to ground		V_S − 0.15		V
Source/Sink Current	OUTP and OUTN held at V_S/2, to 1% change		70		mA
DIFFERENCE LEVEL ADJUST	Pin VLVL				
Voltage Range[3]	OUT[P, N] = FBK[A, B]	0		5	V
OUT[P,N] Voltage Range	OUT[P, N] = FBK[A, B]	0		V_S − 0.15	V
Input Resistance			1		kΩ
TEMPERATURE COMPENSATION	Pin ADJA and ADJB				
Input Voltage Range		0		2.5	V
Input Resistance			>1		MΩ
VOLTAGE REFERENCE	Pin VREF				
Output Voltage	RF in = −55 dBm		2.5		V
Temperature Sensitivity	−40°C ≤ T_A ≤ +85°C		0.4		mV/°C
Current Limit Source/Sink	1% change		10/3		mA
TEMPERATURE REFERENCE	Pin TEMP				
Output Voltage	T_A = 25°C, R_L ≥ 10 kΩ		0.62		V
Temperature Coefficient	−40°C ≤ T_A ≤ +85°C, R_L ≥ 10 kΩ		2		mV/°C
Current Source/Sink	T_A = 25°C to 1% change		1.6/2		mA
POWER-DOWN INTERFACE	Pin PWDN				
Logic Level to Enable	Logic LO enables			1	V
Logic Level to Disable	Logic HI disables	3			V
Input Current	Logic HI PWDN = 5 V		95		µA
	Logic LO PWDN = 0 V		<100		µA
Enable Time	PWDN LO to OUTA/OUTB at 100% final value, $C_{LPA/B}$ = Open, $C_{HPA/B}$ = 10 nF, RF in = 0 dBm		2		µs
Disable Time	PWDN HI to OUTA/OUTB at 10% final value, $C_{LPA/B}$ = Open, $C_{HPA/B}$ = 10nF, RF in = 0 dBm		1.6		µs
POWER INTERFACE	Pin VPS[A, B], VPSR				
Supply Voltage		4.5		5.5	V
Quiescent Current	RF in = −55 dBm, V_S = 5 V		70		mA
	−40°C ≤ T_A ≤ +85°C			90	mA
Supply Current	PWDN enabled, V_S = 5 V		500		µA
	−40°C ≤ T_A ≤ +85°C			900	µA

[1] Best fit line, linear regression.
[2] See Figure 75 for a plot of isolation vs. frequency for a ±1 dB error.
[3] VLVL + OUTA/2 should not exceed VPSA − 1.31 V. Likewise, VLVL + OUTB/2 should not exceed VPSB − 1.31 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPSA, VPSB, VPSR	5.5 V
PWDN, VSTA, VSTB, ADJA, ADJB, FBKA, FBKB	0 V, 5.5 V
Input Power (Referred to 50 Ω)	23 dBm
Internal Power Dissipation	600 mW
θ_{JA}	39.8°C/W[1, 2]
θ_{JC}	3.9°C/W[2]
θ_{JB}	22.8°C/W[2]
Ψ_{JT}	0.4°C/W[1, 2]
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] Still air.
[2] All values are modeled using a standard 4-layer JEDEC test board with the pad soldered to the board and thermal vias in the board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

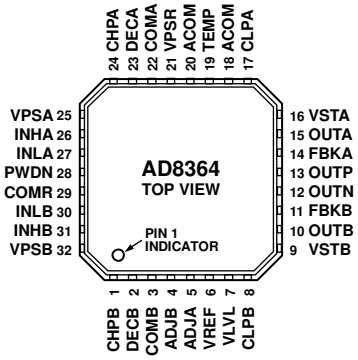

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description	Equiv. Circuit
1	CHPB	Connect to common via a capacitor to determine 3 dB point of Channel B input signal high-pass filter.	
2, 23	DECB, DECA	Decoupling Terminals for INHA/INLA and INHB/INLB. Connect to common via a large capacitance to complete input circuit.	Figure 52
3, 22, 29	COMB, COMA, COMR	Input System Common Connection. Connect via low impedance to system common.	
4, 5	ADJB, ADJA	Temperature Compensation for Channel B and Channel A. An external voltage is connected to these pins to improve temperature drift. This voltage can be derived from VREF, that is, connect a resistor from VREF to ADJ[A, B] and another resistor from ADJ[A, B] to ground. The value of these resistors change as the frequency changes.	Figure 68
6	VREF	General-Purpose Reference Voltage Output of 2.5 V.	Figure 54
7	VLVL	Reference Level Input for OUTP and OUTN. (Usually connected to VREF through a voltage divider or left open).	Figure 58
8, 17	CLPB, CLPA	Channel B and Channel A Connection for Loop Filter Integration (Averaging) Capacitor. Connect a ground-referenced capacitor to this pin. A resistor can be connected in series with this capacitor to improve loop stability and response time.	
9	VSTB	The voltage applied to this pin sets the decibel value of the required RF input voltage to Channel B, which results in zero current flow in the loop integrating capacitor pin, CLPB.	Figure 56
10	OUTB	Channel B Output of Error Amplifier. In measurement mode, normally connected directly to VSTB.	Figure 57
11	FBKB	Feedback Through 1 kΩ to the Negative Terminal of the Integrated Op Amp Driving OUTN.	
12	OUTN	Channel Differencing Op Amp Output. In measurement mode, normally connected directly to FBKB and follows the equation OUTN = OUTA − OUTB + VLVL.	Figure 58
13	OUTP	Channel Differencing Op Amp Output. In measurement mode, normally connected directly to FBKA and follows the equation OUTP = OUTA − OUTB + VLVL.	Figure 58
14	FBKA	Feedback Through 1kΩ to the Negative Terminal of the Integrated Op Amp Driving OUTP.	
15	OUTA	Channel A Output of Error Amplifier. In measurement mode, normally connected directly to VSTA.	Figure 57
16	VSTA	The voltage applied to this pin sets the decibel value of the required RF input voltage to Channel A that results in zero current flow in the loop integrating capacitor pin, CLPA.	Figure 56
18, 20	ACOM	Analog Common for Channels A and B. Connect via low impedance to common.	
21, 25, 32	VPSR, VPSA, VPSB	Supply for the Input System of Channels A and B. Supply for the internal references. Connect to +5 V power supply.	
19	TEMP	Temperature Sensor Output.	Figure 53
24	CHPA	Connect to common via a capacitor to determine 3 dB point of Channel A input signal high-pass filter.	
26, 27	INHA, INLA	Channel A High and Low RF Signal Input Terminal.	Figure 52
28	PWDN	Disable/Enable Control Input. Apply logic high voltage to shut down the AD8364.	Figure 55
30, 31	INLB, INHB	Channel B Low and High RF Signal Input Terminal.	Figure 52
Under Package	Exposed Paddle	The exposed paddle on the underside of the package should be soldered to a ground plane with low thermal and electrical characteristics.	

TYPICAL PERFORMANCE CHARACTERISTICS

V_P = 5 V; T_A = +25°C, −40°C, +85°C; CLPA/B = OPEN. Colors: +25°C black, −40°C blue, +85°C red.

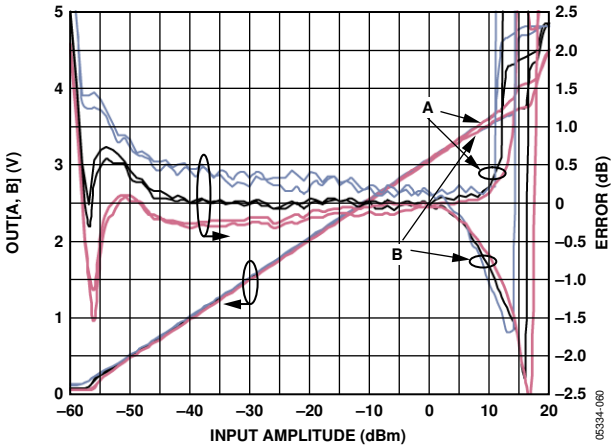

Figure 3. OUT[A, B] Voltage and Log Conformance vs. Input Amplitude at 450 MHz, Typical Device, ADJ[A, B] = 0 V, Sine Wave, Differential Drive, Balun = Macom ETK4-2T

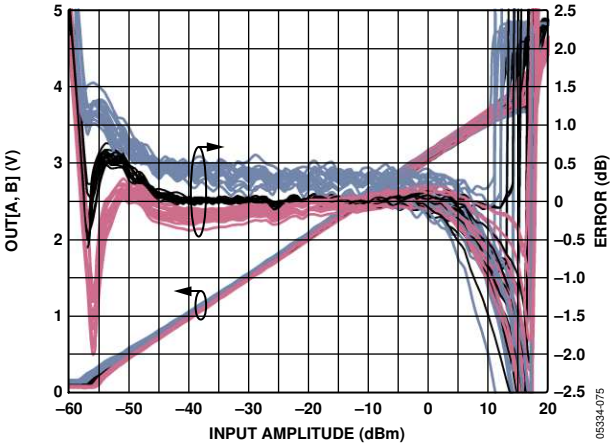

Figure 4. Distribution of OUT[A, B] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 30 Devices from Multiple Lots, Frequency = 450 MHz, ADJ[A, B] = 0 V, Sine Wave, Differential Drive, Balun = Macom ETK4-2T

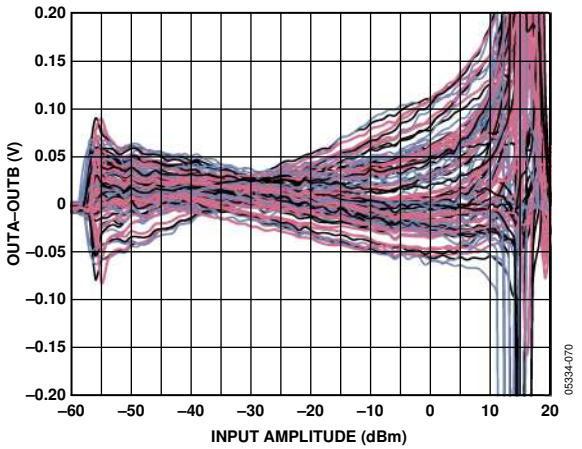

Figure 5. Distribution of [OUTA – OUTB] Voltage vs. Input Amplitude over Temperature for at Least 30 Devices from Multiple Lots, Frequency = 450 MHz, ADJ[A, B] = 0 V, Sine Wave, Differential Drive, Balun = Macom ETK4-2T

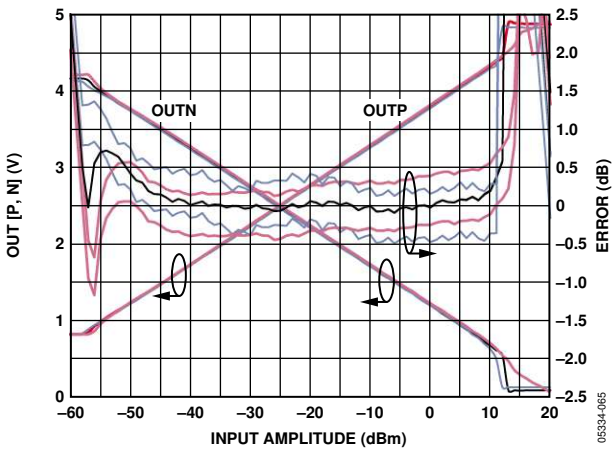

Figure 6. OUT[P, N] Voltage and Log Conformance vs. Input Amplitude at 450 MHz, with B Input Held at −25 dBm and A Input Swept, Typical Device, ADJ[A, B] = 0 V, Sine Wave, Differential Drive, Balun = Macom ETK4-2T (Note that the OUTP and OUTN Error Curves Overlap)

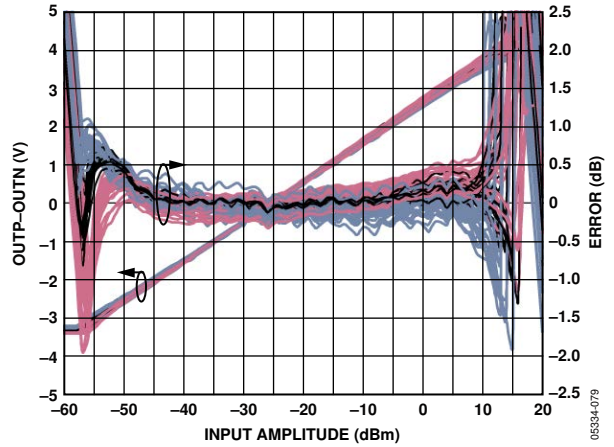

Figure 7. Distribution of [OUTP – OUTN] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 30 Devices from Multiple Lots, Frequency = 450 MHz, ADJ[A, B] = 0 V, Sine Wave, Differential Drive, P_{IN} Ch. B = −25 dBm, Channel A Swept

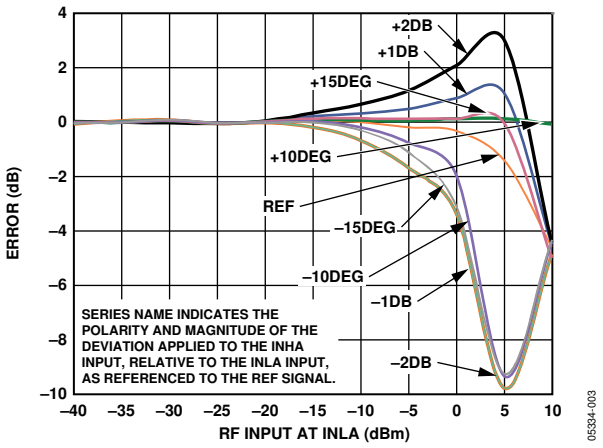

Figure 8. Log Conformance vs. Input Amplitude at various Amplitude and Phase Balance points, 450 MHz, Typical Device, ADJ[A, B] = 0 V, Sine Wave, Differential Drive

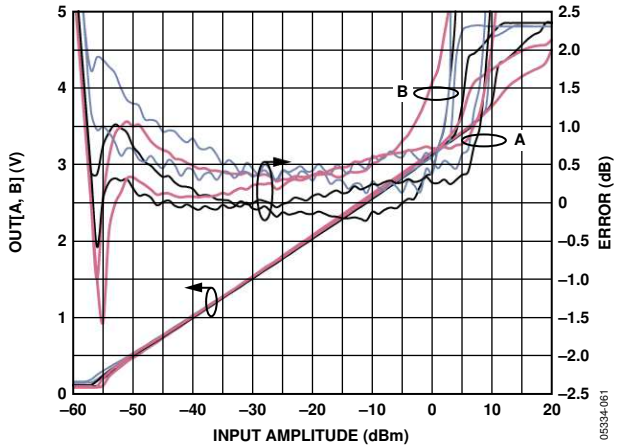

Figure 9. OUT[A, B] Voltage and Log Conformance vs. Input Amplitude at 880 MHz, Typical Device, ADJ[A, B] = 0.5 V, Sine Wave, Differential Drive, Balun = Mini-Circuits JTX-4-10T

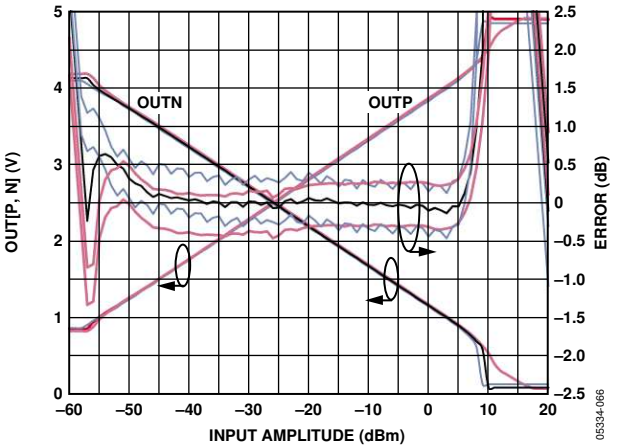

Figure 12. OUT[P, N] Voltage and Log Conformance vs. Input Amplitude at 880 MHz, with B Input Held at −25 dBm and A Input Swept, Typical Device, ADJ[A, B] = 0.5 V, Sine Wave, Differential Drive, Balun = JTX-4-10T (Note that the OUTP and OUTN Error Curves Overlap)

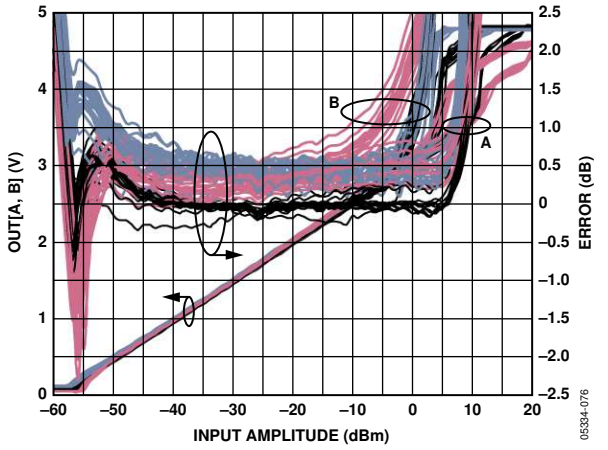

Figure 10. Distribution of OUT[A, B] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 15 Devices from Multiple Lots, Frequency = 880 MHz, ADJ[A, B] = 0.5 V, Sine Wave, Differential Drive, Balun =JTX-4-10T

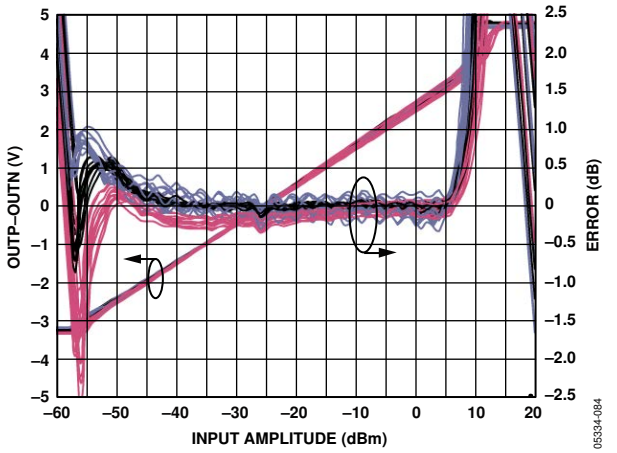

Figure 13. Distribution of [OUTP – OUTN] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 15 Devices from Multiple Lots, Frequency = 880 MHz, ADJ[A, B] =0.5 V, Sine Wave, Differential Drive, P_{IN} Ch. B = −25 dBm, Channel A Swept

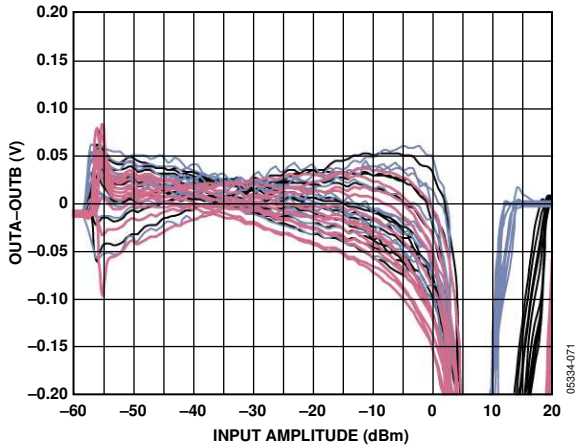

Figure 11. Distribution of [OUTA – OUTB] Voltage vs. Input Amplitude over Temperature for at Least 15 Devices from Multiple Lots, Frequency = 880 MHz, ADJ[A, B] = 0.5 V, Sine Wave, Differential Drive, Balun =JTX-4-10T

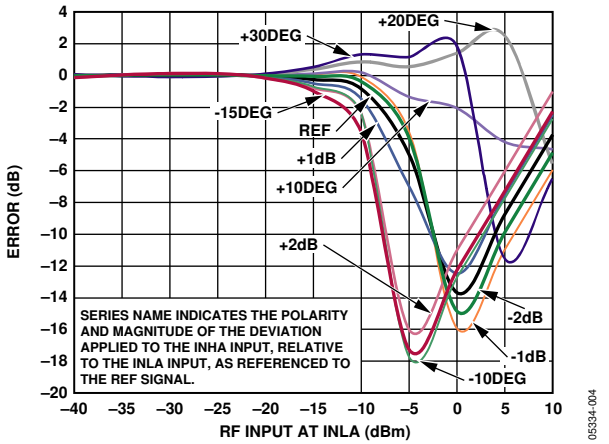

Figure 14. Log Conformance vs. Input Amplitude at Various Amplitude and Phase Balance points, 880 MHz, Typical Device, ADJ[A, B] = 0.5 V, Sine Wave, Differential Drive

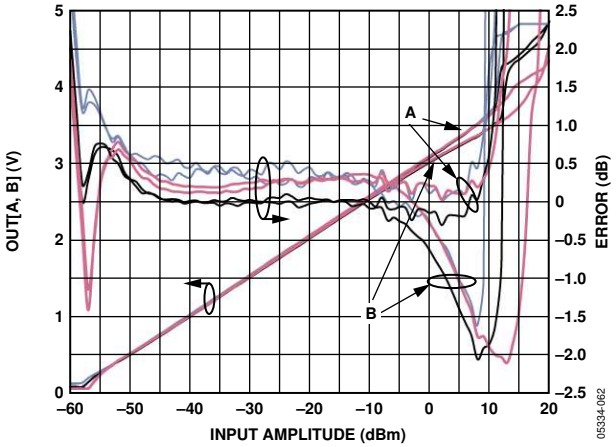

Figure 15. OUT[A, B] Voltage and Log Conformance vs. Input Amplitude at 1.88 GHz, Typical Device, TADJ[A, B]= 0.65 V, Sine Wave, Differential Drive, Balun = Murata LDB181G8820C-110

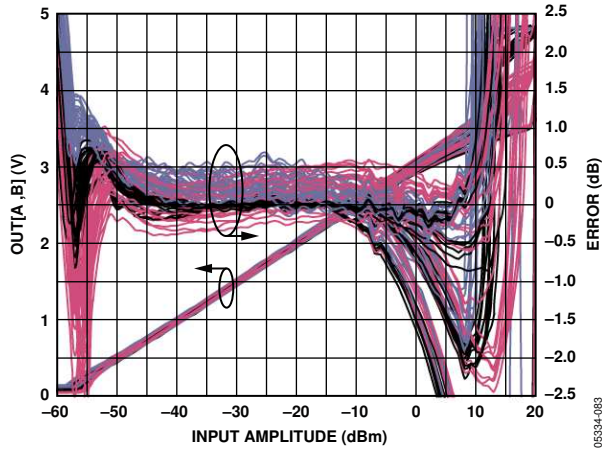

Figure 16. Distribution of OUT[A, B] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 20 Devices from Multiple Lots, Frequency = 1.88 GHz, ADJ[A, B] = 0.65 V, Sine Wave, Differential Drive, Balun = Murata LDB181G8820C-110

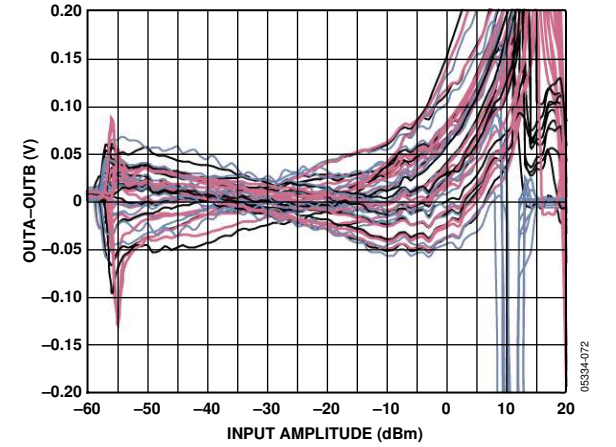

Figure 17. Distribution of [OUTA – OUTB] Voltage vs. Input Amplitude over Temperature for at Least 20 Devices from Multiple Lots, Frequency = 1.88 GHz, ADJ[A, B] = 0.65 V, Sine Wave, Differential Drive, Balun = Murata LDB181G8820C-110

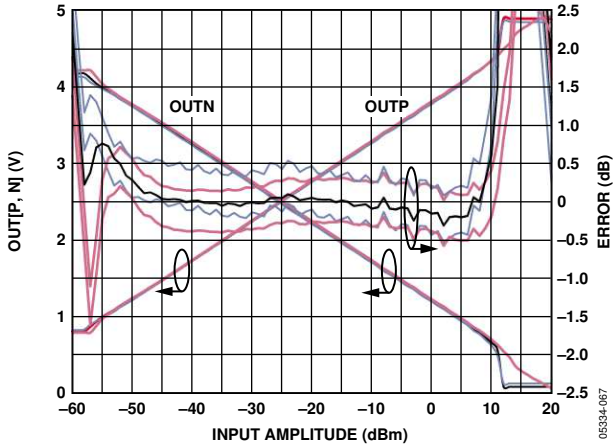

Figure 18. OUT[P, N] Voltage and Log Conformance vs. Input Amplitude at 1.88 GHz, with B Input Held at −25 dBm and A Input Swept, Typical Device, ADJ[A, B] = 0.65 V, Sine Wave, Differential Drive, Balun = Murata LDB181G8820C-110 (Note that the OUTP and OUTN Error Curves Overlap)

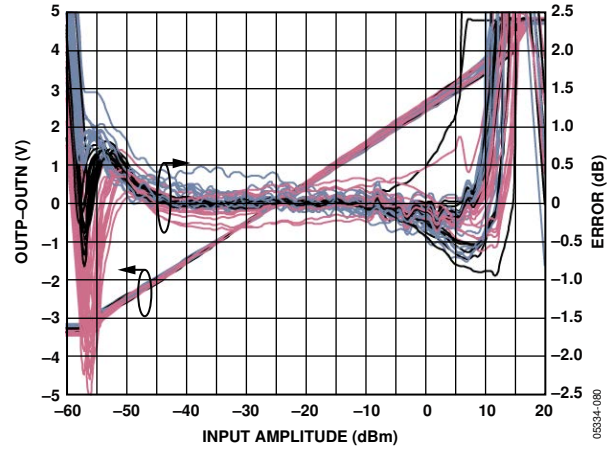

Figure 19. Distribution of [OUTP – OUTN] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 20 Devices from Multiple Lots, Frequency = 1.88 GHz, ADJ[A, B] =0.65 V, Sine Wave, Differential Drive, P_{IN} Ch. B = −25 dBm, Channel A Swept

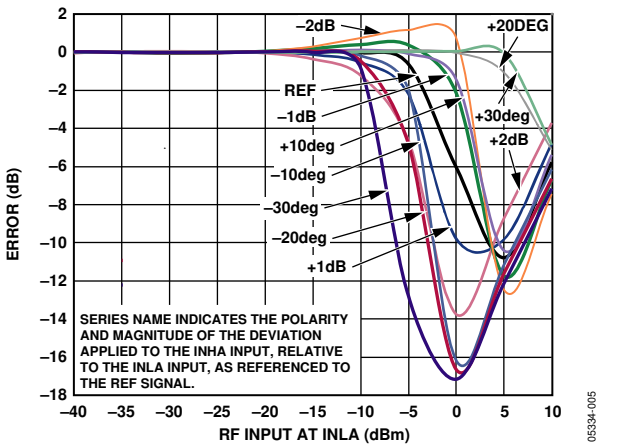

Figure 20. Log Conformance vs. Input Amplitude at Various Amplitude and Phase Balance Points, 1.880 GHz, Typical Device, ADJ[A, B] = 0.65 V, Sine Wave, Differential Drive

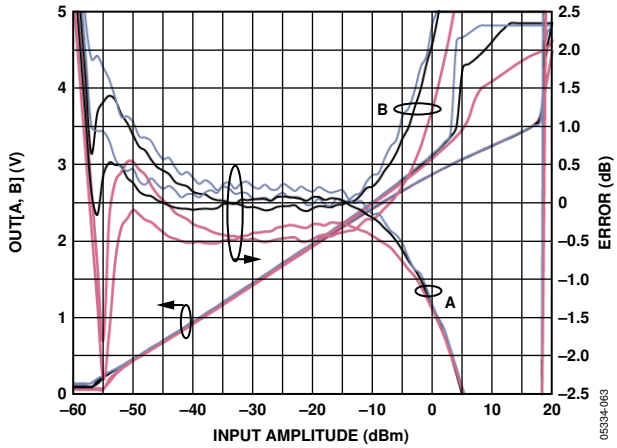

Figure 21. OUT[A, B] Voltage and Log Conformance vs. Input Amplitude at 2.14 GHz, Typical Device, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive, Balun = Murata LDB212G1020C-001

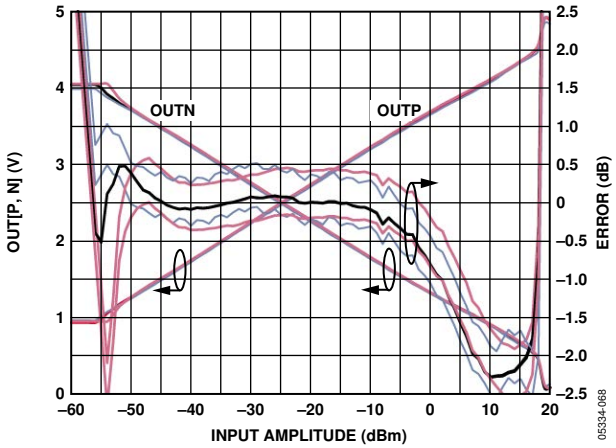

Figure 24. OUT[P, N] Voltage and Log Conformance vs. Input Amplitude at 2.14 GHz, with B Input Held at −25 dBm and A Input Swept, Typical Device, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive, Balun = Murata LDB212G1020C-001 (Note that the OUTP and OUTN Error Curves Overlap)

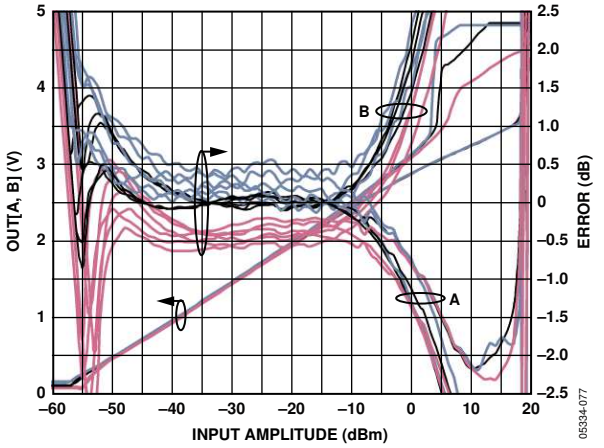

Figure 22. Distribution of OUT[A, B] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 3 Devices from Multiple Lots, Frequency = 2.14 GHz, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive, Balun = Murata LDB212G1020C-001

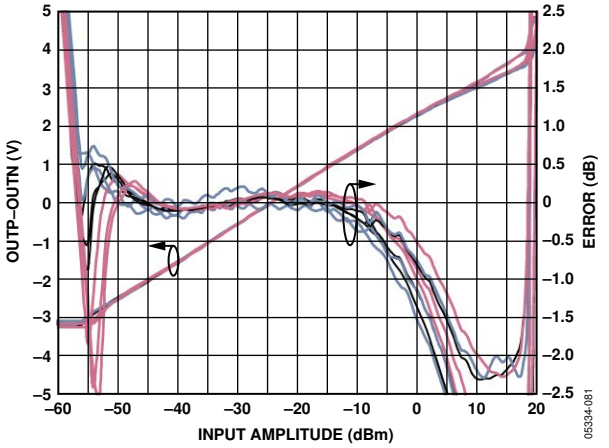

Figure 25. Distribution of [OUTP – OUTN] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 3 Devices from Multiple Lots, Frequency = 2.14 GHz, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive, P_{IN} Ch. B = −25 dBm, Channel A Swept

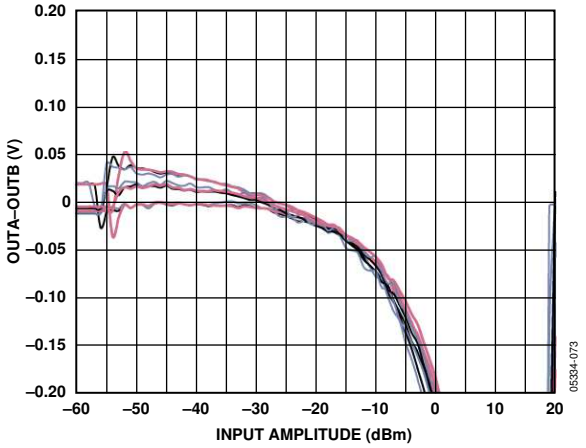

Figure 23. Distribution of [OUTA – OUTB] Voltage vs. Input Amplitude over Temperature for 3 Devices from Multiple Lots, Frequency = 2.14 GHz, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive, Balun = Murata LDB212G1020C-001

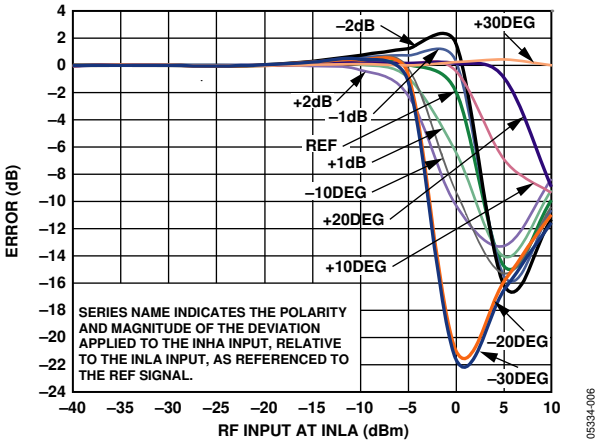

Figure 26. Log Conformance vs. Input Amplitude at Various Amplitude and Phase Balance Points, 2.140 GHz, Typical Device, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive

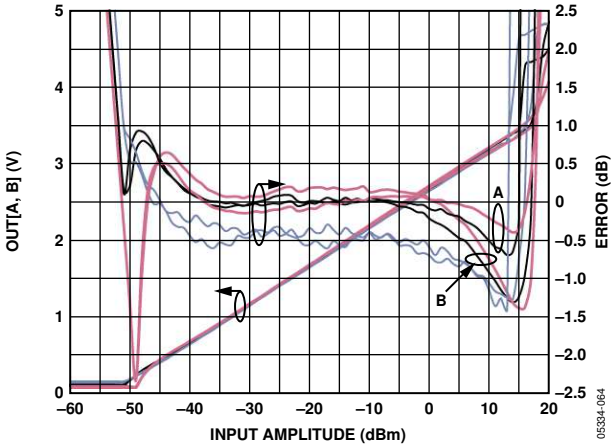

Figure 27. OUT[A, B] Voltage and Log Conformance vs. Input Amplitude at 2.5 GHz, Typical Device, ADJ[A, B] = 1.1 V, Sine Wave, Differential Drive, Balun = Murata LDB182G4520C-110

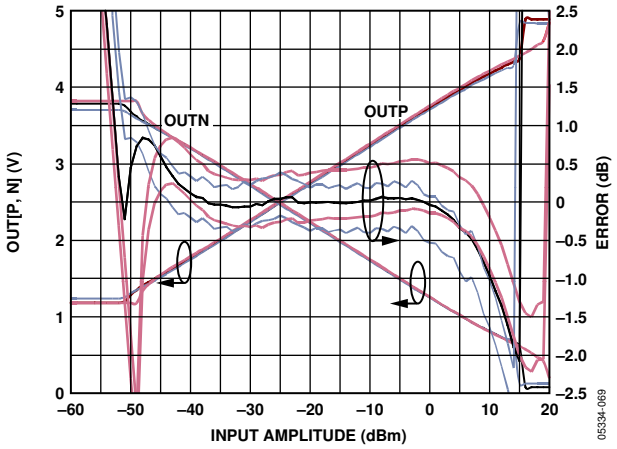

Figure 30. OUT[P, N] Voltage and Log Conformance vs. Input Amplitude at 2.5 GHz, with B Input Held at −25 dBm and A Input Swept, Typical Device, ADJ[A, B] = 1.1 V, Sine Wave, Differential Drive, Balun = Murata LDB182G4520C-110 (Note that the OUTP and OUTN Error Curves Overlap)

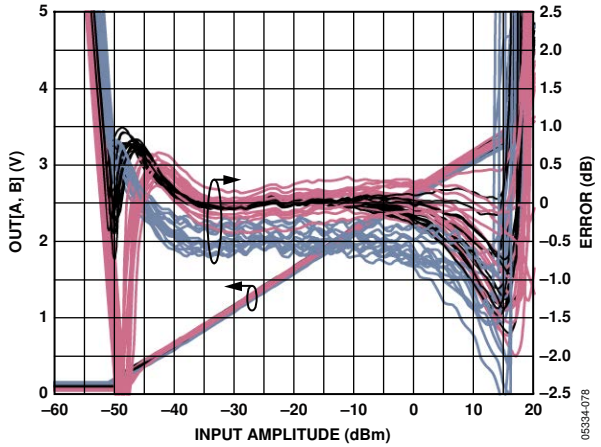

Figure 28. Distribution of OUT[A, B] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 15 Devices from Multiple Lots, Frequency = 2.5 GHz, ADJ[A, B] = 1.1 V, Sine Wave, Differential Drive, Balun = Murata LDB182G4520C-110

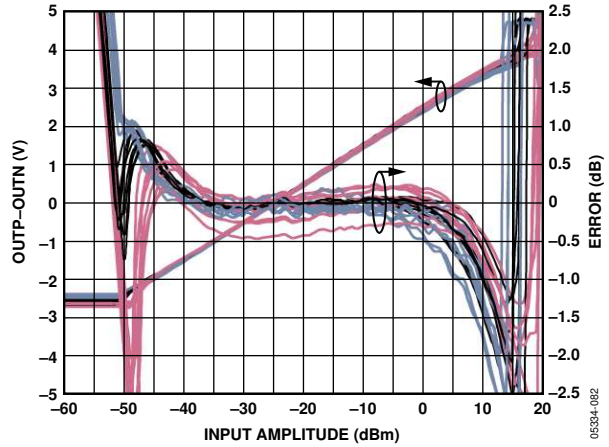

Figure 31. Distribution of [OUTP – OUTN] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 15 Devices from Multiple Lots, Frequency = 2.5 GHz, ADJ[A, B] =1.1 V, Sine Wave, Differential Drive, P_{IN} Ch. B = −25 dBm, Channel A Swept

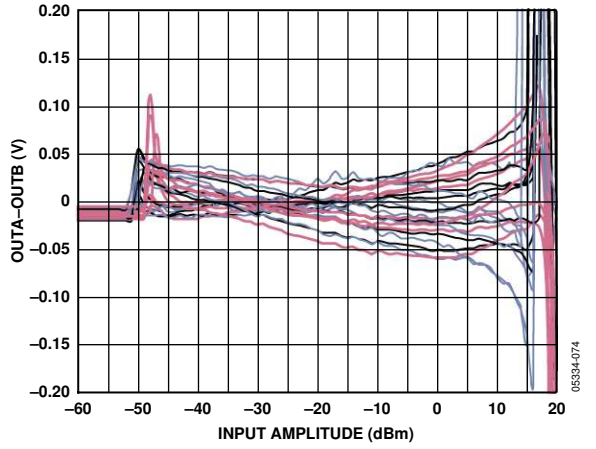

Figure 29. Distribution of [OUTA – OUTB] Voltage vs. Input Amplitude over Temperature for at Least 15 Devices from Multiple Lots, Frequency = 2.5 GHz, ADJ[A, B] = 1.1 V, Sine Wave, Differential Drive, Balun = Murata LDB182G4520C-110

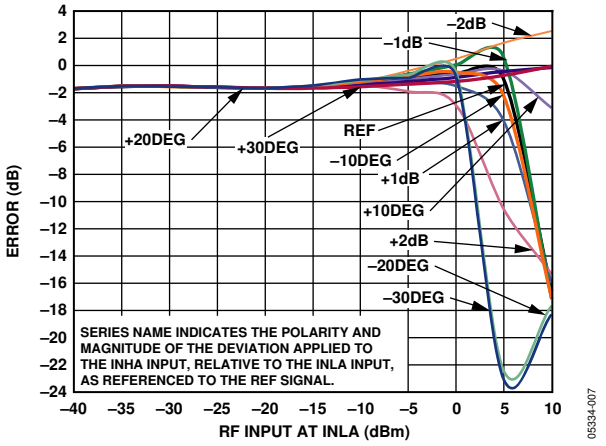

Figure 32. Log Conformance vs. Input Amplitude at Various Amplitude and Phase Balance Points, 2.500 GHz, Typical Device, ADJ[A, B] = 1.1 V, Sine Wave, Differential Drive

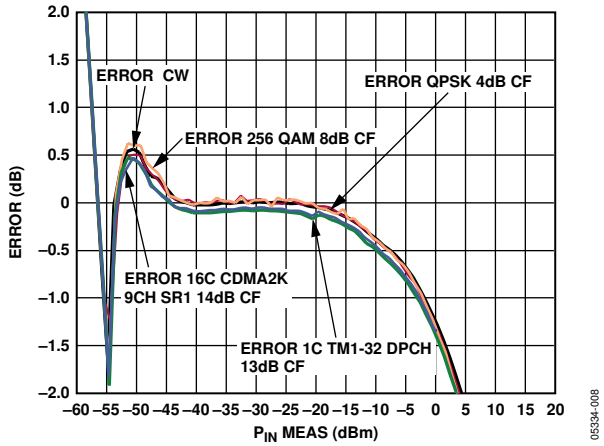

Figure 33. Output Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, CW, QPSK, 256QAM, WCDMA 1-Carrier Test Model 1 with 32 DPCH, CDMA2000, 16-Carrier, 9-Channel SR1 Frequency 2.140 GHz, CLP[A, B] = 1 µF, Balun = Murata LDB212G1020C-001

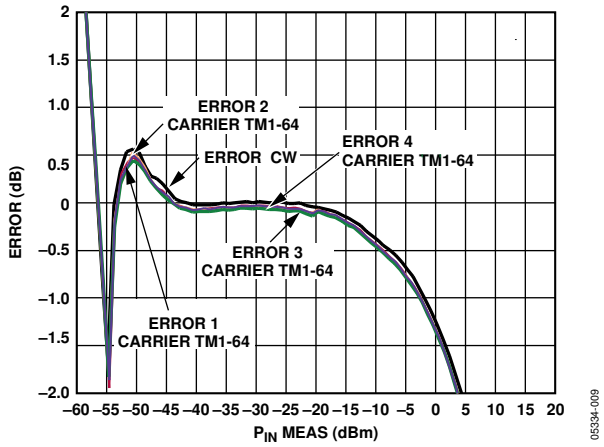

Figure 34. Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, CW, WCDMA1, 2-, 3-, and 4-Carrier, Test Model 1 with 64 DPCH, Frequency 2.14 GHz, Balun = Murata LDB212G1020C-001

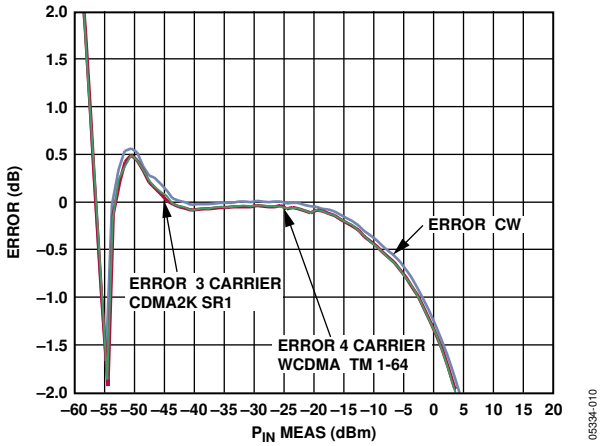

Figure 35. Output Voltage and Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, CW, 3-Carrier CDMA2000 SR1, 4-Carrier WCDMA, Test Model 1 with 64 DPCH, Frequency 2.140 GHz, Balun = Murata LDB212G1020C-001

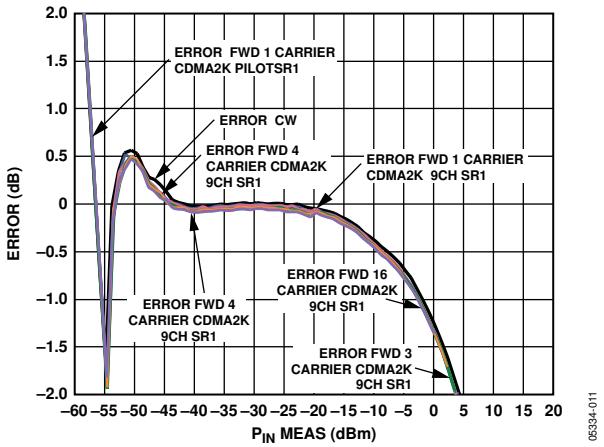

Figure 36. Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, CW, 1-Carrier CDMA2000 Pilot CH SR1, 1-Carrier CDMA2000 9CH SR1, 3-Carrier CDMA2000 9CH SR1, 4-Carrier CDMA2000 9CH SR1 Frequency 16-Carrier CDMA2000 9CH SR1, Frequency 2.140 GHz, Balun = Murata LDB212G1020C-001

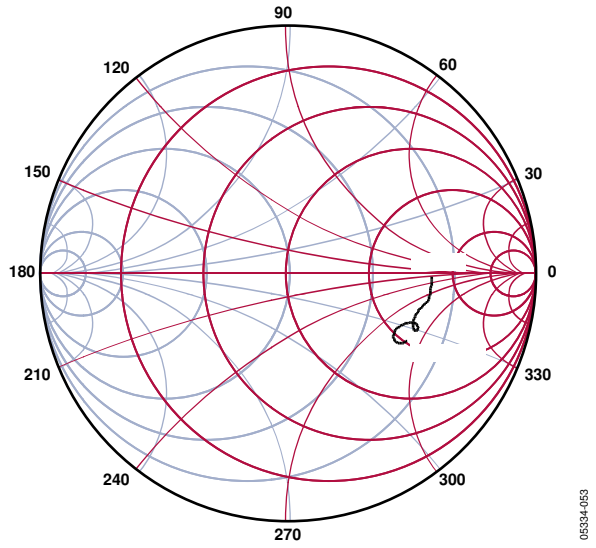

Figure 37. Differential Input Impedance (S11) vs. Frequency; Z_O = 50 Ω

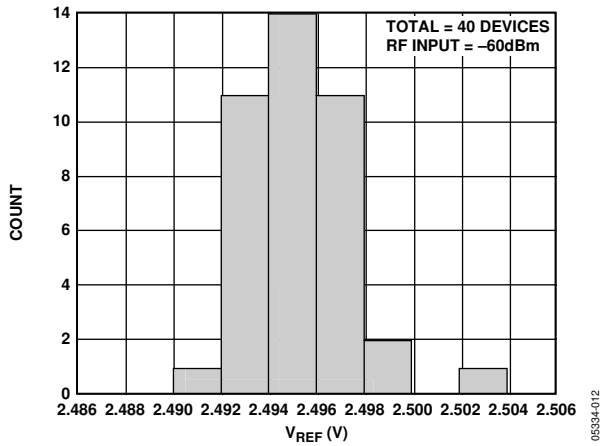

Figure 38. Distribution of VREF for 40 Devices

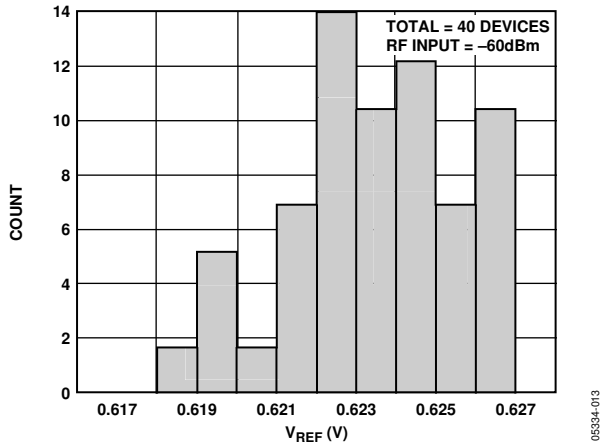

Figure 39. Distribution of TEMP Voltage for 40 Devices

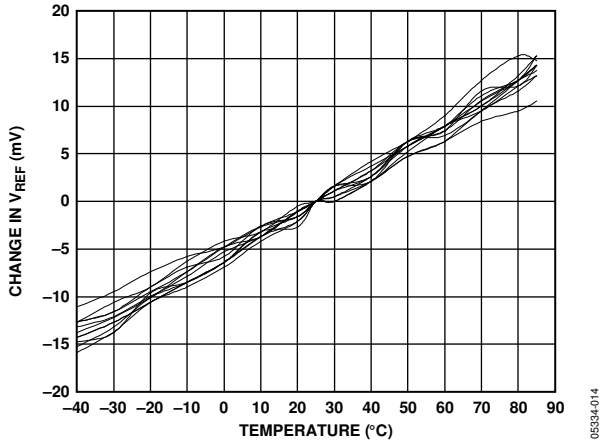

Figure 40. Change in VREF vs. Temperature for 11 Devices

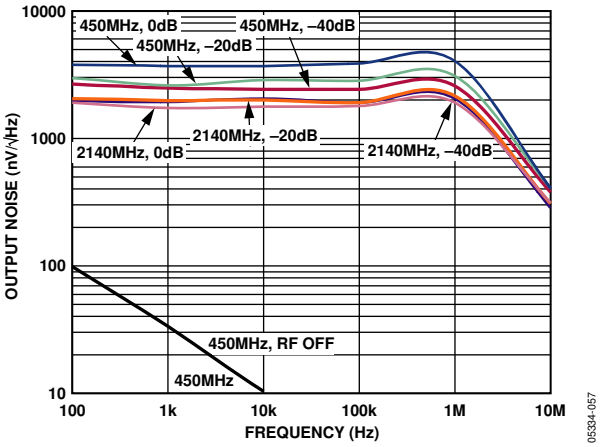

Figure 41. Noise Spectral Density of OUT[A, B]; CLP[A, B] = Open

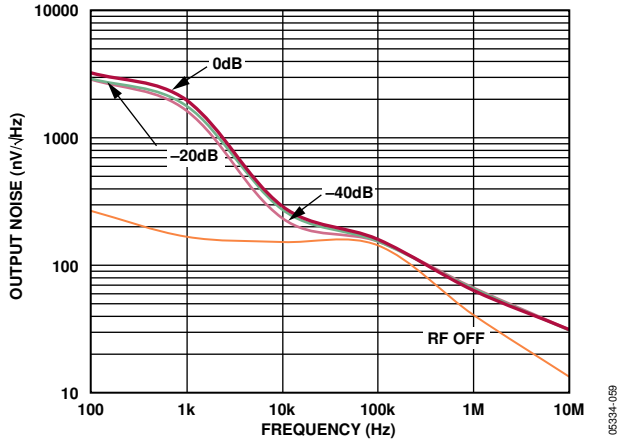

Figure 42. Noise Spectral Density of OUT[P, N]; CLP[A, B] = 0.1 µF, Frequency = 2140 MHz

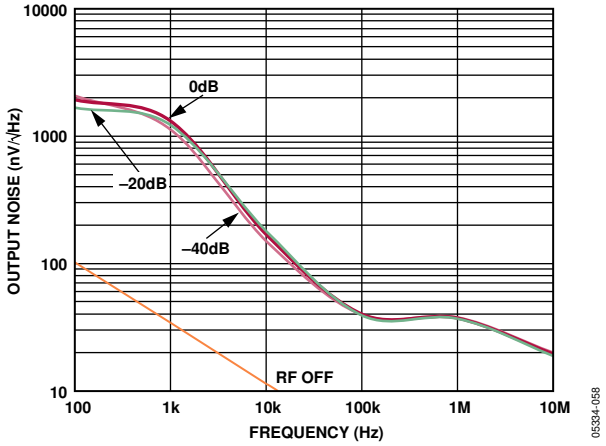

Figure 43. Noise Spectral Density of OUT[A, B]; CLP[A, B] = 0.1 µF, Frequency = 2140 MHz

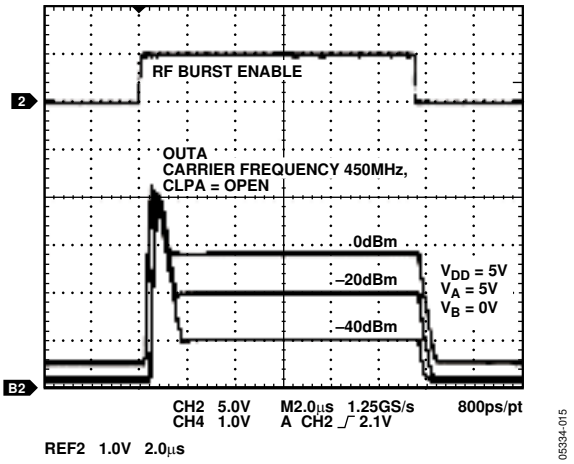

Figure 44. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA = Open

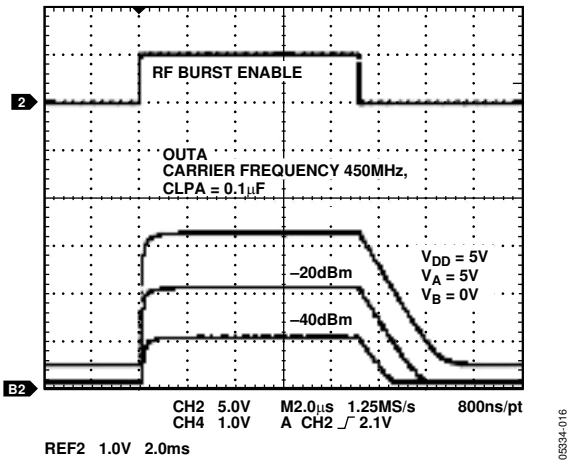

Figure 45. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA = 0.1 µF

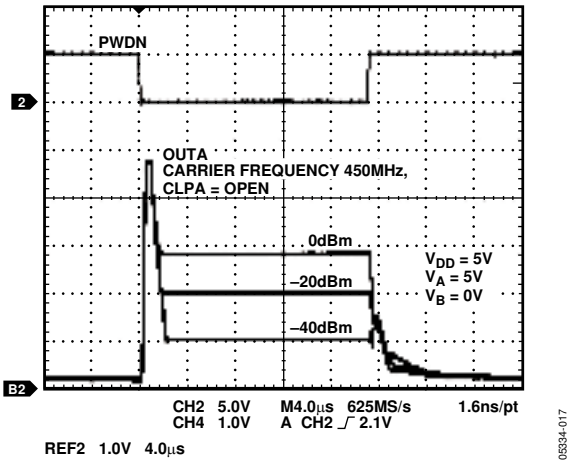

Figure 46. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA = Open

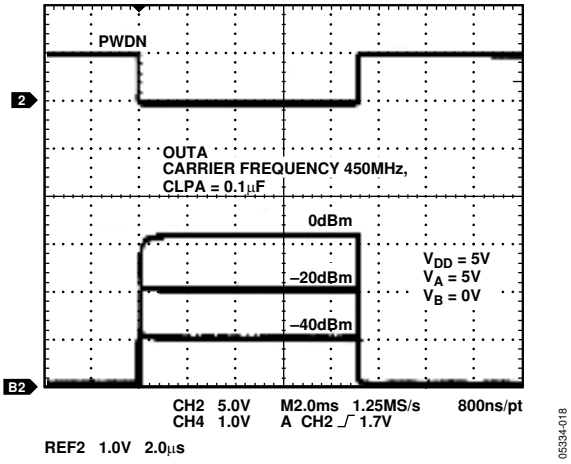

Figure 47. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA = 0.1 µF, CHPA = 10 nF

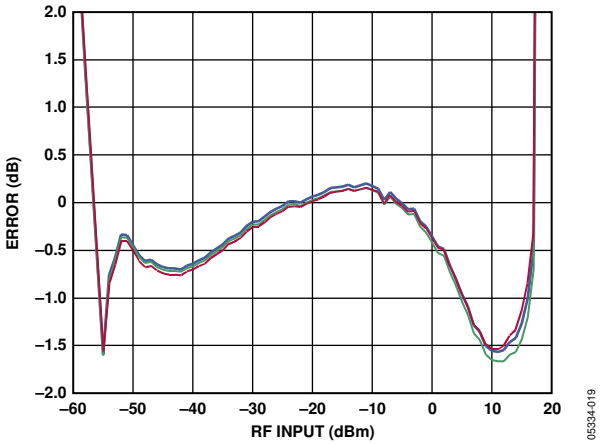

Figure 48. Output Voltage Stability vs. VP (Supply Voltage) at 2.14 GHz, When VP Varies by 10%,ADJ[A, B] =0.85 V, Sine Wave, Differential Drive, Murata LDB212G1020C-001

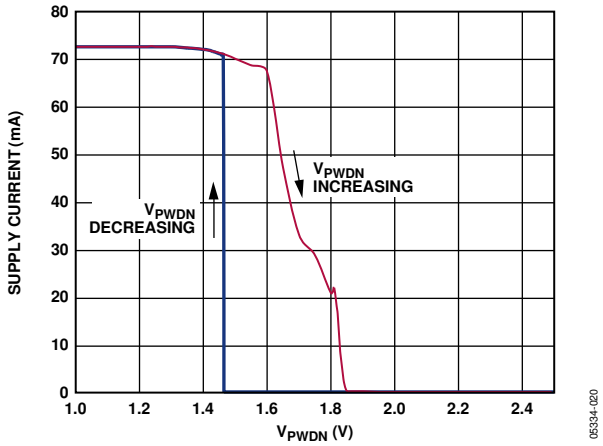

Figure 49. Supply Current vs. V_{PWDN}

GENERAL DESCRIPTION AND THEORY

The AD8364 is a dual-channel, 2.7 GHz, true rms responding detector with 60 dB measurement range. It incorporates two AD8362 channels with shared reference circuitry (See the AD8362 datasheet for more information). Multiple enhancements have been made to the AD8362 cores to improve measurement accuracy. Log-conformance peak-to-peak ripple has been reduced to <±0.2 dB over the entire dynamic range. Temperature stability of the rms output measurements provides <±0.5 dB error over the specified temperature range of −40°C to 85°C through proprietary techniques. The use of well-matched channels offers extremely temperature-stable difference outputs, OUTP and OUTN. Given well-matched channels through IC integration, the rms measurement outputs, OUTA and OUTB, drift in the same manner. With OUTP shorted to FBKA, the function at OUTP is

$$OUTP = OUTA - OUTB + VLVL \quad (1)$$

When OUTN is shorted to FBKB, the function at OUTN is

$$OUTN = OUTB - OUTA + VLVL \quad (2)$$

OUTP and OUTN are insensitive to the common drift due to the difference cancellation of OUTA and OUTB.

The AD8364 is a fully calibrated rms-to-dc converter capable of operating on signals of a few hertz to 2.7 GHz or more. Unlike logarithmic amplifiers, the AD8364 response is waveform independent. The device accurately measures waveforms that have a high peak-to-rms ratio (crest factor). Figure 50 shows a block diagram.

A single channel of the AD8364 consists of a high performance AGC loop. As shown in Figure 51, the AGC loop comprises a wide bandwidth variable gain amplifier (VGA), square law detectors, an amplitude target circuit, and an output driver. For a more detailed description of the functional blocks, see the AD8362 data sheet.

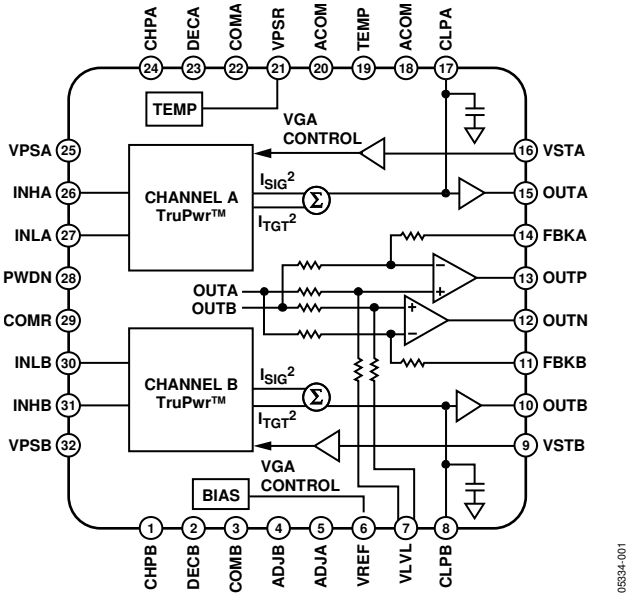

Figure 50. Block Diagram

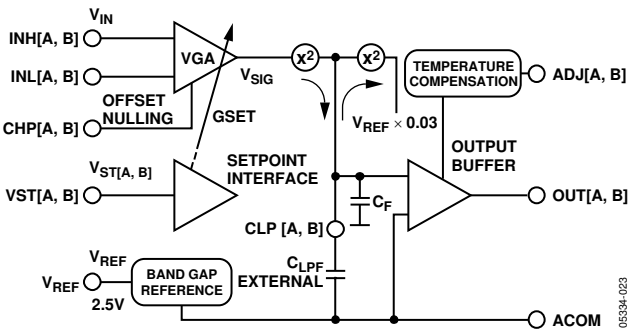

Figure 51. Single-Channel Details

SQUARE LAW DETECTOR AND AMPLITUDE TARGET

The output of the VGA, called V_{SIG}, is applied to a wideband square law detector. The detector provides the true rms response of the RF input signal, independent of waveform, up to a crest factor of 6. The detector output, called I_{SQU}, is a fluctuating current with positive mean value. The difference between I_{SQU} and an internally generated current, $I_{TGT[A, B]}$, is integrated by C_F and a capacitor attached to CLP[A, B]. CF is the on-chip 25 pF filter capacitor. CLP[A, B] can be used to arbitrarily increase the averaging time while trading off response time. When the AGC loop is at equilibrium,

$$MEAN(I_{SQU}) = I_{TGT[A, B]} \quad (3)$$

This equilibrium occurs only when

$$MEAN(V_{SIG}^2) = V_{TGT[A, B]}^2 \quad (4)$$

where V_{TGT} is an attenuated version of the VREF voltage.

Because the square law detectors are electrically identical and well matched, process and temperature dependent variations are effectively cancelled.

By forcing the above identity through varying the VGA setpoint, it is apparent that

$$RMS(V_{SIG}) = \sqrt{(MEAN(V_{SIG}^2))} = \sqrt{(V_{TGT}^2)} = V_{TGT} \quad (5)$$

Substituting the value of V_{SIG}, we have

$$RMS(G0 \times RF_{IN} \exp(-VST[A, B]/V_{GNS})) = V_{TGT} \quad (6)$$

When connected as a measurement device VST[A, B] = OUT[A, B]. Solving for OUT[A, B] as a function of RF_{IN},

$$OUT[A, B] = V_{SLOPE} \times \text{Log10}(RMS(RF_{IN})/V_Z) \quad (7)$$

where V_{SLOPE} is laser trimmed to 1 V/decade (or 50 mV/dB) at 100 MHz. V_Z is the intercept voltage, since Log 10(1) = 0 when $RMS(RF_{IN}) = V_Z$. If desired, the effective value of V_{SLOPE} may be altered by using a resistor divider from OUT[A, B] to drive VST[A, B]. The intercept, V_Z, is also laser trimmed to 180 µV (−62 dBm, referred to 50 Ω) with a CW signal at 100 MHz. This value is extrapolated, because OUT[A, B] do not respond to input of less than approximately −55 dBm with differential drive.

In most applications, the AGC loop is closed through the setpoint interface, VST[A, B]. In measurement mode, OUT[A, B] are tied to VST[A, B], respectively. In controller mode, a control voltage is applied to VST[A, B]. Pins OUT[A, B] drive the control input of a system. The RF feedback signal to the input pins is forced to have an rms value determined by VSTA or VSTB.

RF INPUT INTERFACE

The AD8364's RF inputs are connected as shown in Figure 52. There are 100 Ω resistors connected between DEC[A, B] and INH[A, B] and also between DEC[A, B] and INL[A, B]. The DEC[A, B] pins have a dc level established as (7 × VPS[A, B] + 55 × V_{BE})/30. With a 5 V supply, DEC[A, B] is approximately 2.5 V.

Signal-coupling capacitors must be connected from the input signal to the INH[A, B] and INL[A, B] pins. The high-pass corner is

$$f_{high\text{-}pass} = 1/(2 \times \pi \times 100 \times C) \quad (8)$$

A decoupling capacitor should be connected from DEC[A, B] to ground to attenuate any signal at the midpoint. A 100 pF and 0.1 µF cap from DEC[A, B] to ground are recommended, with a 1 nF coupling capacitor such that signals greater than 1.6 MHz can be measured. For coupling signals less than 1.6 MHz, 100 × $C_{coupling}$ for the DEC[A, B] capacitor generally can be used.

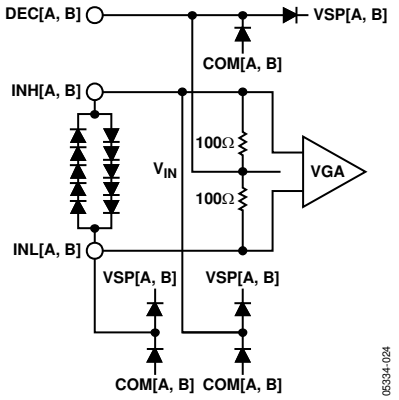

Figure 52. AD8364 RF Inputs

OFFSET COMPENSATION

An offset-nulling loop is used to address small dc offsets in the VGA. The high-pass corner frequency of this loop is internally preset to about 1 MHz using an on-chip capacitor of 25 pF (1/(2 × 5K × 25 pF)), which is sufficiently low for most HF applications. The high-pass corner can be reduced by a capacitor from CHP[A, B] to ground. The input offset voltage varies depending on the actual gain at which the VGA is operating and, thus, on the input signal amplitude. When an excessively large value of CHP[A, B] is used, the offset correction process may lag the more rapid changes in the VGA's gain, which may increase the time required for the loop to fully settle for a given steady input amplitude.

TEMPERATURE SENSOR INTERFACE

The AD8364 provides a temperature sensor output capable of driving about 1.6 mA. A 330 Ω-equivalent internal resistance is connected from TEMP to COMR to provide current sink capability. The temperature scaling factor of the output voltage is approximately 2 mV/°C. The typical absolute voltage at 25°C is about 620 mV.

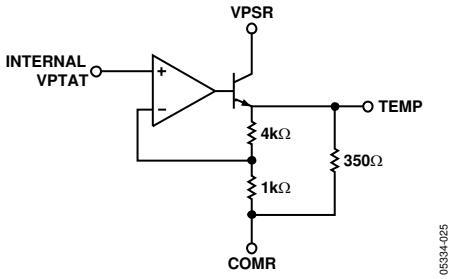

Figure 53. TEMP Interface Simplified Schematic

VREF INTERFACE

An internal voltage reference is provided to the user at Pin VREF. The VREF voltage is a temperature stable 2.5 V reference that can drive about 18 mA. An 830 Ω equivalent internal resistance is connected from VREF to ACOM for 3 mA sink capability.

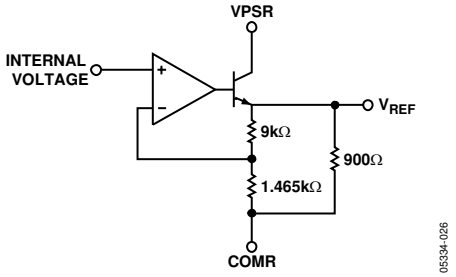

Figure 54. VREF Interface Simplified Schematic

POWER-DOWN INTERFACE

The operating and stand-by currents for the AD8364 at 25°C are approximately 70 mA and 500 µA, respectively. The PWDN pin is connected to an internal resistor divider made with two 42 kΩ resistors. The divider voltage is applied to the base of an NPN transistor to force a power-down condition when the device is active. Typically when PWDN is pulled greater than 2 V, the device is powered down. Figure 46 and Figure 47 show typical response times for various RF input levels. The output reaches to within 0.1 dB of its steady-state value in about 1.6 µs; the reference voltage is available to full accuracy in a much shorter time. This wake-up response vary depending on the input coupling means and the capacitances CDEC[A, B], CHP[A, B], and CLP[A, B].

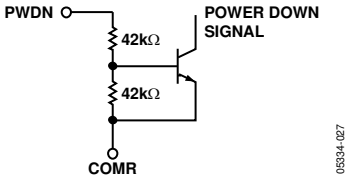

Figure 55. PWDN Interface Simplified Schematic

VST[A, B] INTERFACE

The VST[A, B] interface has a high input impedance of 72 kΩ. The voltage at VST[A, B] is converted to an internal current used to steer the VGA gain. The VGA attenuation control is set to 20 dB/V.

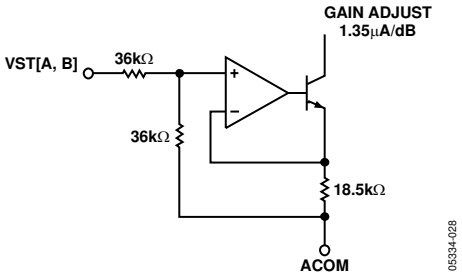

Figure 56. VST[A, B] Interface Simplified Schematic

OUT[A, B, P, N] OUTPUTS

The output drivers used in the AD8364 are different than the output stage on the AD8362. The AD8364 incorporates rail-to-rail output drivers with pull-up and pull-down capabilities. The output noise is approximately 40 nV/√Hz at 100 kHz. OUT[A, B, P, N] can source and sink up to 70 mA. There is also an internal load from both OUTA and OUTB to ACOM of 2.5 kΩ.

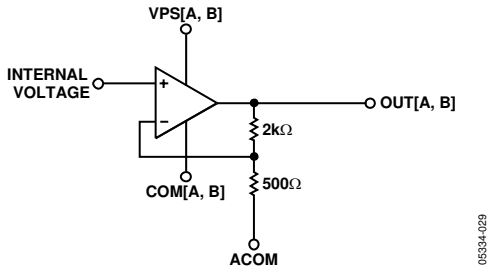

Figure 57. OUT[A, B] Interface Simplified Schematic

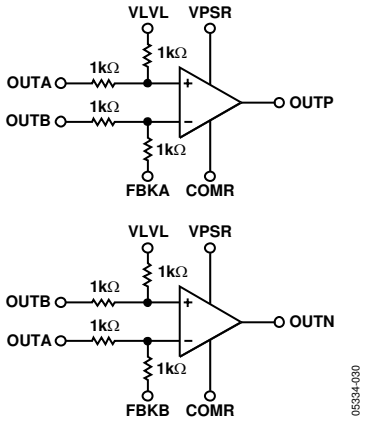

Figure 58. OUT[P, N] Interface Simplified Schematic

MEASUREMENT CHANNEL DIFFERENCE OUTPUT USING OUT[P, N]

The AD8364 incorporates two operational amplifiers with rail-to-rail output capability to provide a channel difference output. As in the case of the output drivers for OUT[A, B], the output stages have the capability of driving 70 mA. The output noise is approximately 40 nV/√Hz at 100 kHz. OUTA and OUTB are internally connected through 1 kΩ resistors to the inputs of each op amp. The pin VLVL is connected to the positive terminal of both op amps through 1 kΩ resistors to provide level shifting. The negative feedback terminal is also made available through a 1 kΩ resistor. The input impedance of VLVL is 1 kΩ and FBK[A, B] is 2 kΩ. See Figure 59 for the connections of these pins.

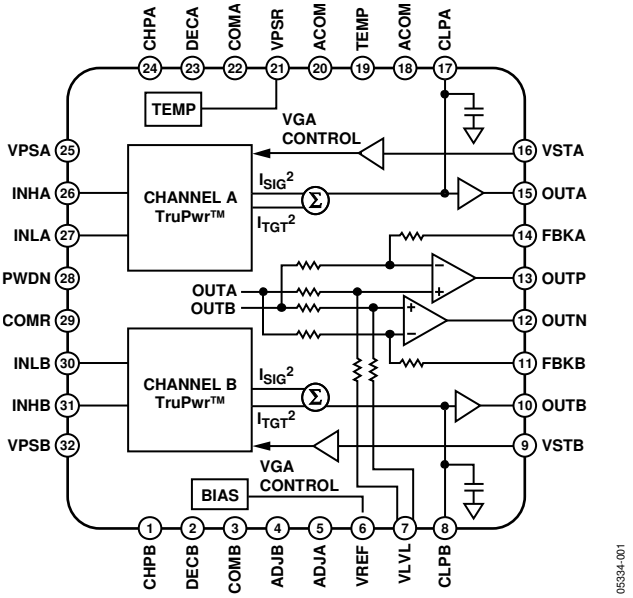

Figure 59. Op Amp Connections (All Resistors are 1 kΩ ± 20%)

If OUTP is connected to FBKA, then OUTP is given as

$$OUTP = OUTA - OUTB + VLVL \quad (9)$$

If OUTN is connected to FBKB, then OUTN is given as

$$OUTN = OUTB - OUTA + VLVL \quad (10)$$

In this configuration, all four measurements, OUT[A, B, P, N], are made available simultaneously. A differential output can be taken from OUTP − OUTN, and VLVL can be used to adjust the common-mode level for an ADC connection.

CONTROLLER MODE

The channel difference outputs can be used for controlling a feedback loop to the AD8364's RF inputs. A capacitor connected between FBKA and OUTP forms an integrator, keeping in mind that the on-chip 1 kΩ feedback resistor forms a zero. (The value of the on-chip resistors can vary as much as ±20% with manufacturing process variation.) If Channel A is driven and Channel B has a feedback loop from OUTP through a PA, then OUTP integrates to a voltage value such that

$$OUTB = (OUTA + VLVL)/2 \quad (11)$$

The output value from OUTN may or may not be useful. It is given by

$$OUTN = 0\ V \quad (12)$$

For VLVL < OUTA/3,

Otherwise,

$$OUTN = (3 \times VLVL - OUTA)/2 \quad (13)$$

If VLVL is connected to OUTA, then OUTB is forced to equal OUTA through the feedback loop. This flexibility provides the user with the capability to measure one channel operating at a given power level and frequency while forcing the other channel to a desired power level at another frequency. ADJA and ADJB should be set to different voltage levels to reduce the temperature drift of the output measurement. The temperature drift will be statistical sum of the drift from Channel A and Channel B. As stated before, VLVL can be used to force the slaved channel to operate at a different power than the other channel. If the two channels are forced to operate at different power levels, then some static offset occurs due to voltage drops across metal wiring in the IC.

If an inversion is necessary in the feedback loop, OUTN can be used as the integrator by placing a capacitor between OUTN and OUTP. This changes the output equation for OUTB and OUTP to

$$OUTB = 2 \times OUTA - VLVL \quad (14)$$

For VLVL < OUTA/2,

$$OUTN = 0\ V \quad (15)$$

Otherwise,

$$OUTN = 2 \times VLVL - OUTA \quad (16)$$

The previous equations are valid when Channel A is driven and Channel B is slaved through a feedback loop. When Channel B is driven and Channel A is slaved, the above equations can be altered by changing OUTB to OUTA and OUTN to OUTP.

RF MEASUREMENT MODE BASIC CONNECTIONS

The AD8364 requires a single supply of nominally 5 V. The supply is connected to the three supply pins, VPSA, VPSB, and VPSR. Each pin should be decoupled using the two capacitors with values equal or similar to those shown in Figure 60. These capacitors must provide a low impedance over the full frequency range of the input, and they should be placed as close as possible to the VPOS pins. Two different capacitors are used in parallel to provide a broadband ac short to ground.

The input signals are applied to the input differentially. The RF inputs of the AD8364 have a differential input impedance of 200 Ω. When the AD8364 RF inputs are driven from a 50 Ω source, a 4:1 balun transformer is recommended to provide the necessary impedance transformation. The inputs can be driven single-ended, however, this reduces the measurement range of the rms detectors (see the Single-Ended Input Operation section).

Table 4. Baluns Used to Characterize the AD8364

Frequency	Balun
450 MHz	MIA-COM ETK4-2T
880 MHz	Mini-Circuits JTX-4-10T
1880 MHz	Murata LDB181G8820C-110
2140 MHz	Murata LDB212G1020C-001
2500 MHz	Murata LDB182G4520C-110

The device is placed in measurement mode by connecting OUTA and/or OUTB to VSTA and/or VSTB, respectively. This closes the AGC loop within the device with OUT[A, B] representing the VGA control voltage, which is required to present the correct rms voltage at the input of the internal square law detector.

As the input signal to Channel A and Channel B are swept over their nominal input dynamic range of +10 dBm to −50 dBm, the output swings from 0 V to 3.5 V. The voltages OUTA and OUTB are also internally applied to a difference amplifier with a gain of two. So as the dB difference between INA and INB ranges from approximately −30 dB to +30 dB, the difference voltage on OUTP and OUTN swings from −3.5 V to +3.5 V. Input differences larger than ±30 dB can be measured as long as the absolute input level at INA and INB are within their nominal ranges of +10 dBm to −50 dBm. However, measurement of large differences between INA and INB are affected by on-chip signal leakage (see the Channel Isolation section). The common-mode level of OUTP and OUTN is set by the voltage applied to VLVL. These output can be easily biased up to a common-mode voltage of 2.5 V by connecting VREF to VLVL. As the gain range is swept, OUTP swings from approximately 1 V to 4.5 V and OUTN swings from 4.5 V to 1 V.

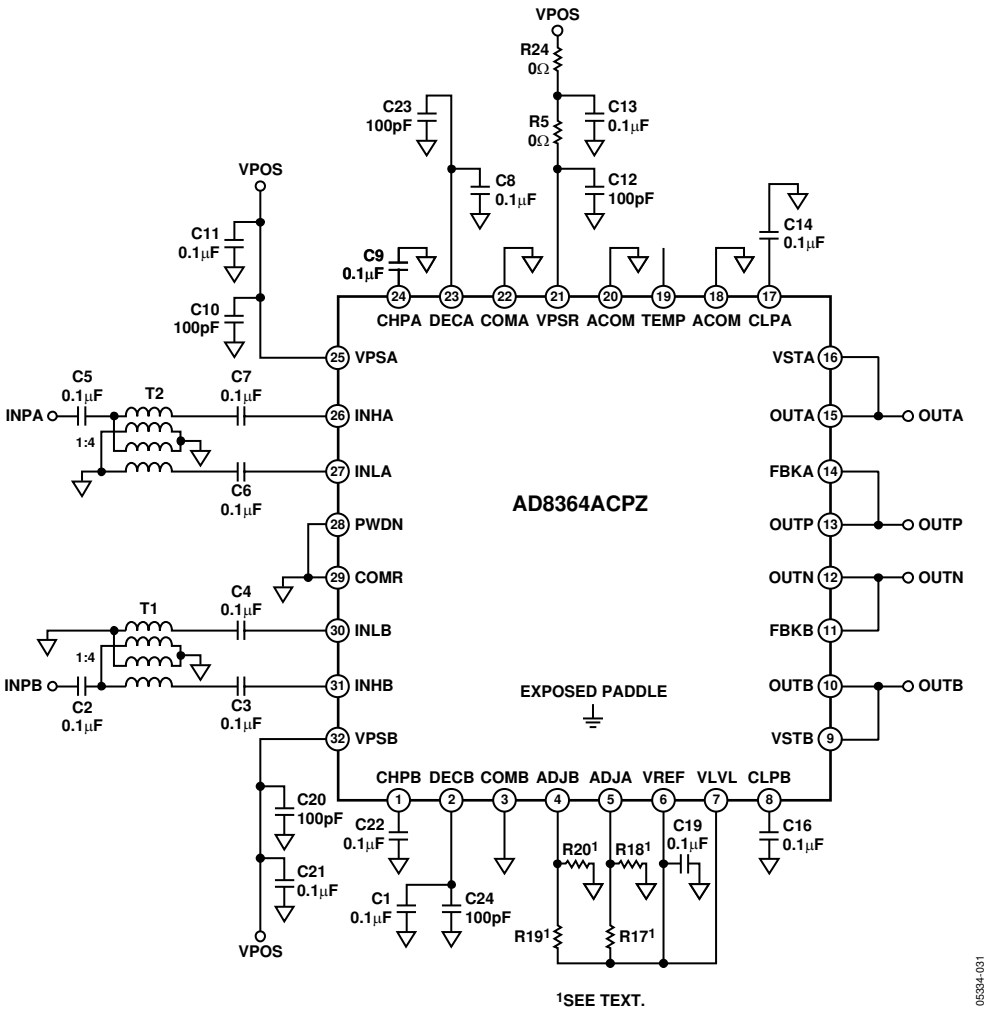

Figure 60. Basic Connections for Operation in Measurement Mode

CONTROLLER MODE BASIC CONNECTIONS

In addition to being a measurement device, the AD8364 can also be configured to measure and control rms signal levels. The AD8364 has two controller modes. Each of the two rms log detectors can be separately configured to set and control the output power level of a variable gain amplifier (VGA) or variable voltage attenuator (VVA). Alternatively, the two rms log detectors can be configured to measure and control the *gain* of an amplifier or signal chain.

Automatic Power Control

Figure 61 shows how the device should be reconfigured to control output *power*.

The RF input to the device is configured as before. A directional coupler taps off some of the power being generated by the VGA (typically a 10 dB to 20 dB coupler is used). A power splitter can be used instead of a directional coupler if there are no concerns about reflected energy from the next stage in the signal chain. Some additional attenuation may be required to set the maximum input signal at the AD8364 to be equal to the recommended maximum input level for optimum linearity and temperature stability at the frequency of operation.

VSTA and OUTA are no longer shorted together. OUTA now provides a bias or gain control voltage to the VGA. The gain control sense of the VGA must be negative and monotonic, that is, increasing voltage tends to decrease gain. However, the gain control transfer function of the device does not need to be well controlled or particularly linear. If the gain control sense of the VGA is positive, an inverting op amp circuit with a dc offset shift can be used between the AD8364 and the VGA to keep the gain control voltage in the 0 V to 5 V range.

VSTA becomes the setpoint input to the system. This can be driven by a DAC, as shown in Figure 61, if the output power is expected to vary, or it can simply be driven by a stable reference voltage if constant output power is required. This DAC should have an output swing that covers the 0 V to 3.5 V range.

When VSTA is set to a particular value, the AD8364 compares this value to the equivalent input power present at the RF input. If these two values do not match, OUTA increases or decreases in an effort to balance the system. The dominant pole of the error amplifier/integrator circuit that drives OUTA is set by the capacitance on Pin CLPA; some experimentation may be necessary to choose the right value for this capacitor. In general, CLPA should be chosen to provide stable loop operation for the complete output power control range. If the slope (in dB/V) of the gain control transfer function of the VGA is not constant, CLPA must be chosen to guarantee a stable loop when the gain control slope is at its maximum. On the other hand, CLPA must provide adequate averaging to the internal low range squaring detector so that the rms computation is valid. Larger values of CLPA tend to make the loop less responsive.

The relationship between VSTA and the RF input follows from the measurement mode behavior of the device. For example, from Figure 9, which shows the measurement mode transfer function at 880 MHz, it can be seen that an input power of −10 dBm yields an output voltage of 2.5 V. Therefore, in controller mode, VSTA should be set to 2.5 V, which results in an input power of −10 dBm to the AD8364.

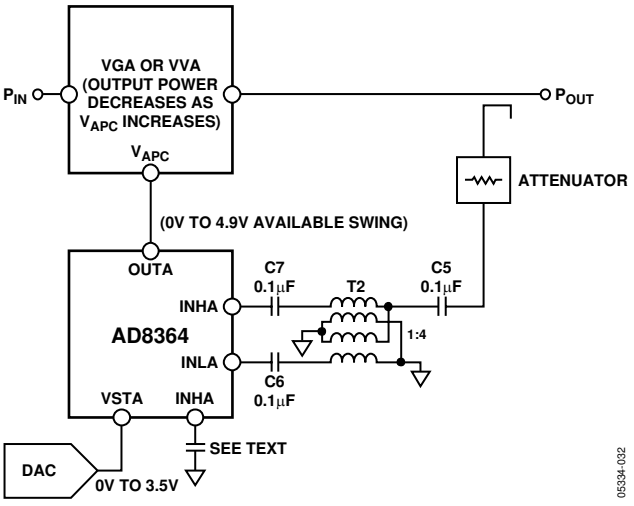

Figure 61. Operation in Controller Mode for Automatic Power Control

Automatic Gain Control

Figure 62 shows how the AD8364 can be connected to provide automatic *gain* control to an amplifier or signal chain. Additional pins are omitted for clarity. In this configuration, both rms detectors are connected in measurement mode with appropriate filtering being used on CLP[A, B] to effect a valid rms computation on both channels. OUTA, however, is also connected to the VLVL pin of the on-board difference amplifier. Also, the OUTP output of the difference amplifier drives a variable gain element (either VVA or VGA) and is connected back to the FBKA input via a capacitor so that it is operating as an integrator.

Assume that OUTA is much bigger than OUTB. Because OUTA also drives VLVL, this voltage is also present on the noninverting input of the op amp driving OUTP. This results in a net current flow from OUTP through the integrating capacitor into the FBKA input. This results in the voltage on OUTP increasing. If the gain control transfer function of the VVA/VGA is positive, this increases the gain, which in turn increases the input signal to INHB. The output voltage on the integrator continues to increase until the power on the two input channels is equal, resulting in a signal chain gain of unity.

If a gain other than 0 dB is required, an attenuator can be used in one of the RF paths, as shown in Figure 62. Alternatively, power splitters or directional couplers of different coupling factors can be used. Another convenient option is to apply a voltage on VLVL other than OUTA. Refer to Equation 11 and the Controller Mode section for more detail.

If the VGA/VVA has a negative gain control sense, the OUTN output of the difference amplifier can be used with the integrating capacitor tied back to FBKB.

The choice of the integrating capacitor affects the response time of the AGC loop. Small values give a faster response time but can result in instability, whereas larger values reduce the response time. Note that in this mode, the capacitors on CLPA and CLPB, which perform the rms averaging function, must still be used and also affect the loop response time.