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Precision Analog Front End and Controller for Battery Test/Formation Systems

Data Sheet **AD8450**

FEATURES

- Integrated constant current and voltage modes with automatic switchover
- Charge and discharge modes
- Precision voltage and current measurement
- Integrated precision control feedback blocks
- Precision interface to PWM or linear power converters
- Programmable gain settings
  - Current sense gains: 26, 66, 133, and 200
  - Voltage sense gains: 0.2, 0.27, 0.4, and 0.8
- Programmable OVP and OCP fault detection
- Current sharing and balancing
- Excellent ac and dc performance
- Maximum offset voltage drift: 0.6 µV/°C
- Maximum gain drift: 3 ppm/°C
- Low current sense amplifier input voltage noise: ≤9 nV/√Hz
- Current sense CMRR: 126 dB minimum (gain = 200)
- TTL compliant logic

APPLICATIONS

- Battery cell formation and testing
- Battery module testing

GENERAL DESCRIPTION

The AD8450 is a precision analog front end and controller for testing and monitoring battery cells. A precision programmable gain instrumentation amplifier (PGIA) measures the battery charge/discharge current, and a programmable gain difference amplifier (PGDA) measures the battery voltage (see Figure 1). Internal laser trimmed resistor networks set the gains for the PGIA and the PGDA, optimizing the performance of the AD8450 over the rated temperature range. PGIA gains are 26, 66, 133, and 200. PGDA gains are 0.2, 0.27, 0.4, and 0.8.

Voltages at the ISET and VSET inputs set the desired constant current (CC) and constant voltage (CV) values. CC to CV switching is automatic and transparent to the system.

A TTL logic level input, MODE, selects the charge or discharge mode (high for charge, low for discharge). An analog output, VCTRL, interfaces directly with the Analog Devices, Inc., ADP1972 PWM controller.

The AD8450 includes resistor programmable overvoltage and overcurrent detection and current sharing circuitry. Current sharing is used to balance the output current of multiple bridged channels.

The AD8450 simplifies designs by providing excellent accuracy, performance over temperature, flexibility with functionality, and overall reliability in a space-saving package. The AD8450 is available in an 80-lead, 14 mm × 14 mm × 1 mm LQFP package and is rated for an operating temperature of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

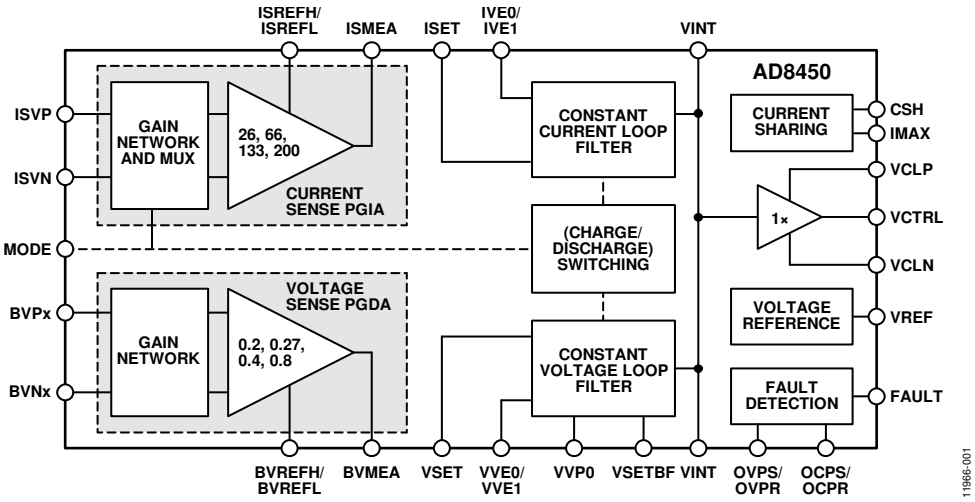

Figure 1.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD8450* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD8450 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1319: Compensator Design for a Battery Charge/ Discharge Unit Using the AD8450 or the AD8451

Data Sheet

- AD8450: Precision Analog Front End and Controller for Battery Test/Formation Systems Data Sheet

User Guides

- UG-845: AD8450/ADP1972 Battery Testing and Formation Evaluation Board

TOOLS AND SIMULATIONS

- AD8450 SPICE Macro Model

REFERENCE MATERIALS

Press

- Analog Devices Introduces the First Integrated Analog Controller Optimizing High-Efficiency Rechargeable Battery Manufacturing

DESIGN RESOURCES

- AD8450 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD8450 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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1/14—Revision 0: Initial Version

SPECIFICATIONS

AVCC = +25 V, AVEE = −5 V; AVCC = +15 V, AVEE = −15 V; DVCC = +5 V; PGIA gain = 26, 66, 133, or 200; PGDA gain = 0.2, 0.27, 0.4, or 0.8; T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT SENSE PGIA					
Internal Fixed Gains			26, 66, 133, 200		V/V
Gain Error	V_{ISMEA} = ±10 V			±0.1	%
Gain Drift	$T_A = T_{MIN}$ to T_{MAX}			3	ppm/°C
Gain Nonlinearity	V_{ISMEA} = ±10 V, R_L = 2 kΩ			3	ppm
Offset Voltage (RTI)	Gain = 200, ISREFH and ISREFL pins grounded	−110		+110	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Input Bias Current			15	30	nA
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			150	pA/°C
Input Offset Current				2	nA
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			10	pA/°C
Input Common-Mode Voltage Range	$V_{ISVP} - V_{ISVN}$ = 0 V	AVEE + 2.3		AVCC − 2.4	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 2.6		AVCC − 2.6	V
Overvoltage Input Range		AVCC − 55		AVEE + 55	V
Differential Input Impedance			150		GΩ
Input Common-Mode Impedance			150		GΩ
Output Voltage Swing		AVEE + 1.5		AVCC − 1.2	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.4	V
Capacitive Load Drive				1000	pF
Short-Circuit Current			40		mA
Reference Input Voltage Range	ISREFH and ISREFL pins tied together	AVEE		AVCC	V
Reference Input Bias Current	$V_{ISVP} = V_{ISVN}$ = 0 V		5		µA
Output Voltage Level Shift	ISREFL pin grounded				
Maximum	ISREFH pin connected to VREF pin	17	20	23	mV
Scale Factor	V_{ISMEA}/V_{ISREFH}	6.8	8	9.2	mV/V
CMRR	ΔV_{CM} = 20 V				
Gain = 26		108			dB
Gain = 66		116			dB
Gain = 133		122			dB
Gain = 200		126			dB
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			0.01	µV/V/°C
PSRR	ΔV_S = 20 V				
Gain = 26		108	122		dB
Gain = 66		116	130		dB
Gain = 133		122	136		dB
Gain = 200		126	140		dB
Voltage Noise	f = 1 kHz				
Gain = 26			9		nV/√Hz
Gain = 66			8		nV/√Hz
Gain = 133			7		nV/√Hz
Gain = 200			7		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz, all fixed gains		0.2		µV p-p
Current Noise	f = 1 kHz		80		fA/√Hz
Current Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		5		pA p-p

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Small Signal −3 dB Bandwidth					
Gain = 26			1.5		MHz
Gain = 66			630		kHz
Gain = 133			330		kHz
Gain = 200			220		kHz
Slew Rate	ΔV_{ISMEA} = 10 V		5		V/µs
VOLTAGE SENSE PGDA					
Internal Fixed Gains			0.2, 0.27, 0.4, 0.8		V/V
Gain Error	V_{IN} = ±10 V			±0.1	%
Gain Drift	$T_A = T_{MIN}$ to T_{MAX}			3	ppm/°C
Gain Nonlinearity	V_{BVMEA} = ±10 V, R_L = 2 kΩ			3	ppm
Offset Voltage (RTO)	BVREFH and BVREFL pins grounded			500	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			4	µV/°C
Differential Input Voltage Range	Gain = 0.8, V_{BVN0} = 0 V, V_{BVREFL} = 0 V				
	AVCC = +15 V, AVEE = −15 V	−16		+16	V
	AVCC = +25 V, AVEE = −5 V	−4		+29	V
Input Common-Mode Voltage Range	Gain = 0.8, V_{BVMEA} = 0 V				
	AVCC = +15 V, AVEE = −15 V	−27		+27	V
	AVCC = +25 V, AVEE = −5 V	−7		+50	V
Differential Input Impedance					
Gain = 0.2			800		kΩ
Gain = 0.27			600		kΩ
Gain = 0.4			400		kΩ
Gain = 0.8			200		kΩ
Input Common-Mode Impedance					
Gain = 0.2			240		kΩ
Gain = 0.27			190		kΩ
Gain = 0.4			140		kΩ
Gain = 0.8			90		kΩ
Output Voltage Swing		AVEE + 1.5		AVCC − 1.5	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.7	V
Capacitive Load Drive				1000	pF
Short-Circuit Current			30		mA
Reference Input Voltage Range	BVREFH and BVREFL pins tied together	AVEE		AVCC	V
Output Voltage Level Shift	BVREFL pin grounded				
Maximum	BVREFH pin connected to VREF pin	4.5	5	5.5	mV
Scale Factor	V_{BVMEA}/V_{BVREFH}	1.8	2	2.2	mV/V
CMRR	ΔV_{CM} = 10 V, all fixed gains, RTO	80			dB
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			0.05	µV/V/°C
PSRR	ΔV_S = 20 V, all fixed gains, RTO	100			dB
Output Voltage Noise	f = 1 kHz, RTI				
Gain = 0.2			325		nV/√Hz
Gain = 0.27			250		nV/√Hz
Gain = 0.4			180		nV/√Hz
Gain = 0.8			105		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz, RTI				
Gain = 0.2			6		µV p-p
Gain = 0.27			5		µV p-p
Gain = 0.4			3		µV p-p
Gain = 0.8			2		µV p-p

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Small Signal −3 dB Bandwidth					
Gain = 0.2			420		kHz
Gain = 0.27			730		kHz
Gain = 0.4			940		kHz
Gain = 0.8			1000		kHz
Slew Rate			0.8		V/µs
CONSTANT CURRENT AND CONSTANT VOLTAGE LOOP FILTER AMPLIFIERS					
Offset Voltage				150	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Input Bias Current		−5		+5	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	−5		+5	nA
Input Common-Mode Voltage Range		AVEE + 1.5		AVCC − 1.8	V
Output Voltage Swing	V_{VCLN} = AVEE + 1 V, V_{VCLP} = AVCC − 1 V	AVEE + 1.5		AVCC − 1	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1	V
Closed-Loop Output Impedance			0.01		Ω
Capacitive Load Drive				1000	pF
Source Short-Circuit Current			1		mA
Sink Short-Circuit Current			40		mA
Open-Loop Gain			140		dB
CMRR	ΔV_{CM} = 10 V			100	dB
PSRR	ΔV_S = 20 V			100	dB
Voltage Noise	f = 1 kHz		10		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		0.3		µV p-p
Current Noise	f = 1 kHz		80		fA/√Hz
Current Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		5		pA p-p
Small Signal Gain Bandwidth Product			3		MHz
Slew Rate	ΔV_{VINT} = 10 V		1		V/µs
CC to CV Transition Time			1.5		µs
UNCOMMITTED OP AMP					
Offset Voltage				150	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Input Bias Current		−5		+5	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	−5		+5	nA
Input Common-Mode Voltage Range		AVEE + 1.5		AVCC − 1.8	V
Output Voltage Swing		AVEE + 1.5		AVCC − 1.5	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.5	V
Closed-Loop Output Impedance			0.01		Ω
Capacitive Load Drive				1000	pF
Short-Circuit Current			40		mA
Open-Loop Gain	R_L = 2 kΩ		140		dB
CMRR	ΔV_{CM} = 10 V			100	dB
PSRR	ΔV_S = 20 V			100	dB
Voltage Noise	f = 1 kHz		10		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		0.3		µV p-p
Current Noise	f = 1 kHz		80		fA/√Hz
Current Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		5		pA p-p
Small Signal Gain Bandwidth Product			3		MHz
Slew Rate	ΔV_{OAVO} = 10 V		1		V/µs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT SHARING BUS AMPLIFIER					
Nominal Gain			1		V/V
Offset Voltage				150	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Output Voltage Swing		AVEE + 1.5		AVCC − 1.5	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.7	V
Capacitive Load Drive				1000	pF
Source Short-Circuit Current			40		mA
Sink Short-Circuit Current			0.5		mA
CMRR	ΔV_{CM} = 10 V			100	dB
PSRR	ΔV_S = 20 V			100	dB
Voltage Noise	f = 1 kHz		10		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		0.4		µV p-p
Small Signal −3 dB Bandwidth			3		MHz
Slew Rate	ΔV_{CS} = 10 V		1		V/µs
Transition Time			1.5		µs
CURRENT SHARING, VINT, AND CONSTANT VOLTAGE BUFFERS					
Nominal Gain			1		V/V
Offset Voltage				150	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Input Bias Current	CV buffer only	−5		+5	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	−5		+5	nA
Input Voltage Range		AVEE + 1.5		AVCC − 1.8	V
Output Voltage Swing					
Current Sharing and Constant Voltage Buffers		AVEE + 1.5		AVCC − 1.5	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.5	V
VINT Buffer		V_{VCLN} − 0.6		V_{VCLP} + 0.6	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	V_{VCLN} − 0.6		V_{VCLP} + 0.6	V
Output Clamps Voltage Range	VINT buffer only				
VCLP Pin		V_{VCLN}		AVCC − 1	V
VCLN Pin		AVEE + 1		V_{VCLP}	V
Closed-Loop Output Impedance			1		Ω
Capacitive Load Drive				1000	pF
Short-Circuit Current			40		mA
PSRR	ΔV_S = 20 V			100	dB
Voltage Noise	f = 1 kHz		10		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		0.3		µV p-p
Current Noise	f = 1 kHz, CV buffer only		80		fA/√Hz
Current Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		5		pA p-p
Small Signal −3 dB Bandwidth			3		MHz
Slew Rate	ΔV_{OUT} = 10 V		1		V/µs
OVERCURRENT AND OVERVOLTAGE FAULT COMPARATORS					
High Threshold Voltage	With respect to OVPR and OCPR pins		30	45	mV
Temperature Coefficient			100		µV/°C
Low Threshold Voltage	With respect to OVPR and OCPR pins	−45	−30		mV
Temperature Coefficient			−100		µV/°C
Input Bias Current			250		nA
Input Voltage Range	OVPR, OCPR, OVPS, and OCPS pins	AVEE		AVCC − 3	V
Differential Input Voltage Range		−7		+7	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Fault Output Logic Levels	FAULT pin (Pin 46)				
Output Voltage High, V_{OH}	I_{LOAD} = 200 µA	4.5			V
Output Voltage Low, V_{OL}	I_{LOAD} = 200 µA			0.5	V
Propagation Delay	C_{LOAD} = 10 pF		500		ns
Fault Rise Time	C_{LOAD} = 10 pF		150		ns
Fault Fall Time	C_{LOAD} = 10 pF		150		ns
VOLTAGE REFERENCE					
Nominal Output Voltage	With respect to AGND		2.5		V
Output Voltage Error				±1	%
Temperature Drift	$T_A = T_{MIN}$ to T_{MAX}			10	ppm/°C
Line Regulation	ΔV_S = 10 V			40	ppm/V
Load Regulation	ΔI_{VREF} = 1 mA (source only)			400	ppm/mA
Output Current, Sourcing				10	mA
Voltage Noise	f = 1 kHz		100		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		5		µV p-p
DIGITAL INTERFACE, MODE INPUT	MODE pin (Pin 39)				
Input Voltage High, V_{IH}	With respect to DGND	2.0		DVCC	V
Input Voltage Low, V_{IL}	With respect to DGND	DGND		0.8	V
Mode Switching Time			500		ns
POWER SUPPLY					
Operating Voltage Range					
AVCC		5		36	V
AVEE		−31		0	V
Analog Supply Range	AVCC − AVEE	5		36	V
DVCC		3		5	V
Quiescent Current					
AVCC			7	10	mA
AVEE			6.5	10	mA
DVCC			40	70	µA
TEMPERATURE RANGE					
For Specified Performance		−40		+85	°C
Operational		−55		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Analog Supply Voltage (AVCC − AVEE)	36 V
Digital Supply Voltage (DVCC − DGND)	36 V
Maximum Voltage at Input Pins (ISVP, ISVN, BVPx, and BVNx)	AVEE + 55 V
Minimum Voltage at Input Pins (ISVP, ISVN, BVPx, and BVNx)	AVCC − 55 V
Maximum Voltage at All Input Pins, Except ISVP, ISVN, BVPx, and BVNx	AVCC
Minimum Voltage at All Input Pins, Except ISVP, ISVN, BVPx, and BVNx	AVEE
Maximum Digital Supply Voltage with Respect to the Positive Analog Supply (DVCC − AVCC)	+0.5 V
Minimum Digital Supply Voltage with Respect to the Negative Analog Supply (DVCC − AVEE)	−0.5 V
Maximum Digital Ground with Respect to the Positive Analog Supply (DGND − AVCC)	+0.5 V
Minimum Digital Ground with Respect to the Negative Analog Supply (DGND − AVEE)	−0.5 V
Maximum Analog Ground with Respect to the Positive Analog Supply (AGND − AVCC)	+0.5 V
Minimum Analog Ground with Respect to the Negative Analog Supply (AGND − AVEE)	−0.5 V
Maximum Analog Ground with Respect to the Digital Ground (AGND − DGND)	+0.5 V
Minimum Analog Ground with Respect to the Digital Ground (AGND − DGND)	−0.5 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The θ_{JA} value assumes a 4-layer JEDEC standard board with zero airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
80-Lead LQFP	54.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

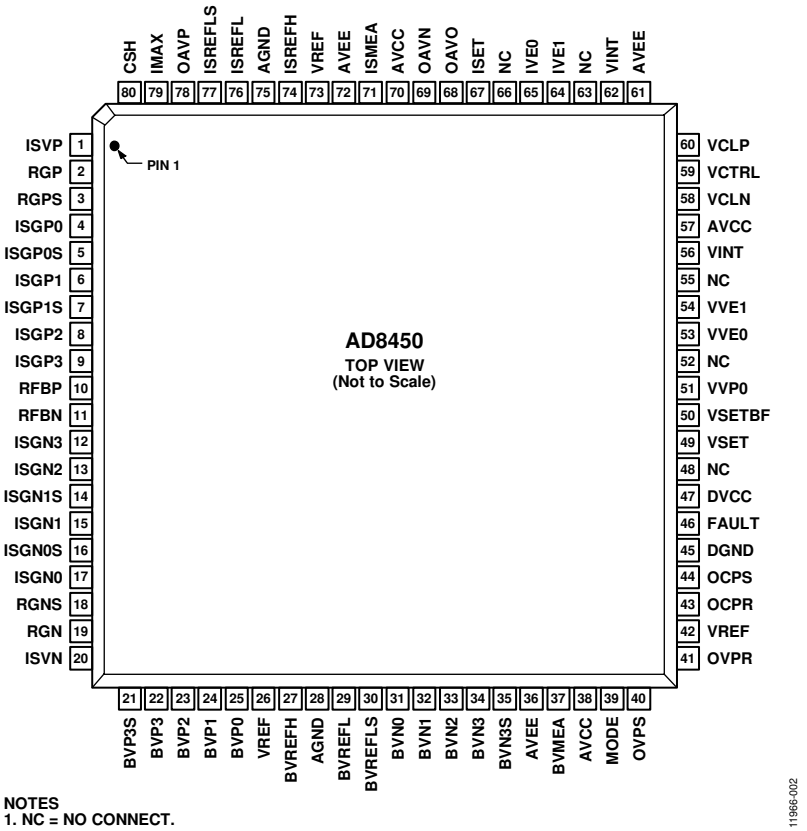

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output[1]	Description
1, 20	ISVP, ISVN	Input	Current Sense Instrumentation Amplifier Positive (Noninverting) and Negative (Inverting) Inputs. Connect these pins across the current sense shunt resistor.
2, 19	RGP, RGN	N/A	Current Sense Instrumentation Amplifier Gain Setting Pins. Connect these pins to the appropriate resistor network gain pins to select the current sense gain (see Table 5).
3, 18	RGPS, RGNS	N/A	Kelvin Sense Pins for the Current Sense Instrumentation Amplifier Gain Setting Pins (RGP and RGN).
4, 6, 8, 9, 12, 13, 15, 17	ISGP0, ISGP1, ISGP2, ISGP3, ISGN3, ISGN2, ISGN1, ISGN0	N/A	Current Sense Instrumentation Amplifier Resistor Network Gain Pins (see Table 5).
5, 7, 14, 16	ISGP0S, ISGP1S, ISGN1S, ISGN0S	N/A	Kelvin Sense Pins for the ISGP0, ISGP1, ISGN1, and ISGN0 Pins.
10, 11	RFBP, RFBN	Output	Current Sense Preamplifier Positive and Negative Outputs.
21, 35	BVP3S, BVN3S	N/A	Kelvin Sense Pins for the Voltage Sense Difference Amplifier Inputs BVP3 and BVN3.
22, 23, 24, 25, 31, 32, 33, 34	BVP3, BVP2, BVP1, BVP0, BVN0, BVN1, BVN2, BVN3	Input	Voltage Sense Difference Amplifier Inputs. Each input pair (BVPx and BVNx) corresponds to a different voltage sense gain (see Table 6).
26, 42, 73	VREF	Output	Voltage Reference Output Pins. VREF = 2.5 V.
27	BVREFH	Input	Reference Input for the Voltage Sense Difference Amplifier. To level shift the voltage sense difference amplifier output by approximately 5 mV, connect this pin to the VREF pin. Otherwise, connect this pin to the BVREFL pin.
28, 75	AGND	N/A	Analog Ground Pins.
29	BVREFL	Input	Reference Input for the Voltage Sense Difference Amplifier. The default connection is to ground.
30	BVREFLS	N/A	Kelvin Sense Pin for the BVREFL Pin.

Pin No.	Mnemonic	Input/ Output[1]	Description
36, 61, 72	AVEE	N/A	Analog Negative Supply Pins. The default voltage is −5 V.
38, 57, 70	AVCC	N/A	Analog Positive Supply Pins. The default voltage is +25 V.
37	BVMEA	Output	Voltage Sense Difference Amplifier Output.
39	MODE	Input	TTL-Compliant Logic Input to Select the Charge or Discharge Mode. Low = discharge, high = charge.
40	OVPS	Input	Noninverting Sense Input of the Overvoltage Protection Comparator.
41	OVPR	Input	Inverting Reference Input of the Overvoltage Protection Comparator. Typically, this pin connects to the 2.5 V reference voltage (VREF).
43	OCPR	Input	Inverting Reference Input of the Overcurrent Protection Sense Comparator. Typically, this pin connects to the 2.5 V reference voltage (VREF).
44	OCPS	Input	Noninverting Sense Input of the Overcurrent Protection Sense Comparator.
45	DGND	N/A	Digital Ground Pin.
46	FAULT	Output	Overvoltage or Overcurrent Fault Detection Logic Output (Active Low).
47	DVCC	N/A	Digital Supply. The default voltage is +5 V.
48, 52, 55, 63, 66	NC	N/A	No Connect. There are no internal connections to these pins.
49	VSET	Input	Target Voltage for the Voltage Sense Control Loop.
50	VSETBF	Output	Buffered Voltage VSET.
51	VVP0	Input	Noninverting Input of the Voltage Sense Integrator for Discharge Mode.
53	VVE0	Input	Inverting Input of the Voltage Sense Integrator for Discharge Mode.
54	VVE1	Input	Inverting Input of the Voltage Sense Integrator for Charge Mode.
56, 62	VINT	Output	Minimum Output of the Voltage Sense and Current Sense Integrator Amplifiers.
58	VCLN	Input	Low Clamp Voltage for VCTRL.
59	VCTRL	Output	Controller Output Voltage. Connect this pin to the input of the PWM controller (for example, the COMP pin of the ADP1972).
60	VCLP	Input	High Clamp Voltage for VCTRL.
64	IVE1	Input	Inverting Input of the Current Sense Integrator for Charge Mode.
65	IVE0	Input	Inverting Input of the Current Sense Integrator for Discharge Mode.
67	ISET	Input	Target Voltage for the Current Sense Control Loop.
68	OAVO	Output	Output of the Uncommitted Operational Amplifier.
69	OAVN	Input	Inverting Input of the Uncommitted Operational Amplifier.
71	ISMEA	Output	Current Sense Instrumentation Amplifier Output.
74	ISREFH	Input	Reference Input for the Current Sense Amplifier. To level shift the current sense instrumentation amplifier output by approximately 20 mV, connect this pin to the VREF pin. Otherwise, connect this pin to the ISREFL pin.
76	ISREFL	Input	Reference Input for the Current Sense Amplifier. The default connection is to ground.
77	ISREFLS	N/A	Kelvin Sense Pin for the ISREFL Pin.
78	OAVP	Input	Noninverting Input of the Uncommitted Operational Amplifier.
79	IMAX	Output	Maximum Voltage of All Voltages Applied to the Current Sharing (CSH) Pin.
80	CSH	N/A	Current Sharing Bus.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, AVCC = +25 V, AVEE = −5 V, R_L = ∞, unless otherwise noted.

PGIA CHARACTERISTICS

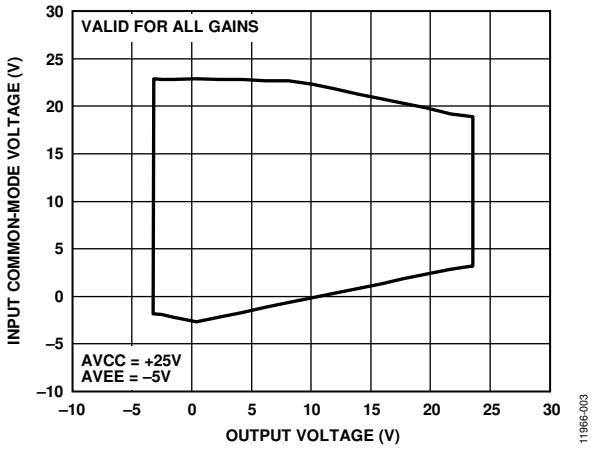

Figure 3. Input Common-Mode Voltage vs. Output Voltage for AVCC = +25 V and AVEE = −5 V

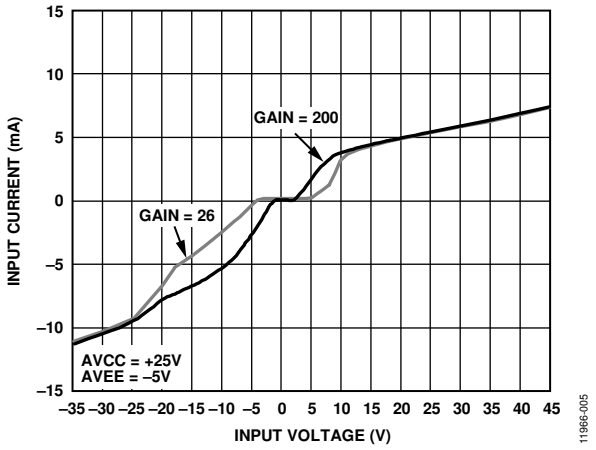

Figure 4. Input Overvoltage Performance for AVCC = +25 V and AVEE = −5 V

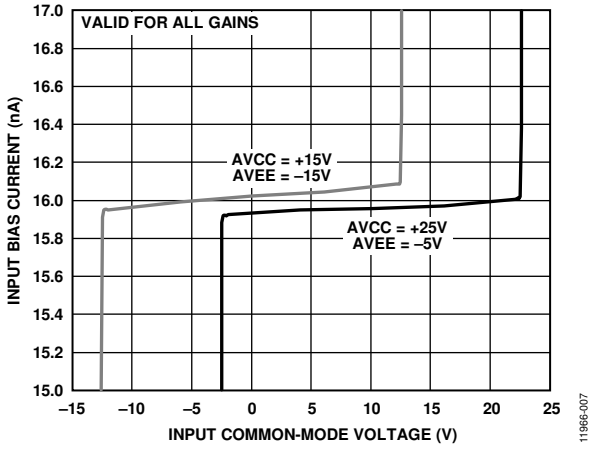

Figure 5. Input Bias Current vs. Input Common-Mode Voltage

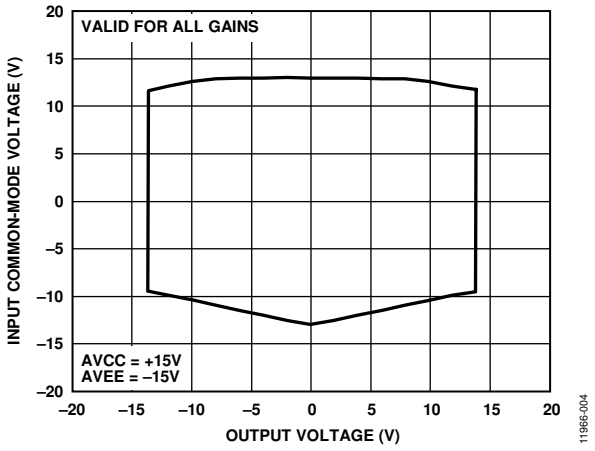

Figure 6. Input Common-Mode Voltage vs. Output Voltage for AVCC = +15 V and AVEE = −15 V

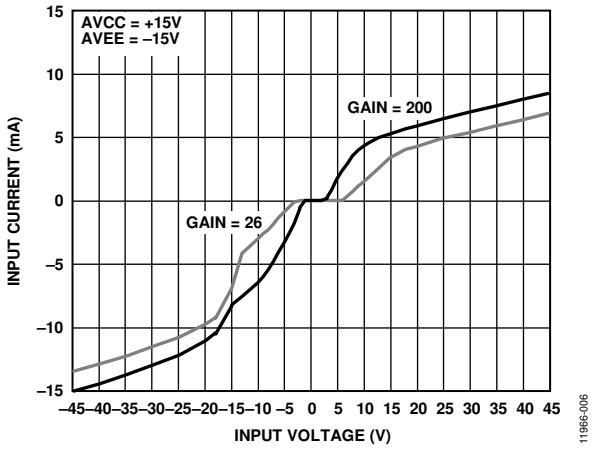

Figure 7. Input Overvoltage Performance for AVCC = +15 V and AVEE = −15 V

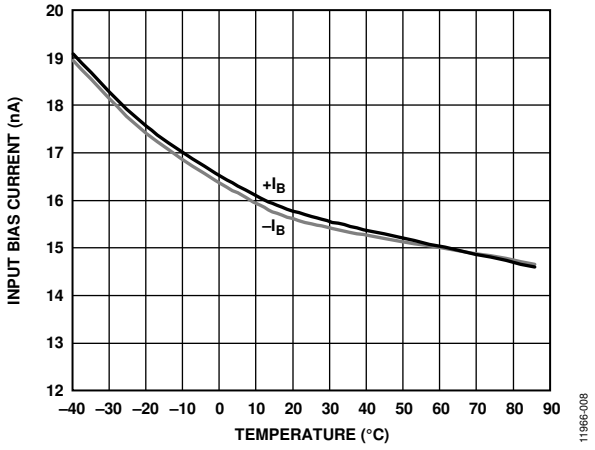

Figure 8. Input Bias Current vs. Temperature

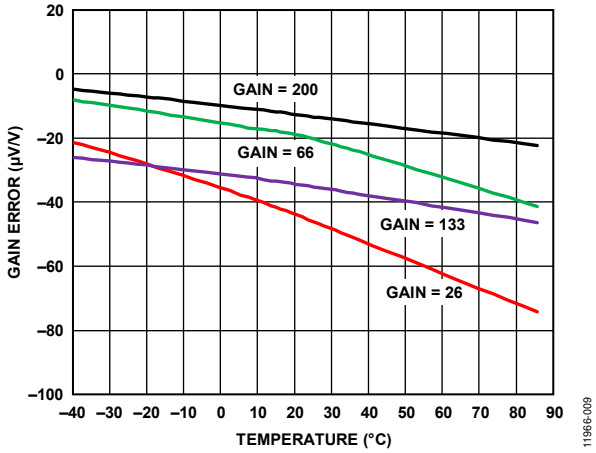

Figure 9. Gain Error vs. Temperature

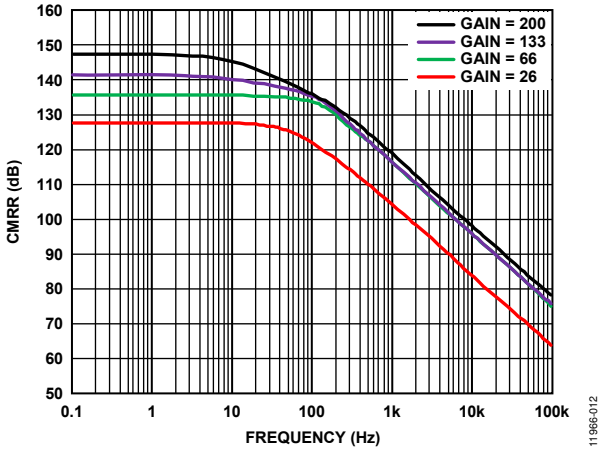

Figure 12. CMRR vs. Frequency

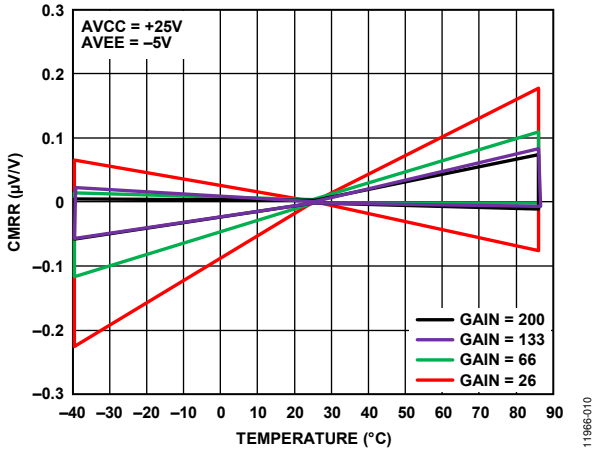

Figure 10. Normalized CMRR vs. Temperature

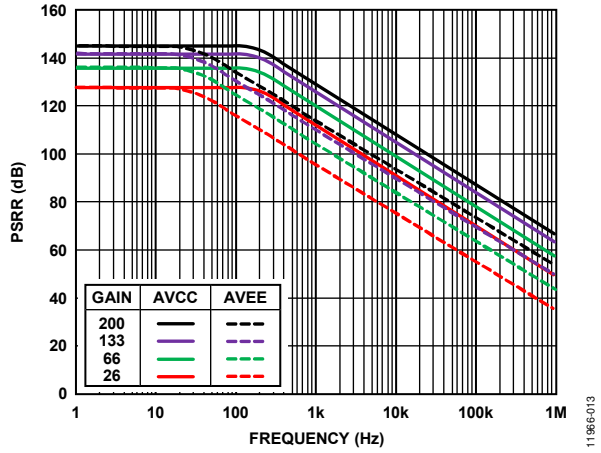

Figure 13. PSRR vs. Frequency

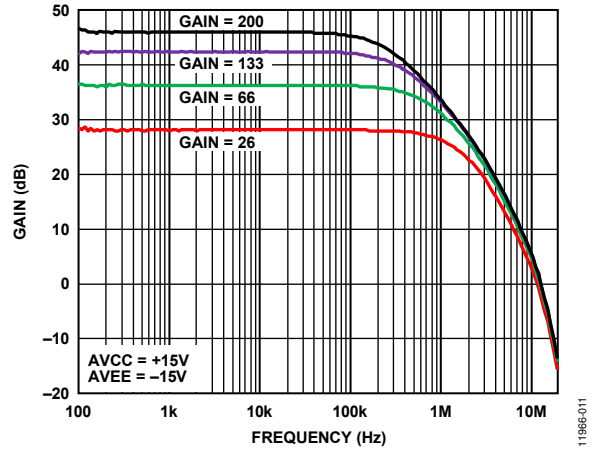

Figure 11. Gain vs. Frequency

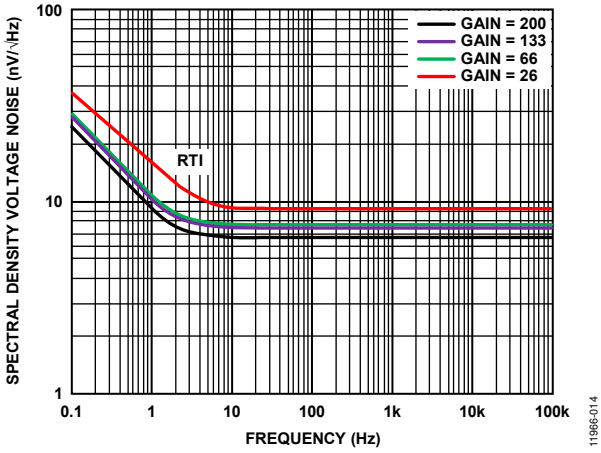

Figure 14. Spectral Density Voltage Noise, RTI vs. Frequency

PGDA CHARACTERISTICS

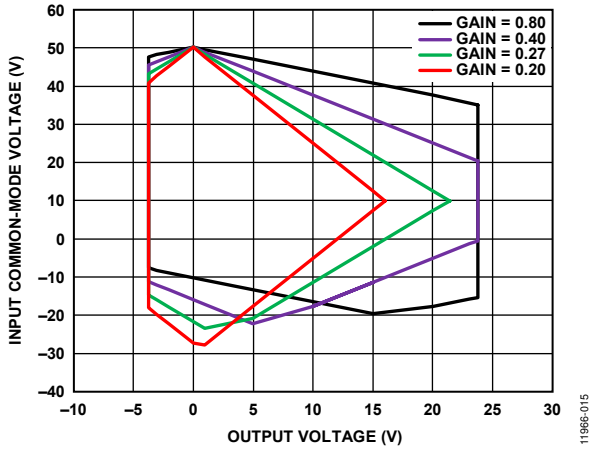

Figure 15. Input Common-Mode Voltage vs. Output Voltage for AVCC = +25 V and AVEE = −5 V

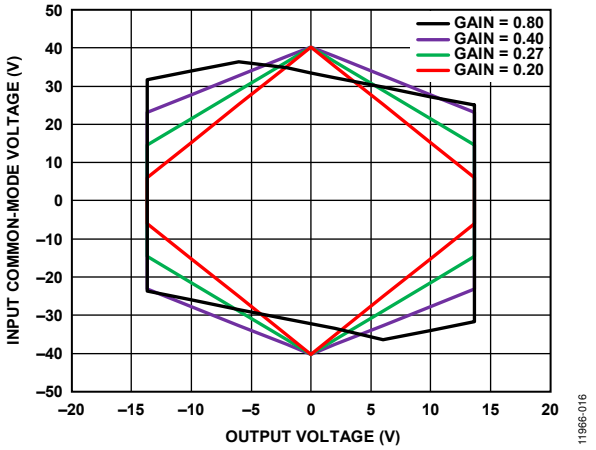

Figure 18. Input Common-Mode Voltage vs. Output Voltage for AVCC = +15 V and AVEE = −15 V

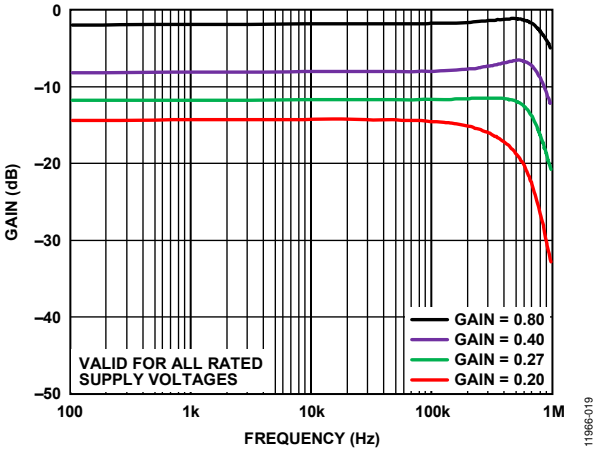

Figure 16. Gain vs. Frequency

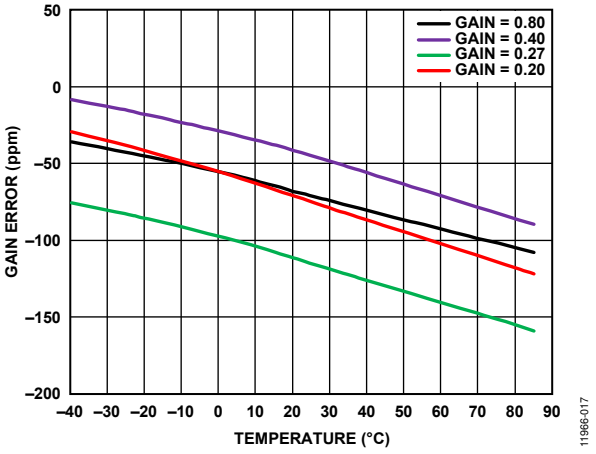

Figure 19. Gain Error vs. Temperature

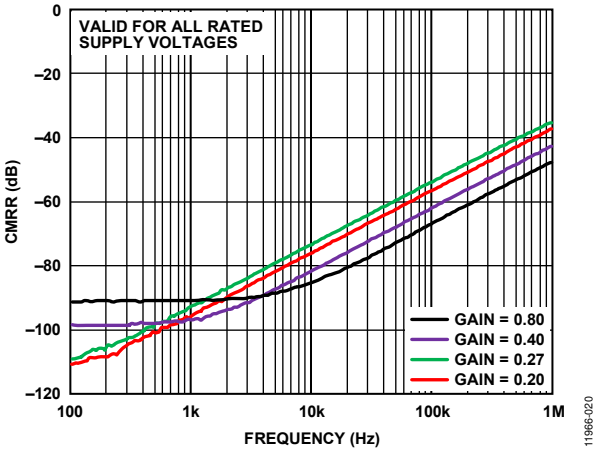

Figure 17. CMRR vs. Frequency

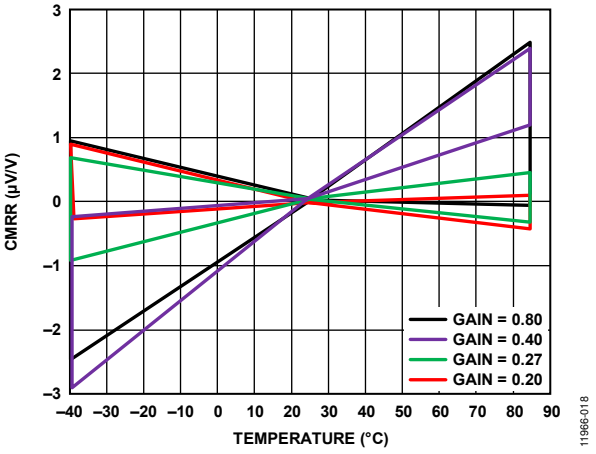

Figure 20. Normalized CMRR vs. Temperature

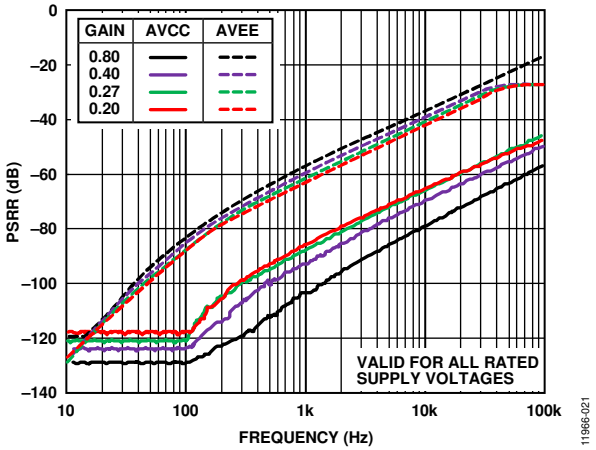

Figure 21. PSRR vs. Frequency

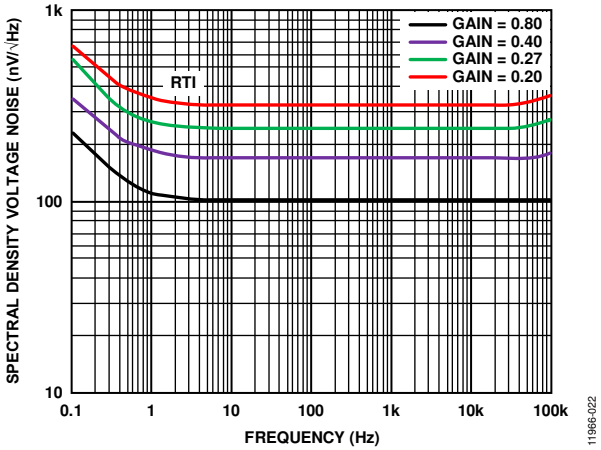

Figure 22. Spectral Density Voltage Noise, RTI vs. Frequency

CC AND CV LOOP FILTER AMPLIFIERS, UNCOMMITTED OP AMP, AND VSET BUFFER

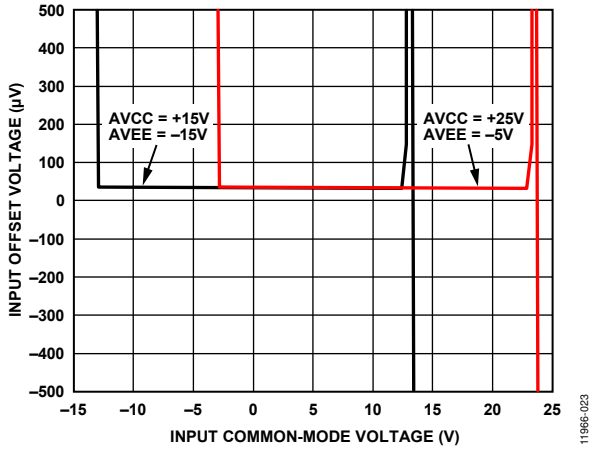

Figure 23. Input Offset Voltage vs. Input Common-Mode Voltage for Two Supply Voltage Combinations

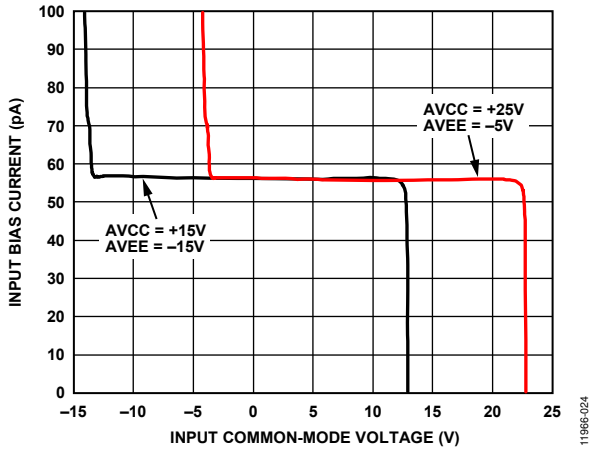

Figure 24. Input Bias Current vs. Input Common-Mode Voltage for Two Supply Voltage Combinations

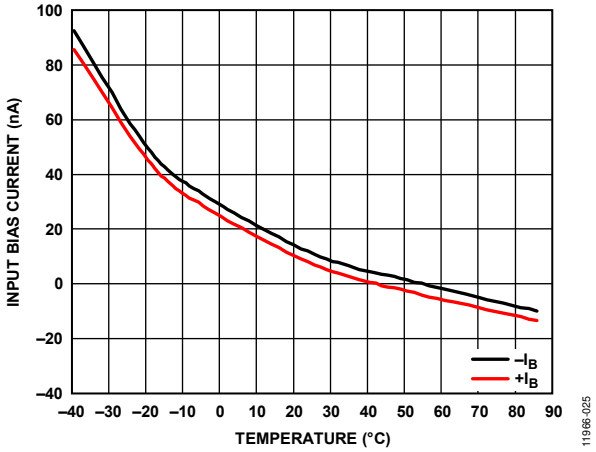

Figure 25. Input Bias Current vs. Temperature

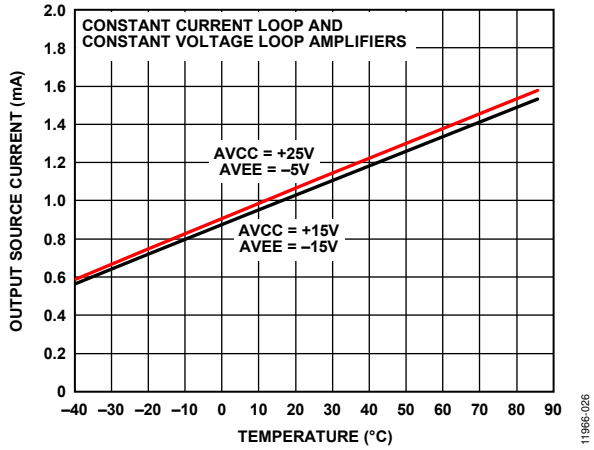

Figure 26. Output Source Current vs. Temperature for Two Supply Voltage Combinations

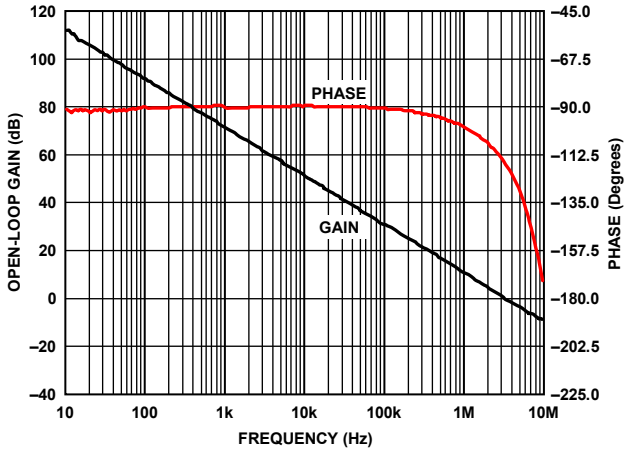

Figure 27. Open-Loop Gain and Phase vs. Frequency

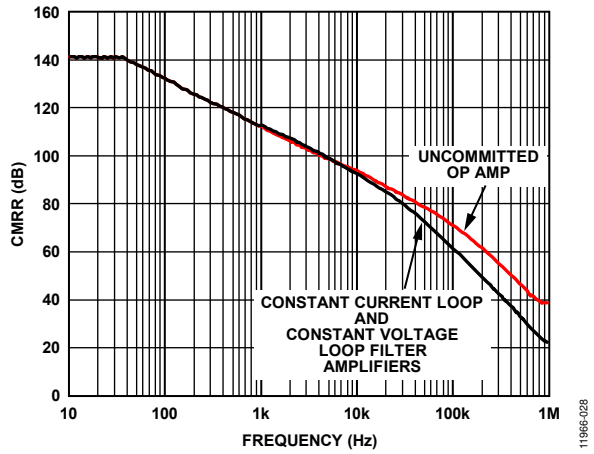

Figure 28. CMRR vs. Frequency

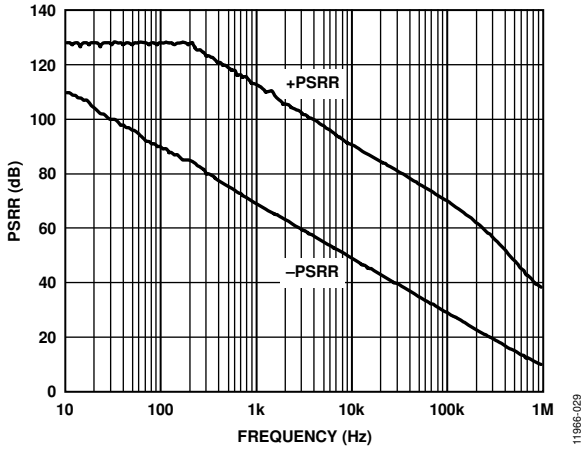

Figure 29. PSRR vs. Frequency

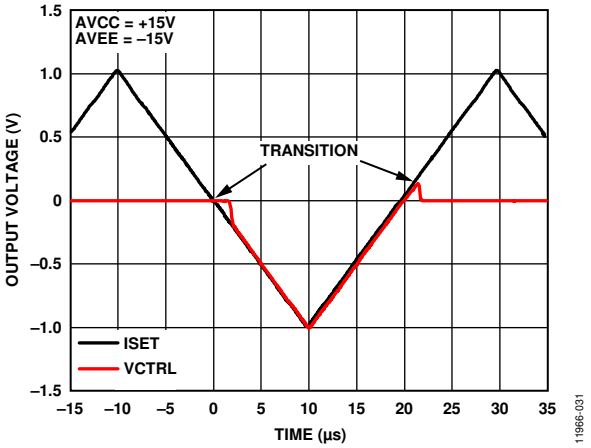

Figure 31. CC to CV Transition

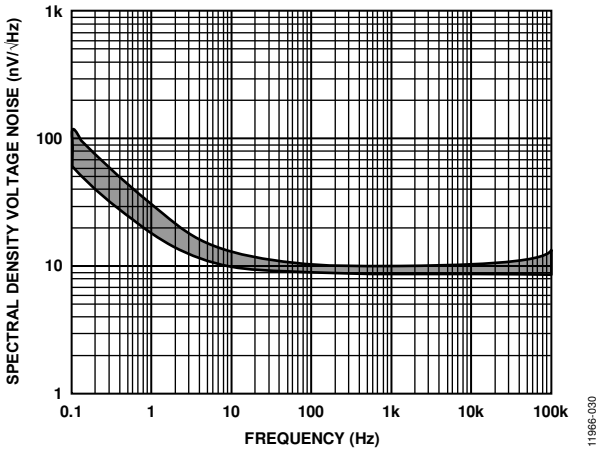

Figure 30. Range of Spectral Density Voltage Noise vs. Frequency for the Op Amps and Buffers

VINT BUFFER

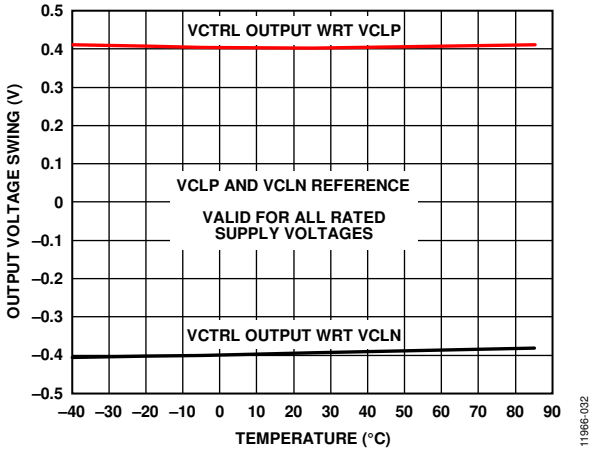

Figure 32. Output Voltage Swing with Respect to VCLP and VCLN vs. Temperature

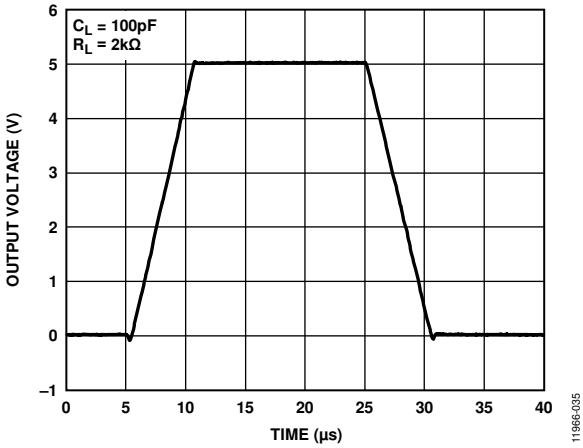

Figure 35. Large Signal Transient Response, R_L = 2 kΩ, C_L = 100 pF

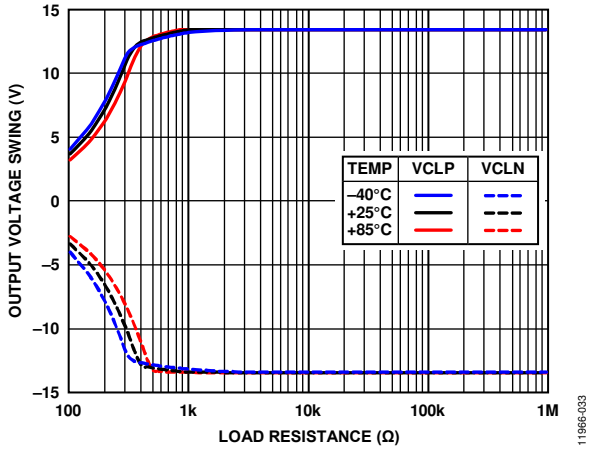

Figure 33. Output Voltage Swing vs. Load Resistance at Three Temperatures

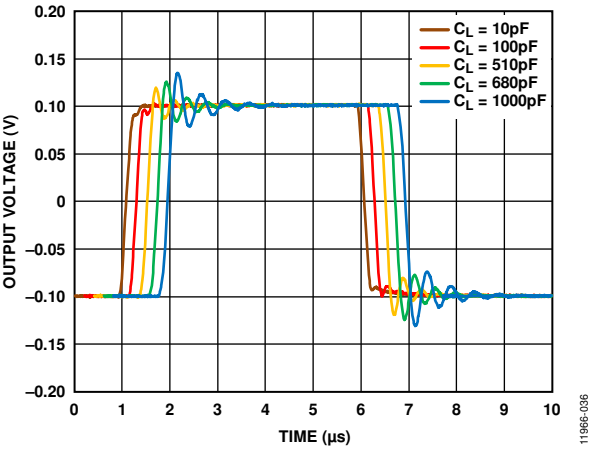

Figure 36. Small Signal Transient Response vs. Capacitive Load

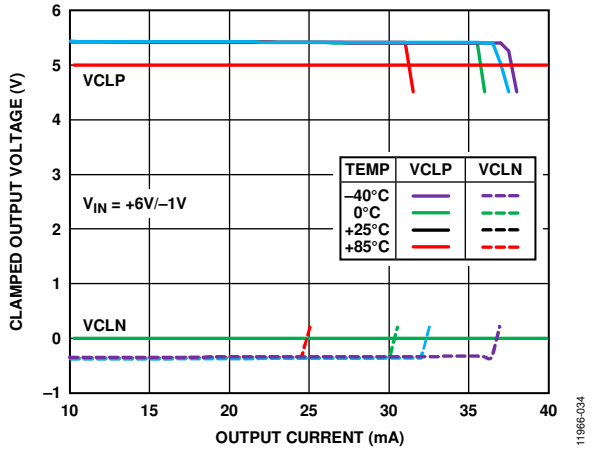

Figure 34. Clamped Output Voltage vs. Output Current at Four Temperatures

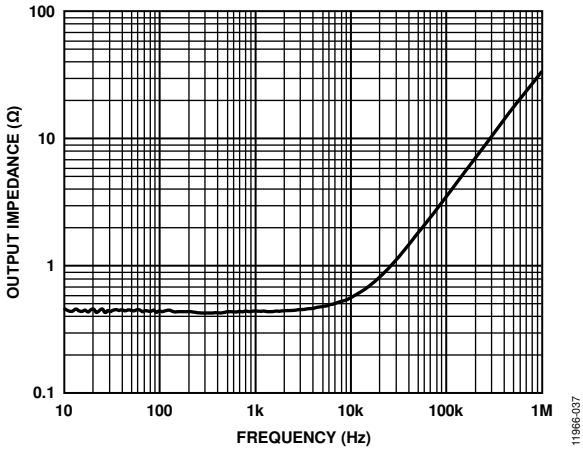

Figure 37. Output Impedance vs. Frequency

CURRENT SHARING AMPLIFIER

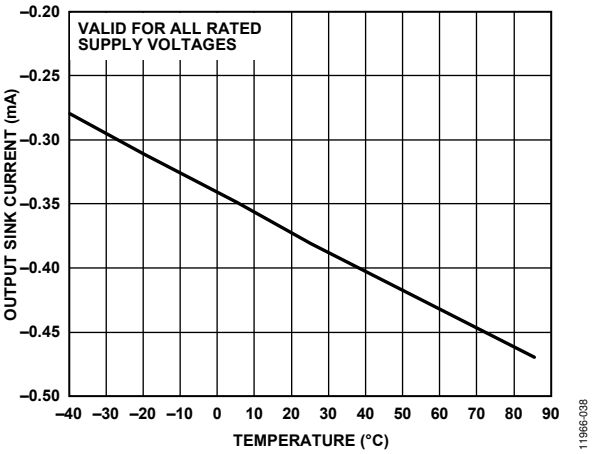

Figure 38. Output Sink Current vs. Temperature

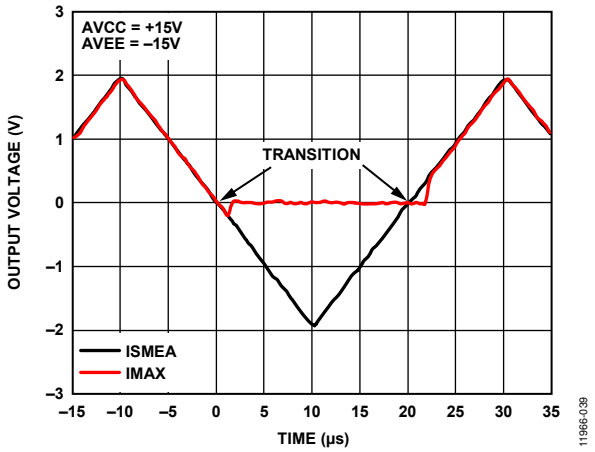

Figure 39. Current Sharing Bus Transition Characteristics

COMPARATORS

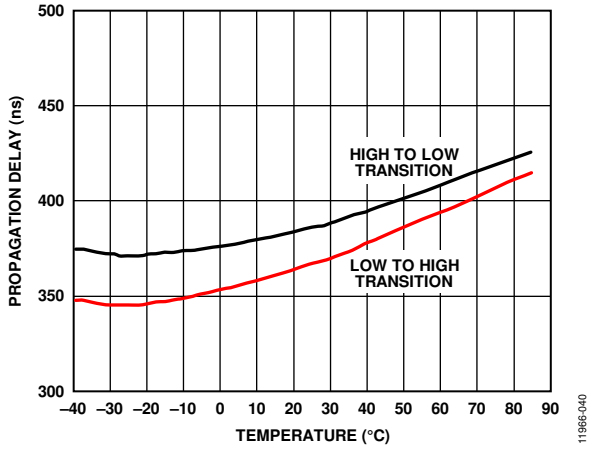

Figure 40. Propagation Delay vs. Temperature

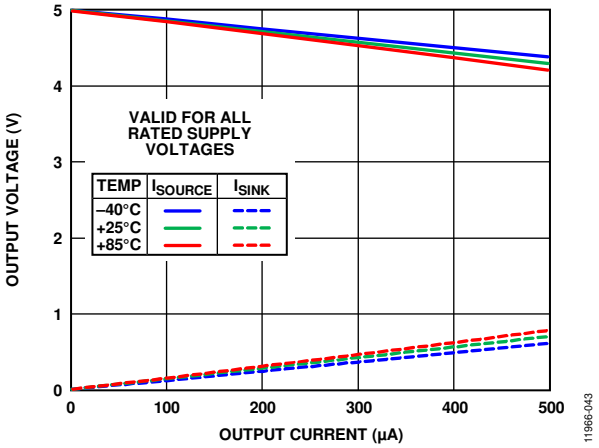

Figure 43. Output Voltage vs. Output Current at Three Temperatures

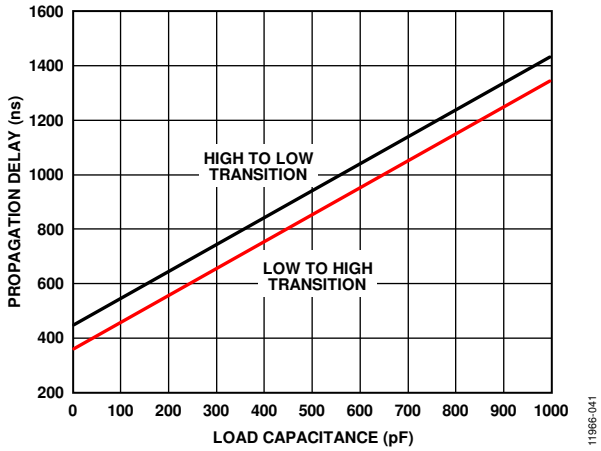

Figure 41. Propagation Delay vs. Load Capacitance

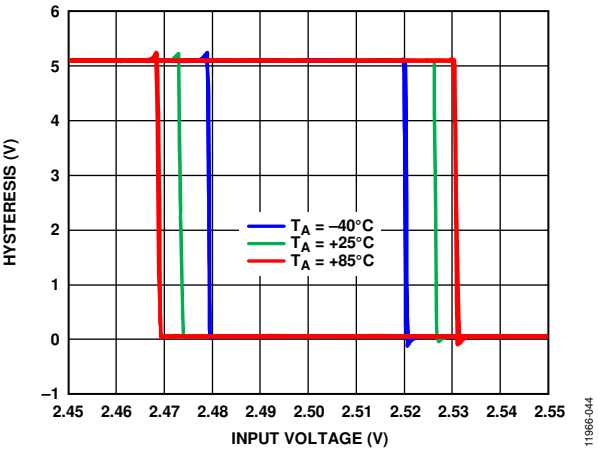

Figure 44. Comparator Transfer Function at Three Temperatures

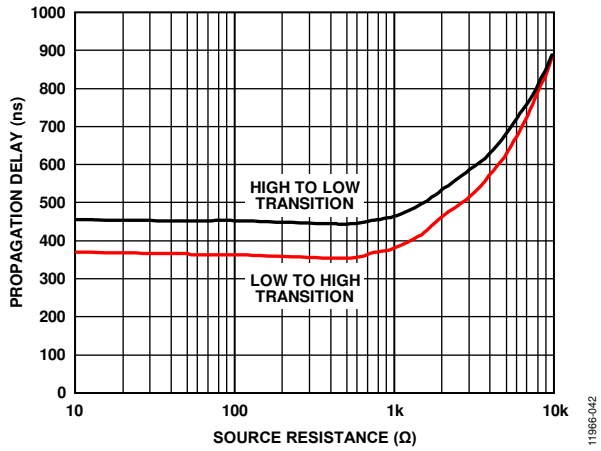

Figure 42. Propagation Delay vs. Source Resistance

REFERENCE CHARACTERISTICS

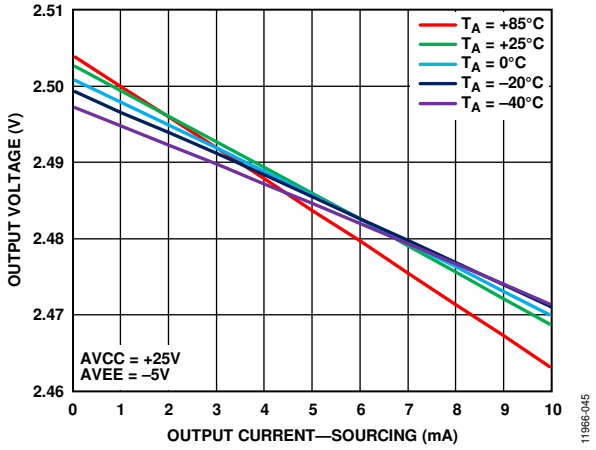

Figure 45. Output Voltage vs. Output Current (Sourcing) over Temperature

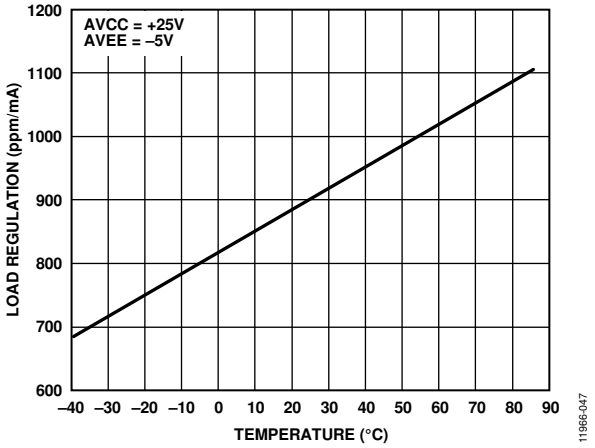

Figure 47. Source and Sink Load Regulation vs. Temperature

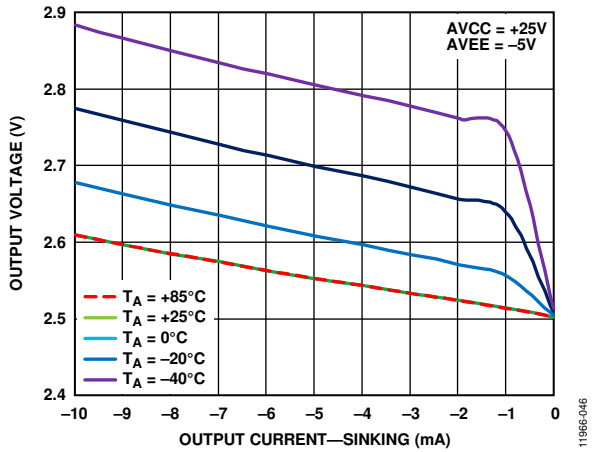

Figure 46. Output Voltage vs. Output Current (Sinking) over Temperature

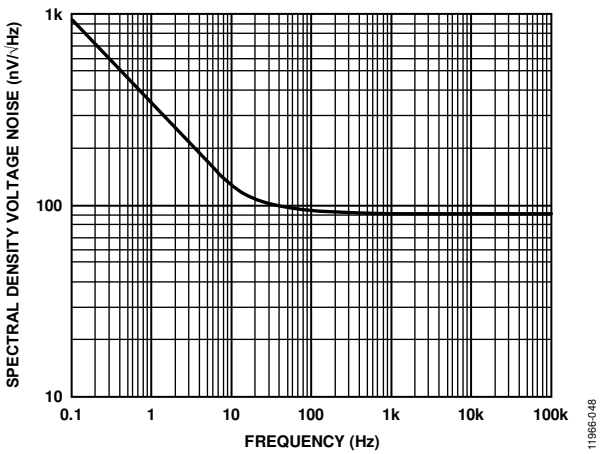

Figure 48. Spectral Density Voltage Noise vs. Frequency

THEORY OF OPERATION

INTRODUCTION

To form and test a battery, the battery must undergo charge and discharge cycles. During these cycles, the battery terminal current and voltage must be precisely controlled to prevent battery failure or a reduction in the capacity of the battery. Therefore, battery formation and test systems require a high precision analog front end to monitor the battery current and terminal voltage.

The analog front end of the AD8450 includes a precision current sense programmable gain instrumentation amplifier (PGIA) to measure the battery current, and a precision voltage sense programmable gain difference amplifier (PGDA) to measure the battery voltage. The gain programmability of the PGIA allows the system to set the battery charge/discharge current to any of four discrete values with the same shunt resistor. The gain programmability of the PGDA allows the system to handle up to four batteries in series (4S).

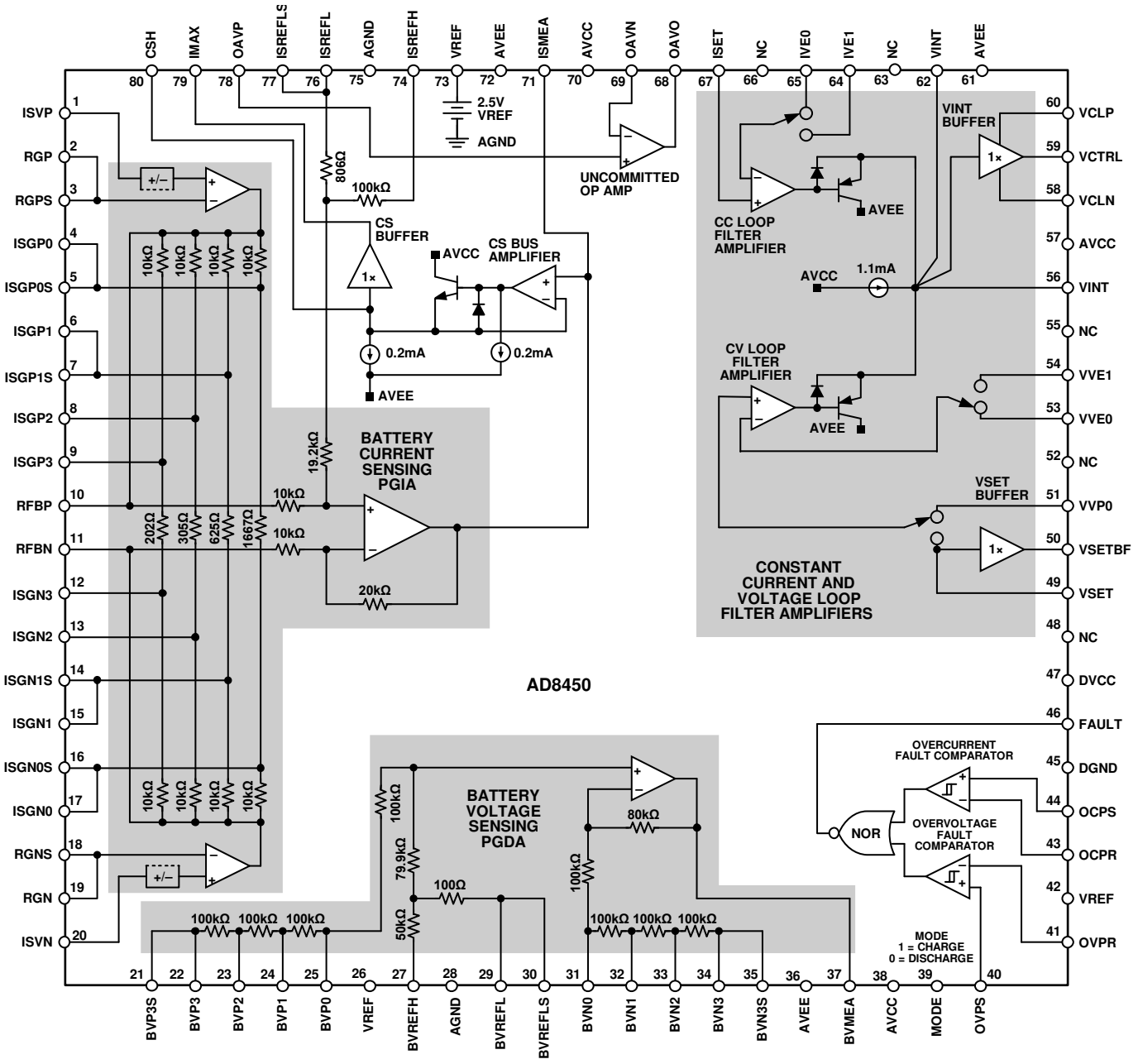

Figure 49. AD8450 Detailed Block Diagram

Battery formation and test systems charge and discharge batteries using a constant current/constant voltage (CC/CV) algorithm. In other words, the system first forces a set constant current in or out of the battery until the battery voltage reaches a target value. At this point, a set constant voltage is forced across the battery terminals.

The AD8450 provides two control loops—a constant current (CC) loop and a constant voltage (CV) loop—that transition automatically after the battery reaches the user defined target voltage. These loops are implemented via two precision specialty amplifiers with external feedback networks that set the transfer function of the CC and CV loops. Moreover, in the AD8450, these loops reconfigure themselves to charge or discharge the battery by toggling the MODE pin.

Battery formation and test systems must also be able to detect overvoltage and overcurrent conditions in the battery to prevent damage to the battery and/or the control system.

The AD8450 includes two comparators to detect overcurrent and overvoltage events. These comparators output a logic low at the FAULT pin when either comparator is tripped.

Battery formation and test systems used to condition high current battery cells often employ multiple independent channels to charge or discharge high currents to or from the battery. To maximize efficiency, these systems benefit from circuitry that enables precise current sharing (or balancing) among the channels—that is, circuitry that actively matches the output current of each channel. The AD8450 includes a specialty precision amplifier that detects the maximum output current among several channels by identifying the channel with the maximum voltage at its PGIA output. This maximum voltage can then be compared to all the PGIA output voltages to actively adjust the output current of each channel.

Figure 49 is a block diagram of the AD8450 that illustrates the distinct sections of the AD8450, including the PGIA and PGDA measurement blocks, the loop filter amplifiers, the fault comparators, and the current sharing circuitry. Figure 50 is a block diagram of a battery formation and test system.

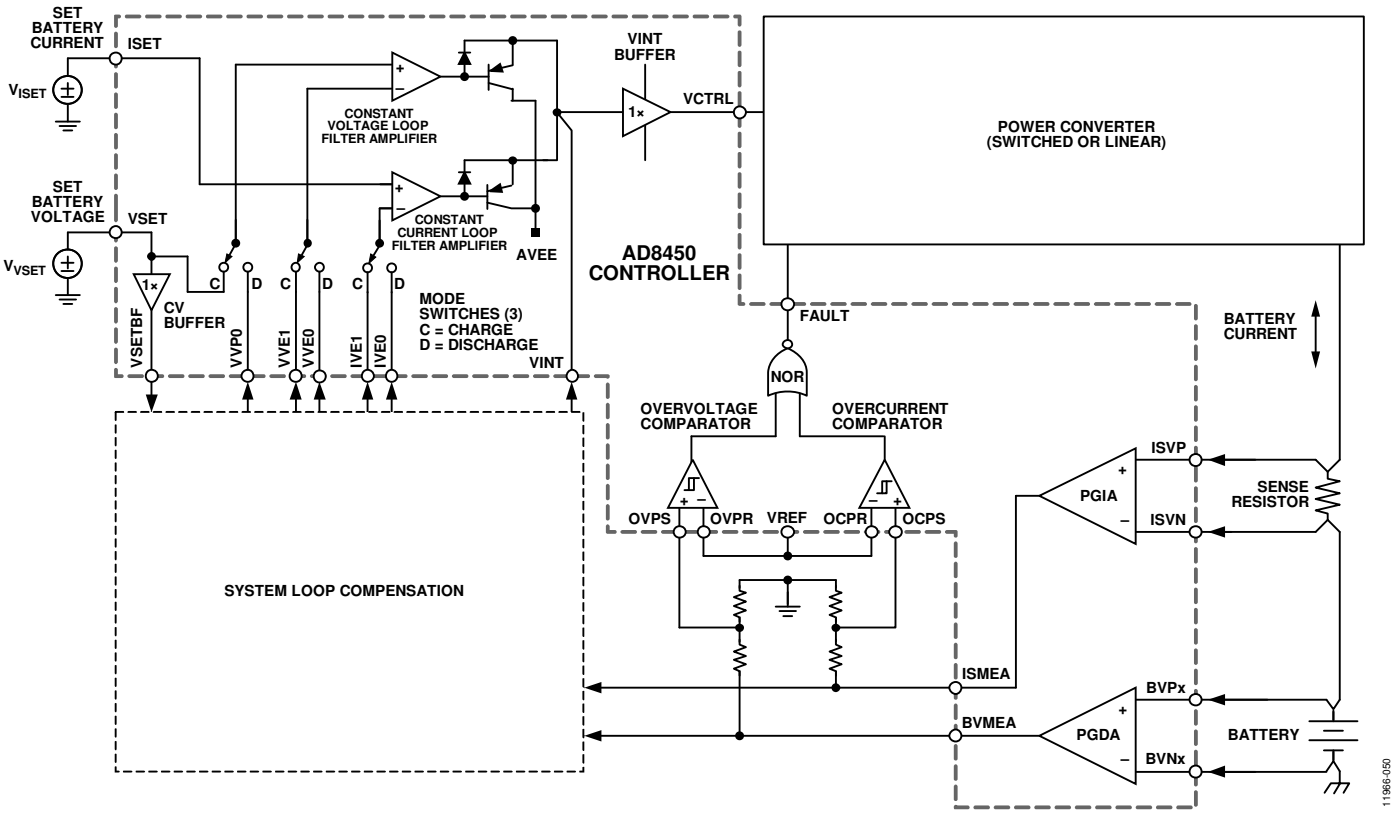

Figure 50. Signal Path of a Li-Ion Battery Formation and Test System Using the AD8450

PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER (PGIA)

Figure 51 is a block diagram of the PGIA, which is used to monitor the battery current. The architecture of the PGIA is the classic 3-op-amp topology, similar to the Analog Devices industry-standard AD8221 and AD620. This architecture provides the highest achievable CMRR at a given gain, enabling high-side battery current sensing without the introduction of significant errors in the measurement. For more information about instrumentation amplifiers, see *A Designer's Guide to Instrumentation Amplifiers*.

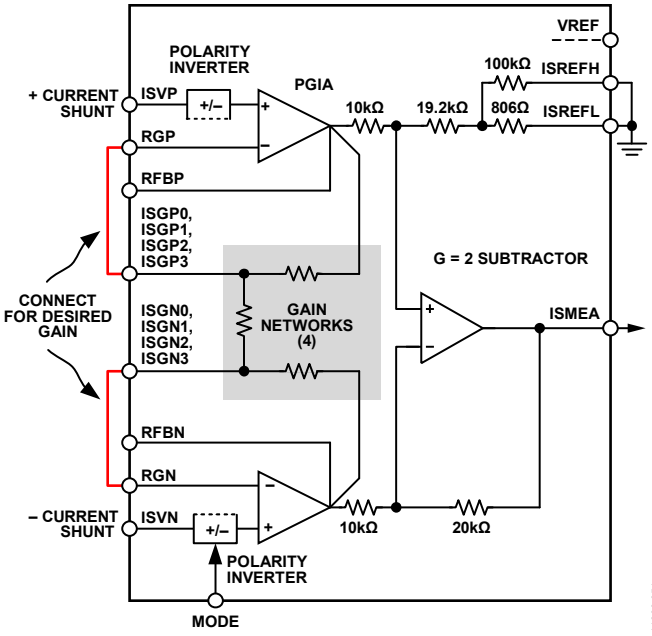

Figure 51. PGIA Simplified Block Diagram

Gain Selection

The PGIA includes four fixed internal gain options. The PGIA can also use an external gain network for arbitrary gain selection. The internal gain options are established via four independent three-resistor networks, which are laser trimmed to a matching level better than ±0.1%. The internal gains are optimized to minimize both PGIA gain error and gain error drift, allowing the controller to set a stable charge/discharge current over temperature. If the built in internal gains are not adequate, the PGIA gain can be set via an external three-resistor network.

The internal gains of the PGIA are selected by tying the inverting inputs of the PGIA preamplifiers (RGP and RGN pins) to the corresponding gain pins of the internal three-resistor network (ISGP[0:3] and ISGN[0:3] pins). For example, to set the PGIA gain to 26, tie the RGP pin to the ISGP0 pin, and tie the RGN pin to the ISGN0 pin. See Table 5 for information about the gain selection connections.

The external PGIA gain is set by tying 10 kΩ feedback resistors between the inverting inputs of the PGIA preamplifiers (RGP and RGN pins) and the outputs of the PGIA preamplifiers (RFBP and RFBN pins) and by tying a gain resistor (R_G) between the RGP and RGN pins. When using external resistors, the PGIA gain is

$$Gain = 2 \times (1 + 20\ k\Omega/R_G)$$

Note that the PGIA subtractor has a closed-loop gain of 2 to increase the common-mode range of the preamplifiers.

Reversing Polarity When Charging and Discharging

Figure 50 shows that during the charge cycle, the power converter feeds current into the battery, generating a positive voltage across the current sense resistor. During the discharge cycle, the power converter draws current from the battery, generating a negative voltage across the sense resistor. In other words, the battery current polarity reverses when the battery discharges.

In the constant current (CC) control loop, this change in polarity can be problematic if the polarity of the target current is not reversed. To solve this problem, the AD8450 PGIA includes a multiplexer preceding its inputs that inverts the polarity of the PGIA gain. This multiplexer is controlled via the MODE pin. When the MODE pin is logic high (charge mode), the PGIA gain is noninverting, and when the MODE pin is logic low (discharge mode), the PGIA gain is inverting.

PGIA Offset Option

As shown in Figure 51, the PGIA reference node is connected to the ISREFL and ISREFH pins via an internal resistor divider. This resistor divider can be used to introduce a temperature insensitive offset to the output of the PGIA such that the PGIA output always reads a voltage higher than zero for a zero differential input. Because the output voltage of the PGIA is always positive, a unipolar ADC can digitize it.

When the ISREFH pin is tied to the VREF pin with the ISREFL pin grounded, the voltage at the ISMEA pin is increased by 20 mV, guaranteeing that the output of the PGIA is always positive for zero differential inputs. Other voltage shifts can be realized by tying the ISREFH pin to an external voltage source. The gain from the ISREFH pin to the ISMEA pin is 8 mV/V. For zero offset, tie the ISREFL and ISREFH pins to ground.

Battery Reversal and Overvoltage Protection

The AD8450 PGIA can be configured for high-side or low-side current sensing. If the PGIA is configured for high-side current sensing (see Figure 50) and the battery is connected backward, the PGIA inputs may be held at a voltage that is below the negative power rail (AVEE), depending on the battery voltage.

To prevent damage to the PGIA under these conditions, the PGIA inputs include overvoltage protection circuitry that allows them to be held at voltages of up 55 V from the opposite power rail. In other words, the safe voltage span for the PGIA inputs extends from AVCC − 55 V to AVEE + 55 V.

PROGRAMMABLE GAIN DIFFERENCE AMPLIFIER (PGDA)

Figure 52 is a block diagram of the PGDA, which is used to monitor the battery voltage. The architecture of the PGDA is a subtractor amplifier with four selectable inputs: the BVP[0:3] and BVN[0:3] pins. Each input pair corresponds to one of the internal gains of the PGDA: 0.2, 0.27, 0.4, and 0.8. These gain values allow the PGDA to funnel the voltage of up to four 5 V batteries in series (4S) to a level that can be read by a 5 V ADC. See Table 6 for information about the gain selection connections.

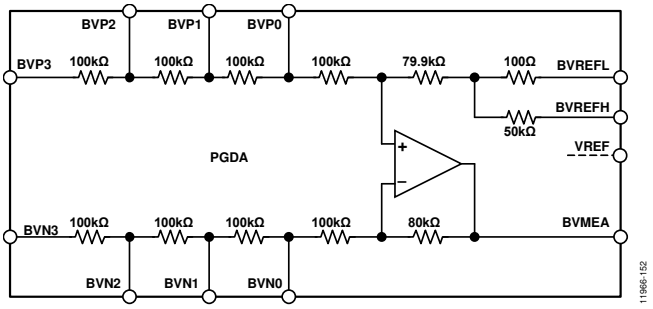

Figure 52. PGDA Simplified Block Diagram

The resistors that form the PGDA gain network are laser trimmed to a matching level better than ±0.1%. This level of matching minimizes the gain error and gain error drift of the PGDA while maximizing the CMRR of the PGDA. This matching also allows the controller to set a stable target voltage for the battery over temperature while rejecting the ground bounce in the battery negative terminal.

Like the PGIA, the PGDA can also level shift its output voltage via an internal resistor divider that is tied to the PGDA reference node. This resistor divider is connected to the BVREFH and BVREFL pins.

When the BVREFH pin is tied to the VREF pin with the BVREFL pin grounded, the voltage at the BVMEA pin is increased by 5 mV, guaranteeing that the output of the PGDA is always positive for zero differential inputs. Other voltage shifts can be realized by tying the BVREFH pin to an external voltage source. The gain from the BVREFH pin to the BVMEA pin is 2 mV/V. For zero offset, tie the BVREFL and BVREFH pins to ground.

CC AND CV LOOP FILTER AMPLIFIERS

The constant current (CC) and constant voltage (CV) loop filter amplifiers are high precision, low noise specialty amplifiers with very low offset voltage and very low input bias current. These amplifiers serve two purposes:

- Using external components, the amplifiers implement active loop filters that set the dynamics (transfer function) of the CC and CV loops.
- The amplifiers perform a seamless transition from CC to CV mode after the battery reaches its target voltage.

Figure 53 is the functional block diagram of the AD8450 CC and CV feedback loops for charge mode (MODE pin is logic high). For illustration purposes, the external networks connected to the loop amplifiers are simple RC networks configured to form single-pole inverting integrators. The outputs of the CC and CV loop filter amplifiers are coupled to the VINT pin via an analog NOR circuit (minimum output selector circuit), such that they can only pull the VINT node down. In other words, the loop amplifier that requires the lowest voltage at the VINT pin is in control of the node. Thus, only one loop amplifier, CC or CV, can be in control of the system charging control loop at any given time.

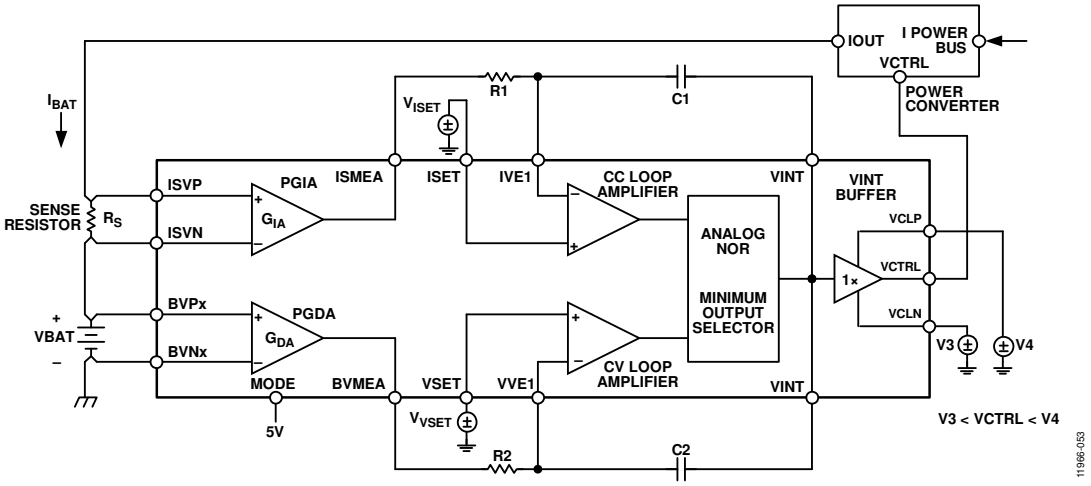

Figure 53. Functional Block Diagram of the CC and CV Loops in Charge Mode (MODE Pin High)