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## Evaluation Board for Zero-Drift, Digitally Programmable Sensor Signal Amplifier

### FEATURES

- Single- or dual-supply operation
- AC and DC signal evaluation
- Built-in 100  $\Omega$  bridge with unbalancing capability
- Provision to create low-pass filter
- Readback feature of programmed values
- External clamp voltage setting
- Interface for PC USB port
- Evaluation software, compatible with Microsoft Windows XP, Windows Vista, and Windows 7
- SOIC/LFCSP socket for easy device replacement
- Supports [AD8555](#), [AD8556](#), and [AD8557](#) ICs

### EQUIPMENT NEEDED

- [AD8556-EVALZ/AD8556CP-EBZ](#) evaluation board
- Analog Devices, Inc., System Demonstration Platform (SDP)
  - SDP-S ([EVAL-SDP-CS1Z](#)) or SDP-B ([EVAL-SDP-CB1Z](#))
- USB cable (included with SDP board)
- Power supplies
- Voltage source
- Voltmeter
- BNCs and power cables
- PC running Windows XP, Windows Vista, or Windows 7

### GENERAL DESCRIPTION

This user guide describes the evaluation board hardware and software used to evaluate the [AD8555](#), [AD8556](#), and [AD8557](#) in SOIC and LFCSP packages. The [AD8556-EVALZ/AD8556CP-EBZ](#) evaluation boards allow the quick demonstration and evaluation of the [AD8555/AD8556/AD8557](#) zero-drift, digitally programmable sensor signal amplifiers.

The [AD8555/AD8556/AD8557](#) are auto-zero instrumentation amplifiers with programmable gain and output offset adjustment features. The evaluation board enables a PC to communicate with the [AD8555/AD8556/AD8557](#). The user can send commands to the evaluation board and read back the programmed values for the device that is being evaluated.

This user guide supplements the information in the [AD8555](#), [AD8556](#), and [AD8557](#) data sheets, which should be consulted in conjunction with this user guide when working with the evaluation board.

### EVALUATION BOARD CONNECTION DIAGRAM

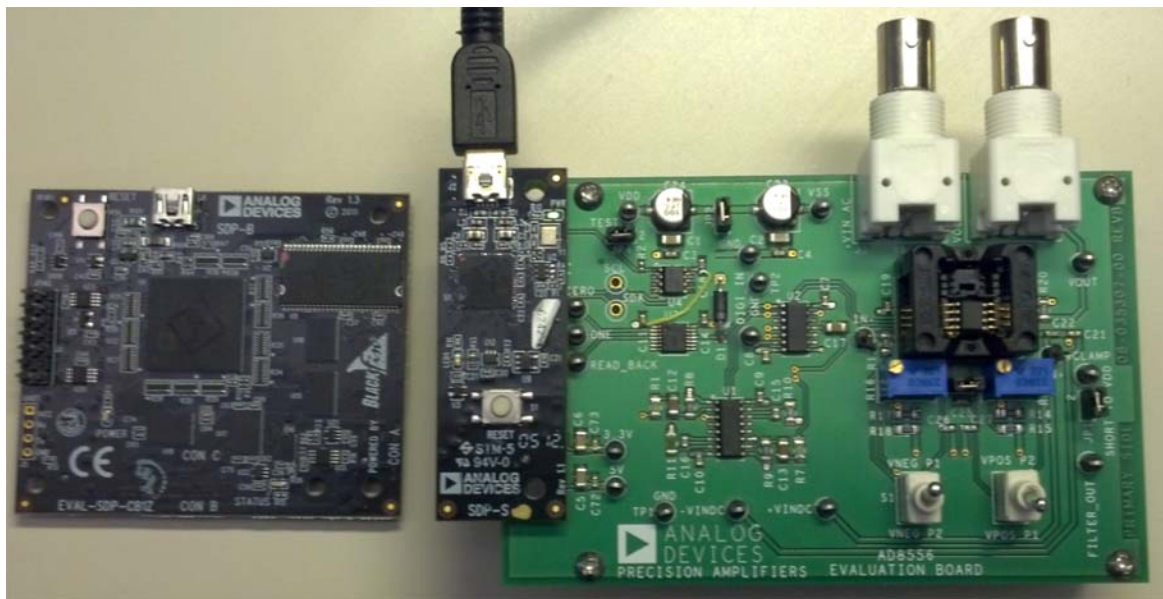


Figure 1. SDP-S board Connected to the [AD8556-EVALZ](#) Board (SDP-B Board Also Shown for Reference)

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**REVISION HISTORY**

**11/15—Rev. 0 to Rev. A**

Updated Layout.....	Universal
Added AD8556CP-EBZ.....	Universal
Added Equipment Needed Section .....	1
Changes to General Description Section .....	1
Changes to Quick Initial Hardware Setup and Output Verification Section and Figure 2 .....	4
Added Figure 12.....	8
Deleted Ordering Guide Section .....	9

**10/13—Revision 0: Initial Version**

## HARDWARE DESCRIPTION

The AD8556-EVALZ/AD8556CP-EBZ evaluation boards are designed for maximum configuration flexibility. An ac signal can be applied to  $+V_{IN}$  ac, and the output can be monitored from  $V_{OUT}$  ac. DC signals can be differentially applied between  $+V_{IN}$  dc and  $-V_{IN}$  dc, and the results can be monitored using a voltmeter at  $V_{OUT}$ . Users can view the filter output signal at the FILT/DIGOUT pin. The board also allows swapping of the polarity of the inputs using the  $V_{NEG}$  P1 and  $V_{POS}$  P1 switches.

Four resistors (R1A, R1B, R2A, and R2B) simulate a 100  $\Omega$  bridge configuration. The bridge can be unbalanced using the provided trim potentiometers (P1 and P2). The top and bottom of the bridge are connected to VDD and VSS, respectively.

Pulse shaping is performed on this board before applying the data to the AD8556-EVALZ data input pin. The pulse widths are set for 5  $\mu$ s, representing the low level (0 V), and 80  $\mu$ s, representing the high level (>2.4 V). This adjustment is made using Resistor RT0 and Resistor RT1. The trim potentiometers are glued to their fixed positions.

Supply current can be monitored by using a resistor in place of R7. Clamp voltage can be applied externally to a level or can be set easily to  $V_{DD}$  by placing a jumper from VCLAMP to VDD. The SOIC/LFCSP socket is soldered for easy programming and removal of the device. Pin 1 is the pin located in the upper left-hand corner of the socket close to R7. Make sure that the device is placed in the socket properly. See Figure 11 for the evaluation board schematic.

## SYSTEM REQUIREMENTS

The evaluation kit has the following system requirements:

- Analog Devices, Inc., SDP-B or SDP-S system demonstration platform (SDP) controller board (available for purchase separately at [www.analog.com/SDP](http://www.analog.com/SDP))
- PC with available USB 2.0 port
- Microsoft® Windows® operating system with administrator access

## COMMUNICATING WITH THE EVALUATION BOARD

The evaluation board connects to the Analog Devices SDP-B or SDP-S board, which connects to the USB port of a PC.

Ensure that the evaluation software provided on the CD is installed before connecting the SDP board and the evaluation board.

## HARDWARE REQUIREMENTS

The following equipment is required:

- Power supplies
- Voltage source
- Voltmeter
- BNCs and power cables
- SDP board with USB mini-B cable

## ADJUSTING FOR 0 V DIFFERENTIAL INPUT

Prior to initial hardware setup and output verification, complete the following to adjust for differential input offset:

1. Connect the positive input (high) of a voltmeter to  $-V_{IN}$  dc.
2. Connect the negative input (low) of the voltmeter to GND of the power supply.
3. Monitor the output ( $V_{OUT}$  dc) voltmeter.
4. Adjust trim Potentiometer P1 to be close to 0 V ( $-0.1$  mV).
5. Connect the positive input (high) of a voltmeter to  $+V_{IN}$  dc.
6. Connect the negative input (low) of the voltmeter to GND of the power supply.
7. Monitor the output ( $V_{OUT}$  dc) voltmeter.
8. Adjust trim Potentiometer P2 to be close to 0 V (0.1 mV).

**QUICK INITIAL HARDWARE SETUP AND OUTPUT VERIFICATION**

For an initial hardware setup and output verification, follow these steps:

1. Connect the evaluation board to the SDP board, which connects to the USB port of your PC system using a USB mini-B cable.
2. Position manual switches to  $V_{POS}$  P2 and  $V_{NEG}$  P2.
3. Jumper the VCLAMP connector pin to the VDD connector pin.

4. Apply 10 mV dc signal between the  $+V_{IN}$  dc and  $-V_{IN}$  dc connectors, and monitor the  $V_{OUT}$  dc output using a voltmeter.
5. Place an AD8555/AD8556/AD8557 device in the SOIC/LFCSP socket, connect the VCLAMP pin to the VDD pin, and apply dc power to the board using an external power supply ( $\pm 2.5$  V).

When this procedure is complete, the output is 70 mV, with the board in this configuration consuming approximately 4 mA.

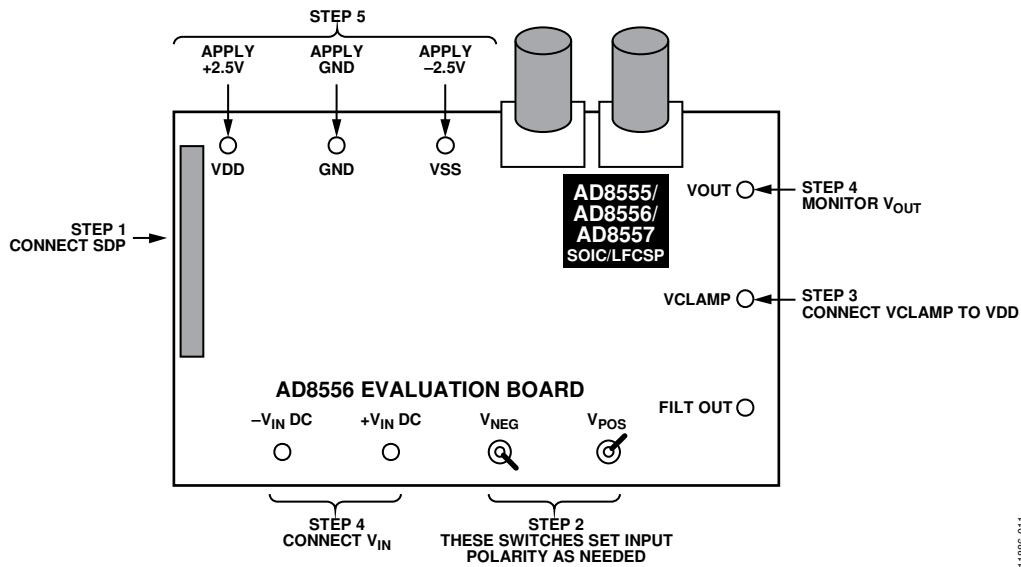


Figure 2. Evaluation Board Block Diagram

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## SOFTWARE INSTALLATION

To install the evaluation software on the PC,

1. Insert the CD-ROM into the CD drive on your PC. After a few moments, a message for the installation appears.
2. Double-click **setup.exe**. (For Windows® 7 onwards, right-click and select **Install** as a system administrator.)
3. Follow the instructions until the software installation is complete.

The evaluation software is developed in LabVIEW®. The software requires a LabVIEW® runtime engine and USB drivers for the SDP (both included in install). Install the software with administrator access, before plugging in the SDP board. The install detects if the SDP board has been installed previously.

The default install location is **C:\Program Files (x86)\Analog Devices\AD855x**.

For the most current data sheet, visit [www.analog.com/AD8555](http://www.analog.com/AD8555), [www.analog.com/AD8556](http://www.analog.com/AD8556) or [www.analog.com/AD8557](http://www.analog.com/AD8557).

## REMOVING THE EVALUATION SOFTWARE

To remove the evaluation software modules,

1. Go to **Start > Settings > Control Panel**.
2. Double-click **Add/Remove Programs** and select **AD855x Evaluation Software**.

## RUNNING THE SOFTWARE

To run the evaluation software application:

1. After the SDP board is plugged into the PC via the USB cable and into the **AD8556-EVALZ/AD8556CP-EBZ** evaluation board via the P1 socket, run the evaluation software. From the **Start** menu, click **AD855x Eval**, and then click **AD855xEVAL**. The graphical user interface (GUI) opens.
2. Select the product for which you have samples and the connector used, and then click **Start**.
3. Set the appropriate gain and offset values, and then click **Simulate**. Monitor the output as the offset is changed to verify communication.
4. Program the gain between 70 and 1280 and the offset between 0 V and 5 V. Click **Simulate** to load these values into the **AD8556-EVALZ/AD8556CP-EBZ** and monitor the output.
5. The output is  $\text{input} \times \text{gain}$  and responds to the specified configuration.
6. After the **AD8556-EVALZ/AD8556CP-EBZ** has been simulated to the final values, click **Program** to permanently blow the internal fuses to the values in the GUI.

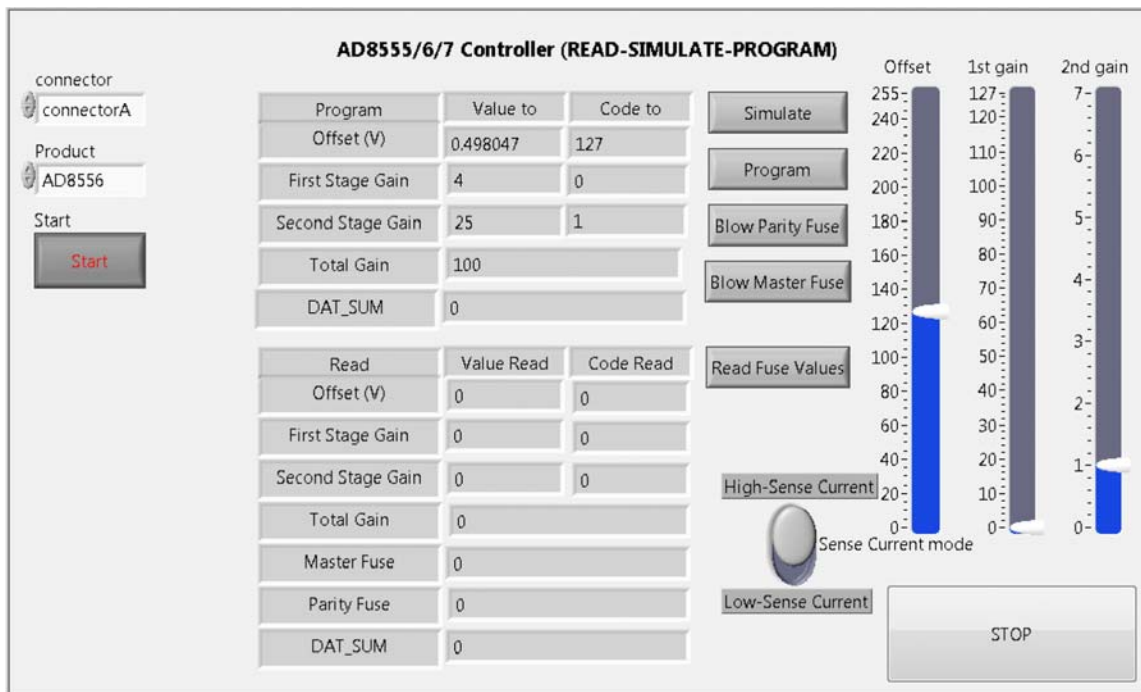


Figure 3. No Programming Dialog Box

Table 1. Evaluation Software Dialog Box Button Functions

Button	Function
Start	Select the connector and the product, and then click <b>Start</b> to begin evaluation.
Connector	Selects the physical connector on the SDP board that is used to connect to the evaluation board. The connectors are labeled on the top silkscreen of the SDP board.
Product	Selects the device under evaluation.
Simulate	Configures the device according to the specified pattern. This button does not blow any fuses.
Program	Blows fuses according to the specified pattern. Blown fuses cannot be reprogrammed.
Blow Parity Fuse	Blows the parity fuse. The parity fuse keeps track of the state of the blown fuses. If, for any reason, the state of this fuse is changed either intentionally or unintentionally, the parity flag is set and the alarm is set.
Blow Master Fuse	Permanently sets the device to the programmed gain and offset and prevents future programming. Click this button only after selecting and programming the gain and the offset. Prior to blowing the master fuse, make sure to first blow the parity fuse, if prompted.
Read Fuse Values	Reads back the state of the programmed fuses after they have been blown. The options are as follows: Low sense current: when dropped across a blown fuse (high impedance), creates a voltage that can trigger an internal comparator and provide the right level in the output. High sense current: reads back the fuse states to make sure that the fuses are blown. A code for blown fuses appears in a pop-up box.

See the [AD8555/AD8556/AD8557](#) data sheet for more information on the theory of operation; simulation, programming, and read modes; and parity error detection. The [AD8555/AD8556/AD8557](#) data sheet also contains more information on programming procedures for the device.

**TYPICAL AC SETUP AND RESPONSE**

**AC Input Example**

Setup requirements are as follows:

- Power supplies
- Function generator
- Scope
- BNCs and cables

**Results**

When the device is powered with  $\pm 2.5$  V, and 50 mV of input is applied, the default conditions are

- $V_{CC} = 2.5$  V
- $V_{SS} = -2.5$  V
- Gain 1 = 4
- Gain 2 = 17.5
- Offset =  $V_{SS}$

The overall gain is 70.

When the switches are placed in  $V_{NEG}$  P1 and  $V_{POS}$  P2, there is one set of outputs. When the switches are changed to  $V_{NEG}$  P2 and  $V_{POS}$  P1, the exact voltage is produced, but with the opposite polarity.

When both switches are on one side (for example,  $V_{NEG}$  P1 and  $V_{POS}$  P1), the inputs are shorted together.

RT0 and RT1 are the trim potentiometers used for pulse width shaping. Do not change their settings. RT0 is adjusted to create a 5  $\mu$ s pulse; RT1 is adjusted to create an 80  $\mu$ s pulse.

Figure 4 shows the output on Channel 2 under these conditions and configuration.

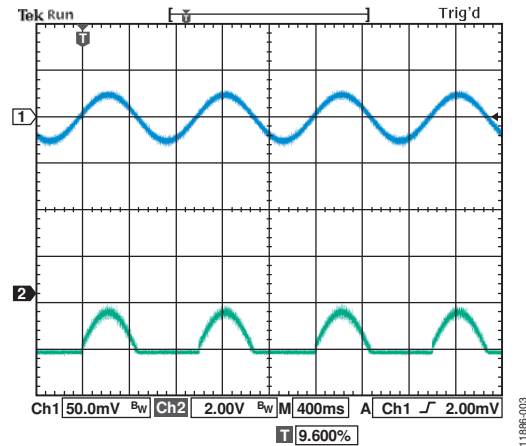


Figure 4. Output on Channel 2

Figure 5 shows the results of the previous conditions with  $V_{OFF} = 2.5$  V or Code 128.

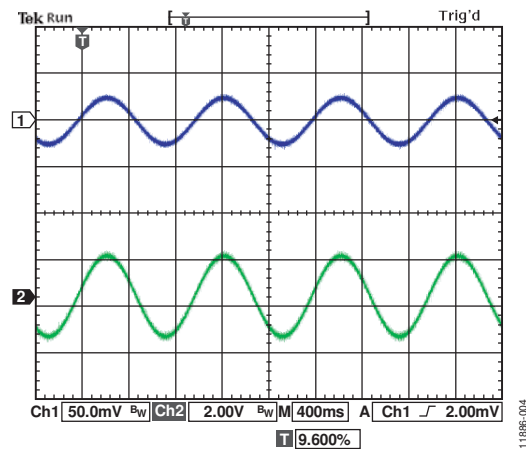


Figure 5. Output on Channel 2,  $V_{OFF} = 2.5$  V

In Figure 6, overall gain = 100 ( $G1 = \text{default} = 4$ ,  $G2 = \text{Code } 1 = 25$ , offset = 2.5 V or Code 128).

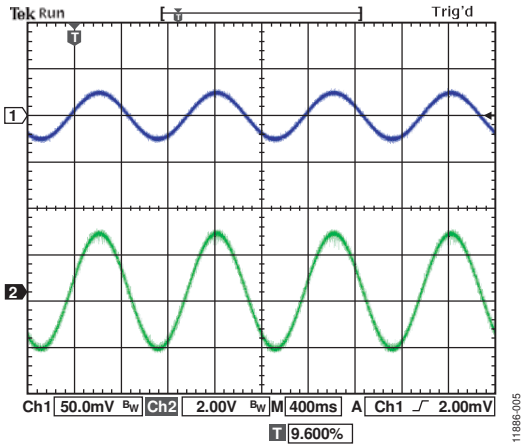


Figure 6. Output with Overall Gain = 100

In Figure 7,  $V_{IN} = 2 \text{ mV p-p}$ ,  $G1 = 6.4$ ,  $G2 = 35$ , and offset = 2.5 V or Code 128.

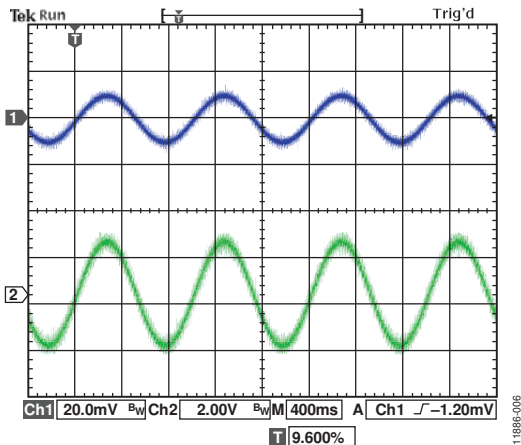


Figure 7. Output at  $V_{IN} = 2 \text{ mV p-p}$ ,  $G1 = 6.4$ ,  $G2 = 35$ , Offset = 2.5 V

### OUTPUT CLAMP FEATURE

The output of the device can be clamped to the desired level. The output clamp feature is provided to protect the circuitry that follows the AD8556-EVALZ, in case the input to AD8556-EVALZ is accidentally larger than anticipated.

In normal situations ( $V_{SUPPLIES} = \pm 2.5 \text{ V}$ , gain = 70,  $V_{OFFSET} = 2.5 \text{ V}$ , input = 40 mV p-p), the response to an input is as shown in Figure 8.

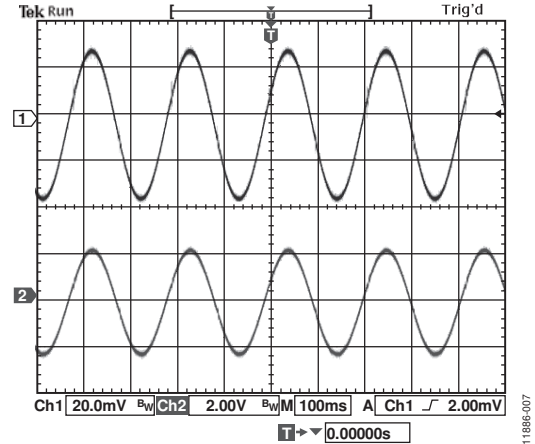


Figure 8. Normal Response

Figure 9 shows the output after VCLAMP is set to 0.8 V.

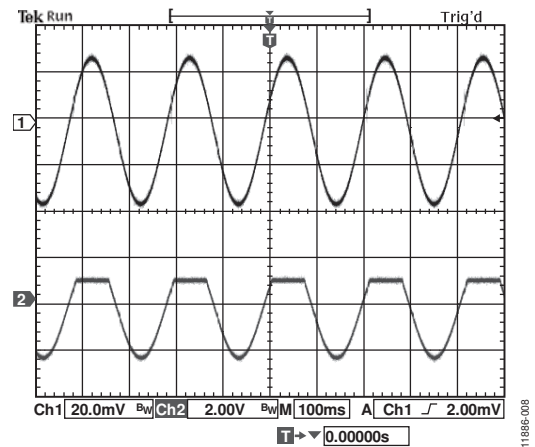


Figure 9. Response with VCLAMP Set

Applying a large gain to an input yields saturation, as shown in Figure 10. The conditions are  $V_{IN} = 20 \text{ mV p-p}$ ,  $G1 = 6.4$ ,  $G2 = 200$ , offset = 2.5 V.

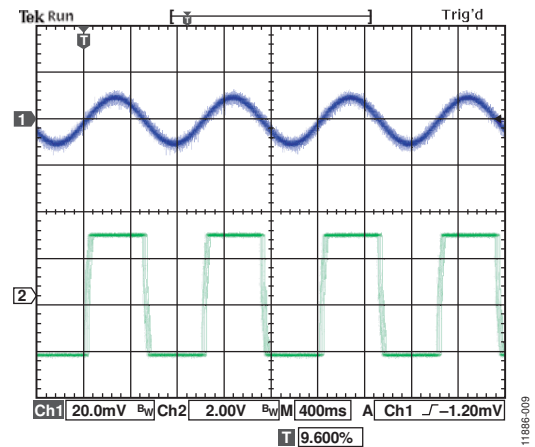


Figure 10. Results with Saturation

Note that Resistor RT1 and Resistor RT2 are used for pulse stretching; do not adjust them. They are factory-adjusted for optimal results.



EVALUATION BOARD SCHEMATICS

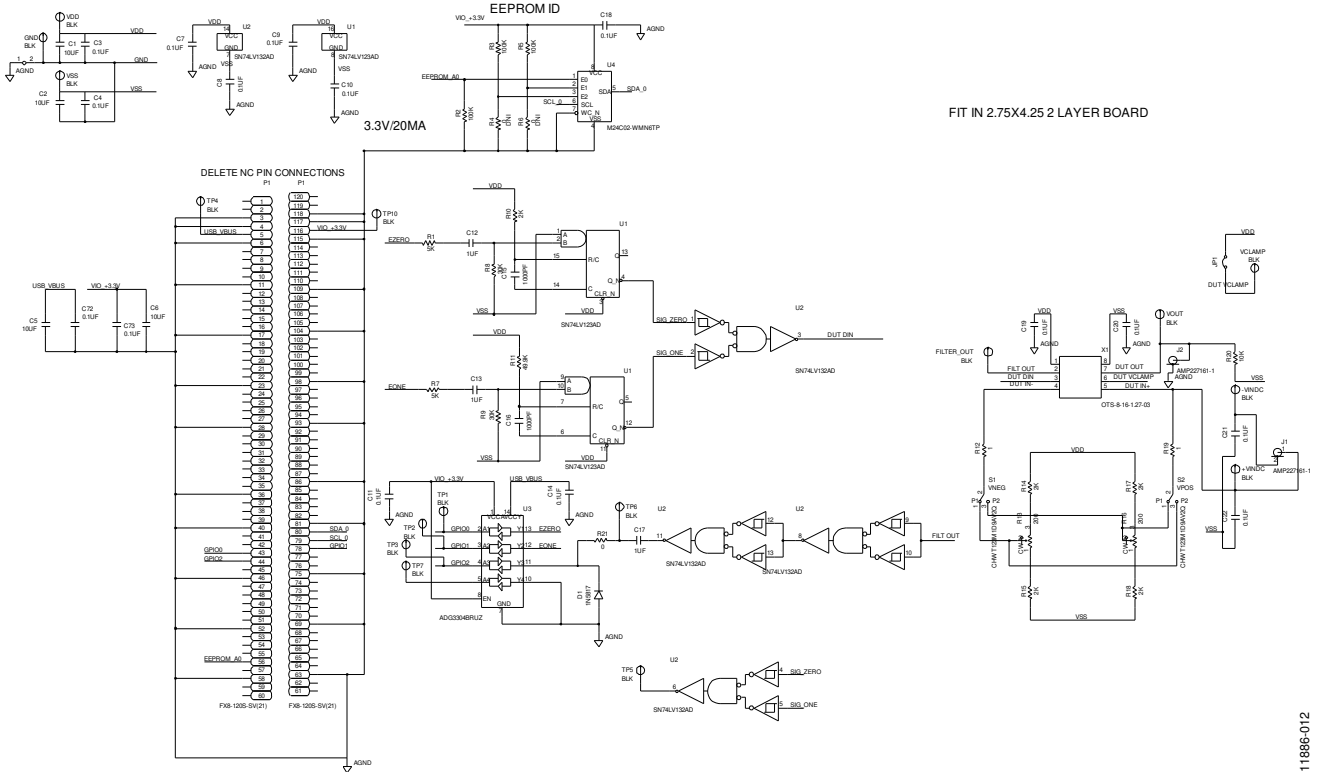


Figure 11. AD8556CP-EBZ Evaluation Board Schematic

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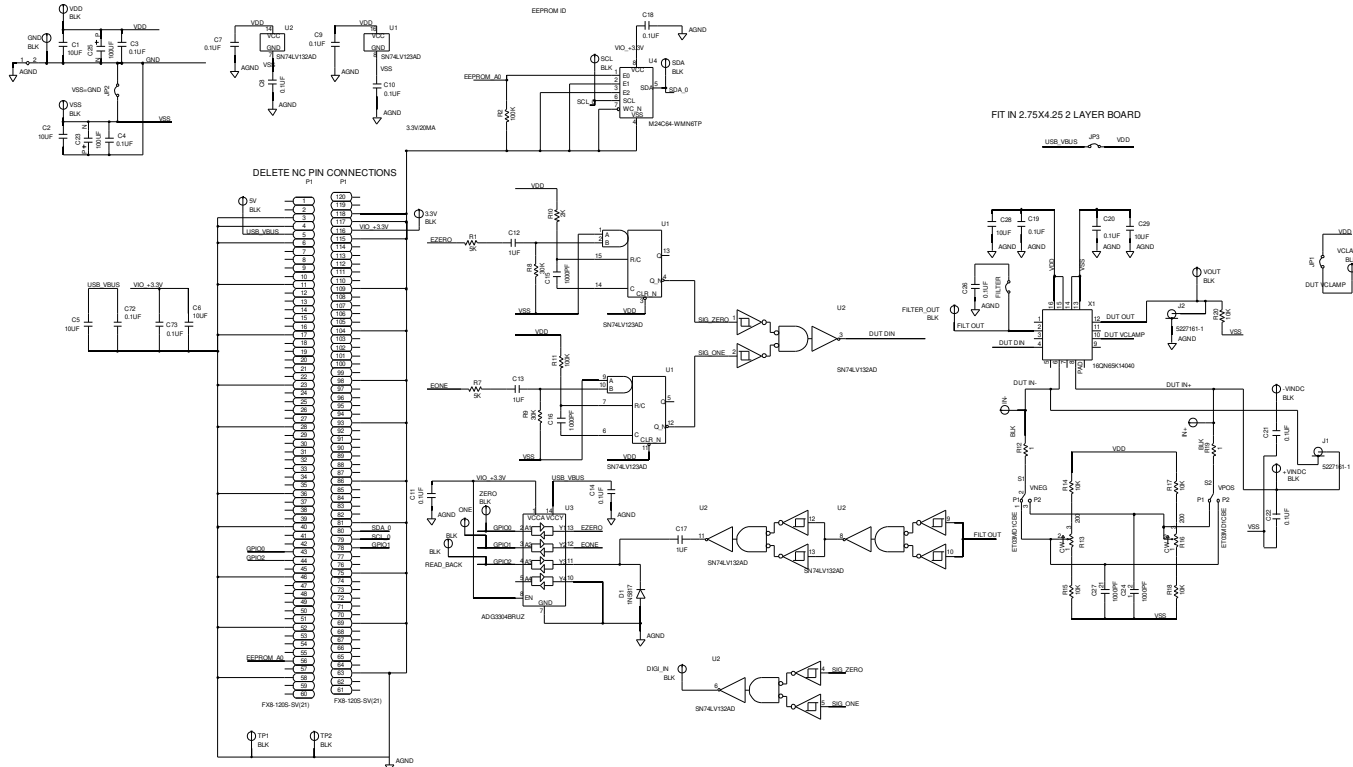


Figure 12. AD8556-EVALZ Evaluation Board Schematic

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## NOTES



### ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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