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Low Power, Rail-to-Rail Output, Precision JFET Amplifiers

Data Sheet

AD8641/AD8642/AD8643

FEATURES

Low supply current: 250 µA max
Very low input bias current: 1 pA max
Low offset voltage: 750 µV max
Single-supply operation: 5 V to 26 V
Dual-supply operation: ±2.5 V to ±13 V
Rail-to-rail output
Unity-gain stable
No phase reversal
SC70 package

APPLICATIONS

Line-/battery-powered instruments
Photodiode amplifiers
Precision current sensing
Medical instrumentation
Industrial controls
Precision filters
Portable audio
ATE

GENERAL DESCRIPTION

The AD8641/AD8642/AD8643 are low power, precision JFET input amplifiers featuring extremely low input bias current and rail-to-rail output. The ability to swing nearly rail-to-rail at the input and rail-to-rail at the output enables designers to buffer complementary metal-oxide semiconductor digital-to-analog converters (CMOS DACs), ASICs, and other wide output swing devices in single-supply systems. The outputs remain stable with capacitive loads of more than 500 pF.

The AD8641/AD8642/AD8643 are suitable for applications utilizing multichannel boards that require low power to manage heat. Other applications include photodiodes, ATE reference level drivers, battery management, and industrial controls.

The AD8641/AD8642/AD8643 are fully specified over the extended industrial temperature range of −40°C to +125°C. The AD8641 is available in 5-lead SC70 and 8-lead SOIC lead-free packages. The AD8642 is available in 8-lead MSOP and 8-lead SOIC lead-free packages. The AD8643 is available in 14-lead SOIC and 16-lead, 3 mm × 3 mm, LFCSP lead-free packages.

PIN CONFIGURATIONS

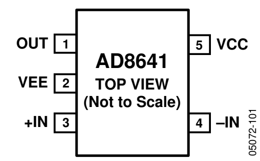

Figure 1. 5-Lead SC70 (KS-5)

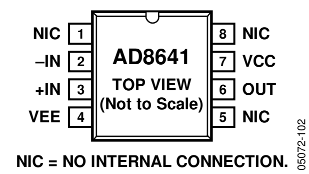

Figure 2. 8-Lead SOIC (R-8)

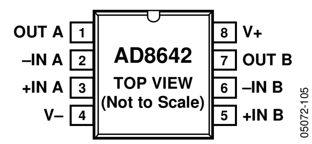

Figure 3. 8-Lead SOIC (R-8)

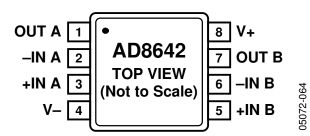

Figure 4. 8-Lead MSOP (RM-8)

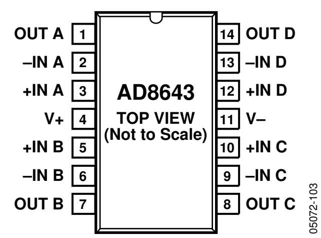

Figure 5. 14-Lead SOIC (R-14)

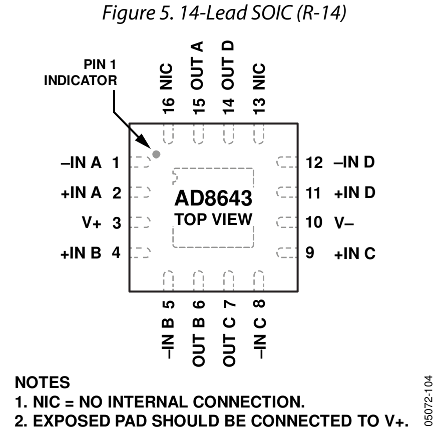

Figure 6. 16-Lead LFCSP (CP-16-27) (Not Drawn to Scale)

Rev. F
Document Feedback

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Tel: 781.329.4700

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10/04—Initial Version: Revision 0

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			50	750	µV
		AD8643 LFCSP only			1	mV
		−40°C < T_A < +85°C			1.5	mV
		+85°C < T_A < +125°C, V_{CM} = 1.5 V			1.6	mV
Input Bias Current	I_B			0.25	1	pA
		−40°C < T_A < +125°C			180	pA
Input Offset Current	I_{OS}				0.5	pA
		−40°C < T_A < +125°C			60	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.5 V	74	93		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 to 4.5 V	80	140		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		2.5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}		4.95			V
		I_L = 1 mA, −40°C to +125°C	4.94			V
Output Voltage Low	V_{OL}				0.05	V
		I_L = 1 mA, −40°C to +125°C		0.01	0.05	V
Output Current	I_{OUT}			±6		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 5 V to 26 V	90	107		dB
Supply Current/Amplifier	I_{SY}			195	250	µA
		−40°C < T_A < +125°C			270	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			2		V/µs
Gain Bandwidth Product	GBP	AD8641, AD8642		3		MHz
		AD8643		2.5		MHz
Phase Margin	$Ø_m$			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		4.0		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		28.5		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.5		fA/√Hz

V_S = ±13 V, V_{CM} = 0 V, T_A =25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			70	750	µV
		AD8643 LFCSP only			1	mV
		−40°C < T_A < +125°C			1.5	mV
Input Bias Current	I_B			0.25	1	pA
		−40°C < T_A < +125°C			260	pA
Input Offset Current	I_{OS}				0.5	pA
		−40°C < T_A < +125°C			65	pA
Input Voltage Range			−13		+10	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −13 V to +10 V	90	107		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = −11 V to +11 V	215	290		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		2.5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}		+12.95			V
		I_L = 1 mA, −40°C to +125°C	+12.94			V
Output Voltage Low	V_{OL}				−12.95	V
		I_L = 1 mA, −40°C to +125°C			−12.94	V
Output Current	I_{OUT}			±12		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±13 V	90	107		dB
Supply Current/Amplifier	I_{SY}			200	290	µA
		−40°C < T_A < +125°C			330	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			3		V/µs
Gain Bandwidth Product	GBP			3.5		MHz
Phase Margin	$Ø_m$			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		4.2		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		27.5		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.5		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	27.3 V
Input Voltage	VS− to VS+
Differential Input Voltage	±Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
KS-5, R-8, RM-8, R-14, CP-16 Packages	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	
KS-5, R-8, RM-8, R-14, CP-16 Packages	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a standard 4-layer board. For the LFCSP, solder the exposed pad to a copper plane, which should be connected to V+.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SC70 (KS)	430	149	°C/W
8-Lead SOIC (R)	121	43	°C/W
8-Lead MSOP (RM)	142	45	°C/W
14-Lead SOIC (R)	110	36	°C/W
16-Lead LFCSP (CP)	81	16	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

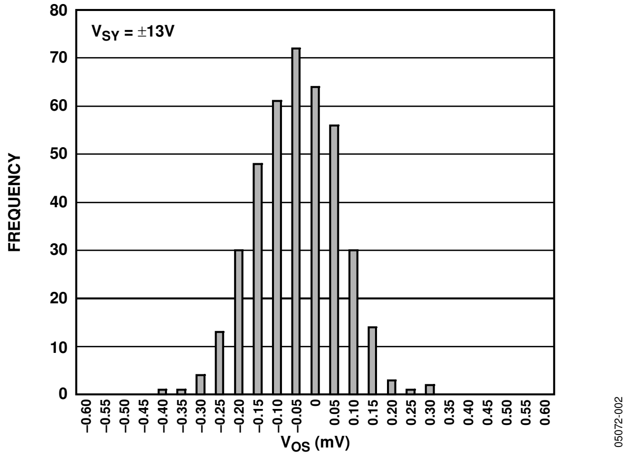
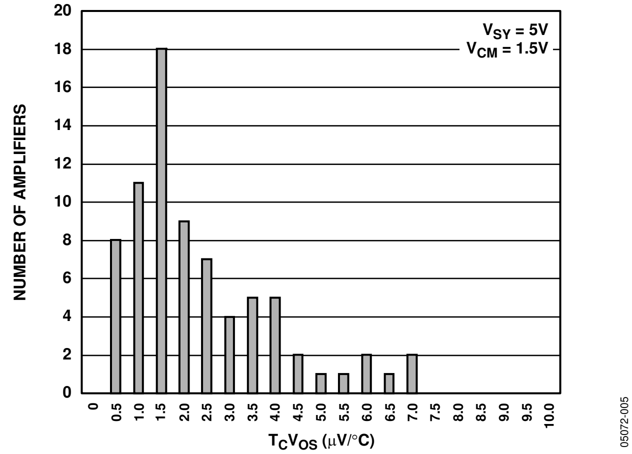


Figure 7. Input Offset Voltage



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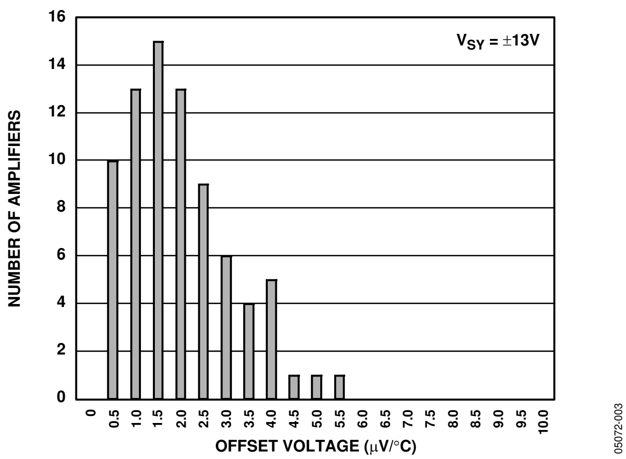

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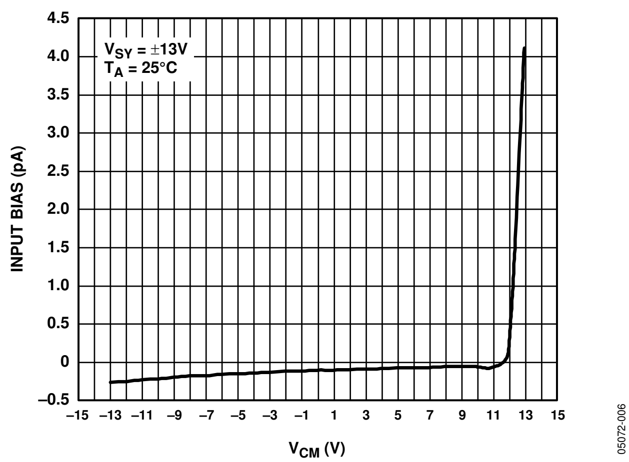

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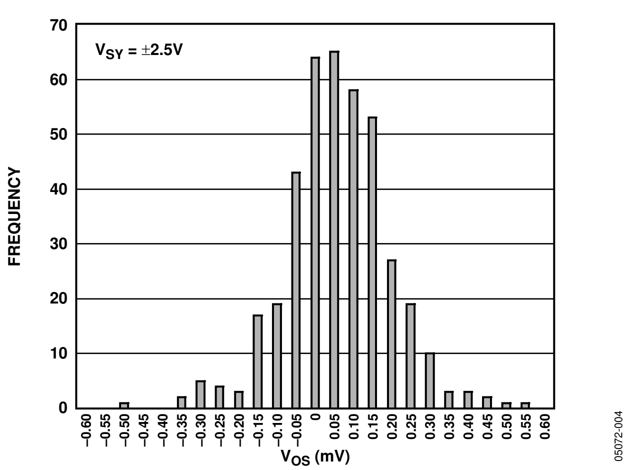

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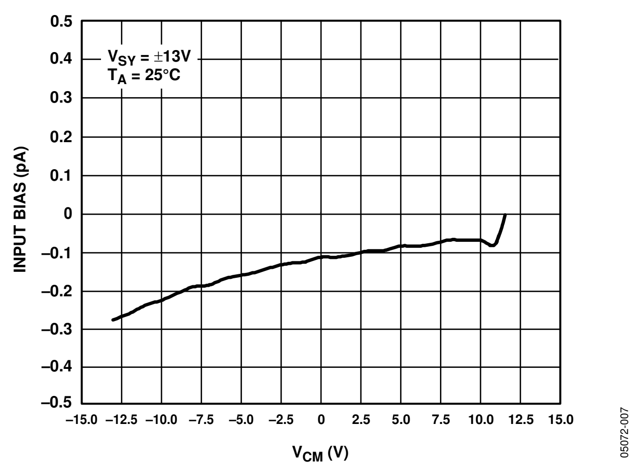

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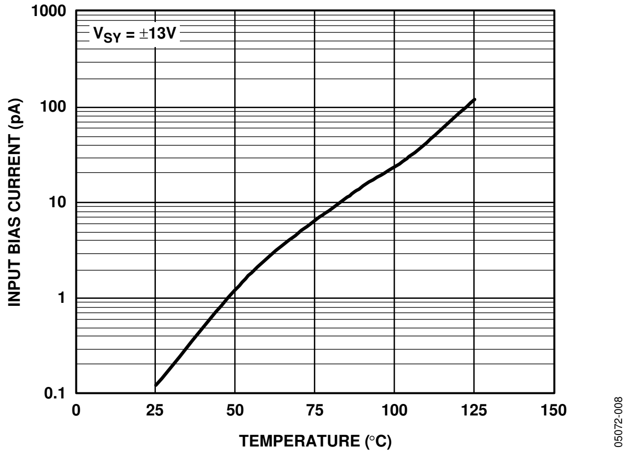

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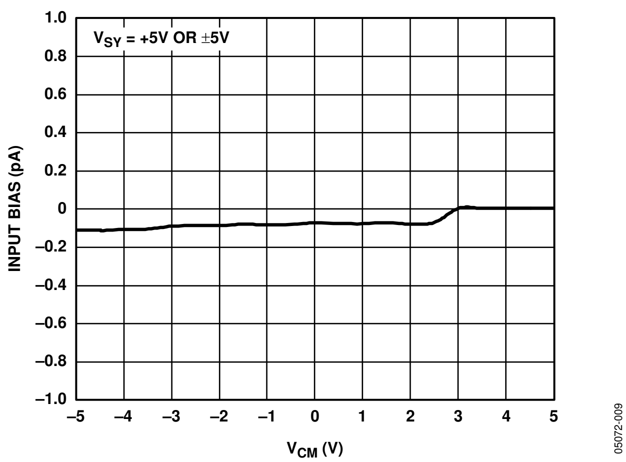

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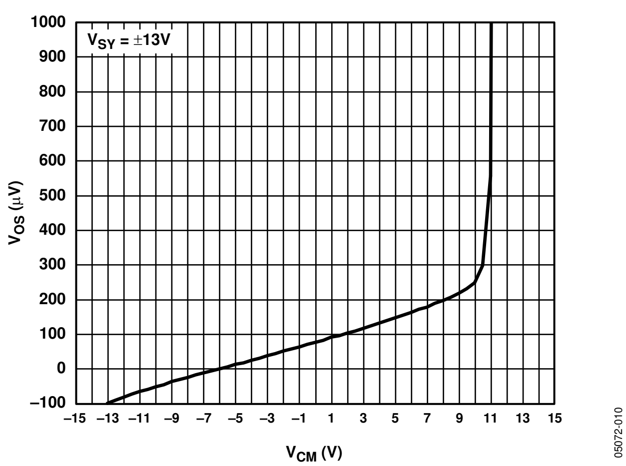

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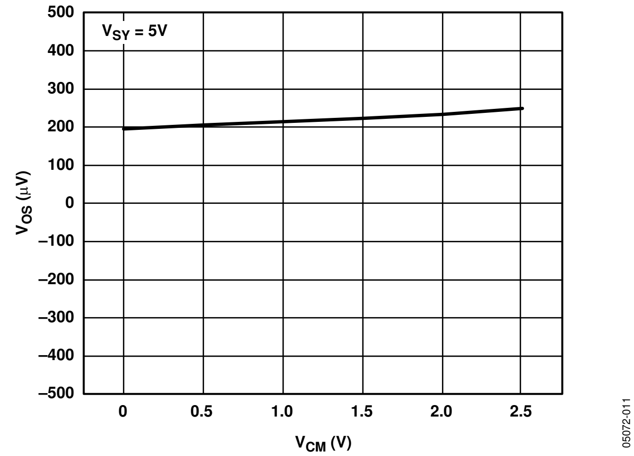

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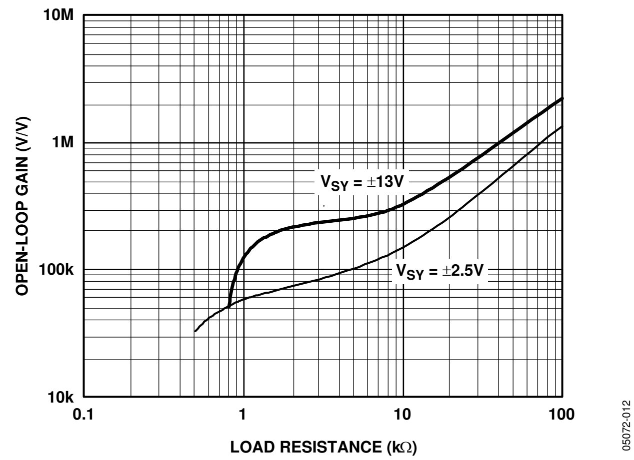

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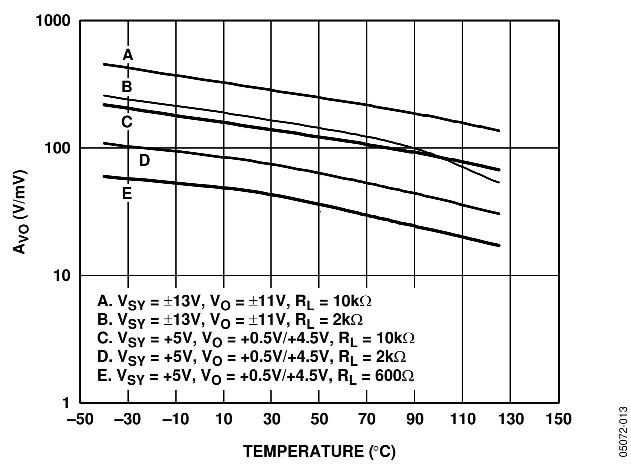

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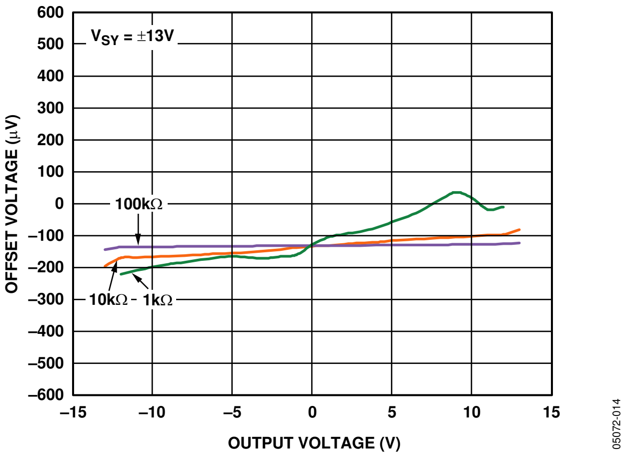

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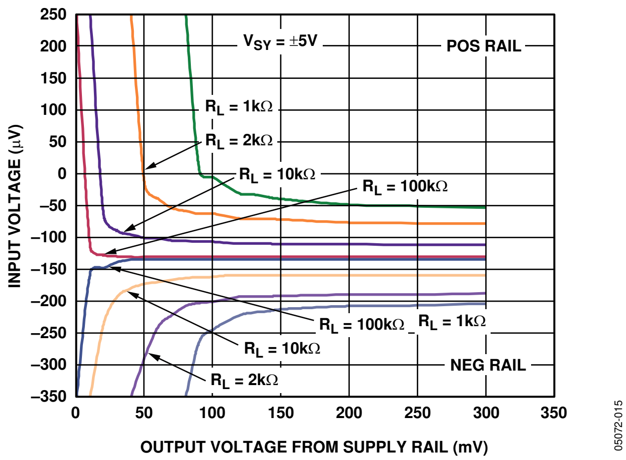

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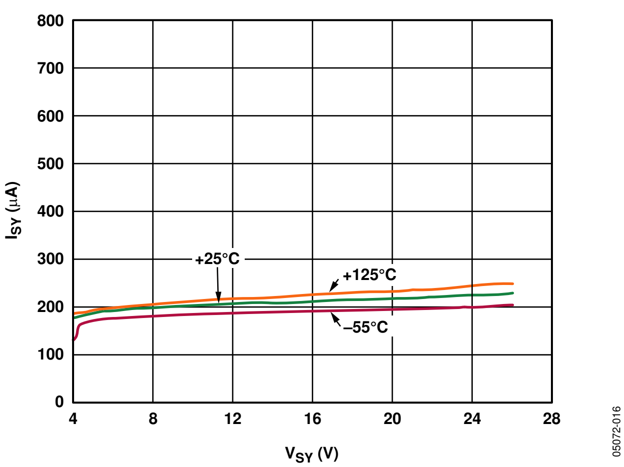

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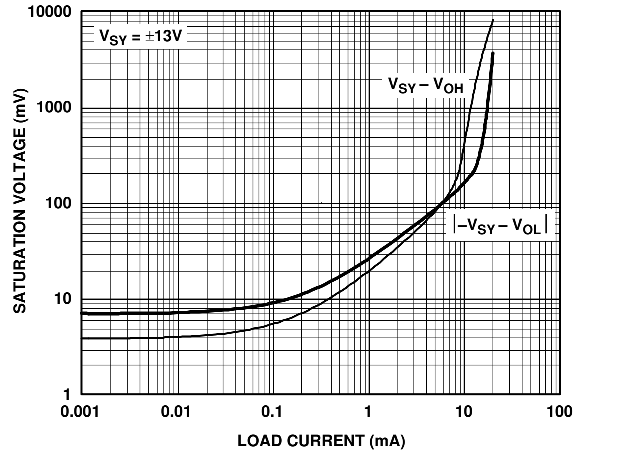

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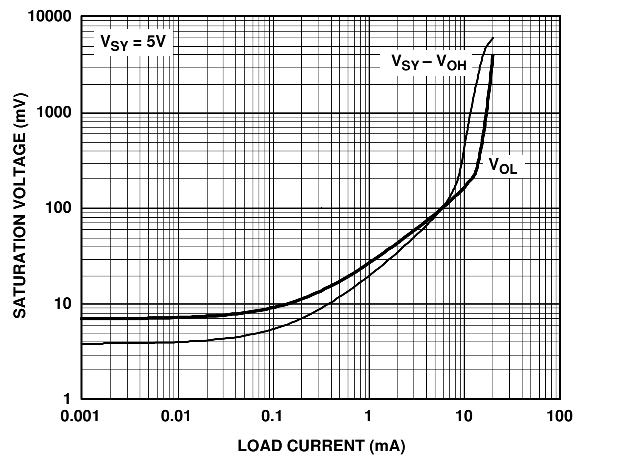

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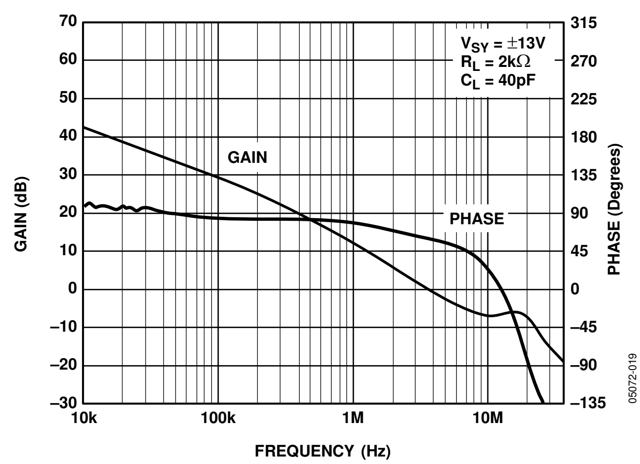

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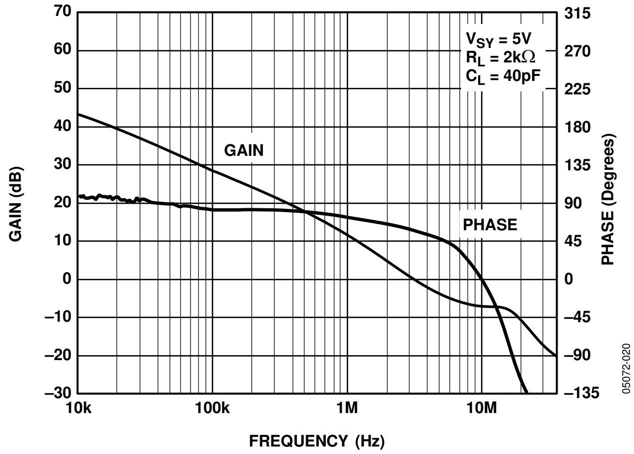

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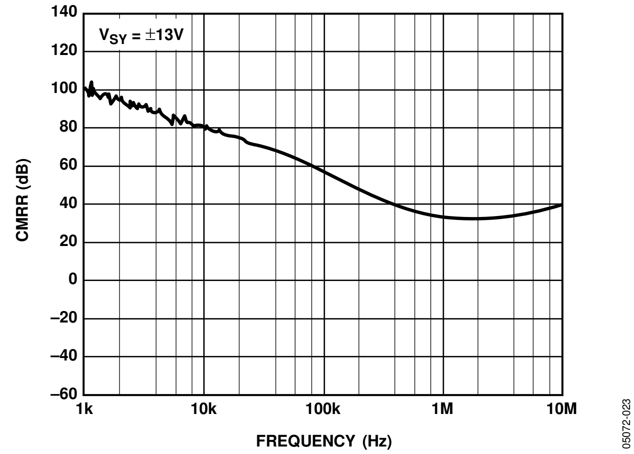

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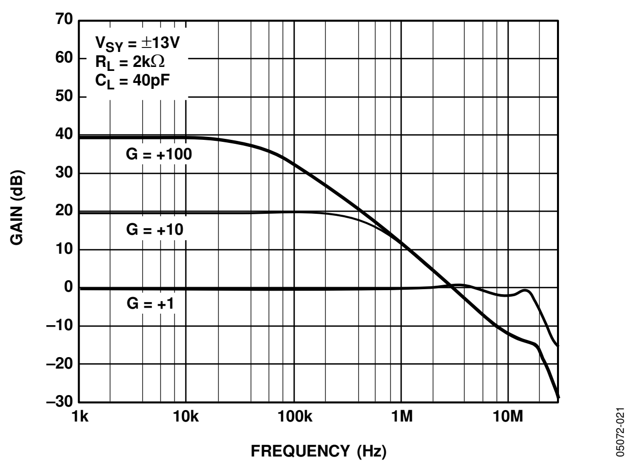

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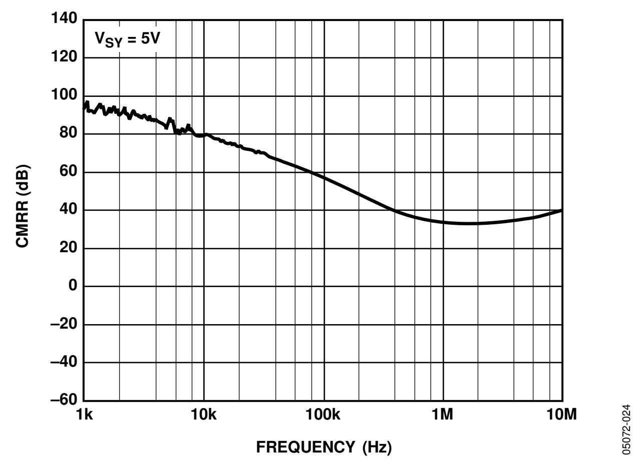

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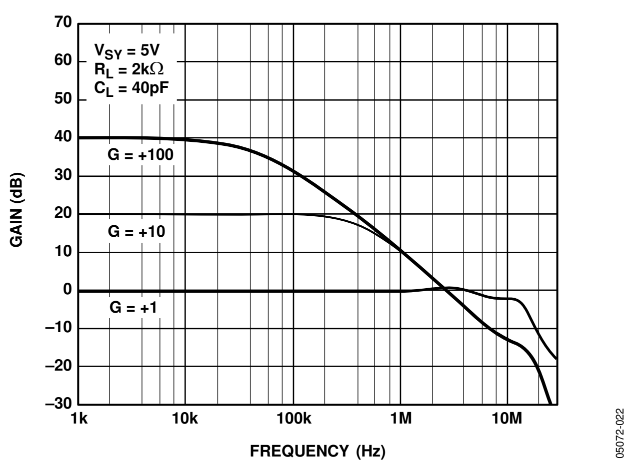

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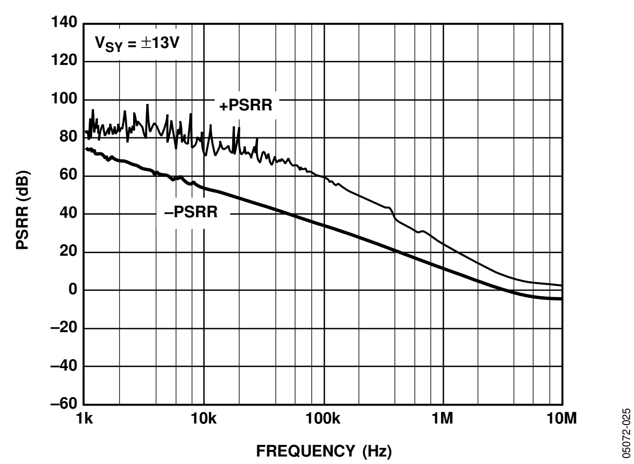

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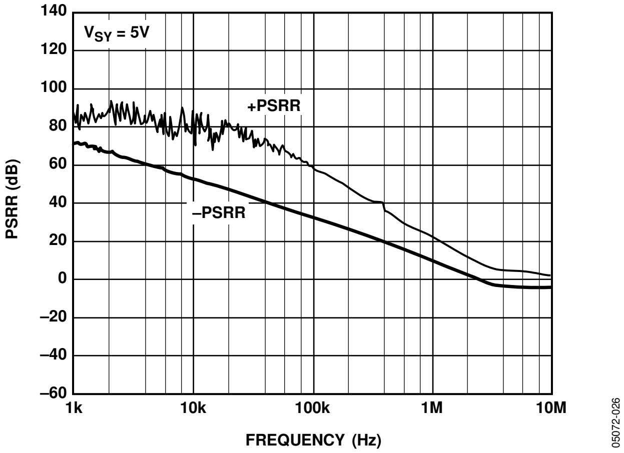

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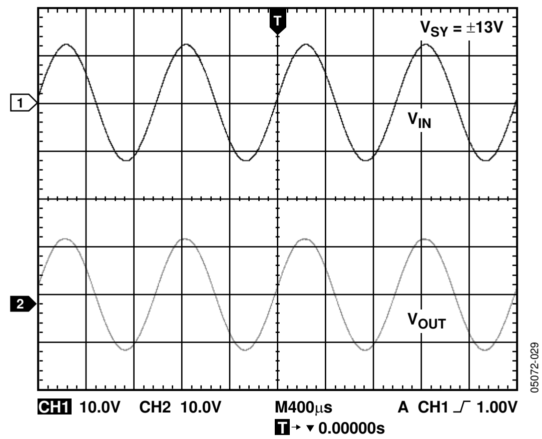

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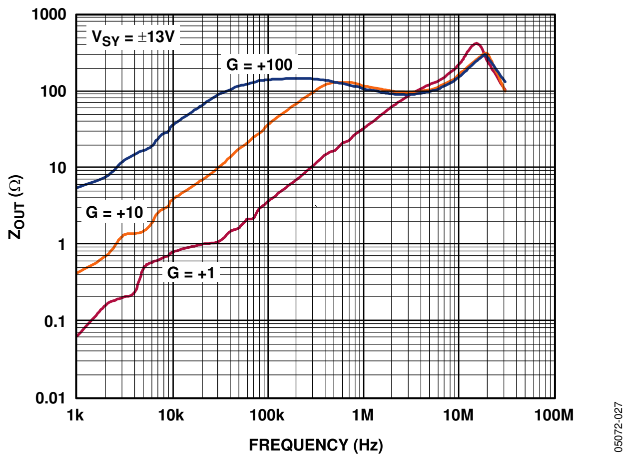

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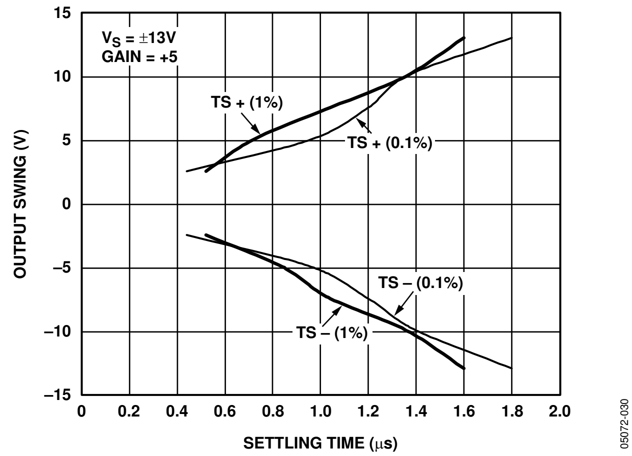

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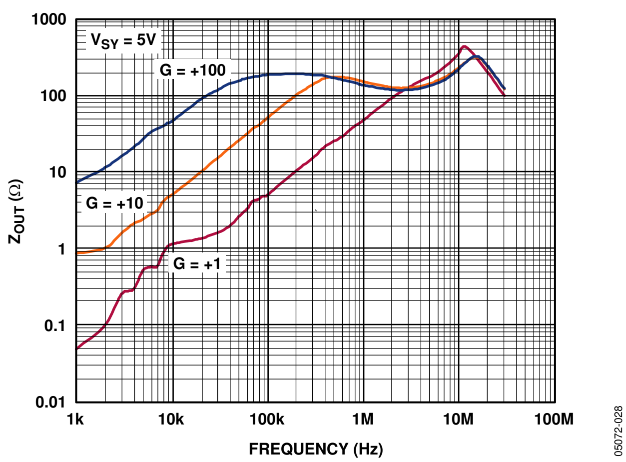


Figure 33. Output Impedance vs. Frequency

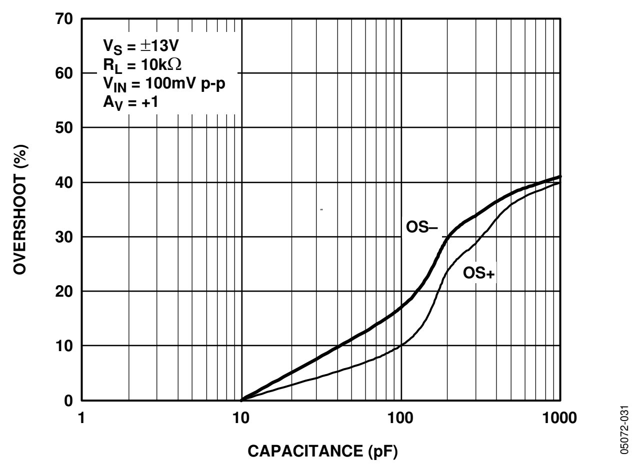


Figure 36. Small Signal Overshoot vs. Load Capacitance

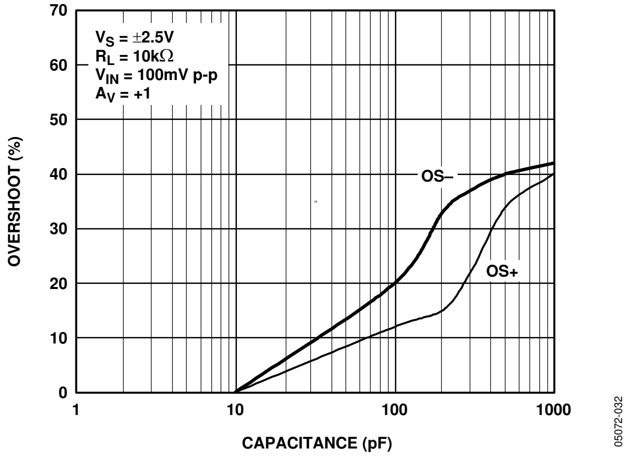


Figure 37. Small Signal Overshoot vs. Load Capacitance

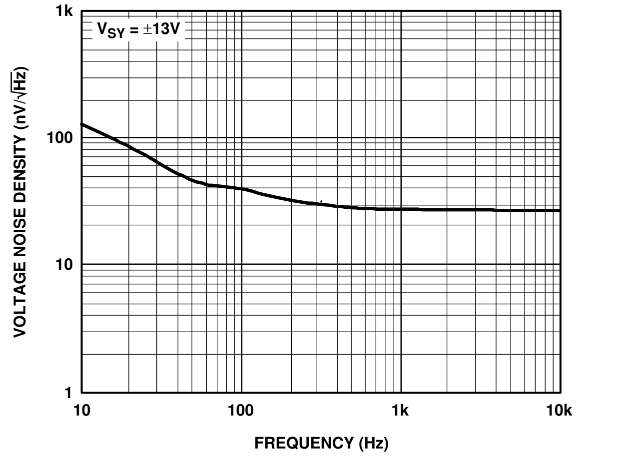
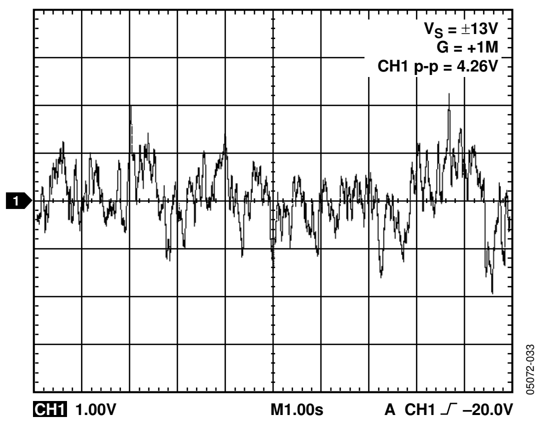


Figure 40. Voltage Noise Density



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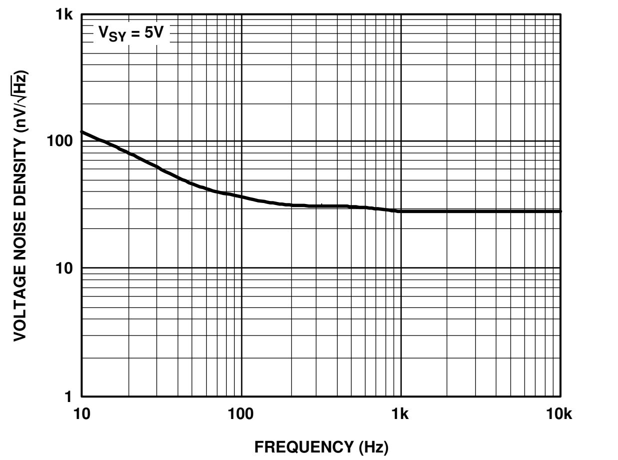

Figure 41. Voltage Noise Density

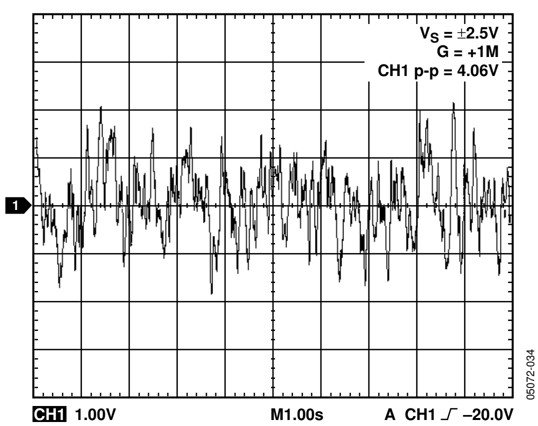

Figure 39. 0.1 Hz to 10 Hz Noise

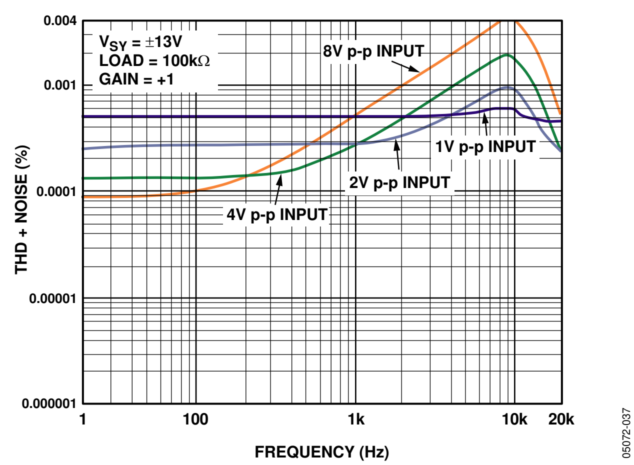

Figure 42. Total Harmonic Distortion + Noise vs. Frequency

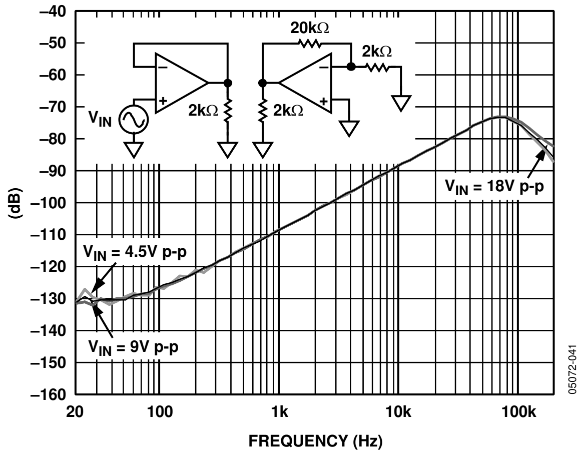

Figure 43. Channel Separation

OUTLINE DIMENSIONS

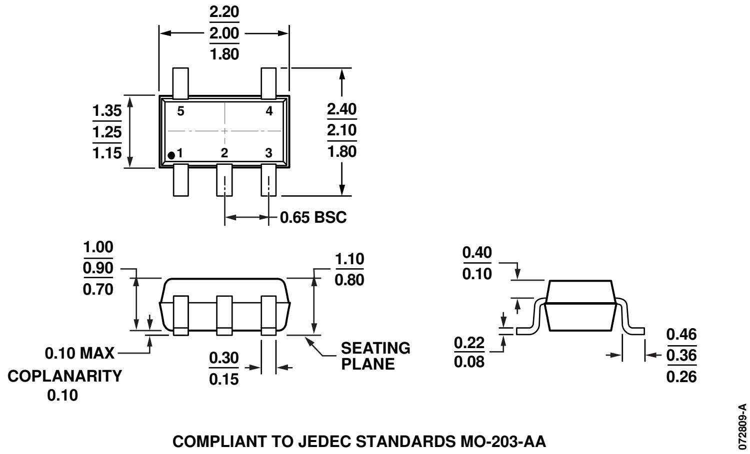

Figure 44. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters

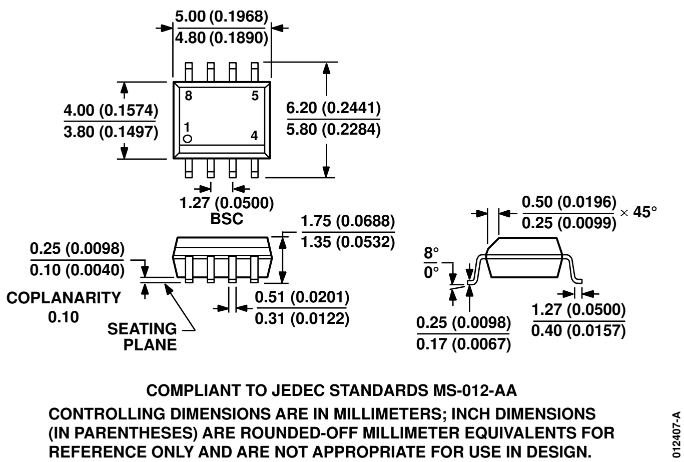

Figure 45. 8-Lead Standard Small Outline Package [SOIC_N]
(R-8)
Dimensions shown in millimeters and (inches)

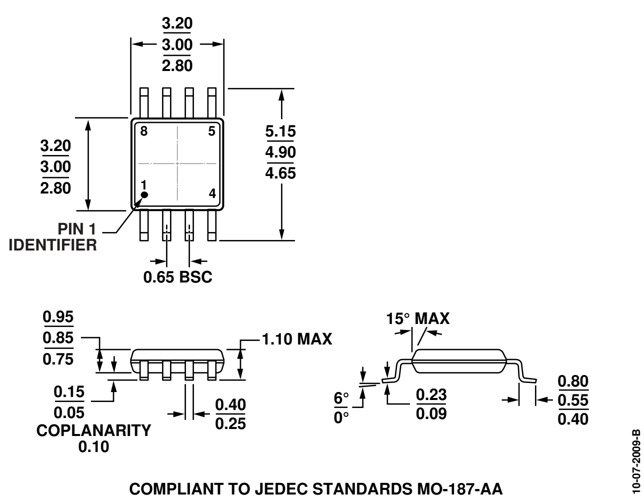

Figure 46. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

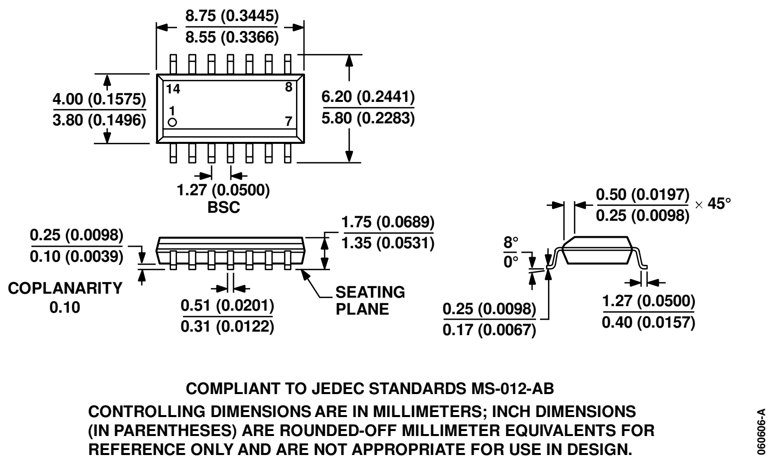

Figure 47. 14-Lead Standard Small Outline Package [SOIC_N] (R-14) Dimensions shown in millimeters and (inches)

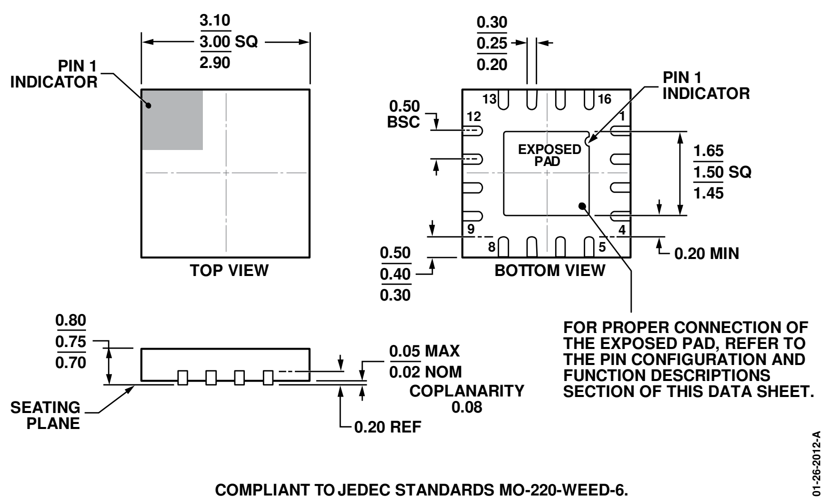

Figure 48. 16-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm × 3 mm Body and 0.75 mm Package Height (CP-16-27) Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8641AKSZ-R2	–40°C to +125°C	5-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-5	A07
AD8641AKSZ-REEL7	–40°C to +125°C	5-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-5	A07
AD8641ARZ	–40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8641ARZ-REEL7	–40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8642ARMZ	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A0A
AD8642ARMZ-REEL	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A0A
AD8642ARZ	–40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8642ARZ-REEL7	–40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8642ARZ-REEL	–40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8643ARZ	–40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
AD8643ARZ-REEL7	–40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
AD8643ACPZ-R2	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-27	AUA
AD8643ACPZ-REEL7	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-27	AUA

[1] Z = RoHS Compliant Part.

NOTES