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AD9102 Evaluation Board Quick Start Guide

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Getting Started with the AD9102 Evaluation Board and Software

WHAT'S IN THE BOX AD9102-EBZ Evaluation Board Mini-USB Cable DAC Evaluation Software Suite CD EXAMPLE EQUIPMENT LIST

+5Vdc Power Supply: Agilent E3630A DAC Clock Source: R&S SML 02 Oscilloscope: Agilent DSO-X 3034A PC: Windows PC with USB 2.0 port

INTRODUCTION

AD9102 EVALUATION BOARD

The AD9102 is a Digital to Analog converter and Waveform Generator. The AD9102-EBZ evaluation board includes a PIC 18F4550 processor programmed to function as a PC USB interface to the SPI port of the device. And an AD9514 clock chip that takes in an up to 1440Mhz signal from the clock source and provides the CLKP/N input to the AD9102. The EVB runs from a single 5 volt supply. Figure 12 is a photo of the top side of the AD9102 EVB.

AD9102 EVALUATION SOFTWARE GUI

The AD9102 Evaluation Board GUI software (Figure 1 and Figure 2) has a number of tabs. Each tab allows the user to view or manually program a subset of AD9102 registers and on-chip data RAM. The RAM tab lets the user download vectors to the RAM. The AD9102 evaluation board CD includes RAM vectors for use with example files described below where appropriate. The DAC1 tab works with the AD9102 DAC. The DAC2, DAC3 and DAC4 tabs are not used with this product. The DAC tab depicts the waveform generation signal chain for the AD9102 DAC. The Register Write Sequence tab is used to select and write register configuration files to the AD9102. Further details on the evaluation software can be found in <u>AD9102 Evaluation System Notes</u> below.

CONFIGRATION EXAMPLE FILES

This quick start guide describes how to set up and run six configuration examples using the AD9102 control panel GUI software. The AD9102 evaluation board CD includes the configuration files shown in Table 1 for each example. Configuring and running the examples is accomplished by downloading these files using the control panel GUI, by following the method described in the <u>Quick Start Procedure</u> below.

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example Load File		Regval File	RAM Vector	
example1	Default.seq	example1.regval	example1_RAM_guassuian.txt	
example2	Default.seq	example2.regval	example2_4096_ramp.txt	
example3	Default.seq	example3.regval	None	
example4	Default.seq	example4.regval	None	
example5	Default.seq	example5.regval	example5_RAM_guassian.txt	
example6	Default.seq	example6.regval	None	

Table 1: Configuration Example Files

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Figure 1: AD9102 evaluation software Control Panel GUI, Board Configuration Tab



AD9102-EBZ



Figure 2: AD9102 evaluation software Control Panel GUI, DAC1 Tab and Register_Write _Sequence Tab





QUICK START PROCEDURE

INITIAL SETUP

- 1. Install AD9102 software and support files on your PC from the CD. The installer will automatically access the National Instruments web site and download NI-VISA-4.6.2 and the Labview 2009 Runtime Engine.
- 2. Connect the EVB to your PC and lab equipment as shown in Figure 3 below. Use a USB cable to connect your PC to the EVB.

It is suggested that the basic set-up is verified before making any modifications to the evaluation board.

Basic Hardware Set-Up

Connect the equipment to the AD9102 evaluation board as follows:

Equipment	Connects to AD9102 Eval Board		
Power Supply	P3 (+5V), P7 (GND)		
Signal Source Clk	J10 (DAC Clock), Set source to 1440MHz or lower, 3dBm output		
PC USB Cable	XP2		
Oscilloscope	J2 (DAC1_P) and J8 (DAC1_N)		



Figure 3: EVB Bench set up

PROCEDURE FOR SETTING UP THE AD9102 TO RUN EXAMPLE CONFIGURATIONS

- 1. Turn on the 5V supply and the clock source
- 2. Start the AD9102 GUI Software
- 3. Follow the steps to get one of the six example configurations running

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Example1 Set-Up

- a. Select the RAM tab
- b. Press the download data from file button
- c. Select the vector file example1_RAM_guassian.txt
- d. Press the "Write Active Tab" button, wait for a write active tab followed by read active tab operation to complete
- e. Select the Register_Write_Sequence tab
- f. Highlight the Default.seq file and example1.regval file see Figure 2
- g. Click on the "Load Register Sequence from File" button
- h. Open the Board Config tab, Set Trigger slide switch to ON, Press Write Active Tab Button
- i. Set trigger slide switch to OFF, Press Write Active Tab Button
- j. The output from J2 and J8 will be as displayed in Figure 4



Figure 4 : Example 1 Result

Example2 Set-Up

- a. Select the RAM tab
- b. Press the download data from file button
- c. Select the vector file example2_4096_ramp.txt
- d. Press the "Write Active Tab" button, wait for a write active tab followed by read active tab operation to complete
- e. Select the Register_Write_Sequence tab
- f. Highlight the Default.seq file and example2.regval file see Figure 2
- g. Click on the "Load Register Sequence from File" button
- h. Open the Board Config tab, Set Trigger slide switch to ON, Press Write Active Tab Button
- i. Set trigger slide switch to OFF, Press Write Active Tab Button
- j. The outputs from J2 and J8 will be displayed as shown in Figure 5





Figure 5 : Example 2 Result

Example3 Set-Up

- a. Select the Register_Write_Sequence tab
- b. Highlight the Default.seq file and example3.regval file see Figure 2Error! Reference source not found.
- c. Click on the "Load Register Sequence from File" button
- d. Open the Board Config tab, Set Trigger slide switch to ON, Press Write Active Tab Button
- e. Set trigger slide switch to OFF, Press Write Active Tab Button
- f. The outputs from J2 and J8 will be as shown in Figure 6



Figure 6 : Example 3 Result

Example4 Set-Up

- a. Select the Register_Write_Sequence tab
- b. Highlight the Default.seq file and example4.regval file see Figure 2
- c. Click on the "Load Register Sequence from File" button
- d. Open the Board Config tab, Set Trigger slide switch to ON, Press Write Active Tab Button
- e. Set trigger slide switch to OFF, Press Write Active Tab Button
- f. The outputs from J2 and J8 will be as shown in Figure 7





Figure 7 : Example 4 Result

Example5 Set-Up

- a. Select the RAM tab
- b. Press the download data from file button
- c. Select the vector file example5_RAM_guassian.txt
- d. Select the Register_Write_Sequence tab
- e. Press the "Write Active Tab" button, wait for a write active tab followed by a read active tab operation to complete
- f. Highlight the Default.seq file and example5.regval file see Figure 2Error! Reference source not found.
- g. Click on the "Load Register Sequence from File" button
- h. Open the Board Config tab, Set Trigger slide switch to ON, Press Write Active Tab Button
- i. Set trigger slide switch to OFF, Press Write Active Tab Button
- j. The outputs from J2 and J8 will be as displayed in Figure 8



Figure 8 : Example 5 Result

Example6 Set-Up

- a. Select the Register_Write_Sequence tab
- b. Highlight the Default.seq file and example6.regval file see Figure 2
- c. Click on the "Load Register Sequence from File" button
- d. Open the Board Config tab, Set Trigger slide switch to ON, Press Write Active Tab Button
- e. Set trigger slide switch to OFF, Press Write Active Tab Button
- f. The outputs from J2 and J8 will be as shown in Figure 9





Figure 9 : Example 6 Result

AD9102 EVALUATION SYSTEM NOTES

AD9102 evaluation Software

When the *Run* 🔂 button is pressed, the evaluation software will run until the STOP Button is pressed. The GUI is arranged in TABs where the AD9102 functionalities are broken into different pages: CONFIG, ANALOG/CAL, PATTERN CONFIG, RAM, DAC1 (TABs DAC2, DAC3, and DAC4 are unused with AD9102). When a TAB is open, the information displayed may not reflect the current state of the AD9102 IC on the evaluation board. To refresh this display the READ ACTIVE TAB button should be pressed.

Several operations can be executed from this GUI:

- RESET: When this button is clicked, a software reset of the part is executed. After the reset a READ ALL TABS operation is performed
- READ ACTIVE TAB: Clicking this button launches a read operation of AD9102 registers displayed on the TAB currently viewed. The results are reported back in the registers in the active tab.
- WRITE ACTIVE TAB: Clicking this button launches a write operation of AD9102 of the registers displayed on the tab currently viewed. After the write operations, a READ ACTIVE TAB operation is automatically executed to verify that the values written were actually stored in the part. If the values change after the WRITE ACTIVE TAB button is clicked, it means that the communication was not successful and the part is not communicating with the PC.
- READ ALL TABS: Clicking this button launches a read operation of all AD9102 registers, but not the AD9102 on-chip RAM. The results are reported back in the registers in the tabs.
- WRITE ALL TABS: Clicking this button launches a write operation of all AD9102 registers, but not the AD9102 on-chip RAM. After the write operations, a READ ALL TABS operation is automatically executed to verify that the values written were actually stored in the part. If the values change after the WRITE ALL TABS button is clicked, it means that the communication was not successful and the part is not communicating with the PC.

The RAM TAB - see Figure 10, can be used to download data into the RAM. As the data is left justified in the AD9102, the GUI proceeds to left justify the data for the user when downloading the data into the AD9102. The RAM data is first stored in the PC in the table displayed in the GUI. The number of samples stored in the variable is showed under the table. As the AD9102 has 4,096 samples care must be taken to not exceed this size as the software will automatically ignore any data outside this range (i.e. the GUI will only write the first 4096 samples in the table). When the data is uploaded to the software correctly, the WRITE ACTIVE TAB button can be clicked to write this data into the RAM.



AD9102-EBZ



Figure 10 :AD9102 Evaluation software RAM TAB

The BOARD CONFIG tab can be used to configure the evaluation board for power supply and signal levels – Figure 11.

BOARD C	ONFIG CONFIG ANALOG/CAL PATTERN C	CONFIG RAM DAC1 DAC2 DAC3 DAC4
		_
	Pin Configuration 1 0 0 0	TREGGER PIC IN
	LDO DVDD_CTRL CVDD_CTRL AVDD_CTRL Configuration 3.3V 3.3V 3.3V	•

Figure 11 :AD9102 Evaluation software BOARD Config TAB

At the bottom of the page, there are also two tabs:

- Register_content Tab : Reports the current register value of the part
- Register_Write_Sequence Tab: Allows configurations to be written to the AD9102 following a pre-determined sequence. Examples of sequence and register configurations are provided in the evaluation software and user defined configuration can be saved and loaded.

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Figure 12: AD9102-EBZ Evaluation Board

Using the AD9514

By default the AD9514 is configured to provide a 180Mhz clock input to the AD9102 from a 1.44 Ghz sine wave input to J10 of the EVB. The AD9514 has a configurable divider that can be set through external resistors on the EVB. The AD9102 evaluation board allows the AD9514 divider to be set by changing resistors. Output 0 from the AD9514 is used as a PECL output to drive the AD9102 CLKP/CLKN inputs. Output 2 is used to drive the external clock on J9.

Table 2 summarizes a few common settings used to divide the input clock by 2, 4, 8 and 16.

	S9			S10		
	1/3			0		
÷2	R142 open	R136 open	R141 open	R147 0Ω	R143 open	R144 open
. 4		1			0	
÷4	open	open	0Ω	0Ω	open	open
. 0	2/3			1/3		
÷ð	open	0Ω	open	open	open	open
÷16	1			2/3		
	open	open	0Ω	open	$\Omega\Omega$	open

Table 2: AD9514 settings



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Using the AD9102 with 1.8V power supply

By default the AD9102-EBZ evaluation board uses 3.3V digital and clock power supplies. On-chip CLDO, DLDO1 and DLDO2 supplies are used. P15, P13, and P11 are not installed.

It is possible to operate the AD9102 with 1.8V power supply only. To achieve this, a few changes are needed:

- 1. Set the voltage of the DVDD and CVDD regulators on the AD9102 evaluation board to 1.8V on the BOARD CONFIG tab of the AD9102 evaluation software see Figure 11. This will assure that SPI communication and the AD9102 clock power supply pins are powered with 1.8V
- 2. Install jumpers in P15, P13 and P11. These jumpers connect 1.8V regulators on the evaluation board with DLDO1, DLDO2 and CLKLDO pins of the AD9102.

