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Low Power, 14-Bit, 180 MSPS, Digital-to-Analog Converter and Waveform Generator

Data Sheet

AD9102

FEATURES

On-chip 4096 × 14-bit pattern memory
On-chip DDS
Power dissipation @ 3.3 V, 4 mA output
96.54 mW @ 180 MSPS
Sleep mode: <5 mW @ 3.3 V
Supply voltage: 1.8 V to 3.3 V
SFDR to Nyquist
87 dBc @ 10 MHz output
Phase noise @ 1 kHz offset, 180 MSPS, 8 mA: −150 dBc/Hz
Differential current outputs: 8 mA max @ 3.3 V
Small footprint, 32-lead, 5 mm × 5 mm LFCSP with 3.6 mm × 3.6 mm exposed paddle, and Pb-free package

APPLICATIONS

Medical instrumentation
Portable instrumentation
Signal generators, arbitrary waveform generators
Automotive radar

GENERAL DESCRIPTION

The AD9102 TxDAC® and waveform generator is a high performance digital-to-analog converter (DAC) integrating on-chip pattern memory for complex waveform generation with a direct digital synthesizer (DDS).

The DDS is a 14-bit output, up to 180 MSPS master clock sine wave generator with a 24-bit tuning word, allowing 10.8 Hz/LSB frequency resolution.

SRAM data can include directly generated stored waveforms, amplitude modulation patterns applied to DDS outputs, or DDS frequency tuning words.

An internal pattern control state machine lets the user program the pattern period for the DAC as well the start delay within the pattern period for the signal output on the DAC .

A SPI interface is used to configure the digital waveform generator and load patterns into the SRAM.

A gain adjustment factor and an offset adjustment are applied to the digital signal on their way into the DAC.

The AD9102 offers exceptional ac and dc performance and supports DAC sampling rates of up to 180 MSPS.

The flexible power supply operating range of 1.8 V to 3.3 V and low power dissipation of the AD9102 make it well suited for portable and low power applications.

PRODUCT HIGHLIGHTS

1. High Integration.
   On-chip DDS and 4096 × 14 pattern memory.
2. Low Power.
   Power-down mode provides for low power idle periods.

FUNCTIONAL BLOCK DIAGRAM

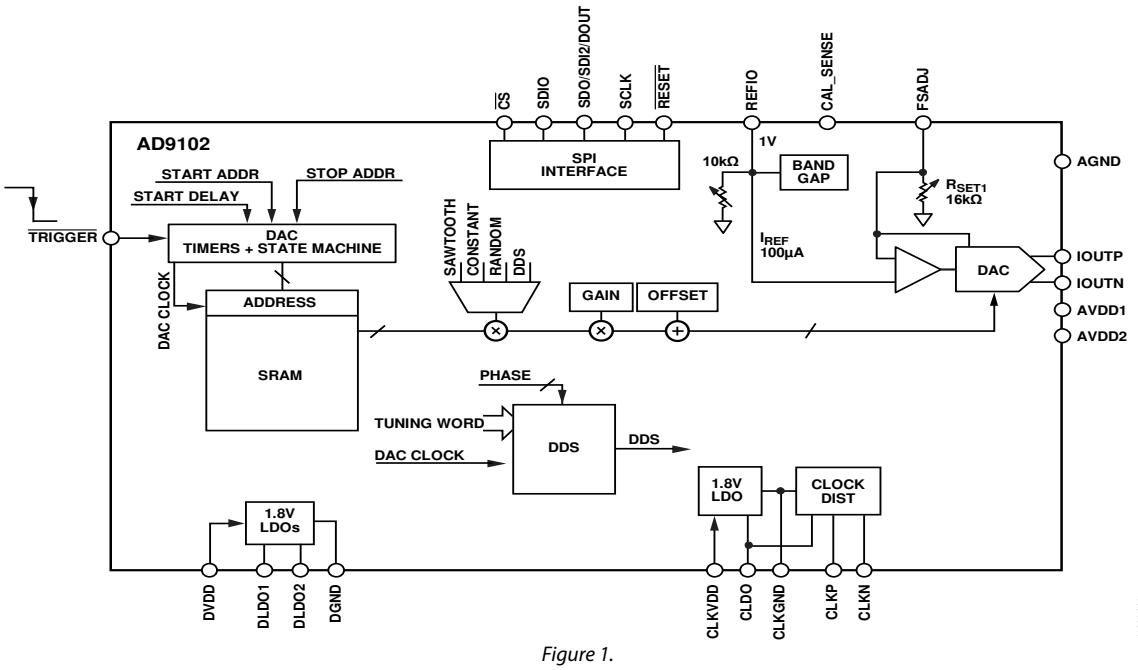

Figure 1.

Rev. 0

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Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

AD9102* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9102 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9102: Low Power, 14 Bit, 180MSPS, Digital to Analog Converter and Waveform Generator Data Sheet

TOOLS AND SIMULATIONS

- AD9102 IBIS Model

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Press

- Quad 12-Bit and Single 14-Bit, 180-MSPS D/A Converters Integrate Complex Waveform Generation Function

DESIGN RESOURCES

- AD9102 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9102 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

1/13—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}; AVDD = 3.3 V; DVDD = 3.3 V, CLKVDD = 3.3 V; internal CLDO, DLDO1 and DLDO2; I_{OUTFS} = 8 mA; maximum sample rate, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		14		Bits
ACCURACY @ 3.3 V				
Differential Nonlinearity (DNL)		±1.4		LSB
Integral Nonlinearity (INL)		±2.0		LSB
DAC OUTPUT				
Offset Error		±0.00025		% of FSR
Gain Error Internal Reference—No Automatic I_{OUTFS} Calibration	−1.0		+1.0	% of FSR
Full-Scale Output Current				
3.3 V	2	4	8	mA
Output Resistance		200		MΩ
Output Compliance Voltage	−0.5		+1.0	V
DAC TEMPERATURE DRIFT				
Gain with Internal Reference		±251		ppm/°C
Internal Reference Voltage		±119		ppm/°C
REFERENCE OUTPUT				
Internal Reference Voltage with AVDD = 3.3 V	0.8	1.0	1.2	V
Output Resistance		10		kΩ
REFERENCE INPUT				
Voltage Compliance	0.1		1.25	V
Input Resistance External Reference Mode		1		MΩ

DC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}; AVDD = 1.8 V; DVDD = DLDO1 = DLDO2 = 1.8 V; CLKVDD = CLDO = 1.8 V; I_{OUTFS} = 4 mA; maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
RESOLUTION		14		Bits
ACCURACY @ 1.8 V				
Differential Nonlinearity (DNL)		±1.5		LSB
Integral Nonlinearity (INL)		±1.4		LSB
DAC OUTPUTS				
Offset Error		±0.00025		% of FSR
Gain Error Internal Reference—No Automatic I_{OUTFS} Calibration	−1.0		+1.0	% of FSR
Full-Scale Output Current				
V_{CC} = 1.8 V	2	4	4	mA
Output Resistance		200		MΩ
Output Compliance Voltage	−0.5		+1.0	V
DAC TEMPERATURE DRIFT				
Gain		±228		ppm/°C
Reference Voltage		±131		ppm/°C
REFERENCE OUTPUT				
Internal Reference Voltage with AVDD = 1.8 V	0.8	1.0	1.2	V
Output Resistance		10		kΩ
REFERENCE INPUT				
Voltage Compliance	0.1		1.25	V
Input Resistance External Reference Mode		1		MΩ

DIGITAL TIMING SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}; AVDD = 3.3 V; DVDD = 3.3 V, CLKVDD = 3.3 V, internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 8 mA; maximum sample rate, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKIN)				
Maximum Clock Rate	180			MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)	80			MHz
Minimum Pulse Width High		6.25		ns
Minimum Pulse Width Low		6.25		ns
Setup Time SDIO to SCLK	4.0			ns
Hold Time SDIO to SCLK	5.0			ns
Output Data Valid SCLK to SDO/SDI2/DOUT or SDIO		6.2		ns
Setup Time $\overline{CS}$ to SCLK	4.0			ns

DIGITAL TIMING SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}; AVDD = 1.8 V; DVDD = DLDO1 = DLDO2 = 1.8 V; CLKVDD = CLDO = 1.8 V; I_{OUTFS} = 4 mA; maximum sample rate, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKIN)				
Maximum Clock Rate	180			MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)	80			MHz
Minimum Pulse Width High		6.25		ns
Minimum Pulse Width Low		6.25		ns
Setup Time SDIO to SCLK	4.0			ns
Hold Time SDIO to SCLK	5.0			ns
Output Data Valid SCLK to SDO/SDI2/DOUT or SDIO		8.8		ns
Setup Time $\overline{CS}$ to SCLK	4.0			ns

INPUT/OUTPUT SIGNAL SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL (SCLK, $\overline{CS}$, SDIO, SDO/SDI2/DOUT, $\overline{RESET}$, $\overline{TRIGGER}$)					
Input V_{IN} Logic High	DVDD = 1.8 V	1.53			V
	DVDD = 3.3 V	2.475			V
Input V_{IN} Logic Low	DVDD = 1.8 V			0.27	V
	DVDD = 3.3 V			0.825	V
CMOS OUTPUT LOGIC LEVEL (SDIO, SDO/SDI2/DOUT)					
Output V_{OUT} Logic High	DVDD = 1.8 V	1.79			V
	DVDD = 3.3 V	3.28			V
Output V_{OUT} Logic Low	DVDD = 1.8 V			0.25	V
	DVDD = 3.3 V			0.625	V
DAC CLOCK INPUT (CLKP, CLKN)					
Minimum Peak-to-Peak Differential Input Voltage, V_{CLKP}/V_{CLKN}			150		mV
Maximum Voltage at V_{CLKP} or V_{CLKN}			V_{DVDD}		V
Minimum Voltage at V_{CLKP} or V_{CLKN}			V_{DGND}		V
Common-Mode Voltage	Generated on Chip		0.9		V

AC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}; AVDD = 3.3 V; DVDD = 3.3 V, CLKVDD = 3.3 V, internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 8 mA; maximum sample rate, unless otherwise noted.

Table 6.

Parameter	Min	Typ	Max	Unit
SPURIOUS FREE DYNAMIC RANGE				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		87		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		67		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		88		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		68		dBc
NSD				
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		−163		dBm/Hz
PHASE NOISE @ 1 kHz FROM CARRIER				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		−150		dBc/Hz
DYNAMIC PERFORMANCE				
Output Settling Time, Full-Scale Output Step (to 0.1%)[1]		31.2		ns
Trigger to Output Delay, f_{DAC} = 180 MSPS[2]		96		ns
Rise Time, Full-Scale Swing[1]		3.25		ns
Fall Time, Full-Scale Swing[1]		3.26		ns

[1] Based on 85 Ω resistors from DAC output terminals to ground.
[2] Start delay = 0 f_{DAC} clock cycles.

AC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}; AVDD = 1.8 V; DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V; I_{OUTFS} = 4 mA; maximum sample rate, unless otherwise noted.

Table 7.

Parameter	Min	Typ	Max	Unit
SPURIOUS FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		84		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		73		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		91		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		86		dBc
NSD				
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		−163		dBm/Hz
PHASE NOISE @ 1kHz FROM CARRIER				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		−150		dBc/Hz
DYNAMIC PERFORMANCE				
Output Settling Time (to 0.1%)[1]		31.2		ns
Trigger to Output Delay, f_{DAC} = 180 MSPS2[2]		96		ns
Rise Time[1]		3.25		ns
Fall Time[1]		3.26		ns

[1] Based on 85 Ω resistors from DAC output terminals to ground.
[2] Start delay = 0 f_{DAC} clock cycles.

POWER SUPPLY VOLTAGE INPUTS AND POWER DISSIPATION

Table 8.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG SUPPLY VOLTAGES					
AVDD1, AVDD2		1.7		3.6	V
CLKVDD		1.7		3.6	V
CLDO	On-chip LDO not in use	1.7		1.9	V
DIGITAL SUPPLY VOLTAGES					
DVDD		1.7		3.6	V
DLDO1, DLDO2	On-chip LDO not in use	1.7		1.9	V
POWER CONSUMPTION	AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, internal CLDO, DLDO1, AND DLDO2				
f_{DAC} = 180 MSPS, Pure CW Sine Wave	12.5 MHz (DDS only)		96.54		mW
I_{AVDD}			7.67		mA
I_{DVDD}					
DDS Only	CW sine wave output		17.73		mA
RAM Only	50% duty cycle FS pulse output		11.31		mA
DDS and RAM Only	50% duty cycle sine wave output		14.6		mA
I_{CLKVDD}			3.85		mA
Power-Down Mode	REF on, DACs sleep, CLK power down, external CLK and supplies on		4.73		mW
POWER CONSUMPTION	AVDD = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V				
f_{DAC} = 180 MSPS, Pure CW Sine Wave	12.5 MHz (DDS only)		51.33		mW
I_{AVDD}			7.54		mA
I_{DVDD}			0.15		mA
I_{DLDO2}					
DDS Only	CW sine wave output		16.03		mA
RAM Only	50% duty cycle FS pulse output		10.07		mA
DDS and RAM Only	50% duty cycle sine wave output		13.26		mA
I_{DLDO1}			1.129		mA
I_{CLKVDD}			0.0096		mA
I_{CLDO}			3.65		mA
Power-Down Mode	REF on, DACs sleep, CLK power down, external CLK and supplies on		1.49		mW

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
AVDD1, AVDD2, DVDD to AGND, DGND, CLKGND	−0.3 V to +3.9 V
CLKVDD to AGND, DGND, CLKGND	−0.3 V to +3.9 V
CLDO, DLDO1, DLDO2 to AGND, DGND, CLKGND	−0.3 V to 2.2 V
AGND to DGND, CLKGND	−0.3 V to +0.3 V
DGND to AGND, CLKGND	−0.3 V to +0.3 V
CLKGND to AGND, DGND	−0.3 V to +0.3 V
$\overline{CS}$, SDIO, SCLK, SDO/ SDI2/DOUT, $\overline{RESET}$, $\overline{TRIGGER}$ to DGND	−0.3 V to DVDD + 0.3 V
CLKP, CLKN to CLKGND	−0.3 V to CLKVDD + 0.3 V
REFIO to AGND	−1.0 V to AVDD + 0.3 V
IOUTP, IOUTN to AGND	−0.3 V to DVDD + 0.3 V
FSADJ, CAL_SENSE to AGND	−0.3 V to AVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a standard circuit board for surface-mount packages. θ_{JC} is measured from the solder side (bottom) of the package.

Table 10. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
32-Lead LFCSP with Exposed Paddle	30.18	6.59	3.84	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

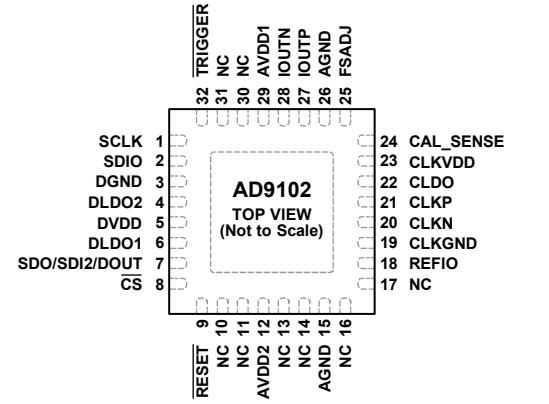

Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	SPI Clock Input.
2	SDIO	SPI Data Input/Output. Primary bidirectional data line for the SPI port.
3	DGND	Digital Ground.
4	DLDO2	1.8 V Internal Digital LDO1 Outputs. When the internal digital LDO1 is enabled, bypass this pin with a 0.1 µF capacitor.
5	DVDD	3.3 V External Digital Power Supply. DVDD defines the level of the digital interface of the AD9102 (SPI interface).
6	DLDO1	1.8 V Internal Digital LDO2 Outputs. When the internal digital LDO2 is enabled, bypass this pin with a 0.1 µF capacitor.
7	SDO/SDI2/DOUT	Digital I/O Pin. In 4-wire SPI mode (SDO), this pin outputs the data from the SPI. In double-SPI mode (SDI2), this pin is a second data input line for the SPI port that writes to the SRAM. In data out mode (DOUT), this terminal is a programmable pulse output.
8	$\overline{CS}$	SPI Port Chip Select, Active Low.
9	$\overline{RESET}$	Active Low Reset Pin. Resets registers to their default values.
10	NC	Not Connected. Do not connect to this pin.
11	NC	Not Connected. Do not connect to this pin.
12	AVDD2	1.8 V to 3.3 V Power Supply Input.
13	NC	Not Connected. Do not connect to this pin.
14	NC	Not Connected. Do not connect to this pin.
15	AGND	Analog Ground.
16	NC	Not Connected. Do not connect to this pin.
17	NC	Not Connected. Do not connect to this pin.
18	REFIO	DAC Voltage Reference Input/Output.
19	CLKGND	Clock Ground.
20	CLKN	Clock Input, Negative Side.
21	CLKP	Clock Input, Positive Side.
22	CLDO	Clock Power Supply Output (Internal Regulator in Use), Clock Power Supply Input (Internal Regulator Bypassed).
23	CLKVDD	Clock Power Supply Input.
24	CAL_SENSE	Sense Input for Automatic I_{OUTFS} Calibration.
25	FSADJ	External Full-Scale Current Output Adjust for DAC or Full-Scale Current Output Adjust Reference for Automatic I_{OUTFS} Calibration.
26	AGND	Analog Ground.
27	IOUTP	DAC Current Output, Positive Side.
28	IOUTN	DAC Current Output, Negative Side.

Pin No.	Mnemonic	Description
29	AVDD1	1.8 V to 3.3 V Power Supply Input for DAC.
30	NC	Not Connected. Do not connect to this pin.
31	NC	Not Connected. Do not connect to this pin.
32	$\overline{\text{TRIGGER}}$	Pattern Trigger Input.
	EPAD	Exposed Pad. It is recommended that the exposed pad be thermally connected to a copper ground plane for enhanced electrical and thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, internal CLDO, DLDO1, and DLDO2.

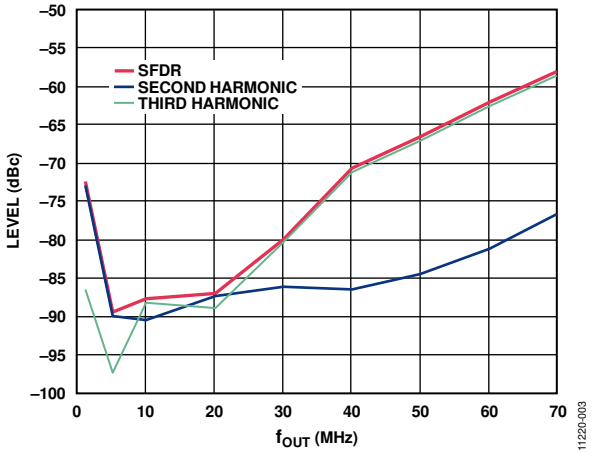

Figure 3. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 8 mA vs. f_{OUT}

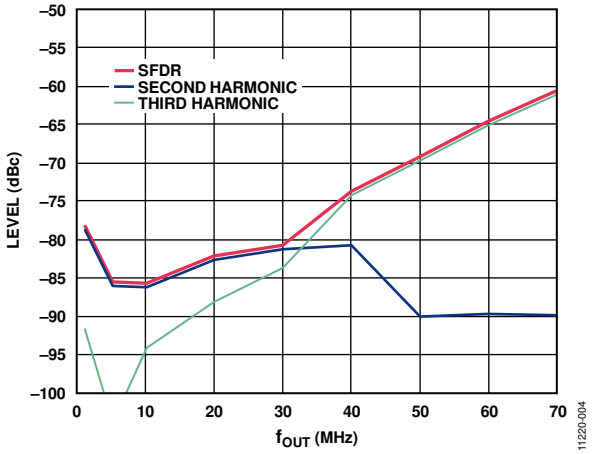

Figure 4. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 4 mA vs. f_{OUT}

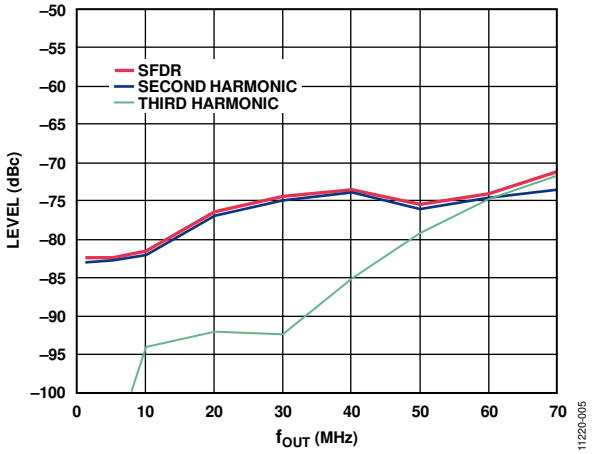

Figure 5. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 2 mA vs. f_{OUT}

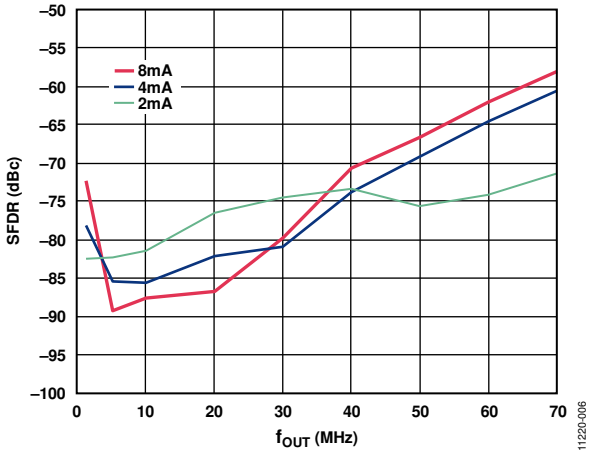

Figure 6. SFDR at Three I_{OUTFS} Values vs. f_{OUT}

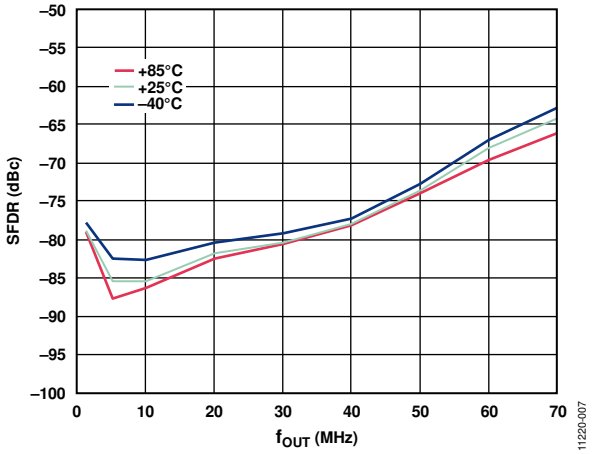

Figure 7. SFDR at Three Temperatures vs. f_{OUT}

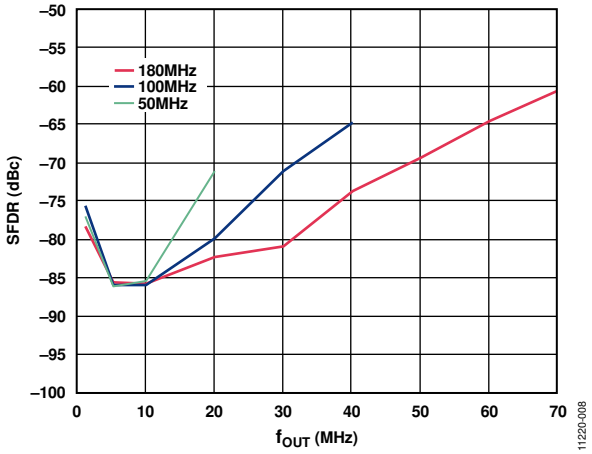

Figure 8. SFDR at Three f_{DAC} Values vs. f_{OUT}

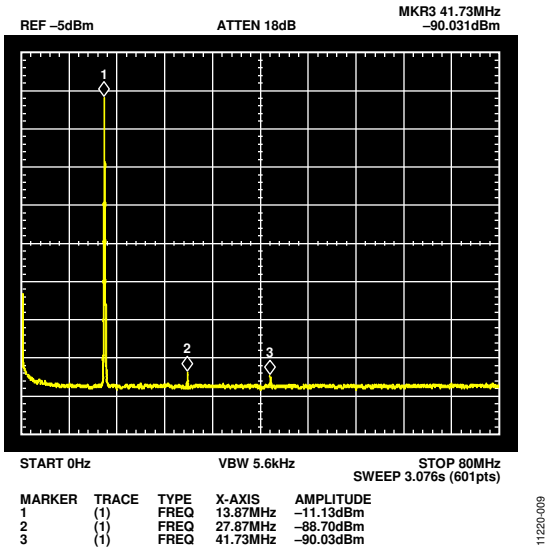

Figure 9. Output Spectrum, f_{OUT} = 13.87 MHz

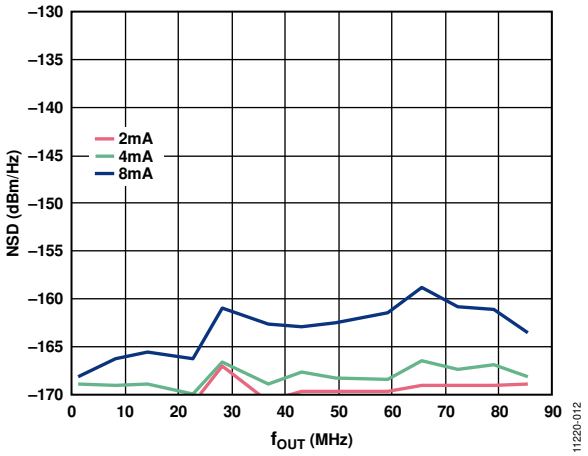

Figure 12. NSD vs. f_{OUT}, Three I_{OUTFS} Values

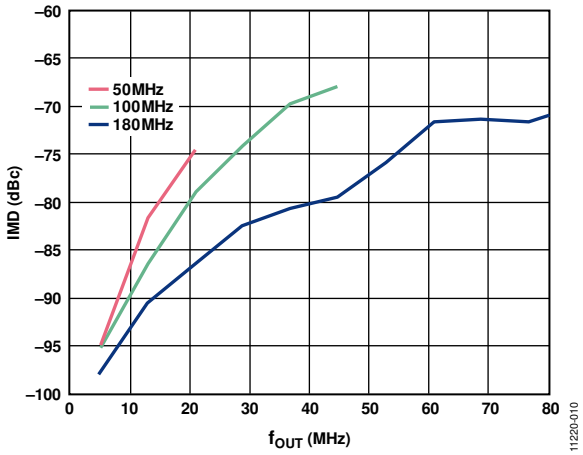

Figure 10. IMD vs. f_{OUT}, Three f_{DAC} Values

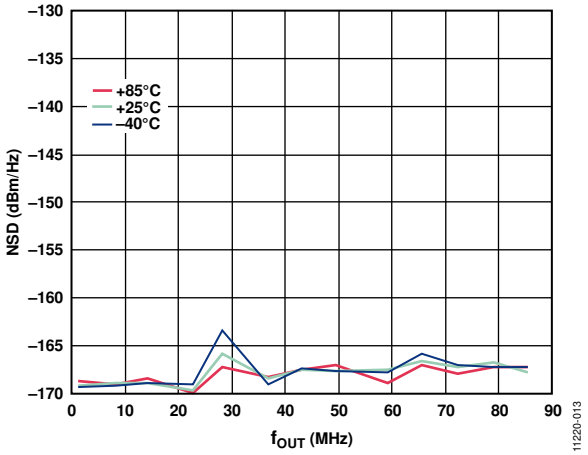

Figure 13. NSD vs. f_{OUT} at Three Temperatures

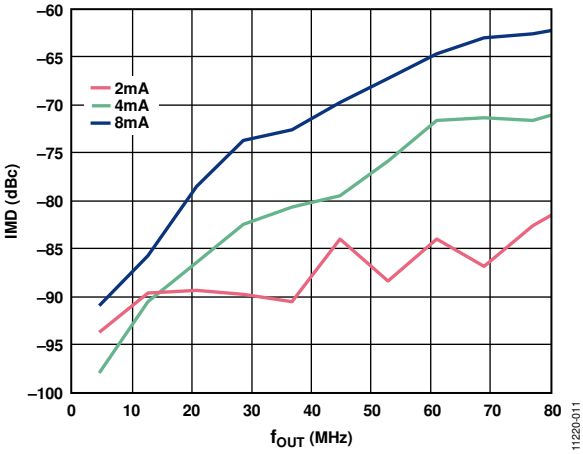

Figure 11. IMD vs. f_{OUT}, Three I_{OUTFS} Values

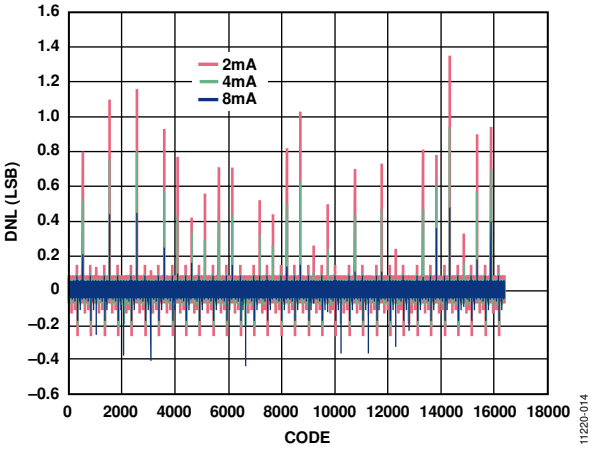

Figure 14. DNL, Three I_{OUTFS} Values

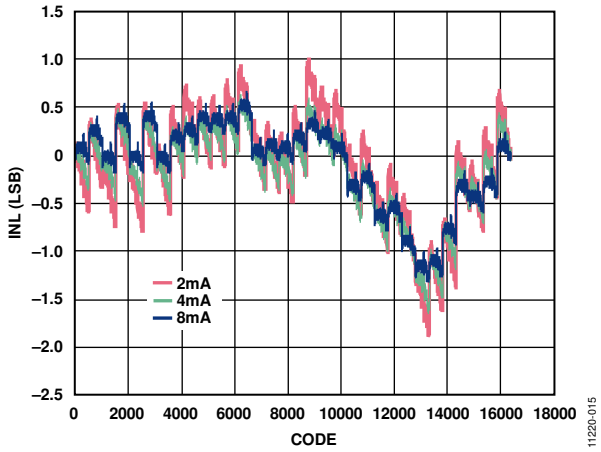

Figure 15. INL, Three I_{OUTFS} Values

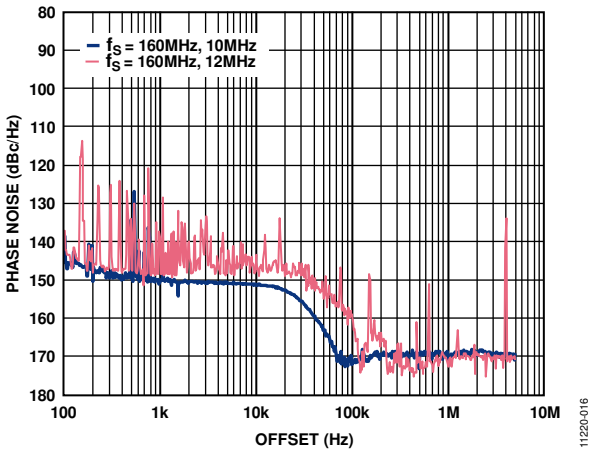

Figure 16. Phase Noise vs. Offset

AVDD = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V

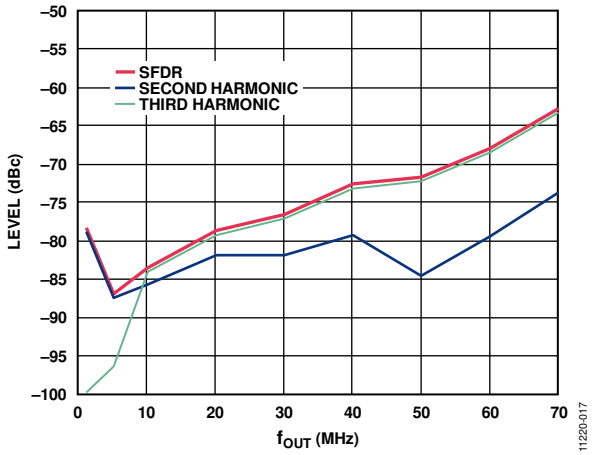

Figure 17. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 4 mA vs. f_{OUT}

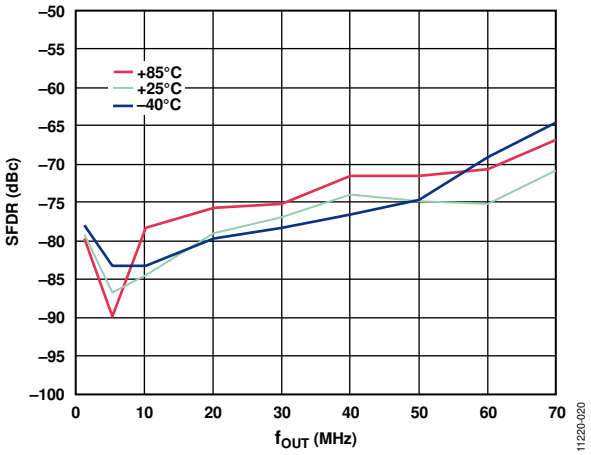

Figure 20. SFDR at Three Temperatures vs. f_{OUT}

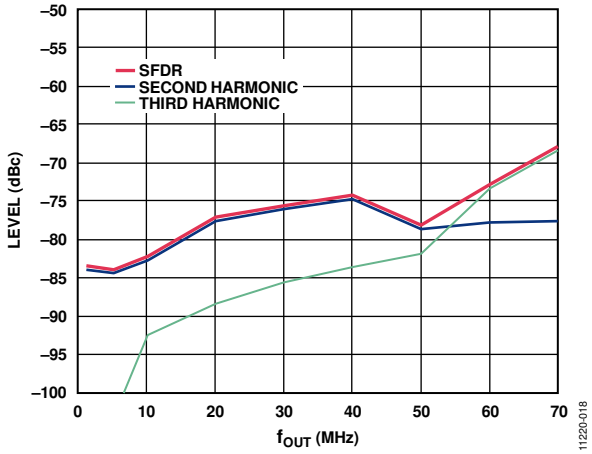

Figure 18. SFDR, 2nd and 3rd Harmonics at I_{OUTFS} = 2 mA vs. f_{OUT}

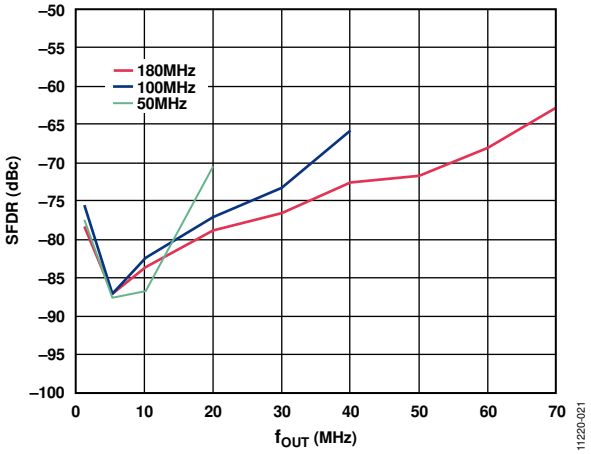

Figure 21. SFDR at Three f_{DAC} Values vs. f_{OUT}

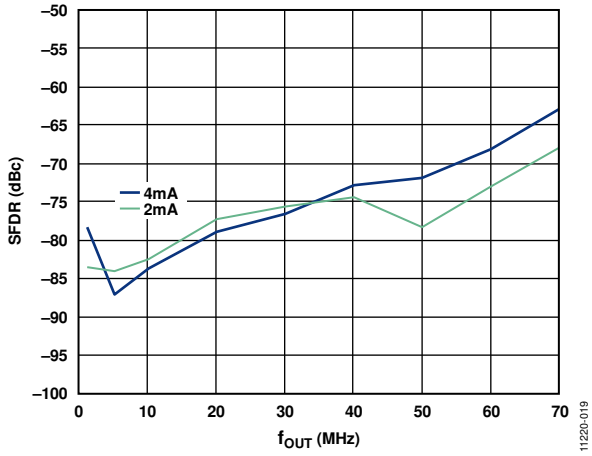

Figure 19. SFDR at Two I_{OUTFS} Values vs. f_{OUT}

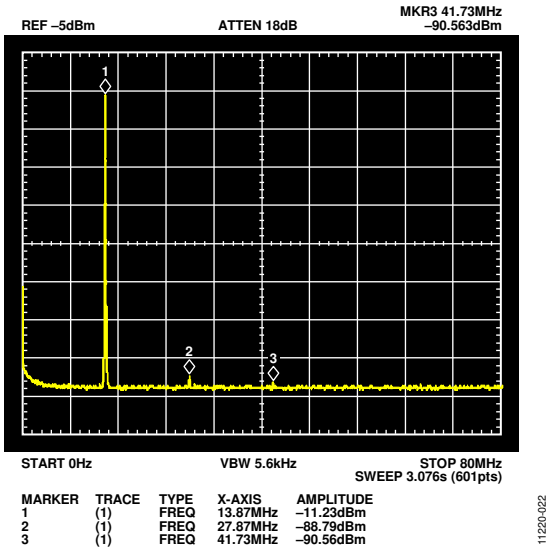

Figure 22. Output Spectrum, f_{OUT} = 13.87 MHz

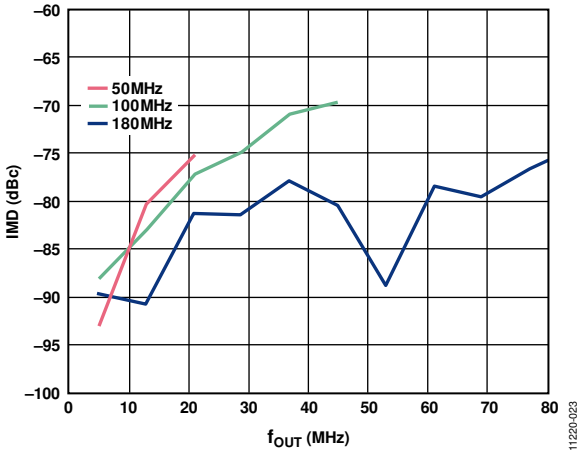

Figure 23. IMD vs. f_{OUT}, Three f_{OUT} Values

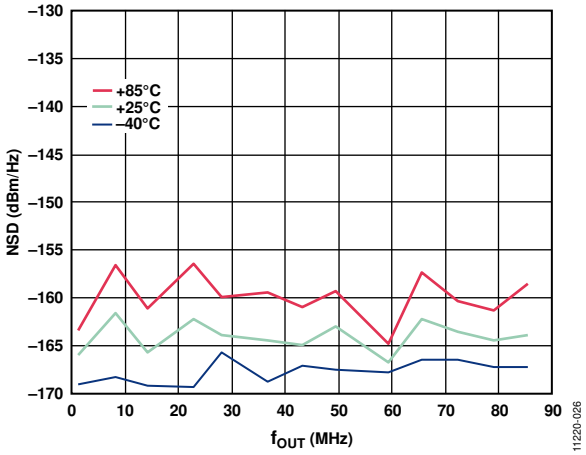

Figure 26. NSD vs. f_{OUT} at Three Temperatures

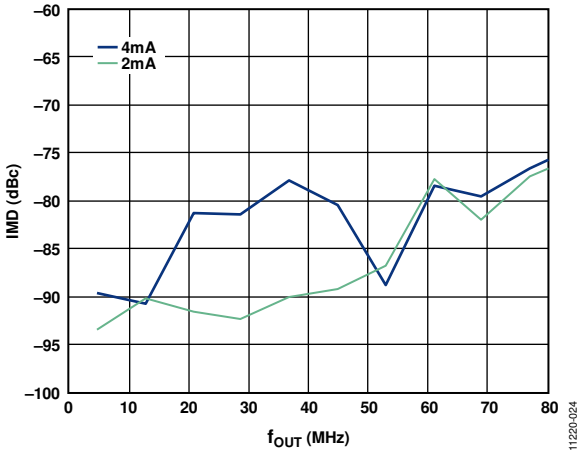

Figure 24. IMD vs. f_{OUT}, Two I_{OUTFS} Values

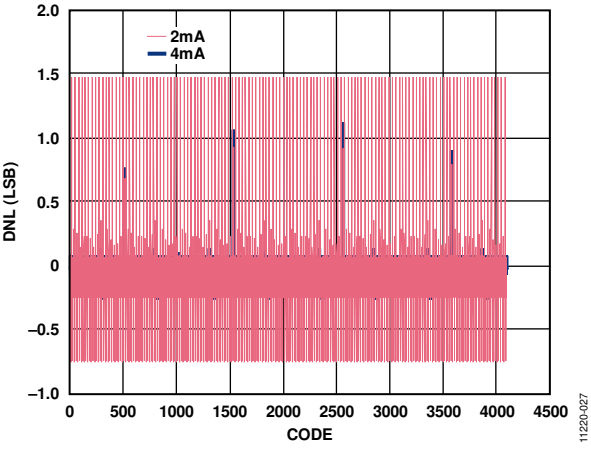

Figure 27. DNL, Two I_{OUTFS} Values

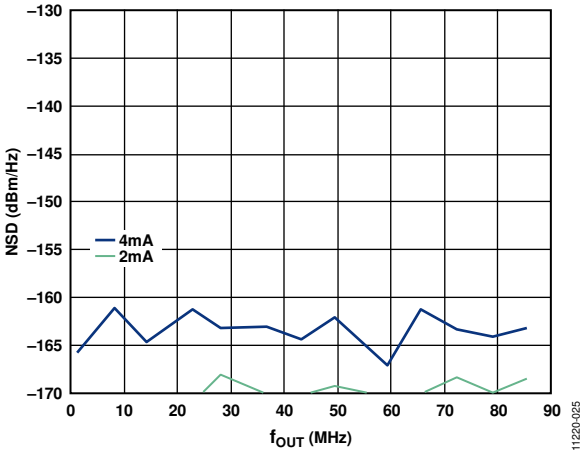

Figure 25. NSD vs. f_{OUT}, Two I_{OUTFS} Values

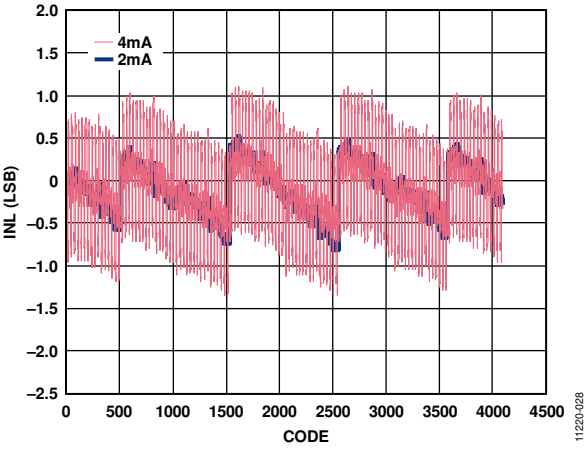

Figure 28. INL, Two I_{OUTFS} Values

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A digital-to-analog converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
Offset error is the deviation of the output current from the ideal of zero. For IOUTP, 0 mA output is expected when the inputs are all 0s. For IOUTN, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1, minus the output when all inputs are set to 0. The ideal gain is calculated using the measured V_{REF}. Therefore, the gain error does not include effects of the reference.

Output Compliance Voltage
Output compliance voltage is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
Power supply rejection is the maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in picovolt-seconds (pV-s).

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Noise Spectral Density (NSD)
Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone.

THEORY OF OPERATION

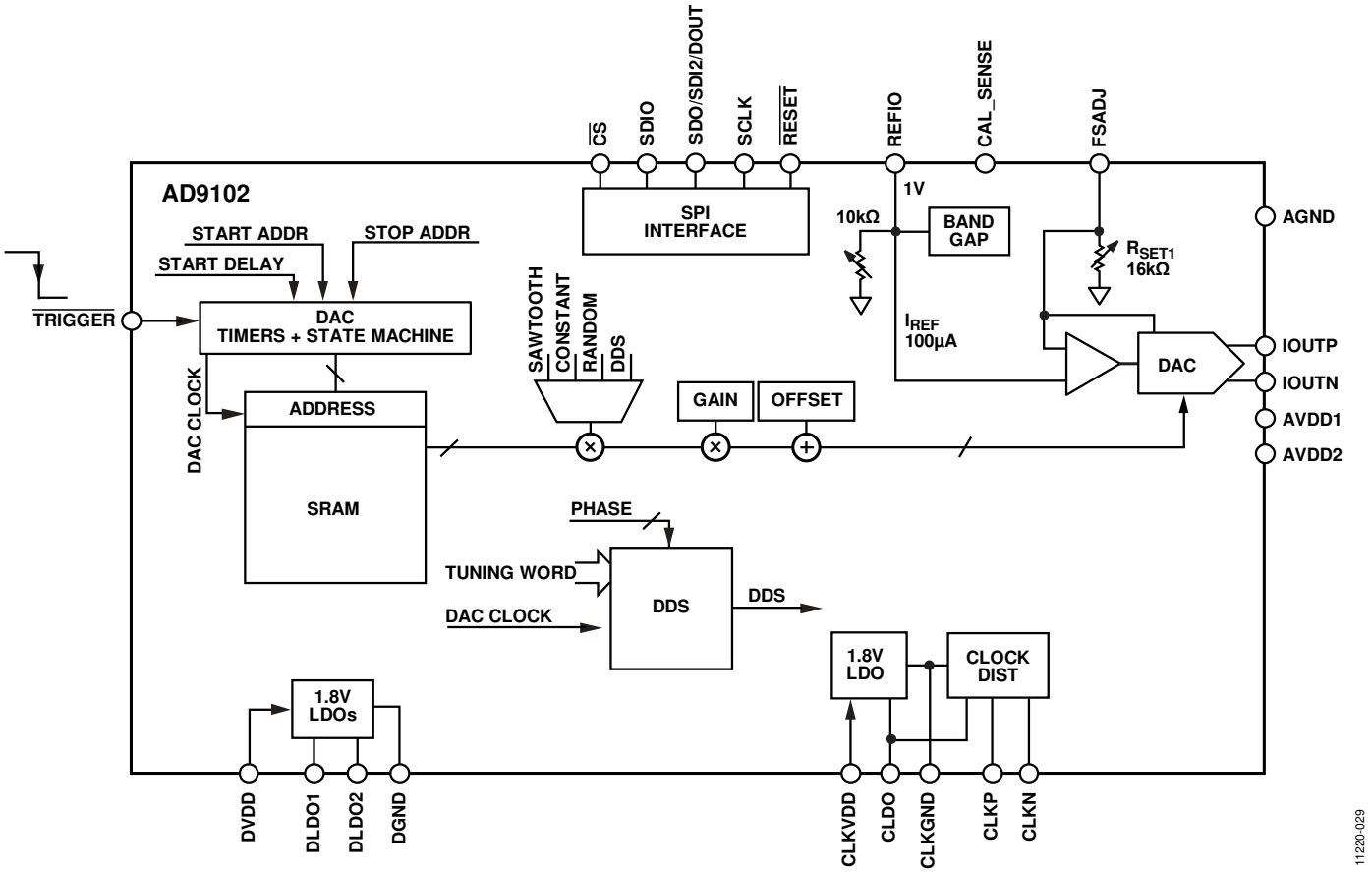

Figure 29. AD9102 Block Diagram

Figure 29 is a block diagram of the AD9102. The AD9102 has a single 14-bit current output DAC.

An on-chip band gap reference is included. Optionally, an off-chip voltage reference may be used. The full-scale DAC output current, also known as gain, is governed by the current, I_{REF}. I_{REF} is the current that flows through the I_{REF} resistor. The I_{REF} set resistor can be on or off chip at the user's discretion. When the on-chip R_{SET} resistor is in use, DAC gain accuracy can be improved by employing the built in automatic gain calibration capability. Automatic calibration can be used with the on-chip reference or an external REFIO voltage. A procedure for automatic gain calibration follows.

The power supply rails for the AD9102 are AVDD for analog circuits, CLKVDD/CLKLDO for clock input receivers, and DVDD/DLDO1/DLDO2 for digital I/O and for the on-chip digital datapath. AVDD, DVDD, and CLKVDD can range from 1.8 V to 3.3 V nominal. DLDO1, DLDO2, and CLDO run at 1.8 V. If DVDD = 1.8 V, connect DLDO1 and DLDO2 to DVDD, with the on-chip LDOs disabled. All three supplies are provided externally in this case. If CLKVDD = 1.8 V, connect CLKVDD to CLDO with the on-chip LDOs enabled.

Digital signals input to the 14-bit DAC are generated by on-chip digital waveform generation resources. The 14-bit samples are input to the DAC at the CLKP/CLKN sample rate from the digital datapath. The datapath includes gain and offset corrections and a digital waveform source selection multiplexer. Waveform sources are SRAM, direct digital synthesizer (DDS), DDS output amplitude modulated by SRAM data, sawtooth generator, dc constant, and pseudorandom sequence generator. The waveforms output by the source selection multiplexer have programmable pattern characteristics. The waveforms can be set up to be continuous, continuous pulsed (fixed pattern period and start delay within each pattern period), or finite pulsed (a set number of pattern periods are output, then the pattern stops).

Pulsed waveforms (finite or continuous) have a programmed pattern period and start delay. The waveform is present in each pulse period following the programmed pattern period start and the start delay.

A SPI port enables loading of data into SRAM and programming of all the control registers inside the device.

SPI PORT

The AD9102 provides a flexible, synchronous serial communications (SPI) port that allows easy interfacing to ASICs, FPGAs, and industry-standard microcontrollers. The interface allows read/write access to all registers that configure the AD9102 and to the on-chip SRAM. Its data rate can be up to the SCLK clock speed listed in Table 3 and Table 4.

The SPI interface operates as a standard synchronous serial communication port. $\overline{CS}$ is a low true chip select. When $\overline{CS}$ goes true, SPI address and data transfer begin. The first bit coming from the SPI master on SDIO is a read write indicator (high for read, low for write). The next 15 bits are the initial register address. The SPI port automatically increments the register address if $\overline{CS}$ stays low beyond the first data-word allowing writes to or reads from a set of contiguous addresses.

Table 12. Command Word

MSB							LSB
DB15	**DB14**	**DB13**	**DB12**	**...**	**DB2**	**DB1**	**DB0**
R/$\overline{W}$	A14	A13	A12	…	A2	A1	A0

When the first bit of this command byte is a logic low (R/$\overline{W}$ bit = 0), the SPI command is a write operation. In this case, SDIO remains an input; see Figure 30.

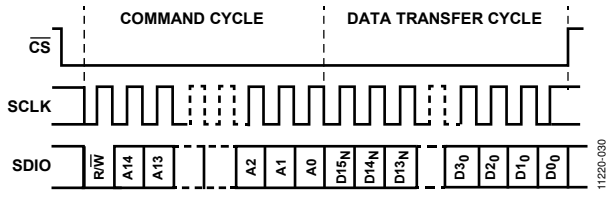

Figure 30. Serial Register Interface Timing, MSB First Write, 3-Wire SPI

When the first bit of this command byte is a logic high (R/$\overline{W}$ bit = 1), the SPI command is a read operation. In this case, data is driven out of the SPI port as shown in Figure 31 and Figure 33. The SPI communication finishes after the $\overline{CS}$ pin goes high.

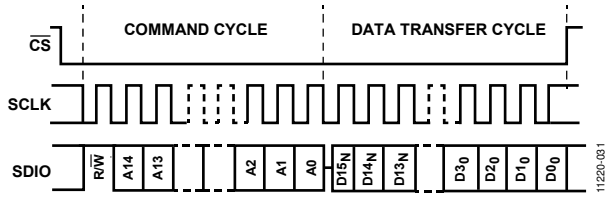

Figure 31. Serial Register Interface Timing, MSB First Read, 3-Wire SPI

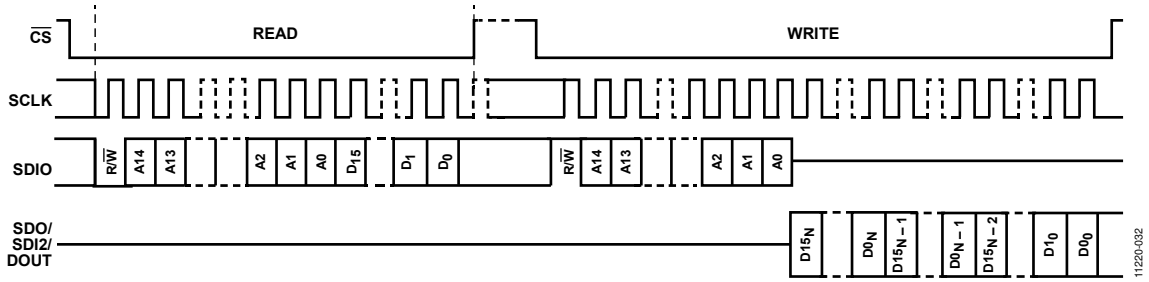

Figure 33. Serial Register Interface Timing, MSB First Read, 4-Wire SPI

Writing to On-Chip SRAM

The AD9102 includes an internal 4096 × 12 SRAM. The SRAM address space is 0x6000 to 0x6FFF of the AD9102 SPI address map.

Double SPI for Write for SRAM

The time to write data to the entire SRAM can be halved using the SPI access mode shown in Figure 32. The SDO/SDI2/DOUT line becomes a second serial data input line, doubling the achievable update rate of the on-chip SRAM. SDO/SDI2/DOUT is write only in this mode. The entire SRAM can be written in $(2 + 2 \times 4096) \times 8/(2 \times f_{SLCK})$ seconds.

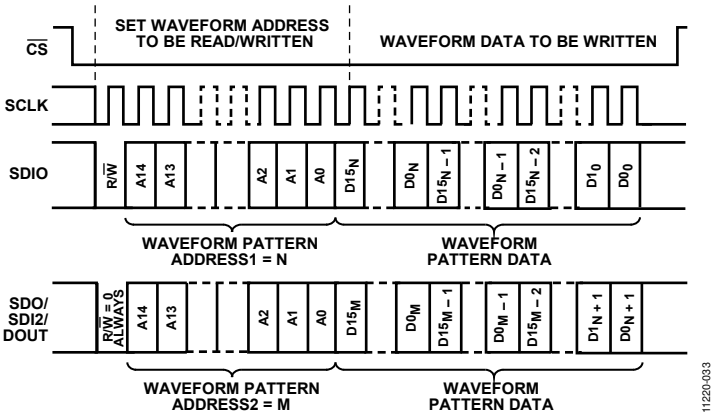

Figure 32. Double SPI Write of SRAM Data

Configuration Register Update Procedure

Most SPI accessible registers are double buffered. An active register set controls operation of the AD9102 during pattern generation. A set of shadow registers stores updated register values. Register updates can be written at any time. When configuration update is complete, the user writes a 1 to the UPDATE bit in the RAMUPDATE register. The UPDATE bit arms the register set for transfer from shadow registers to active registers. The AD9102 performs this transfer automatically the next time the pattern generator is off. This procedure does not apply to the 4k × 14 SRAM. For the SRAM update procedure, see the SRAM section.

DAC TRANSFER FUNCTION

The AD9102 DAC provides a differential current output, IOUTP/IOUTN.

The DAC output current equations are as follows:

$$IOUTP = I_{OUTFS} \times DAC\ INPUT\ CODE/2^{14} \quad (1)$$

$$IOUTN = I_{OUTFS} \times ((2^{14} - 1) - DAC\ INPUT\ CODE)/2^{14} \quad (2)$$

where *DAC INPUT CODE* = 0 to $2^{14} - 1$. Full-scale current or DAC Gain I_{OUTFS} is 32 times I_{REF}.

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where $I_{REF} = V_{REFIO}/R_{SET}$.

I_{REF} is the current that flows through the I_{REF} resistor. The I_{REF} resistor may be on or off chip at the users' discretion. When an on-chip R_{SET} resistor is in use, DAC gain accuracy can be improved by employing the built-in automatic gain calibration capability.

ANALOG CURRENT OUTPUTS

Optimum linearity and noise performance of DAC outputs can be achieved when they are connected differentially to an amplifier or a transformer. In these configurations, common-mode signals at the DAC outputs are rejected.

The output compliance voltage specifications listed in Table 1 and Table 2 must be adhered to for the performance specifications in those tables to be met.

SETTING I_{OUTFS}, DAC GAIN

As expressed in Equation 3, DAC gain (I_{OUTFS}) is a function of the reference voltage at the REFIO terminal and R_{SET}.

Voltage Reference

The AD9102 contains an internal 1.0 V nominal band gap reference. The internal reference can be used, or replaced by a more accurate off-chip reference. An external reference can provide tighter reference voltage tolerances and/or lower temperature drift than the on-chip band gap.

By default, the on-chip reference is powered up and ready to be used. When using the on-chip reference, the REFIO terminal needs to be decoupled to AGND using a 0.1 µF capacitor as shown in Figure 34.

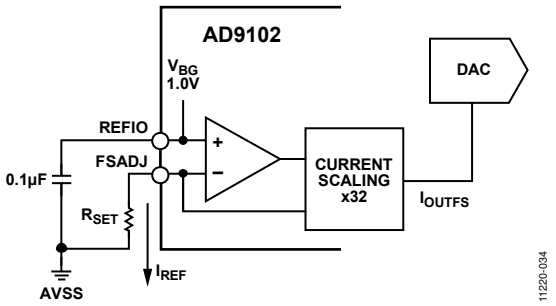

Figure 34. On-Chip Reference with External R_{SET} Resistor

Table 13 summarizes reference connections and programming.

Table 13. Reference Operation

Reference Mode	REFIO Pin
Internal	Connect 0.1µF capacitor
External	Connect off-chip reference

When using an external reference, it is recommended to apply the external reference to the REFIO pin.

Programming Internal V_{REFIO}

The internal REFIO voltage level is programmable.

When the internal voltage reference is in use, the BGDR field in the lower six bits in Register 0x03 adjusts the V_{REFIO} level. This adds or subtracts up to 20% from the nominal band gap voltage on REFIO. The voltage across the FSADJ resistor tracks this change. As a result, I_{REF} varies by the same amount. Figure 35 shows V_{REFIO} vs. BGDR code for an on-chip reference with a default voltage (BGDR = 0x00) of 1.04 V.

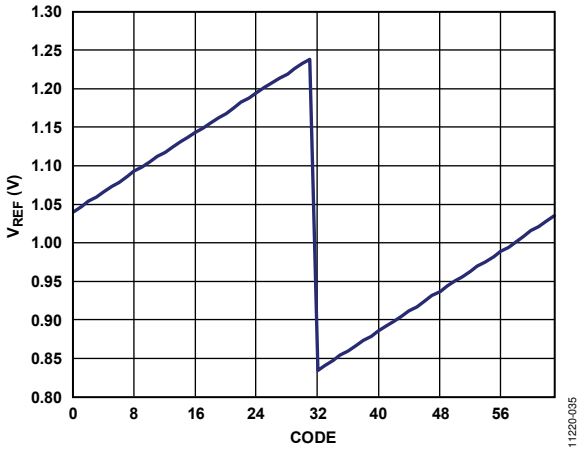

Figure 35. Typical V_{REFIO} Voltage vs. BGDR

R_{SET} Resistors

R_{SET} in the where statement for Equation 3 can be an internal resistor or a board level resistor of the user's choosing connected to the FSADJ terminal.

To make use of the on-chip R_{SET} resistor, set Bit 15 of the FSADJ register to Logic 1. Bits[4:0] of the FSADJ register are used to program values for the on-chip R_{SET} manually.

AUTOMATIC I_{OUTFS} CALIBRATION

Many applications require tight DAC gain control. The AD9102 provides an automatic I_{OUTFS} calibration procedure used with an on-chip R_{SET} resistor only. The voltage reference, V_{REFIO}, can be the on-chip reference or an off-chip reference. The automatic calibration procedure does a fine adjustment of the internal R_{SET} value and the current, I_{REF}.

When using automatic calibration, the following board level connections are required:

1. Connect the FSADJ pin and the CAL_SENSE pin together.
2. Install a resistor between the CAL_SENSE pin and AGND. To calculate the value of this resistor, use the following equation:

$$R_{CAL\_SENSE} = 32 \times V_{REFIO}/I_{OUTFS}$$

where I_{OUTFS} is the target full-scale current.

Automatic calibration uses an internal clock. This calibration clock is equal to the DAC clock divided by the division factor chosen by the CAL_CLK_DIV bits of Register 0x0D. Each calibration cycle is between 4 and 512 DAC clock cycles, depending on the value of CAL_CLK_DIV[2:0]. The frequency of the calibration clock should be less than 500 kHz.

To perform an automatic calibration, the following steps must be followed:

1. Set the calibration ranges in Register 0x008[7:0] and Register 0x0D[5:4] to their minimum values to allow best calibration.
2. Enable the calibration clock bit, CAL_CLK_EN, in Register 0x0D.
3. Set the divider ratio for the calibration clock by setting the CAL_CLK_DIV[2:0] bits in Register 0x0D. The default is 512.
4. Set the CAL_MODE_EN bit in Register 0x0D to Logic 1.
5. Set the START_CAL bit in Register 0x0E to Logic 1. This begins the calibration of the comparator, R_{SET}, and gain.
6. The CAL_MODE flag in Register 0x0D goes to Logic 1 while the part is calibrating. The CAL_FIN flag in Register 0x0E goes to Logic 1 when the calibration is complete.
7. Set the START_CAL bit in Register 0x0E to Logic 0.
8. After calibration, verify that the overflow and underflow flags in Register 0x0D are not set (Bits[14:8]). If they are set, change the corresponding calibration range to the next larger range and start from Step 5 again.
9. If no flag is set, read the DAC_RSET_CAL and DAC_GAIN_CAL values in the DACRSET and DACAGAIN registers respectively and write them into their corresponding DAC_RSET and DAC_GAIN register fields.
10. Reset the CAL_MODE_EN bit and the calibration clock bit, CAL_CLK_EN, in Register 0x0D to Logic 0 to disable the calibration clock.
11. Set the CAL_MODE_EN bit in Register 0x0D to Logic 0. This points the R_{SET} and gain control muxes toward the regular registers.
12. Disable the calibration clock bit CAL_CLK_EN in Register 0x0D.

To reset the calibration, pulse the CAL_RESET bit in Register 0x0D to Logic 1 and Logic 0, pulse the $\overline{\text{RESET}}$ pin, or pulse the RESET bit in the SPICONFIG register.

CLOCK INPUT

For optimum DAC performance, the AD9102 clock input signal pair (CLKP/CLKN) should be a very low jitter, fast rise time differential signal. The clock receiver generates its own common-mode voltage, requiring these two inputs to be ac-coupled.

Figure 36 shows the recommended interface to a number of Analog Devices LVDS clock drivers that work well with the AD9102. A 100 Ω termination resistor and two 0.1 µF coupling capacitors are used. Figure 38 is an interface to an Analog Devices differential PECL driver. Figure 39 shows a single-ended to differential converter using a balun driving CLKP/CLKN.

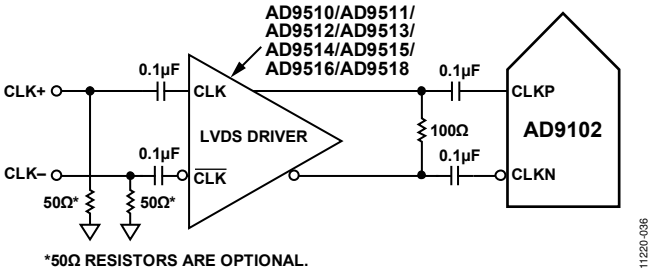

Figure 36. Differential LVDS Clock Input

In applications where the analog output signals are at low frequencies, the AD9102 clock input can be driven with a single-ended CMOS signal. Figure 37 shows such an interface. CLKP is driven directly from a CMOS gate, and the CLKN pin is bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor. The optional resistor is a series termination.

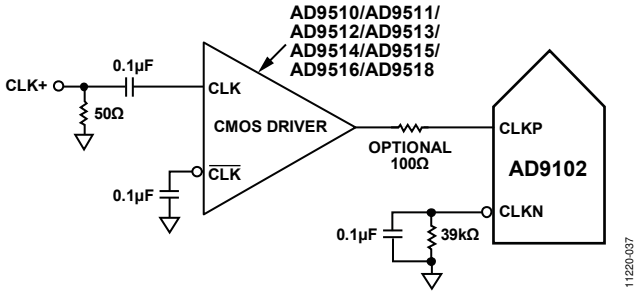

Figure 37. Single-Ended 1.8 V CMOS Sample Clock

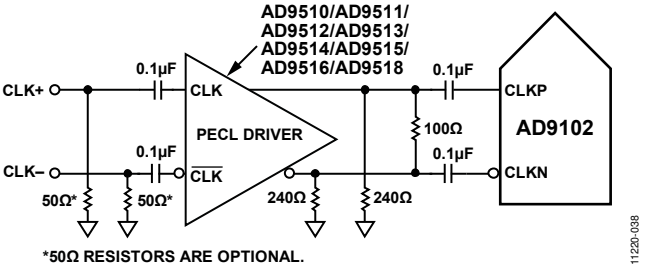

Figure 38. Differential PECL Sample Clock

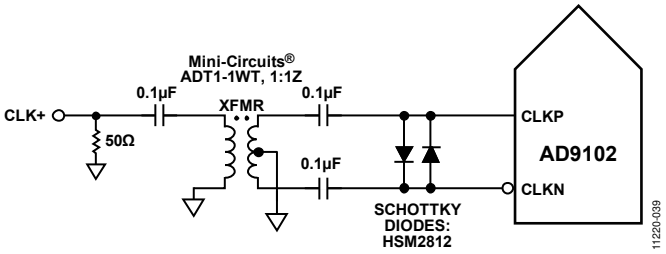

Figure 39. Transformer Coupled Clock

DAC OUTPUT CLOCK EDGE

The DAC can be configured to output samples on the rising or falling edge of the CLKP/CLKN clock input by configuring the DAC_INV_CLK bit in the CLOCKCONFIG register (Register 0x02). This functionality sets the DAC output timing resolution at $1/(2 \times f_{CLKP/CLKN})$.

GENERATING SIGNAL PATTERNS

The AD9102 can generate three types of signal patterns under control of its programmable pattern generator.

- Continuous waveforms
- Periodic pulse train waveforms that repeat indefinitely
- Periodic pulse train waveforms that repeat a finite number of times

RUN Bit

Setting the RUN bit in the PAT_STATUS register (Register 0x1E) to 1 arms the AD9102 for pattern generation. Clearing this bit shuts down the pattern generator as shown in Figure 43.

$\overline{\text{TRIGGER}}$ Pin

A falling edge on the $\overline{\text{TRIGGER}}$ pin starts the generation of a pattern. If the RUN bit is set to 1, the falling edge of the $\overline{\text{TRIGGER}}$ pin starts the pattern generation. As shown in Figure 41, the pattern generator state goes to pattern on a number of CLKP/CLKN clock cycles following the falling edge of the $\overline{\text{TRIGGER}}$ pin. This delay is programmed in the PATTERN_DELAY bit field.

The rising edge on the $\overline{\text{TRIGGER}}$ pin is a request for termination of pattern generation; see Figure 42.

PATTERN Bit (Read Only)

When the read only PATTERN bit in the PAT_STATUS register is set to 1, it indicates that the pattern generator is in the pattern on state. A 0 indicates that the pattern generator is in the pattern off state.

Pattern Types

- Continuous waveforms are output by the DAC for the duration of the pattern on state of the pattern generator. Continuous waveforms ignore pattern periods.
- Periodic pulse trains that repeat indefinitely are waveforms that are output once during each pattern period. Pattern periods occur one after the other as long as the pattern generator is in the pattern on state.
- Periodic pulse trains that repeat a finite number of times are the same as those that repeat indefinitely, except that the waveforms are output during a finite number of consecutive pattern periods.

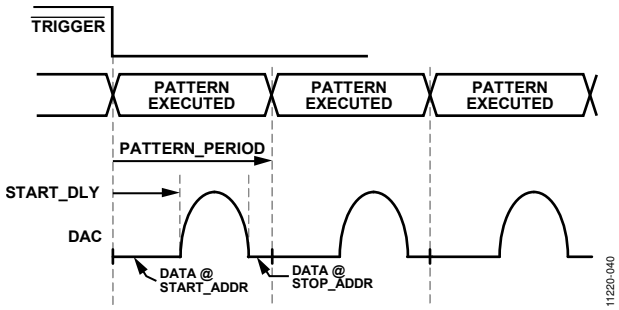

Figure 40. Periodic Pulse Trains Output on All DACs

PATTERN GENERATOR PROGRAMMING

Figure 40 shows periodic pulse train waveforms as seen at the output to each of the DACs. The waveform is generated in each pattern period. The start delay (START_DLY) is the delay between the start of each pattern period and the start of the waveform. The DAC waveform is a digital signal stored in SRAM and multiplied by the DAC digital gain factor. The SRAM data is read using the DAC address counter.

Setting Pattern Period

Two register bit fields are used to set the pattern period. The PAT_PERIOD_BASE field in the PAT_TIMEBASE register sets the number of CLKP/CLKN clocks per PATTERN_PERIOD LSB. The PATTERN_PERIOD is programmed in the PAT_PERIOD register. The longest pattern period available is $65,535 \times 16/f_{CLKP/N}$.

Setting Waveform Start Delay Base

The waveform start delay base is programmed in the START_DELAY_BASE bits of the PAT_TIMEBASE register (Register 0x28[3:0]). The START_DELAY register (Register 0x5C) is described in the DAC Input Datapaths section. The start delay base determines how many CLKP/CLKN clock cycles there are per START_DELAY LSB.

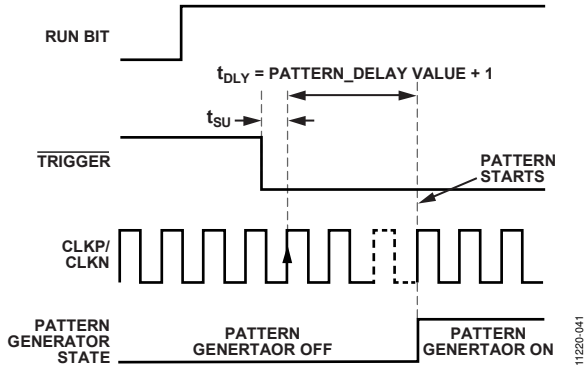

Figure 41. $\overline{\text{TRIGGER}}$ Pin Initiated Pattern Start with Pattern Delay

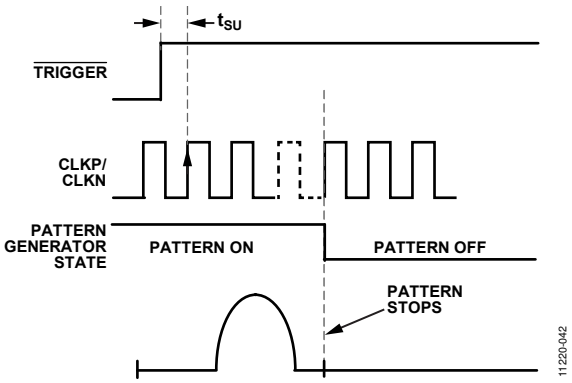

Figure 42. Trigger Rising Edge Initiated Pattern Stop

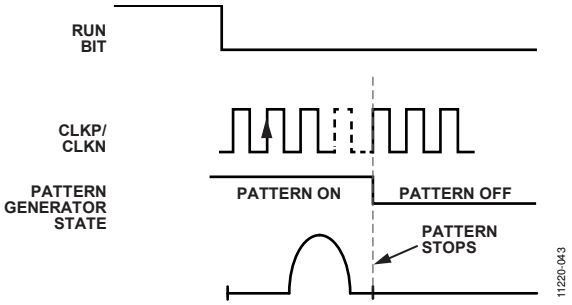

Figure 43. RUN Bit Driven Pattern Stop

DAC INPUT DATAPATHS

Timing in the DAC datapaths is governed by the pattern generator. The datapath includes a waveform selector, a waveform repeat controller, RAM output and DDS output multiplier (RAM output can amplitude modulate DDS output), DDS cycle counter, DAC digital gain multiplier, and a DAC digital offset summer.

DAC Digital Gain Multiplier

On its way into the DAC, the samples are multiplied by a 12-bit gain factor that has a range of ±2.0. These gain values are programmed in the DAC_DGAIN register (Register 0x35).

DAC Digital Offset Summer

DAC input samples are summed with a 12-bit dc offset value. The dc offset values are programmed in the DACDOF register (Register 0x25).

DAC Waveform Selectors

Waveform selector inputs are:

- Sawtooth generator output
- Pseudorandom sequence generator output
- DC constant generator output
- Pulsed, phase shifted DDS sine wave output
- RAM output
- Pulsed, phase shifted DDS sine wave output amplitude, modulated by RAM output

Waveform selection for the DAC is made by programming the WAV_CONFIG register (Register 0x27).

Pattern Period Repeat Controller

The PATTERN_RPT bit in the PAT_TYPE register (Register 0x1F[0]) controls whether the pattern output auto repeats (periodic pulse train repeats indefinitely) or repeats a number of consecutive times defined by the DAC_REPEAT_CYCLE bits in Register 0x2B. The latter are periodic pulse trains that repeat a finite number of times.

Number of DDS Cycles

The DAC input datapath establishes the pulse width of the sine wave output from the DDS in a number of sine wave cycles. The cycle counts are programmed in the DDS_CYC register.

DDS Phase Shift

The DAC input datapath shifts the phase of the output of the single common DDS. The phase shift is programmed using the DDS_PHASE field.

DOUT FUNCTION

In applications where the AD9102 DAC drives a high voltage amplifier, such as in ultrasound transducer array element driver signal chains, it can be useful to turn on and off each amplifier at precise times relative to the waveform generated by the AD9102 DAC. The SDO/SDI2/DOUT terminal can be configured to provide this function.

The SPI interface needs to be configured in 3-wire mode (Figure 30 and Figure 31). This is accomplished by setting the SPI3WIRE or SPI3WIREM bits in the SPICONFIG register (Register 0x00). When the SPI_DRV or SPI_DRVM bits of the SPICONFIG register are set to Logic 1, the SDO/SDI2/DOUT terminal provides the DOUT function.

Manually Controlled DOUT

If the DOUT_MODE bit = 0 in the DOUT_CONFIG register (Register 0x2D), DOUT can be turned on or off using the DOUT_VAL bit of that same register.

Pattern Generator Controlled DOUT

Figure 44 depicts the rising edge of a pattern generator controlled DOUT pulse. Figure 45 shows the falling edge. A pattern generator controlled DOUT is set up by setting the DOUT_MODE bit = 1. Next, the start delay is programmed in the DOUT_START register (Register 0x2C) and the stop delay is programmed into the DOUT_STOP bit of the DOUT_CONFIG register.

DOUT goes high when DOUT_START[15:0] CLKP/$\overline{\text{CLKN}}$ cycles after the falling edge of the signal input to the $\overline{\text{TRIGGER}}$ pin. DOUT stays high as long as a pattern is being generated. DOUT goes low when DOUT_STOP[3:0] CLKP/CLKN cycles after the clock edge that causes pattern generation to stop.

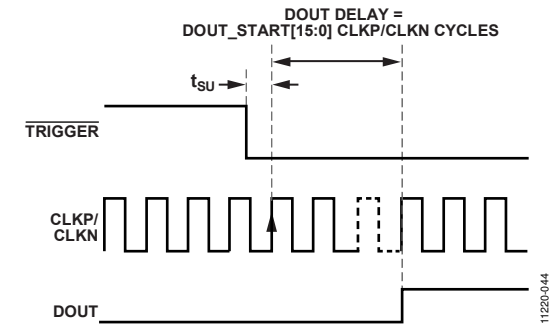

Figure 44. DOUT Start Sequence

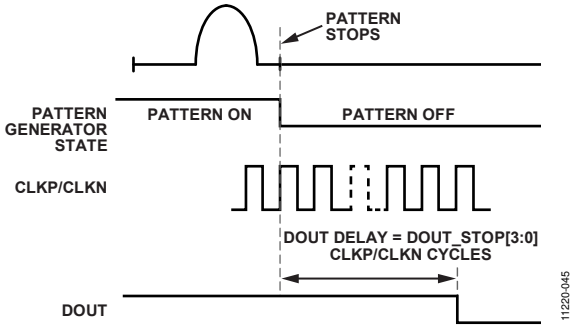

Figure 45. DOUT Stop Sequence

DIRECT DIGITAL SYNTHESIZER (DDS)

The DDS generates sinusoid at a frequency determined by its tuning word input. The tuning word is 24 bits wide. The resolution of DDS tuning is $f_{CLKP/N}/2^{24}$. The DDS output frequency is DDS_TW × $f_{CLKP/N}/2^{24}$.

The DDS tuning word is programmed using one of two methods. For a fixed frequency, the DDSTW_MSB and DDSTW_LSB bit fields are programmed with a constant. When the frequency of the DDS needs to change within each pattern period, a sequence of values stored in SRAM is combined with a selection of DDSTW_MSB bits to form the tuning word.

SRAM

The AD9102 4k × 14 SRAM can contain signal samples, amplitude modulation patterns, lists of DDS tuning words, or lists of DDS output phase offset words. Any SRAM data address can be written to and read from the SPI port as long as the SRAM is not actively engaged in pattern generation (RUN bit = 0). To write to any SRAM address, set up the PAT_STATUS register (Register 0x1E) as follows:

- BUF_READ = 0
- MEM_ACCESS = 1
- RUN = 0

To read data from any SRAM address, set up the PAT_STATUS as follows:

- BUF_READ = 1
- MEM_ACCESS = 1
- RUN = 0

The AD9102 allows SPI read/write access to the SRAM while the SRAM is actively engaged in pattern generation (RUN = 1) with some restrictions.

The SPI port address space for SRAM is Location 0x6000 through Location 0x6FFF.

SRAM can be accessed using any of the SPI operating modes shown in Figure 30 through Figure 32. Using the SPI modes of operation shown in Figure 31 and Figure 33, the entire SRAM can be written in (2 + 2 × 4096) ×8/f_{SLCK} seconds.

When the PAT_STATUS register RUN bit =1 (pattern generation enabled) data is read using the SRAM address counter. The address counter has a START_ADDR (start address) and STOP_ADDR (stop address). During each pattern period, data is read from SRAM after the START_DELAY period and while each address counter is incrementing.

While the PAT_STATUS register RUN bit = 1 (pattern generation enabled), data can be written to or read from SRAM via the SPI port outside the address range defined by START_ADDR and STOP_ADDR.

Incrementing Pattern Generation Mode SRAM Address Counters

The SRAM address counter can be programmed to be incremented by CLKP/CLKN (default) or by the rising edge of the DDS MSB. The DDS_MSB_EN bit in the DDS_CONFIG register makes this selection. For example, DDS MSB can be used to clock the address counter when generating a chirp waveform from the DDS using a list of tuning words in SRAM. Each frequency setting dwells for one DDS output sine wave cycle.

SAWTOOTH GENERATOR

When sawtooth is selected in the PRESTORE_SEL bits in the WAV_CONFIG register, the sawtooth generator is connected to the DAC digital datapath.

Sawtooth types, shown in Figure 46, are selected using the SAW_TYPE bits in the SAW_CONFIG register. The number of samples per sawtooth waveform step is programmed in the SAW_STEP bits.

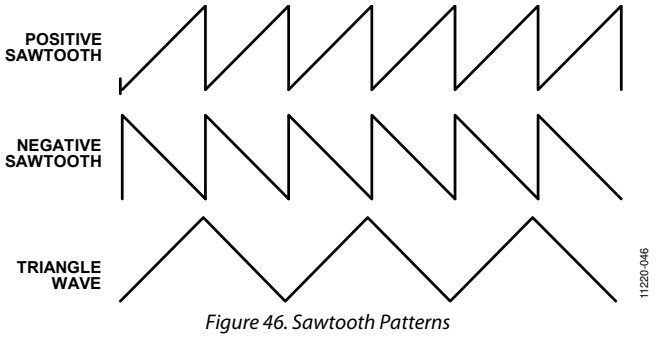

Figure 46. Sawtooth Patterns

PSEUDORANDOM SIGNAL GENERATOR

The pseudorandom noise generator generates a noise signal on each DAC output when a pseudorandom sequence is selected in the PRESTORE_SEL fields in the WAV_CONFIG register. Pseudorandom noise signals are generated as continuous waveforms only.

DC CONSTANT

A programmable dc current between 0.0 and I_{OUTFS} can be generated on the DAC when a constant value is selected in the PRESTORE_SEL bits of the WAV_CONFIG register. DC constant current is generated as a continuous waveform only.

The dc current level is programmed by writing to the DAC_CONST field in the appropriate DAC_CST register.

POWER SUPPLY NOTES

The AD9102 supply rails are specified in Table 9. The AD9102 includes three on-chip linear regulators. The supply rails driven by these regulators are run at 1.8 V. Some usage rules for these regulators include:

- When CLKVDD is 2.5 V or higher, the 1.8 V on-chip CLDO regulator may be used. If CLKVDD = 1.8 V, the CLDO regulator must be disabled by setting the PDN_LDO_CLK bit in the POWERCONFIG register. CLKVDD and CLDO are connected together.
- When DVDD is 2.5 V or higher, the 1.8 V on-chip DLDO1 and DLDO2 regulators may be used. If DVVD is 1.8 V, the DLDO1 and DLDO2 regulators must be disabled by setting the PDN_LDO_DIG1 and PDN_LDO_DIG2 bits in the POWERCONFIG register. DVDD, DLDO1, and DLDO2 are connected together.

POWER DOWN CAPABILITIES

The POWERCONFIG register lets the user place the AD9102 in a reduced power dissipation configuration while the CLKP/CLKN input is running and the power supplies are on. The DAC can be put to sleep by setting the DAC_SLEEP bit in the POWERCONFIG register. Clocking of the waveform generator and the DACs can be turned on and off by setting the CLK_PDN bit in the CLOCKCONFIG register. Taking these actions places the AD9102 in the power down mode, specified in Table 8.