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Dual Low Power, 8-/10-/12-/14-Bit TxDAC Digital-to-Analog Converters

Data Sheet

AD9114/AD9115/AD9116/AD9117

FEATURES

Power dissipation @ 3.3 V, 20 mA output

191 mW @ 10 MSPS

232 mW @ 125 MSPS

Sleep mode: <3 mW @ 3.3 V

Supply voltage: 1.8 V to 3.3 V

SFDR to Nyquist

86 dBc @ 1 MHz output

85 dBc @ 10 MHz output

AD9117 NSD @ 1 MHz output, 125 MSPS, 20 mA: -162 dBc/Hz

Differential current outputs: 2 mA to 20 mA

2 on-chip auxiliary DACs

CMOS inputs with single-port operation

Output common mode: adjustable 0 V to 1.2 V

Small footprint 40-lead LFCSP RoHS-compliant package

APPLICATIONS

Wireless infrastructures

Picocell, femtocell base stations

Medical instrumentation

Ultrasound transducer excitation

Portable instrumentation

Signal generators, arbitrary waveform generators

GENERAL DESCRIPTION

The AD9114/AD9115/AD9116/AD9117 are pin-compatible dual, 8-/10-/12-/14-bit, low power digital-to-analog converters (DACs) that provide a sample rate of 125 MSPS. These TxDAC[®] converters are optimized for the transmit signal path of communication systems. All the devices share the same interface, package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost.

The AD9114/AD9115/AD9116/AD9117 offer exceptional ac and dc performance and support update rates up to 125 MSPS.

The flexible power supply operating range of 1.8 V to 3.3 V and low power dissipation of the AD9114/AD9115/AD9116/AD9117 make them well suited for portable and low power applications.

PRODUCT HIGHLIGHTS

1. **Low Power.** DACs operate on a single 1.8 V to 3.3 V supply; total power consumption reduces to 225 mW at 100 MSPS. Sleep and power-down modes are provided for low power idle periods.
2. **CMOS Clock Input.** High speed, single-ended CMOS clock input supports a 125 MSPS conversion rate.
3. **Easy Interfacing to Other Components.** Adjustable output common mode from 0 V to 1.2 V allows for easy interfacing to other components that accept common-mode levels greater than 0 V.

Rev. C

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TABLE OF CONTENTS

Features	1	SPI Register Descriptions	36
Applications	1	Digital Interface Operation	40
General Description	1	Digital Data Latching and Retimer Section	41
Product Highlights	1	Estimating the Overall DAC Pipeline Delay	42
Revision History	3	Reference Operation	43
Functional Block Diagram	4	Reference Control Amplifier	43
Specifications	5	DAC Transfer Function	43
DC Specifications	5	Analog Output	44
Digital Specifications	7	Self-Calibration	44
AC Specifications	8	Coarse Gain Adjustment	45
Absolute Maximum Ratings	9	Using the Internal Termination Resistors	46
Thermal Resistance	9	Applications Information	47
ESD Caution	9	Output Configurations	47
Pin Configurations and Function Descriptions	10	Differential Coupling Using a Transformer	47
Typical Performance Characteristics	18	Single-Ended Buffered Output Using an Op Amp	47
Terminology	31	Differential Buffered Output Using an Op Amp	48
Theory of Operation	32	Auxiliary DACs	48
Serial Peripheral Interface (SPI)	33	DAC-to-Modulator Interfacing	49
General Operation of the Serial Interface	33	Correcting for Nonideal Performance of Quadrature	
Instruction Byte	33	Modulators on the IF-to-RF Conversion	49
Serial Interface Port Pin Descriptions	33	I/Q Channel Gain Matching	49
MSB/LSB Transfers	34	LO Feedthrough Compensation	50
Serial Port Operation	34	Results of Gain and Offset Correction	50
Pin Mode	34	Outline Dimensions	51
SPI Register Map	35	Ordering Guide	52

REVISION HISTORY**3/13—Rev. B to Rev. C**

Change to Features Section	1
Change to Endnote 1, Table 1	6
Changes to Figure 86 and Figure 88	34
Change to Table 13	35
Change to Version Register Description, Table 14	39
Changes to Table 17 and Reference Control Amplifier Section	43
Changes to Using the Internal Termination Resistors Section	46
Changes to Single-Ended Buffered Output Using an Op Amp Section	47
Changes to Differential Buffered Output Using an Op Amp Section	48
Updated Outline Dimensions.....	51

5/12—Rev. A to Rev. B

Changes to Table 1	5
Changes to Table 2	7
Changes to Table 3 and Table 4	8
Changes to Theory of Operation Section	32
Changes to SCLK—Serial Clock Section	33
Changes to Pin Mode Section.....	34
Changes to Table 14	37
Changes to Self-Calibration Section.....	44
Deleted Modifying the Evaluation Board to Use the ADL5370 On-Board Quadrature Modulator Section.....	51
Deleted Evaluation Board Schematics and Artwork Section and Figure 111 to Figure 133, Renumbered Sequentially.....	52
Updated Outline Dimensions.....	51
Changes to Ordering Guide.....	52
Deleted Bill of Materials Section and Table 18.....	75

3/09—Rev. 0 to Rev. A

Changes to Product Title and General Description Section	1
Changes to Figure 1	4
Changed $I_{OUTFS} = 2 \text{ mA}$ to $I_{XOUTFS} = 20 \text{ mA}$	5
Changes to Table 1	6
Changed $I_{OUTFS} = 2 \text{ mA}$ to $I_{XOUTFS} = 20 \text{ mA}$	7
Changes to Table 2	7
Changed DVDDIO = 1.8 V to DVDDIO = 3.3 V, Table 3 and CVDD = 3.3 V to CVDD = 1.8 V, Table 4	8
Changes to Table 5 and Table 6	9
Changes to Table 7	10
Changes to Table 8	12
Changes to Table 9	14
Changes to Table 10	16
Changes to Typical Performance Characteristics Section	18
Changes to Theory of Operation Section and Figure 84	32
Added Figure 85 to Figure 88; Renumbered Sequentially.....	34
Changes to Table 13	35
Changes to Table 14	36
Changes to Digital Interface Operation Section and Figure 89, Figure 90, Figure 91, Figure 92, and Figure 93.....	40
Changes to Figure 94, Digital Data Latching Section, and Retimer Section	41
Added Reference Operation Section, Reference Control Amplifier Section, DAC Transfer Function Section, Figure 96, and Table 17	43
Added Analog Output Section	44
Changes to Auxiliary DACs Section.....	48
Changes to DAC to Modulator Interfacing Section, Figure 107, and Figure 108	49
Added Figure 111 to Figure 133.....	52
Added Table 18	75

8/08—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

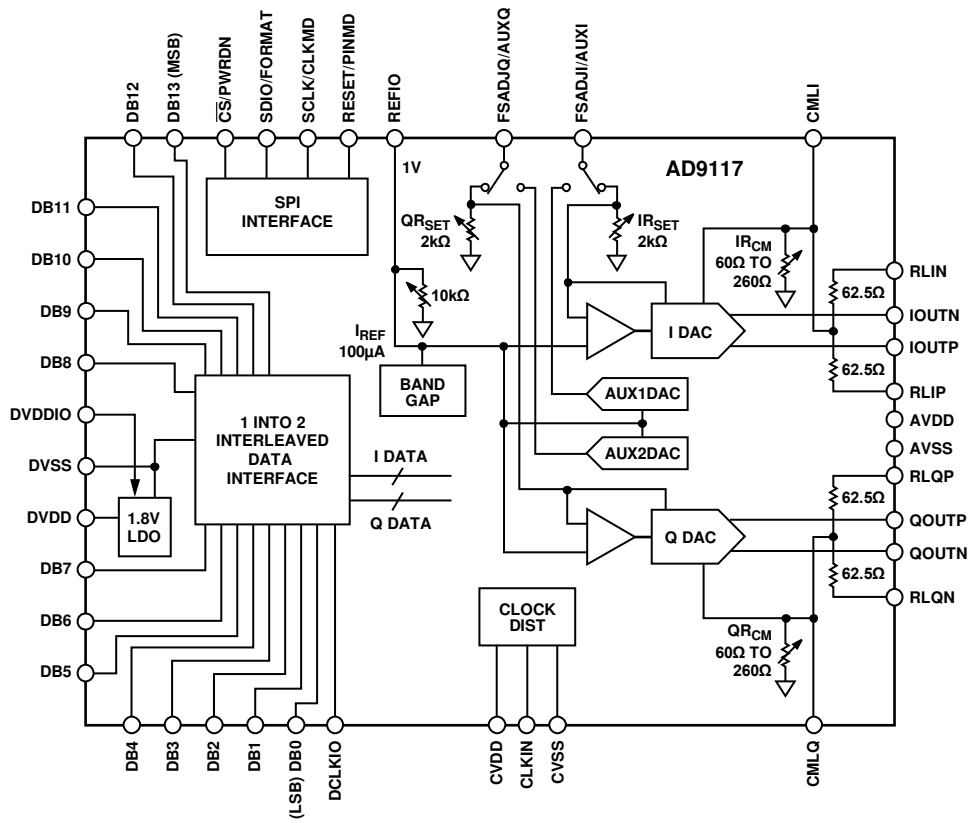


Figure 1.

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SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX} , AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{XOUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1.

Parameter	AD9114			AD9115			AD9116			AD9117			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION	8			10			12			14			Bits
ACCURACY, AVDD = DVDDIO = CVDD = 3.3 V													
Differential Nonlinearity (DNL)													
Pecalibration	±0.02			±0.06			±0.4			±1.4			LSB
Postcalibration	±0.02			±0.04			±0.2			±0.6			LSB
Integral Nonlinearity (INL)													
Pecalibration	±0.03			±0.19			±0.68			±1.2			LSB
Postcalibration	±0.03			±0.07			±0.42			±0.6			LSB
ACCURACY, AVDD = DVDDIO = CVDD = 1.8 V													
Differential Nonlinearity (DNL)													
Pecalibration	±0.02			±0.08			±0.5			±1.8			LSB
Postcalibration	±0.01			±0.06			±0.2			±1.0			LSB
Integral Nonlinearity (INL)													
Pecalibration	±0.04			±0.2			±0.5			±1.8			LSB
Postcalibration	±0.02			±0.1			±0.3			±1.1			LSB
MAIN DAC OUTPUTS													
Offset Error	-1		+1	-1		+1	-1		+1	-1		+1	mV
Gain Error Internal Reference	-2		+2	-2		+2	-2		+2	-2		+2	% of FSR
Full-Scale Output Current ¹													
AVDD = 3.3 V	2	8	20	2	8	20	2	8	20	2	8	20	mA
AVDD = 1.8 V	2		8	2		8	2		8	2		8	mA
Output Common-Mode Level (8 mA CMLx Pin)	-0.5	0	+1.2	-0.5	0	+1.2	-0.5	0	+1.2	-0.5	0	+1.2	V
Output Compliance Range													
AVDD = 3.3 V, 8 mA Output													
Common Mode Level = -0.5	-0.9		-0.1	-0.9		-0.1	-0.9		-0.1	-0.9		-0.1	V
Common Mode Level = 0	-0.4		+0.4	-0.4		+0.4	-0.4		+0.4	-0.4		+0.4	V
Common Mode Level = +1.2	0.8		1.5	0.8		1.5	0.8		1.5	0.8		1.5	V
Output Resistance	200			200			200			200			MΩ
Crosstalk, Q DAC to I DAC (f_{OUT} = 30 MHz)	95			95			95			95			dB
Crosstalk, Q DAC to I DAC (f_{OUT} = 60 MHz)	76			76			76			76			dB
MAIN DAC TEMPERATURE DRIFT													
Offset	0			0			0			0			ppm/°C
Gain	±40			±40			±40			±40			ppm/°C
Reference Voltage	±25			±25			±25			±25			ppm/°C

Parameter	AD9114			AD9115			AD9116			AD9117			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
AUXDAC OUTPUTS													
Resolution		10			10			10			10		Bits
Full-Scale Output Current (Current Sourcing Mode)		125			125			125			125		μ A
Voltage Output Mode													
Output Compliance Range (Sourcing 1 mA)	V_{SS}		$V_{DD} - 0.25$	V_{SS}		$V_{DD} - 0.25$	V_{SS}		$V_{DD} - 0.25$	V_{SS}		$V_{DD} - 0.25$	V
Output Compliance Range (Sinking 1 mA)	$V_{SS} + 0.25$		V_{DD}	$V_{SS} + 0.25$		V_{DD}	$V_{SS} + 0.25$		V_{DD}	$V_{SS} + 0.25$		V_{DD}	V
Output Resistance in Current Output Mode AV_{SS} to 1 V		1			1			1			1		M Ω
AUXDAC Monotonicity Guaranteed		10			10			10			10		Bits
REFERENCE OUTPUT													
Internal Reference Voltage	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	V
Output Resistance		10			10			10			10		k Ω
REFERENCE INPUT													
Voltage Compliance													
AVDD = 3.3 V	0.1		1.25	0.1		1.25	0.1		1.25	0.1		1.25	V
AVDD = 1.8 V	0.1		1.0	0.1		1.0	0.1		1.0	0.1		1.0	V
Input Resistance External Reference Mode		1			1			1			1		M Ω
DAC MATCHING													
Gain Matching	-1		+1	-1		+1	-1		+1	-1		+1	% of FSR
ANALOG SUPPLY VOLTAGES													
AVDD	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
CVDD	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
DIGITAL SUPPLY VOLTAGES													
DVDD	1.7		1.9	1.7		1.9	1.7		1.9	1.7		1.9	V
DVDDIO	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
POWER CONSUMPTION, AVDD = DVDDIO = CVDD = 3.3 V													
$f_{DAC} = 125$ MSPS, $I_F = 12.5$ MHz		220			220			220			220		mW
I_{AVDD}		55			55			55			55		mA
$I_{DVDD} + I_{DVDDIO}$		10			10			10			10		mA
I_{CVDD}		3			3			3			3		mA
Power-Down Mode with Clock		8.5			8.5			8.5			8.5		mW
Power-Down Mode No Clock		3			3			3			3		mW
Power Supply Rejection Ratio		-0.009			-0.009			-0.009			-0.009		% FSR/V
POWER CONSUMPTION, AVDD = DVDDIO = CVDD = 1.8 V													
$f_{DAC} = 125$ MSPS, $I_F = 12.5$ MHz		58			58			58			58		mW
I_{AVDD}		24			24			24			24		mA
$I_{DVDD} + I_{DVDDIO}$		8			8			8			8		mA
I_{CVDD}		2			2			2			2		mA
Power-Down Mode with Clock		12			12			12			12		mW
Power-Down Mode No Clock		850			850			850			850		μ W
Power Supply Rejection Ratio		-0.007			-0.007			-0.007			-0.007		% FSR/V
OPERATING RANGE	-40	+25	+85	-40	+25	+85	-40	+25	+85	-40	+25	+85	$^{\circ}$ C

¹ Based on a 1.6 k Ω external resistor for 20 mA full-scale current.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX} , AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{KOUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKIN)				
V_{IH}	2.1	3		V
V_{IL}		0	0.9	V
Maximum Clock Rate			125	MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)		25		MHz
Minimum Pulse Width High		20		ns
Minimum Pulse Width Low		20		ns
Minimum SDIO and to SCLK Setup, t_{DS}		10		ns
Minimum SCLK to SDIO Hold, t_{DH}		5		ns
Maximum SCLK to Valid SDIO, t_{DV}		20		ns
Minimum SCLK to Invalid SDIO, t_{DNV}		5		ns
INPUT DATA				
1.8 V Q Channel or DCLKIO Falling Edge				
Setup		0.25		ns
Hold		1.2		ns
1.8 V I Channel or DCLKIO Rising Edge				
Setup		0.13		ns
Hold		1.1		ns
3.3 V Q Channel or DCLKIO Falling Edge				
Setup		-0.2		ns
Hold		1.5		ns
3.3 V I Channel or DCLKIO Rising Edge				
Setup		-0.2		ns
Hold		1.6		ns
DVDDIO = 3.3 V				
V_{IH}	2.1	3		V
V_{IL}		0	0.9	V
DVDDIO = 1.8 V				
V_{IH}	1.2	1.8		V
V_{IL}		0	0.5	V

AC SPECIFICATIONS

T_{MIN} to T_{MAX} , AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{KOUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 3.

Parameter	AD9114			AD9115			AD9116			AD9117			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE													
Output Settling Time (t_{ST}) to 0.1%	11.5			11.5			11.5			11.5			ns
Output Rise Time (10% to 90%)	0.27			0.27			0.27			0.27			ns
Output Fall Time (90% to 10%)	0.27			0.27			0.27			0.27			ns
Output Noise (I_{OUTFS} = 20mA)	1471			465			117			37			pA/√Hz
SPURIOUS FREE DYNAMIC RANGE (SFDR)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz	76			85			85			85			dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz	55			55			55			55			dBc
TWO TONE INTERMODULATION DISTORTION (IMD)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz	81			81			81			82			dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz	60			60			60			61			dBc
NOISE SPECTRAL DENSITY (NSD), EIGHT-TONE, 500 kHz TONE SPACING													
f_{DAC} = 125 MSPS, f_{OUT} = 1 MHz	-131			-141			-153			-163			dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz	-132			-143			-153			-157			dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz	-128			-138			-146			-149			dBc/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER													
f_{DAC} = 61.44 MSPS, f_{OUT} = 20 MHz	-78			-78			-78			-78			dBc
f_{DAC} = 122.88 MSPS, f_{OUT} = 30 MHz	-80			-80			-80			-80			dBc

T_{MIN} to T_{MAX} , AVDD = 1.8 V, DVDD = 1.8 V, DVDDIO = 1.8 V, CVDD = 1.8 V, I_{KOUTFS} = 8 mA, maximum sample rate, unless otherwise noted.

Table 4.

Parameter	AD9114			AD9115			AD9116			AD9117			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SPURIOUS FREE DYNAMIC RANGE (SFDR)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz	73			76			76			76			dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz	48			48			48			48			dBc
TWO TONE INTERMODULATION DISTORTION (IMD)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz	76			76			76			76			dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz	50			50			50			50			dBc
NOISE SPECTRAL DENSITY (NSD), EIGHT-TONE, 500 kHz TONE SPACING													
f_{DAC} = 125 MSPS, f_{OUT} = 1 MHz	-131			-143			-152			-158			dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz	-132			-143			-151			-152			dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz	-128			-138			-140			-141			dBc/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER													
f_{DAC} = 61.44 MSPS, f_{OUT} = 20 MHz	-69			-69			-69			-69			dBc
f_{DAC} = 122.88 MSPS, f_{OUT} = 30 MHz	-72			-72			-72			-72			dBc

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD, DVDDIO, CVDD to AVSS, DVSS, CVSS	−0.3 V to +3.9 V
DVDD to DVSS	−0.3 V to +2.1 V
AVSS to DVSS, CVSS	−0.3 V to +0.3 V
DVSS to AVSS, CVSS	−0.3 V to +0.3 V
CVSS to AVSS, DVSS	−0.3 V to +0.3 V
REFIO, FSADJQ, FSADJI, CMLQ, CMLI to AVSS	−0.3 V to AVDD + 0.3 V
QOUTP, QOUTN, IOUTP, IOUTN, RLQP, RLQN, RLIP, RLIN to AVSS	−1.0 V to AVDD + 0.3 V
DBn ¹ (MSB) to D0 (LSB), CS, SCLK, SDIO, RESET to DVSS	−0.3 V to DVDDIO + 0.3 V
CLKIN to CVSS	−0.3 V to CVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

¹ n stands for 7 for the AD9114, 9 for the AD9115, 11 for the AD9116, and 13 for the AD9117.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6.

Package Type	θ_{JA}	θ_{JB}^1	θ_{JC}^1	Unit
40-Lead LFCSP (with No Airflow Movement)	29.8	19.0	3.4	°C/W

¹ These calculations are intended to represent the thermal performance of the indicated packages using a JEDEC multilayer test board. Do not assume the same level of thermal performance in actual applications without a careful inspection of the conditions in the application to determine that they are similar to those assumed in these calculations.

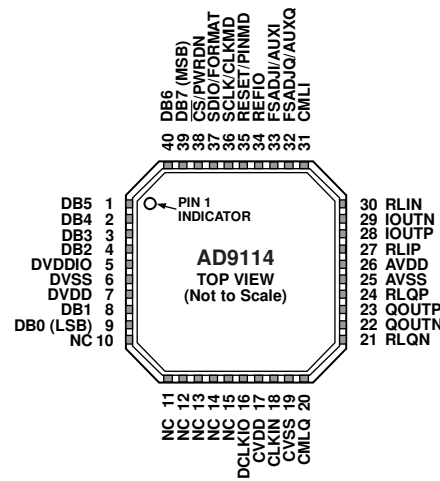
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



- NOTES
1. NC = NO CONNECT
 2. THE EXPOSED PAD IS CONNECTED TO AVSS AND MUST BE SOLDERED TO THE GROUND PLANE. EXPOSED METAL AT PACKAGE CORNERS IS CONNECTED TO THIS PAD.

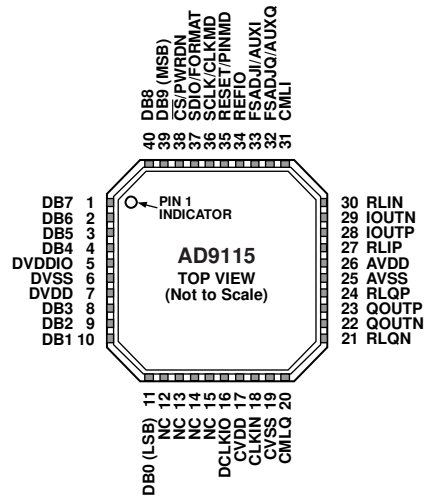
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Figure 2. AD9114 Pin Configuration

Table 7. AD9114 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[5:2]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage Input (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage Output (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 μ F capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8	DB1	Digital Inputs
9	DB0 (LSB)	Digital Input (LSB).
10 to 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage Input (1.8 V to 3.3 V). CVDD must be \geq DVDD.
18	CLKIN	LVCOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on-chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on-chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor, see the Using the Internal Termination Resistors section. Recommended value for this external resistor is 0 Ω .
21	RLQN	Load Resistor (62.5 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (62.5 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage Input (1.8 V to 3.3 V).
27	RLIP	Load Resistor (62.5 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.

Pin No.	Mnemonic	Description
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (62.5 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.
31	CMLI	I DAC Output Common-Mode Level. When the internal on-chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on-chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor, see the Using the Internal Termination Resistors section. Recommended value for this external resistor is 0 Ω .
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor, see the Theory of Operation section. Nominal value for this external resistor is 4 k Ω for 8 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on-chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on-chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor, see the Theory of Operation section. Nominal value for this external resistor is 4 k Ω for 8 mA output current. Auxiliary I DAC Output (AUXI). When the internal on-chip (IR_{SET}) is enabled, it is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 μ F capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values.
36	SCLK/CLKMD	A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD). Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When $DCLKIO = CLKIN$, tie it to 0. When $DCLKIO \neq CLKIN$, pulse 0 to 1 to edge trigger the internal retimer, see the Retimer section.
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	\overline{CS} /PWRDN	Active Low Chip Select (\overline{CS}). In SPI mode, this pin serves as the active low chip select. Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB7 (MSB)	Digital Input (MSB).
40	DB6	Digital Input.
	EP (EPAD)	The exposed pad is connected to AVSS and must be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.



NOTES

1. NC = NO CONNECT
2. THE EXPOSED PAD IS CONNECTED TO AVSS AND MUST BE SOLDERED TO THE GROUND PLANE. EXPOSED METAL AT PACKAGE CORNERS IS CONNECTED TO THIS PAD.

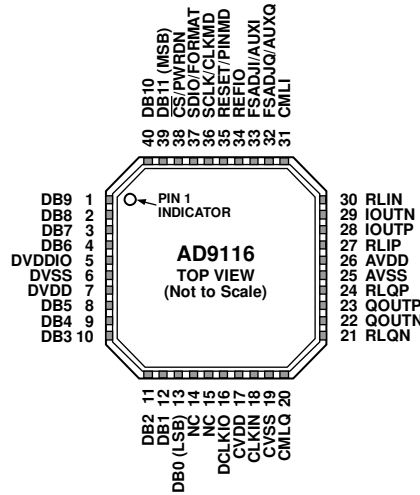
07466-004

Figure 3. AD9115 Pin Configuration

Table 8. AD9115 Pin Function Description

Pin No.	Mnemonic	Description
1 to 4	DB[7:4]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage Input (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage Output (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 μ F capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8 to 10	DB[3:1]	Digital Inputs.
11	DB0 (LSB)	Digital Input (LSB).
12 to 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage Input (1.8 V to 3.3 V). CVDD must be \geq DVDD.
18	CLKIN	LVC MOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on-chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on-chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor, see the Using the Internal Termination Resistors section. Recommended value for this external resistor is 0 Ω .
21	RLQN	Load Resistor (62.5 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (62.5 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage Input (1.8 V to 3.3 V).
27	RLIP	Load Resistor (62.5 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (62.5 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on-chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on-chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor, see the Using the Internal Termination Resistors section. Recommended value for this external resistor is 0 Ω .
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor, see the Theory of Operation section. Nominal value for this external resistor is 4 k Ω for 8 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on-chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on-chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor, see the Theory of Operation section. Nominal value for this external resistor is 4 k Ω for 8 mA output current. Auxiliary I DAC Output (AUXI). When the internal on-chip (IR_{SET}) is enabled, it is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 μ F capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When $DCLKIO = CLKIN$, tie it to 0. When $DCLKIO \neq CLKIN$, pulse 0 to 1 to edge trigger the internal retime, see the Retimer section.
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	\overline{CS} /PWRDN	Active Low Chip Select (\overline{CS}). In SPI mode, this pin serves as the active low chip select. Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB9 (MSB)	Digital Input (MSB).
40	DB82	Digital Input.
	EP (EPAD)	The exposed pad is connected to AVSS and must be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.



NOTES
 1. NC = NO CONNECT
 2. THE EXPOSED PAD IS CONNECTED TO AVSS AND MUST BE SOLDERED TO THE GROUND PLANE. EXPOSED METAL AT PACKAGE CORNERS IS CONNECTED TO THIS PAD.

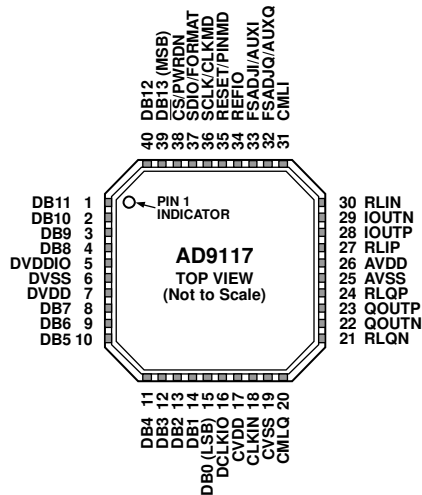
07466-003

Figure 4. AD9116 Pin Configuration

Table 9. AD9116 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[9:6]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage Input (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage Output (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 μ F capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8 to 12	DB[5:1]	Digital Inputs.
13	DB0 (LSB)	Digital Input (LSB).
14, 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage Input (1.8 V to 3.3 V). CVDD must be \geq DVDD.
18	CLKIN	LVC MOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on-chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on-chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor, see the Using the Internal Termination Resistors section. Recommended value for this external resistor is 0 Ω .
21	RLQN	Load Resistor (62.5 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (62.5 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage Input (1.8 V to 3.3 V).
27	RLIP	Load Resistor (62.5 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (62.5 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on-chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on-chip (IR_{CML}) is disabled, this pin is the common mode load for I DAC and must be connected to AVSS through a resistor, see the Using the Internal Termination Resistors section. Recommended value for this external resistor is $0\ \Omega$.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor, see the Theory of Operation section. Nominal value for this external resistor is $4\ k\Omega$ for $8\ mA$ output current. Auxiliary Q DAC Output (AUXQ). When the internal on-chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on-chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor, see the Theory of Operation section. Nominal value for this external resistor is $4\ k\Omega$ for $8\ mA$ output current. Auxiliary I DAC Output (AUXI). When the internal on-chip (IR_{SET}) is enabled, it is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a $1.0\ V$ reference output when in internal reference mode (a $0.1\ \mu F$ capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When $DCLKIO = CLKIN$, tie it to 0. When $DCLKIO \neq CLKIN$, pulse 0 to 1 to edge trigger the internal retime, see the Retimer section.
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	\overline{CS} /PWRDN	Active Low Chip Select (\overline{CS}). In SPI mode, this pin serves as the active low chip select. Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB11 (MSB)	Digital Input (MSB).
40	DB10	Digital Input.
	EP (EPAD)	The exposed pad is connected to AVSS and must be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.



NOTES
 1. THE EXPOSED PAD IS CONNECTED TO AVSS AND MUST BE SOLDERED TO THE GROUND PLANE. EXPOSED METAL AT PACKAGE CORNERS IS CONNECTED TO THIS PAD.

07466-002

Figure 5. AD9117 Pin Configuration

Table 10. AD9117 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[11:8]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage Input (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage Output (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 μF capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8 to 14	DB[7:1]	Digital Inputs.
15	DB0 (LSB)	Digital Input (LSB).
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage Input (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVC MOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on-chip (QR _{CML}) is enabled, this pin is connected to the on-chip QR _{CML} resistor. It is recommended to leave this pin unconnected. When the internal on-chip (QR _{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor, see the Using the Internal Termination Resistors section. Recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (62.5 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (62.5 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage Input (1.8 V to 3.3 V).
27	RLIP	Load Resistor (62.5 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (62.5 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on-chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on-chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor, see the Using the Internal Termination Resistors section. Recommended value for this external resistor is $0\ \Omega$.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor, see the Theory of Operation section. Nominal value for this external resistor is $4\ k\Omega$ for $8\ mA$ output current. Auxiliary Q DAC Output (AUXQ). When the internal on-chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on-chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor, see the Theory of Operation section. Nominal value for this external resistor is $4\ k\Omega$ for $8\ mA$ output current. Auxiliary I DAC Output (AUXI). When the internal on-chip (IR_{SET}) is enabled, it is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a $1.0\ V$ reference output when in internal reference mode (a $0.1\ \mu F$ capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When $DCLKIO = CLKIN$, tie it to 0. When $DCLKIO \neq CLKIN$, pulse 0 to 1 to edge trigger the internal retime, see the Retimer section.
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	\overline{CS} /PWRDN	Active Low Chip Select (\overline{CS}). In SPI mode, this pin serves as the active low chip select. Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB13 (MSB)	Digital Input (MSB).
40	DB12	Digital Input.
	EP (EPAD)	The exposed pad is connected to AVSS and must be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD, DVDD, DVDDIO, CVDD = 1.8 V, I_{KOUTES} = 8 mA, maximum sample rate (125 MSPS), unless otherwise noted.

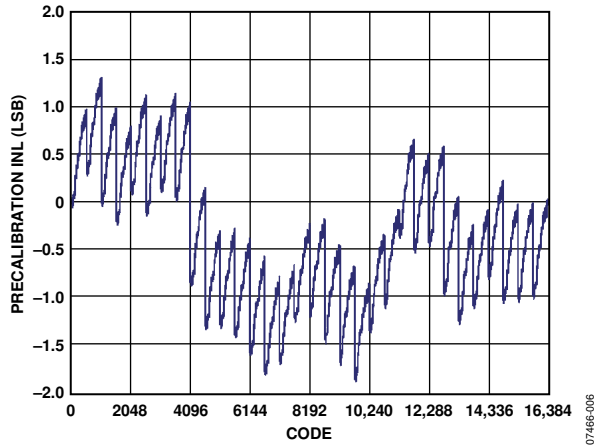


Figure 6. AD9117 Precalibration INL at 1.8 V, 8 mA (DVDD = 1.8 V)

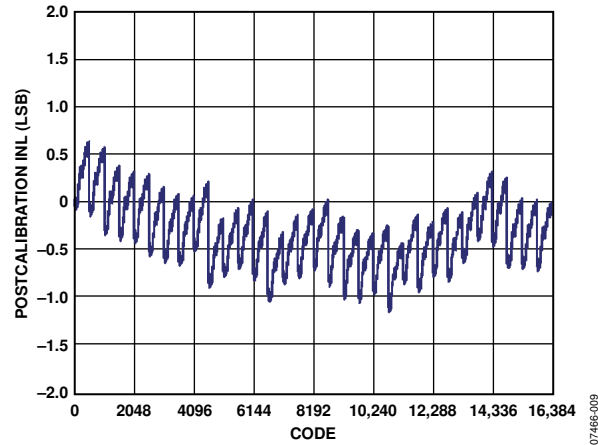


Figure 9. AD9117 Postcalibration INL at 1.8 V, 8 mA (DVDD = 1.8 V)

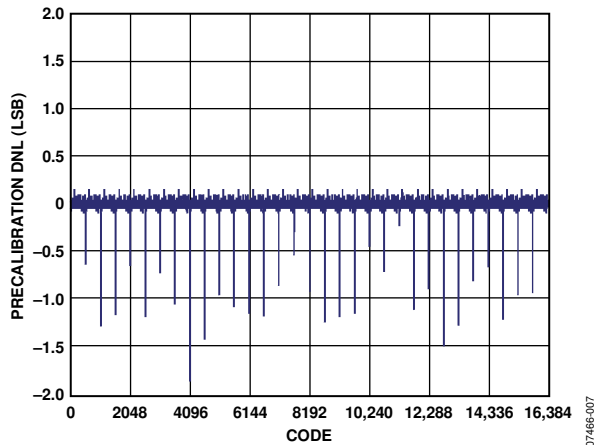


Figure 7. AD9117 Precalibration DNL at 1.8 V, 8 mA (DVDD = 1.8 V)

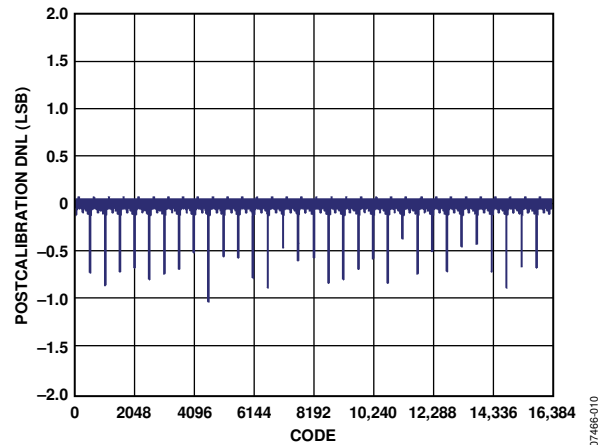


Figure 10. AD9117 Postcalibration DNL at 1.8 V, 8 mA (DVDD = 1.8 V)

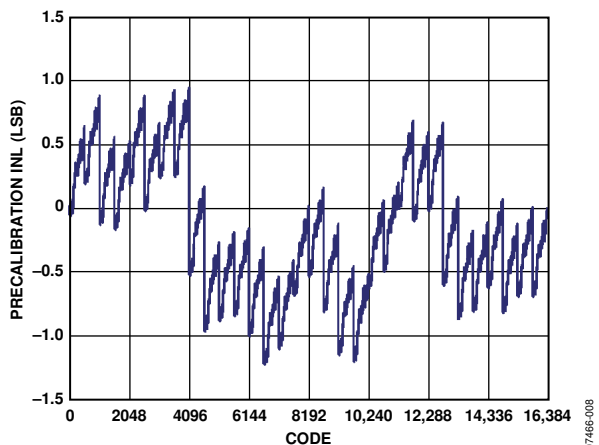


Figure 8. AD9117 Precalibration INL at 3.3 V, 20 mA (DVDD = 1.8 V)

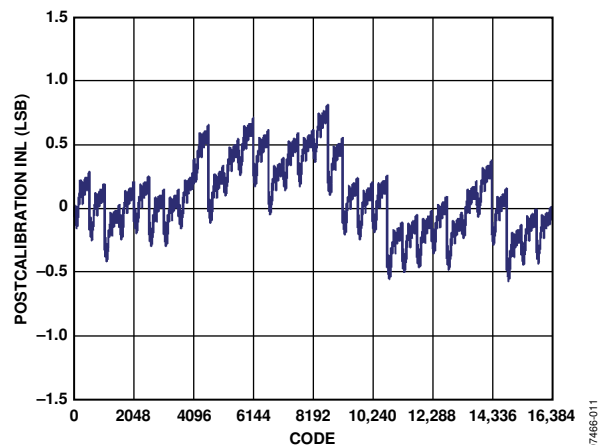


Figure 11. AD9117 Postcalibration INL at 3.3 V, 20 mA (DVDD = 1.8 V)

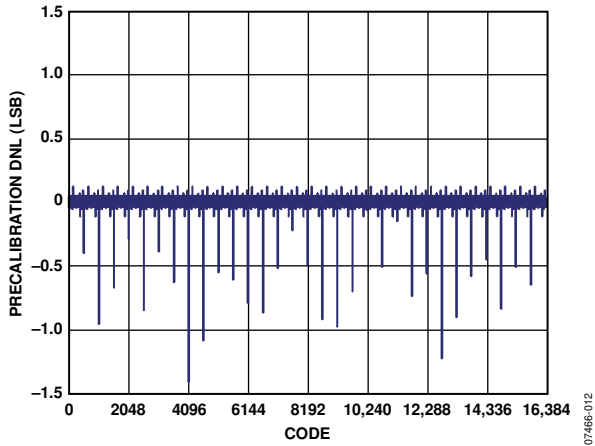


Figure 12. AD9117 Precalibration DNL at 3.3 V, 20 mA

07466-012

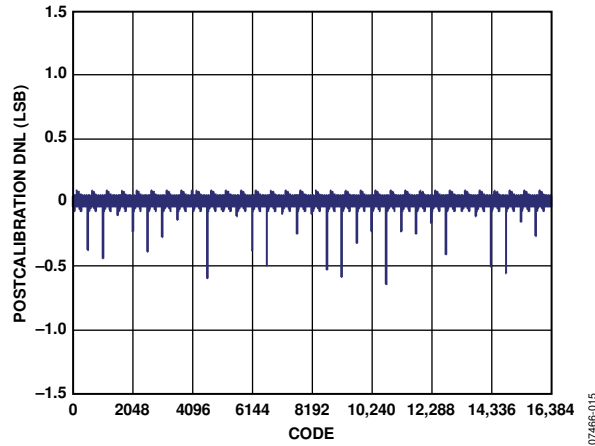


Figure 15. AD9117 Postcalibration DNL at 3.3 V, 20 mA

07466-015

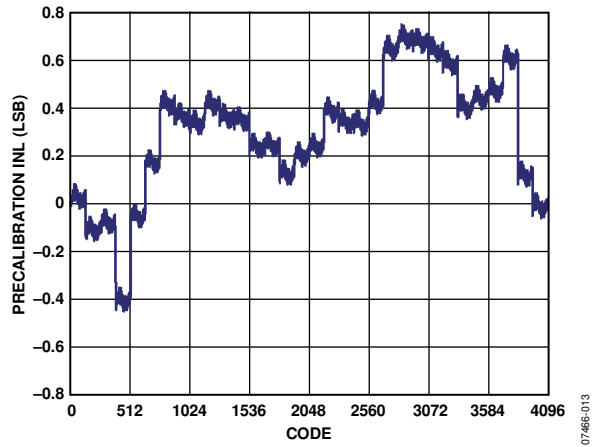


Figure 13. AD9116 Precalibration INL at 1.8 V, 8 mA

07466-013

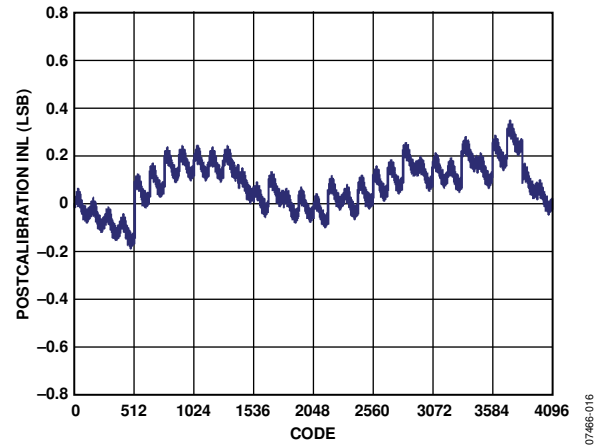


Figure 16. AD9116 Postcalibration INL at 1.8 V, 8 mA

07466-016

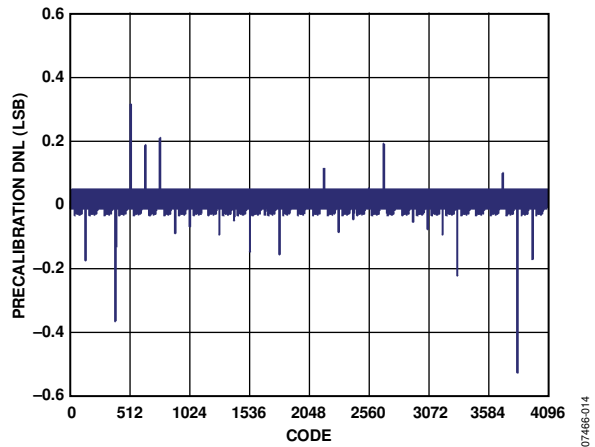


Figure 14. AD9116 Precalibration DNL at 1.8 V, 8 mA

07466-014

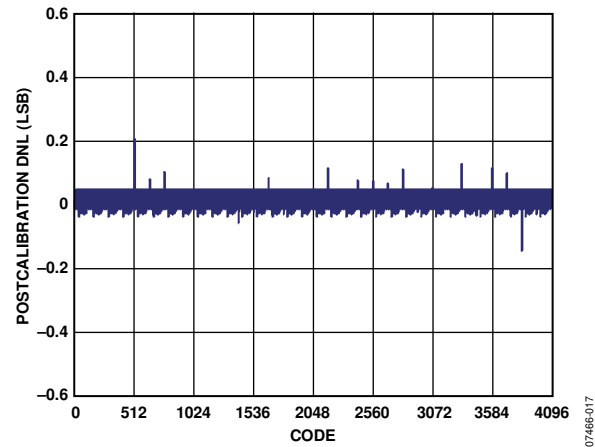


Figure 17. AD9116 Postcalibration DNL at 1.8 V, 8 mA

07466-017

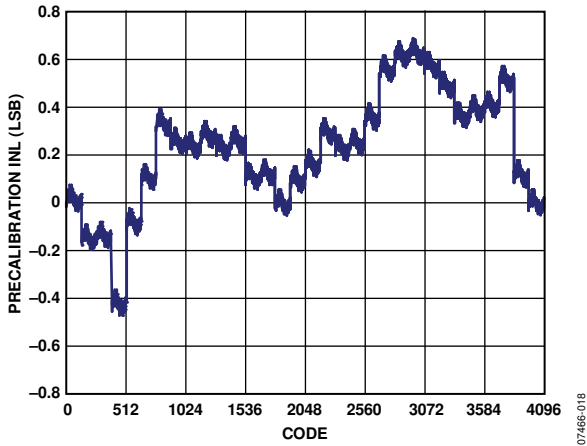


Figure 18. AD9116 Precalibration INL at 3.3 V, 20 mA

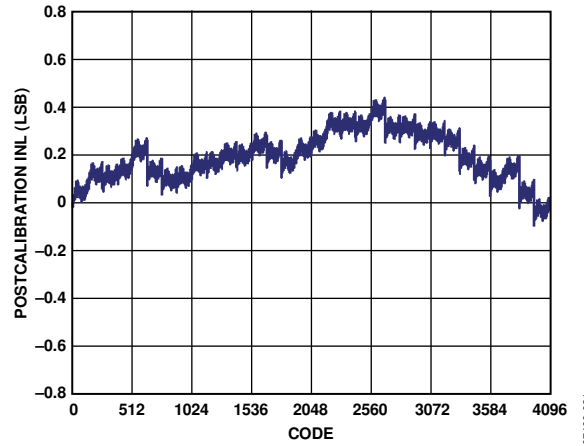


Figure 21. AD9116 Postcalibration INL at 3.3 V, 20 mA

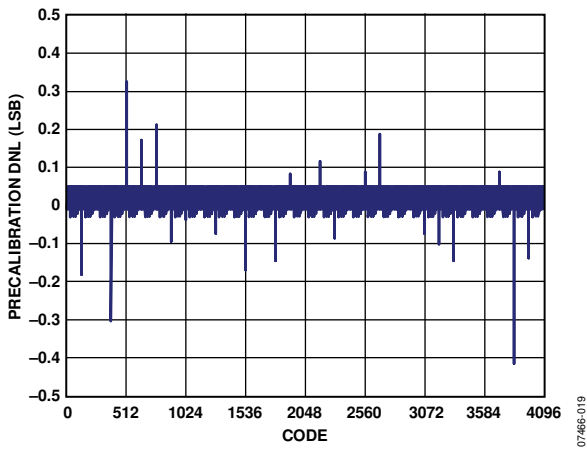


Figure 19. AD9116 Precalibration DNL at 3.3 V, 20 mA

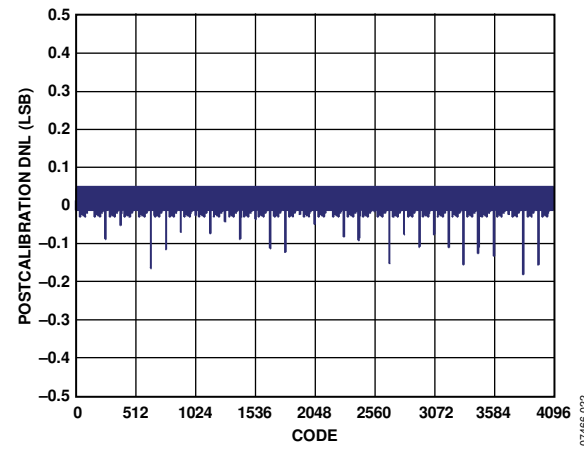


Figure 22. AD9116 Postcalibration DNL at 3.3 V, 20 mA

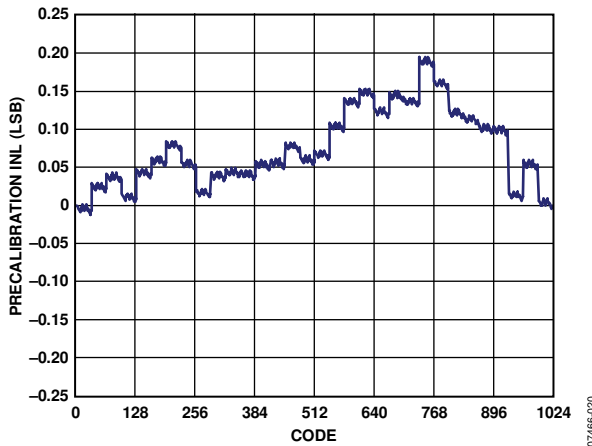


Figure 20. AD9115 Precalibration INL at 1.8 V, 8 mA

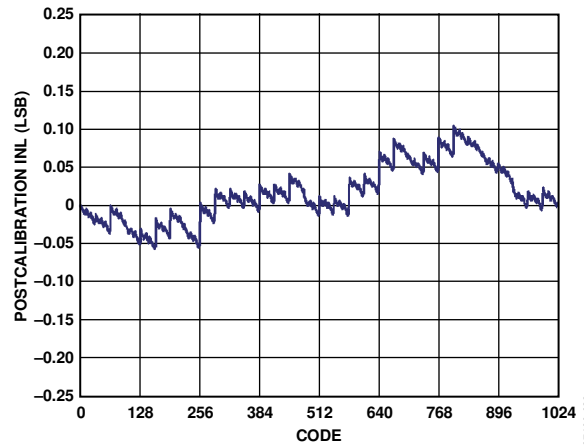


Figure 23. AD9115 Postcalibration INL at 1.8 V, 8 mA

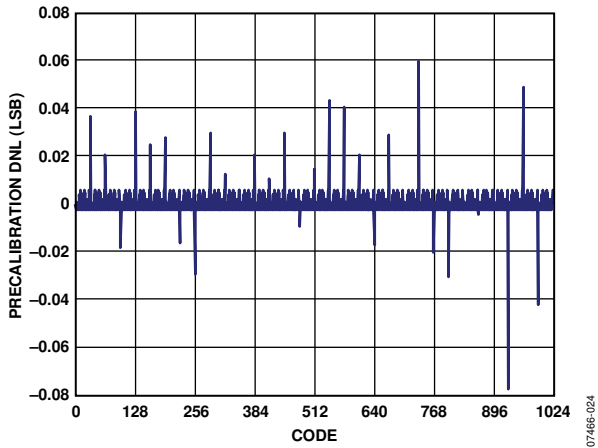


Figure 24. AD9115 Precalibration DNL at 1.8 V, 8 mA

07466-024

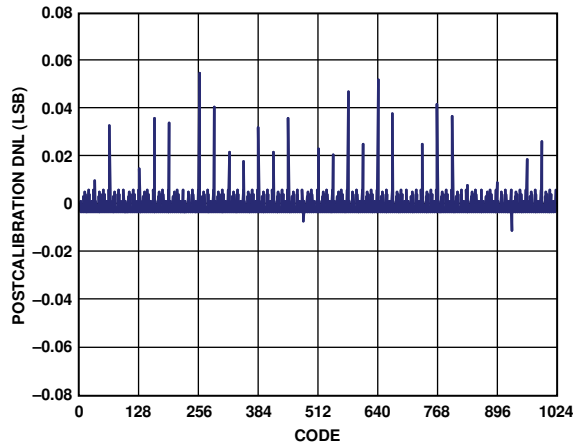


Figure 27. AD9115 Postcalibration DNL at 1.8 V, 8 mA

07466-027

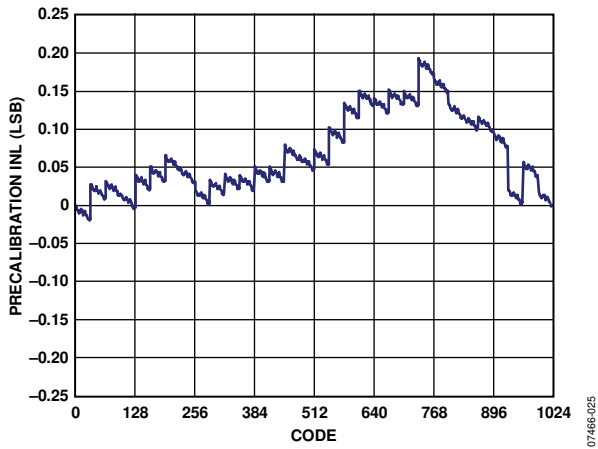


Figure 25. AD9115 Precalibration INL at 3.3 V, 20 mA

07466-025

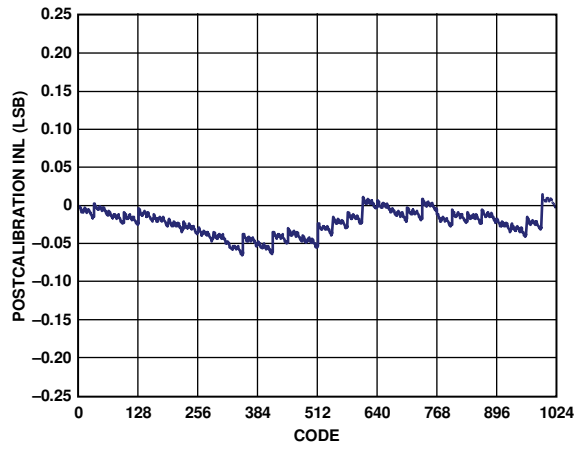


Figure 28. AD9115 Postcalibration INL at 3.3 V, 20 mA

07466-028

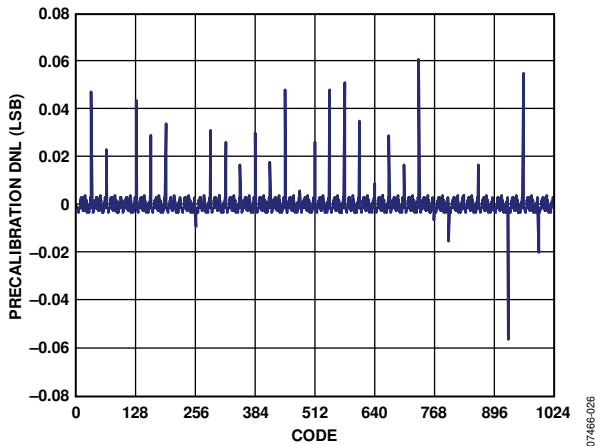


Figure 26. AD9115 Precalibration DNL at 3.3 V, 20 mA

07466-026

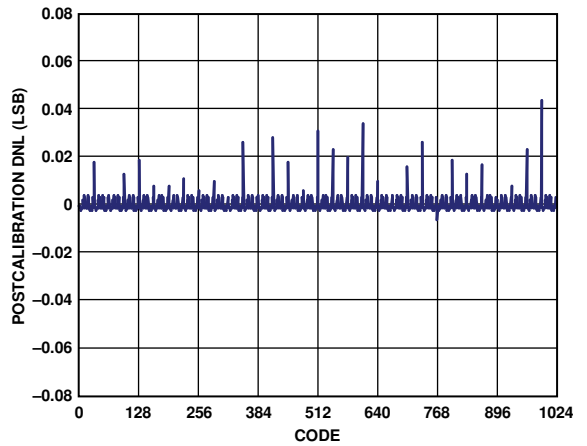


Figure 29. AD9115 Postcalibration DNL at 3.3 V, 20 mA

07466-029

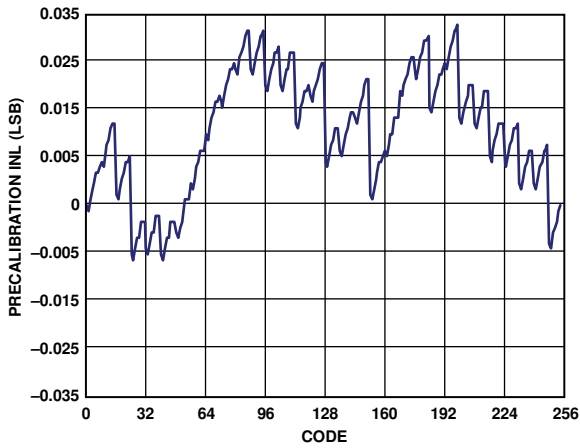


Figure 30. AD9114 Precalibration INL at 1.8 V, 8 mA

07466-030

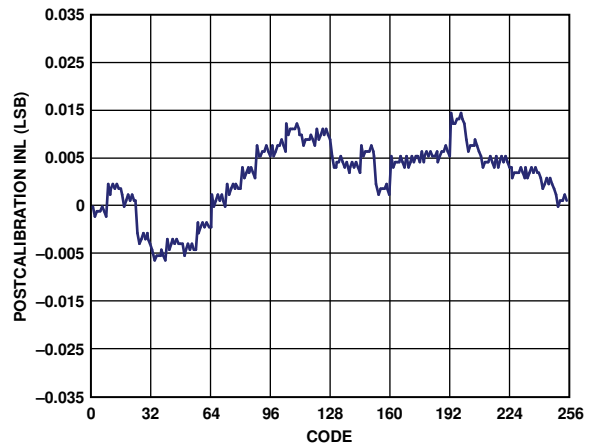


Figure 33. AD9114 Postcalibration INL at 1.8 V, 8 mA

07466-033

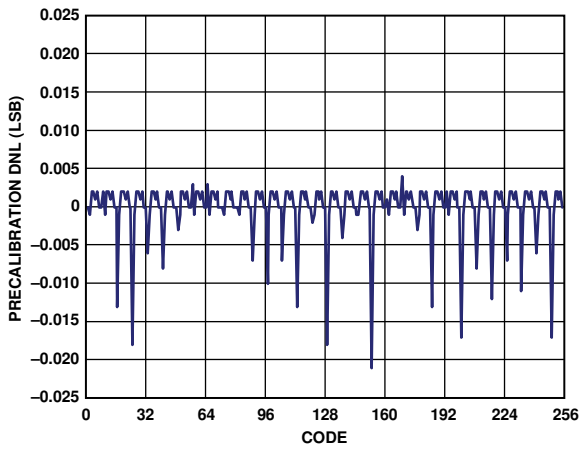


Figure 31. AD9114 Precalibration DNL at 1.8 V, 8 mA

07466-031

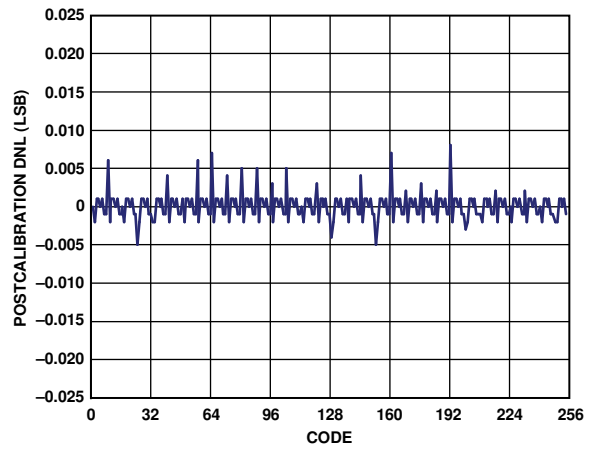


Figure 34. AD9114 Postcalibration DNL at 1.8 V, 8 mA

07466-034

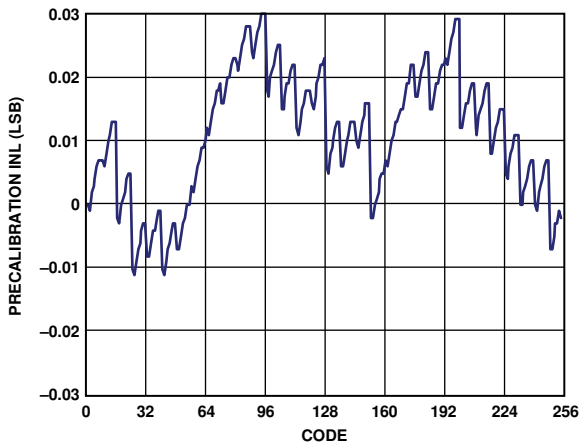


Figure 32. AD9114 Precalibration INL at 3.3 V, 20 mA

07466-032

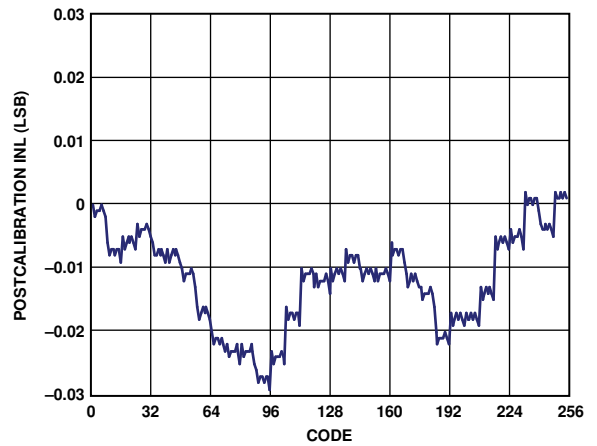


Figure 35. AD9114 Postcalibration INL at 3.3 V, 20 mA

07466-035

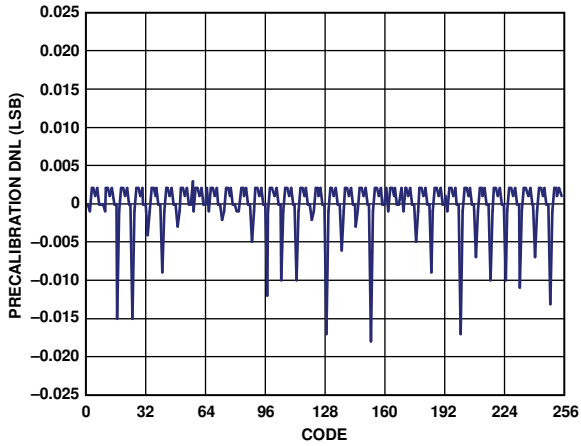


Figure 36. AD9114 Precalibration DNL at 3.3 V, 20 mA

07466-038

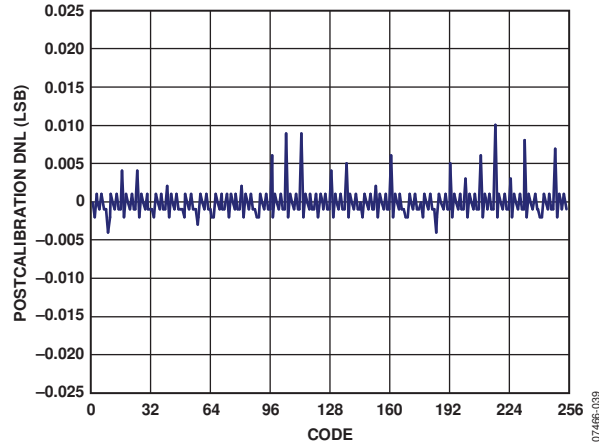


Figure 39. AD9114 Postcalibration DNL at 3.3 V, 20 mA

07466-039

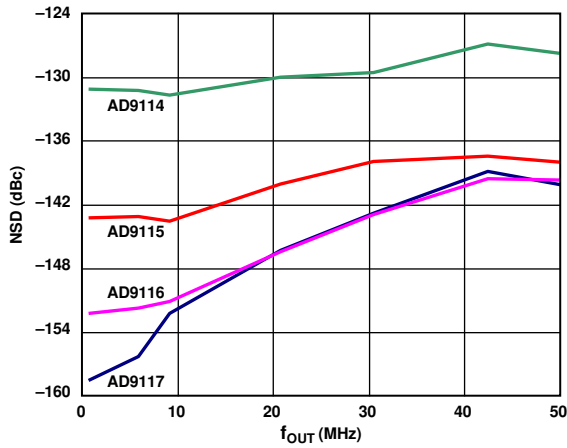


Figure 37. NSD at 8 mA vs. f_{OUT} , 1.8 V

07466-137

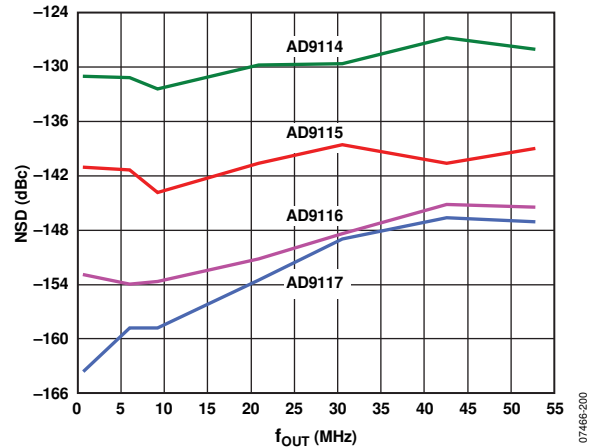


Figure 40. NSD at 20 mA vs. f_{OUT} , 3.3 V

07466-200

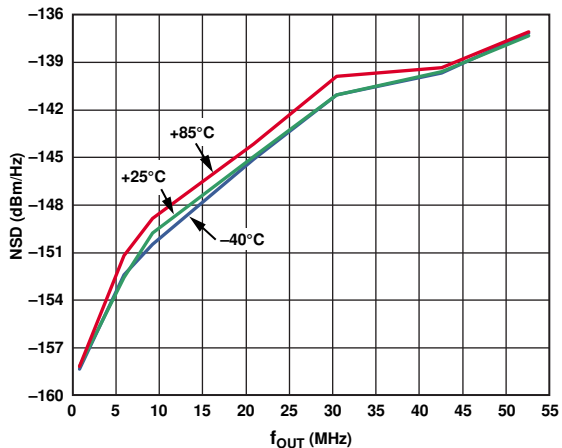


Figure 38. AD9117 NSD at Three Temperatures 8 mA vs. f_{OUT} , 1.8 V

07466-201

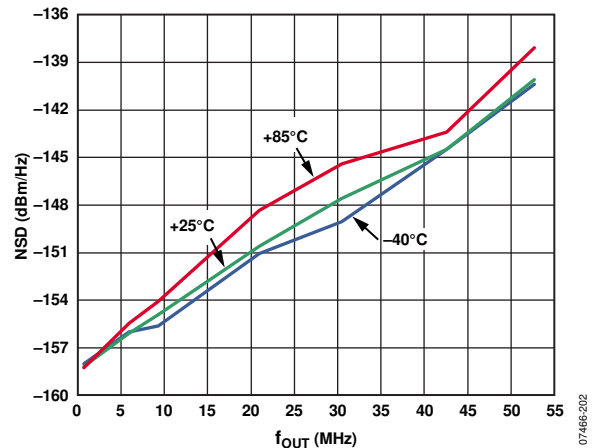


Figure 41. AD9117 NSD at Three Temperatures 8 mA vs. f_{OUT} , 3.3 V

07466-202

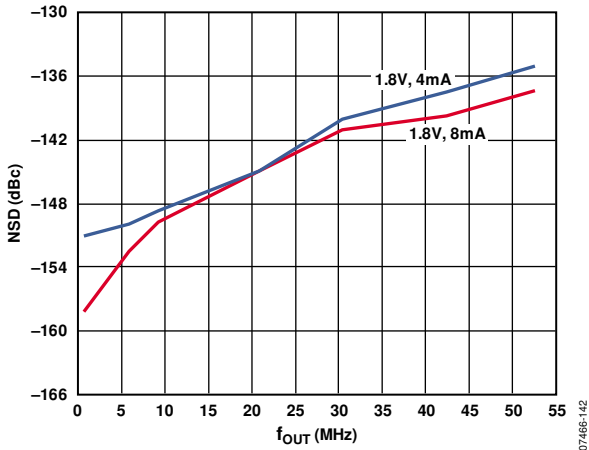


Figure 42. AD9117 NSD at Two Output Currents vs. f_{OUT} , 1.8 V

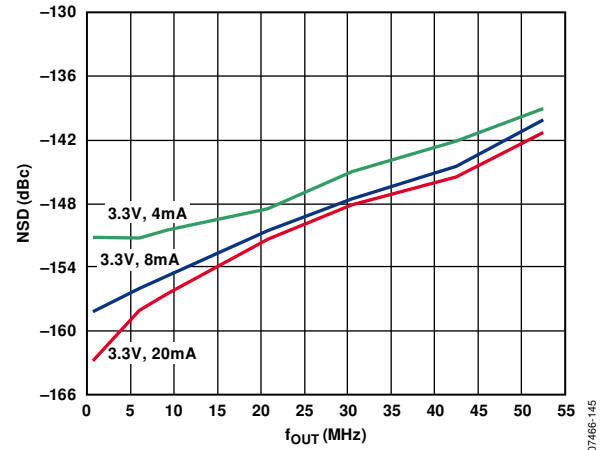


Figure 45. AD9117 NSD at Three Output Currents vs. f_{OUT} , 3.3 V

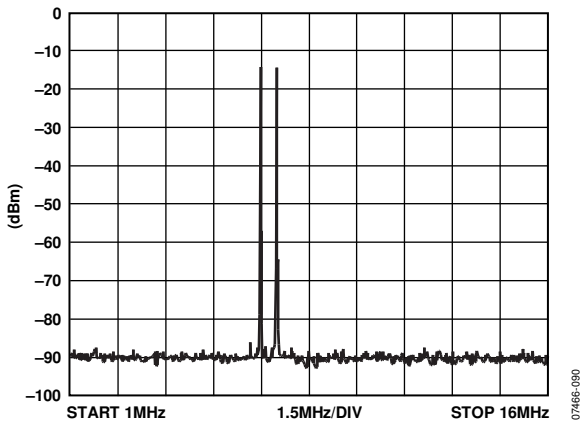


Figure 43. AD9117 Two Tone Spectrum at 1.8 V

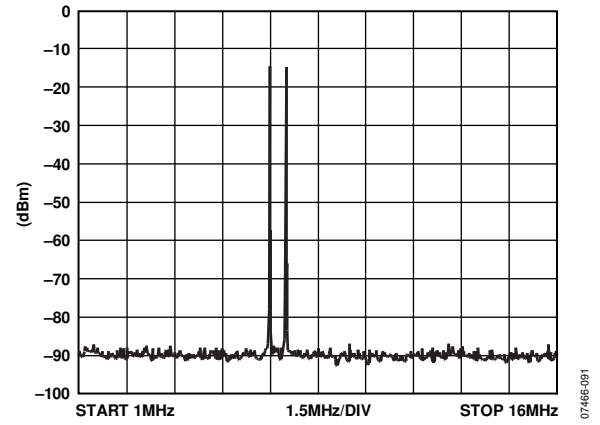


Figure 46. AD9117 Two Tone Spectrum at 3.3 V

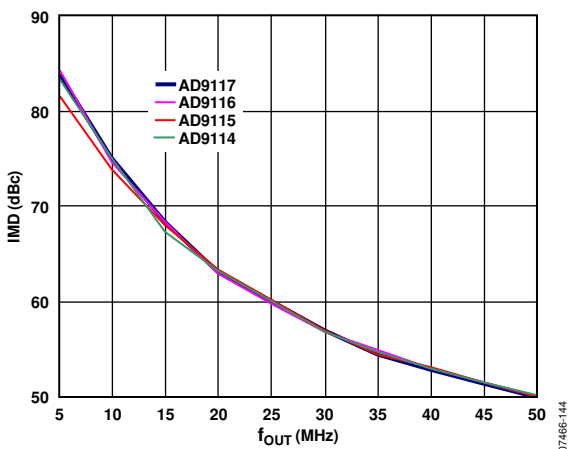


Figure 44. All IMD 8 mA vs. f_{OUT} , 1.8 V

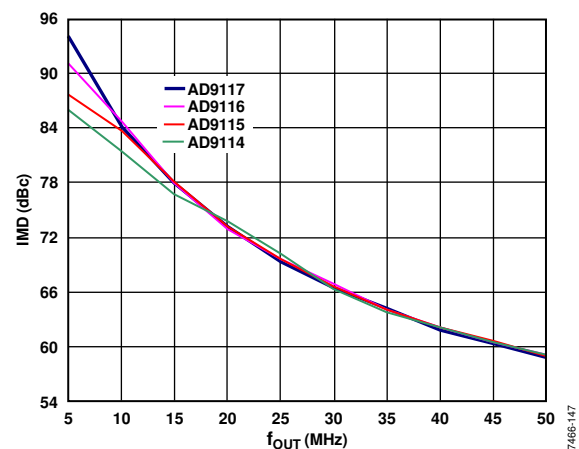


Figure 47. All IMD 20 mA vs. f_{OUT} , 3.3 V

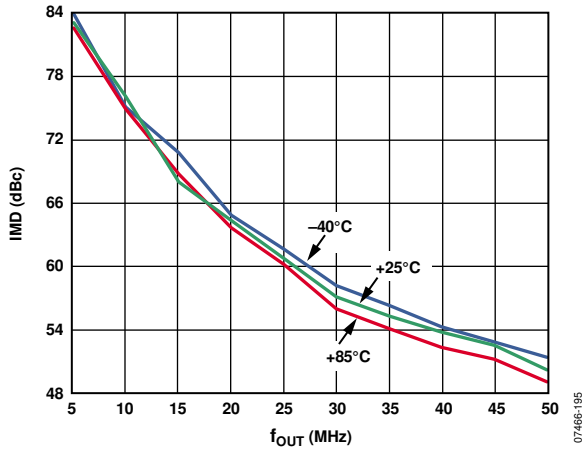


Figure 48. AD9117 IMD at Three Temperatures 8 mA vs. f_{OUT} , 1.8 V

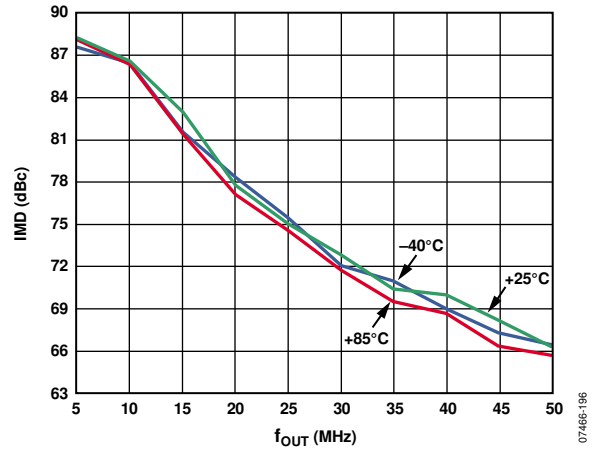


Figure 51. AD9117 IMD at Three Temperatures 20 mA vs. f_{OUT} , 3.3 V

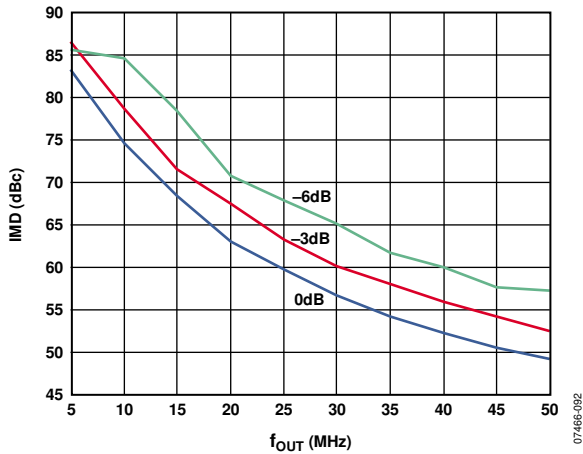


Figure 49. AD9117 IMD at Three Digital Signal Levels vs. f_{OUT} , 1.8 V

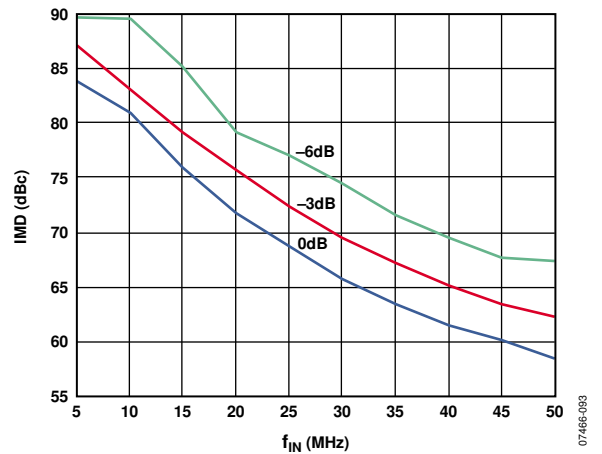


Figure 52. AD9117 IMD at Three Digital Signal Levels vs. f_{OUT} , 3.3 V

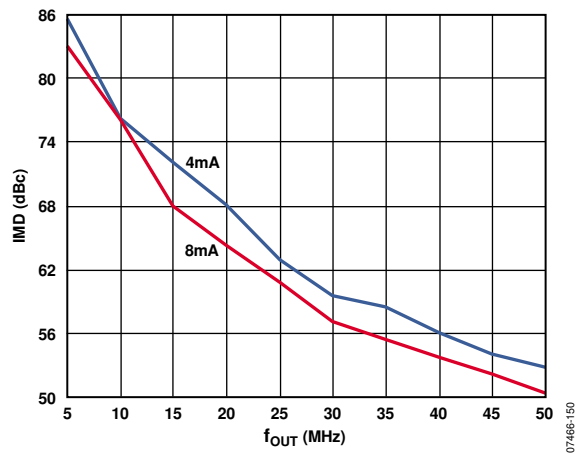


Figure 50. AD9117 IMD at Two Output Currents vs. f_{OUT} , 1.8 V

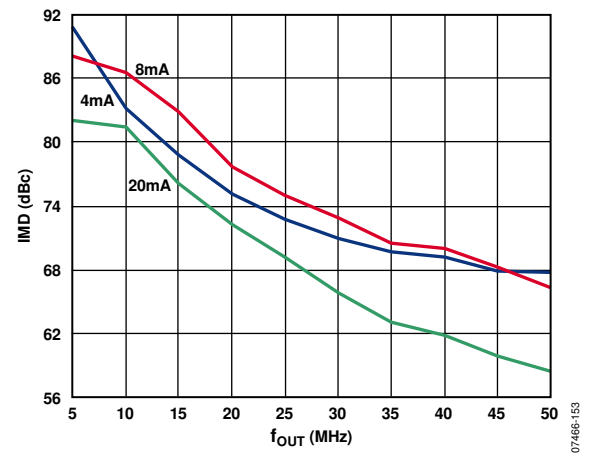


Figure 53. AD9117 IMD at Three Output Currents vs. f_{OUT} , 3.3 V