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Dual, 14-Bit, 1230 MSPS, TxDAC+ Digital-to-Analog Converter

Data Sheet

AD9121

FEATURES

Flexible LVDS interface allows word or byte load
Single-carrier W-CDMA ACLR = 82 dBc at 122.88 MHz IF
Analog output: adjustable 8.7 mA to 31.7 mA, R_L = 25 Ω to 50 Ω
Integrated 2×/4×/8× interpolator/complex modulator allows carrier placement anywhere in the DAC bandwidth
Gain, dc offset, and phase adjustment for sideband suppression
Multiple chip synchronization interfaces
High performance, low noise PLL clock multiplier
Digital inverse sinc filter
Low power: 1.5 W at 1.2 GSPS, 800 mW at 500 MSPS, full operating conditions
72-lead, exposed paddle LFCSP

APPLICATIONS

Wireless infrastructure
W-CDMA, CDMA2000, TD-SCDMA, WiMAX, GSM, LTE
Digital high or low IF synthesis
Transmit diversity
Wideband communications: LMDS/MMDS, point-to-point

GENERAL DESCRIPTION

The AD9121 is a dual, 14-bit, high dynamic range digital-to-analog converter (DAC) that provides a sample rate of 1230 MSPS, permitting multicarrier generation up to the Nyquist frequency.

The AD9121 TxDAC+® includes features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators, such as the ADL537x F-MOD series from Analog Devices, Inc. A 4-wire serial port interface provides for programming/readback of many internal parameters. Full-scale output current can be programmed over a range of 8.7 mA to 31.7 mA. The AD9121 comes in a 72-lead LFCSP.

PRODUCT HIGHLIGHTS

1. Ultralow noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies (IF).
2. Proprietary DAC output switching technique enhances dynamic performance.
3. Current outputs are easily configured for various single-ended or differential circuit topologies.
4. Flexible LVDS digital interface allows the standard 28-wire bus to be reduced to one-half of the width.

COMPANION PRODUCTS

IQ Modulators: ADL5370, ADL537x family
IQ Modulators with PLL and VCO: ADRF6701, ADRF670x family
Clock Drivers: AD9516, AD951x family
Voltage Regulator Design Tool: ADIsimPower

TYPICAL SIGNAL CHAIN

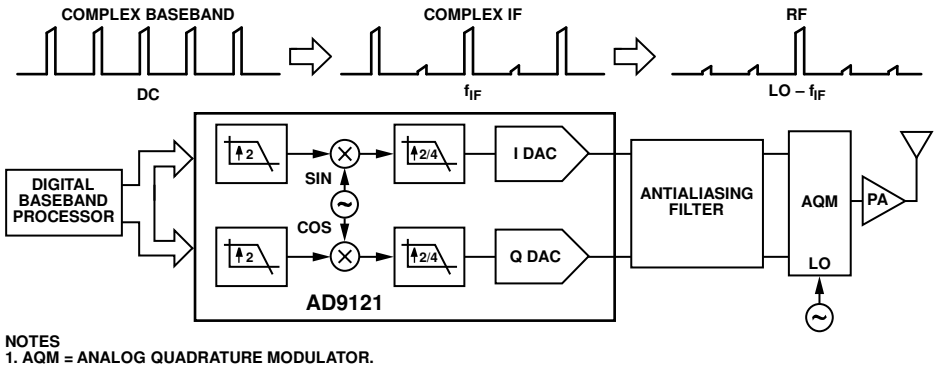


Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

AD9121* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9121 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9121: Dual, 14-bit, 1230 MSPS, TxDAC+ Digital-to-Analog Converter

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

DESIGN RESOURCES

- AD9121 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9121 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

10/12—Rev. 0 to Rev. B

Updated Outline Dimensions.....60

FUNCTIONAL BLOCK DIAGRAM

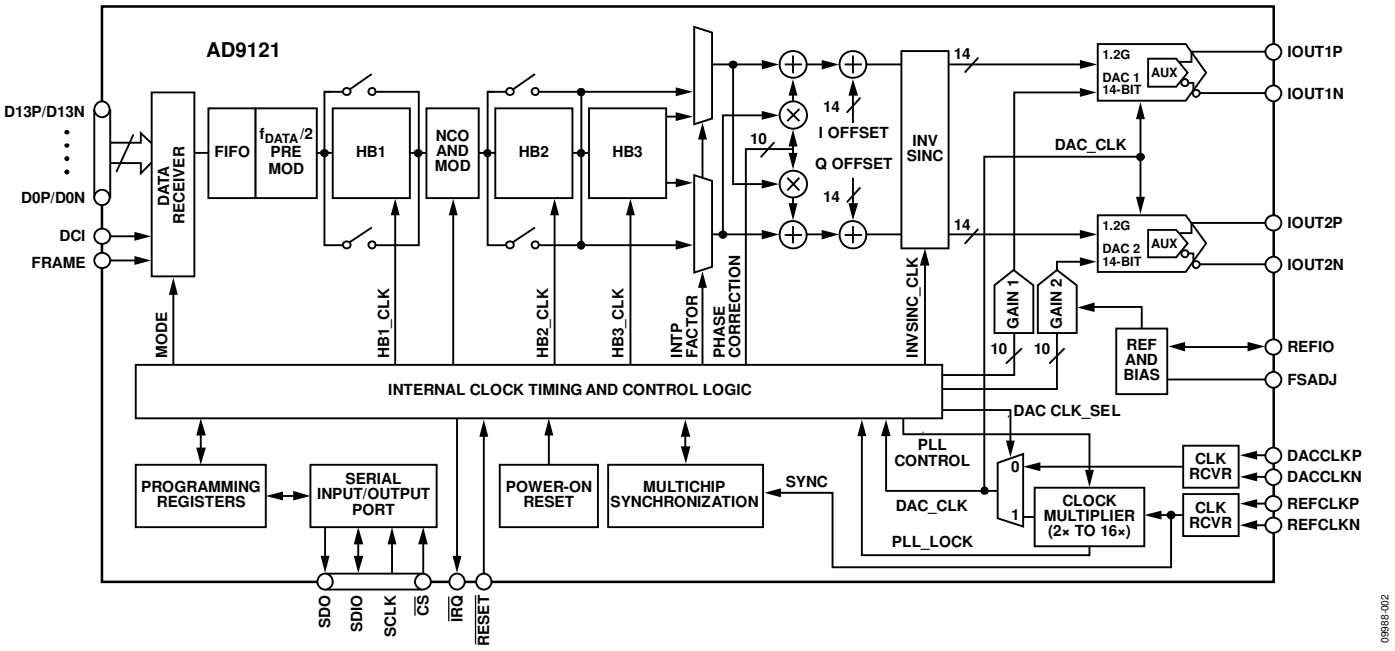


Figure 2.

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		14		Bits
ACCURACY				
Differential Nonlinearity (DNL)		±0.5		LSB
Integral Nonlinearity (INL)		±1.0		LSB
MAIN DAC OUTPUTS				
Offset Error	−0.001	0	+0.001	% FSR
Gain Error (with Internal Reference)	−3.6	±2	+3.6	% FSR
Full-Scale Output Current[1]	8.66	19.6	31.66	mA
Output Compliance Range	−1.0		+1.0	V
Power Supply Rejection Ratio, AVDD33	−0.3		+0.3	% FSR/V
Output Resistance		10		MΩ
Gain DAC Monotonicity		Guaranteed		
Settling Time to Within ±0.5 LSB		20		ns
MAIN DAC TEMPERATURE DRIFT				
Offset		0.04		ppm/°C
Gain		100		ppm/°C
Reference Voltage		30		ppm/°C
REFERENCE				
Internal Reference Voltage		1.2		V
Output Resistance		5		kΩ
ANALOG SUPPLY VOLTAGES				
AVDD33	3.13	3.3	3.47	V
CVDD18	1.71	1.8	1.89	V
DIGITAL SUPPLY VOLTAGES				
DVDD18	1.71	1.8	1.89	V
IOVDD	1.71	1.8/3.3	3.47	V
POWER CONSUMPTION				
2× Mode, f_{DAC} = 491.22 MSPS, IF = 10 MHz, PLL Off		834		mW
2× Mode, f_{DAC} = 491.22 MSPS, IF = 10 MHz, PLL On		913		mW
8× Mode, f_{DAC} = 800 MSPS, IF = 10 MHz, PLL Off		1135	1241	mW
AVDD33		55	57	mA
CVDD18		85	90	mA
DVDD18		444	495	mA
Power-Down Mode (Register 0x01 = 0xF0)		6.5	18.8	mW
POWER-UP TIME		260		ms
OPERATING RANGE	−40	+25	+85	°C

[1] Based on a 10 kΩ external resistor between FSADJ and AVSS.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, IOVDD = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High	IOVDD = 1.8 V	1.2			V
	IOVDD = 2.5 V	1.6			V
	IOVDD = 3.3 V	2.0			V
Input V_{IN} Logic Low	IOVDD = 1.8 V			0.6	V
	IOVDD = 2.5 V, 3.3 V			0.8	V
CMOS OUTPUT LOGIC LEVEL					
Output V_{OUT} Logic High	IOVDD = 1.8 V	1.4			V
	IOVDD = 2.5 V	1.8			V
	IOVDD = 3.3 V	2.4			V
Output V_{OUT} Logic Low	IOVDD = 1.8 V, 2.5 V, 3.3 V			0.4	V
LVDS RECEIVER INPUTS[1]	Applies to data, DCI, and FRAME inputs				
Input Voltage Range, V_{IA} or V_{IB}		825		1675	mV
Input Differential Threshold, V_{IDTH}		−100		+100	mV
Input Differential Hysteresis, V_{IDTHH} to V_{IDTHL}			20		mV
Receiver Differential Input Impedance, R_{IN}		80		120	Ω
LVDS Input Rate	See Table 5				
DAC CLOCK INPUT (DACCLKP, DACCLKN)					
Differential Peak-to-Peak Voltage		100	500	2000	mV
Common-Mode Voltage	Self-biased input, ac-coupled		1.25		V
Maximum Clock Rate		1230			MHz
REFCLK INPUT (REFCLKP, REFCLKN)					
Differential Peak-to-Peak Voltage		100	500	2000	mV
Common-Mode Voltage			1.25		V
REFCLK Frequency (PLL Mode)	1 GHz ≤ f_{VCO} ≤ 2.1 GHz	15.625		600	MHz
REFCLK Frequency (SYNC Mode)	See the Multichip Synchronization section for conditions	0		600	MHz
SERIAL PORT INTERFACE					
Maximum Clock Rate (SCLK)		40			MHz
Minimum Pulse Width High (t_{PWH})				12.5	ns
Minimum Pulse Width Low (t_{PWL})				12.5	ns
Setup Time, SDIO to SCLK (t_{DS})		1.9			ns
Hold Time, SDIO to SCLK (t_{DH})		0.2			ns
Data Valid, SDO to SCLK (t_{DV})		2.3			ns
Setup Time, $\overline{CS}$ to SCLK (t_{DCSB})			1.4		ns

[1] LVDS receiver is compliant with the IEEE 1596 reduced range link, unless otherwise noted.

DIGITAL INPUT DATA TIMING SPECIFICATIONS

Table 3.

Parameter	Value	Unit
LATENCY (DACCLK CYCLES)		
1× Interpolation (With or Without Modulation)	64	Cycles
2× Interpolation (With or Without Modulation)	135	Cycles
4× Interpolation (With or Without Modulation)	292	Cycles
8× Interpolation (With or Without Modulation)	608	Cycles
Inverse Sinc	20	Cycles
Fine Modulation	8	Cycles

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 100 MSPS, f_{OUT} = 20 MHz		78		dBc
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		80		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 70 MHz		69		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 70 MHz		72		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		84		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 60 MHz		86		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		84		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 100 MHz		81		dBc
NOISE SPECTRAL DENSITY (NSD), EIGHT-TONE, 500 kHz TONE SPACING				
f_{DAC} = 200 MSPS, f_{OUT} = 80 MHz		−162		dBm/Hz
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		−163		dBm/Hz
f_{DAC} = 800 MSPS, f_{OUT} = 80 MHz		−164		dBm/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE-CARRIER				
f_{DAC} = 491.52 MSPS, f_{OUT} = 10 MHz		84		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 122.88 MHz		82		dBc
f_{DAC} = 983.04 MSPS, f_{OUT} = 122.88 MHz		83		dBc
W-CDMA SECOND ACLR, SINGLE-CARRIER				
f_{DAC} = 491.52 MSPS, f_{OUT} = 10 MHz		88		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 122.88 MHz		86		dBc
f_{DAC} = 983.04 MSPS, f_{OUT} = 122.88 MHz		88		dBc

Table 5. Maximum Rate (MSPS) with DVDD and CVDD Supply Regulation

		$f_{INTERFACE}$ (MSPS)			f_{DAC} (MSPS)		
		DVDD18, CVDD18 =			DVDD18, CVDD18 =		
Bus Width	Interpolation Factor	1.8 V ± 5%	1.8 V ± 2%	1.9 V ± 2%	1.8 V ± 5%	1.8 V ± 2%	1.9 V ± 2%
Byte (7 Bits)	1×	1100	1200	1230	275	300	307.5
	2×	1100	1200	1230	550	600	615
	4×	1100	1200	1230	1100	1200	1230
	8×	550	600	615	1100	1200	1230
Word (14 Bits)	1×	1100	1200	1230	550	600	615
	2× (HB1)	900	1000	1000	900	1000	1000
	2× (HB2)	1100	1200	1230	1100	1200	1230
	4×	550	600	615	1100	1200	1230
	8×	275	300	307.5	1100	1200	1230

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD33 to AVSS, EPAD, CVSS, DVSS	−0.3 V to +3.6 V
IOVDD to AVSS, EPAD, CVSS, DVSS	−0.3 V to +3.6 V
DVDD18, CVDD18 to AVSS, EPAD, CVSS, DVSS	−0.3 V to +2.1 V
AVSS to EPAD, CVSS, DVSS	−0.3 V to +0.3 V
EPAD to AVSS, CVSS, DVSS	−0.3 V to +0.3 V
CVSS to AVSS, EPAD, DVSS	−0.3 V to +0.3 V
DVSS to AVSS, EPAD, CVSS	−0.3 V to +0.3 V
FSADJ, REFIO, IOUT1P, IOUT1N, IOUT2P, IOUT2N to AVSS	−0.3 V to AVDD33 + 0.3 V
D[15:0]P, D[15:0]N, FRAMEP, FRAMEN, DCIP, DCIN to EPAD, DVSS	−0.3 V to DVDD18 + 0.3 V
DACCLKP, DACCLKN, REFCLKP, REFCLKN to CVSS	−0.3 V to CVDD18 + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{CS}}$, SCLK, SDIO, SDO to EPAD, DVSS	−0.3 V to IOVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed pad (EPAD) of the 72-lead LFCSP must be soldered to the ground plane (AVSS). The EPAD provides an electrical, thermal, and mechanical connection to the board.

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA} and θ_{JB}.

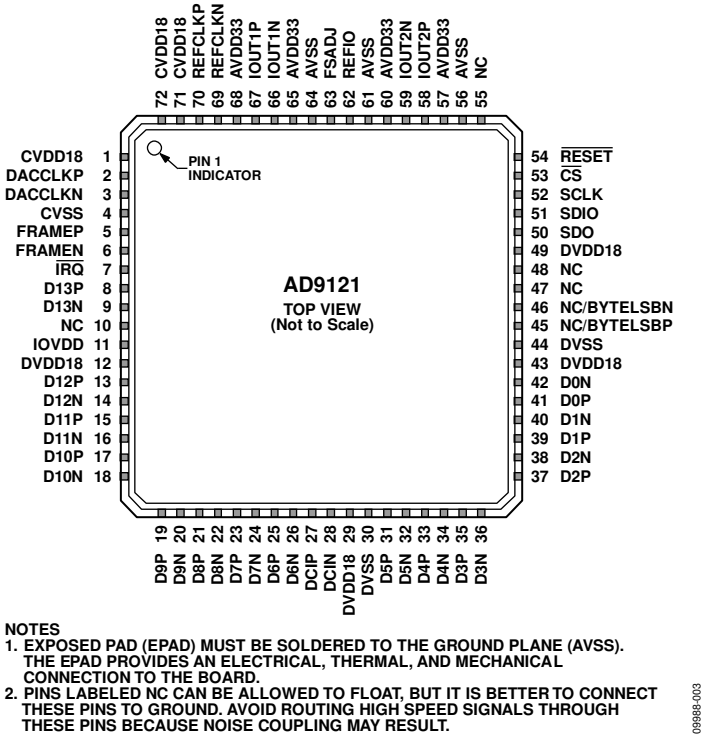
Table 7. Thermal Resistance

Package	θ_{JA}	θ_{JB}	θ_{JC}	Unit	Conditions
72-Lead LFCSP	20.7	10.9	1.1	°C/W	EPAD soldered to ground plane

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD (EPAD) MUST BE SOLDERED TO THE GROUND PLANE (AVSS). THE EPAD PROVIDES AN ELECTRICAL, THERMAL, AND MECHANICAL CONNECTION TO THE BOARD.
2. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
2	DACCLKP	DAC Clock Input, Positive.
3	DACCLKN	DAC Clock Input, Negative.
4	CVSS	Clock Supply Common.
5	FRAMEP	Frame Input, Positive. This pin must be tied to DVSS if not used.
6	FRAMEN	Frame Input, Negative. This pin must be tied to DVDD18 if not used.
7	IRQ	Interrupt Request. Open-drain, active low output. Connect an external pull-up to IOVDD through a 10 kΩ resistor.
8	D13P	Data Bit 13 (MSB), Positive.
9	D13N	Data Bit 13 (MSB), Negative.
10	NC	This pin is not connected internally (see Figure 3).
11	IOVDD	Supply Pin for Serial Port I/O Pins, RESET, and IRQ. 1.8 V to 3.3 V can be supplied to this pin.
12	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
13	D12P	Data Bit 12, Positive.
14	D12N	Data Bit 12, Negative.
15	D11P	Data Bit 11, Positive.
16	D11N	Data Bit 11, Negative.
17	D10P	Data Bit 10, Positive.
18	D10N	Data Bit 10, Negative.
19	D9P	Data Bit 9, Positive.
20	D9N	Data Bit 9, Negative.
21	D8P	Data Bit 8, Positive.
22	D8N	Data Bit 8, Negative.

Pin No.	Mnemonic	Description
23	D7P	Data Bit 7, Positive.
24	D7N	Data Bit 7, Negative.
25	D6P	Data Bit 6, Positive.
26	D6N	Data Bit 6, Negative.
27	DCIP	Data Clock Input, Positive.
28	DCIN	Data Clock Input, Negative.
29	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
30	DVSS	Digital Common.
31	D5P	Data Bit 5, Positive.
32	D5N	Data Bit 5, Negative.
33	D4P	Data Bit 4, Positive.
34	D4N	Data Bit 4, Negative.
35	D3P	Data Bit 3, Positive.
36	D3N	Data Bit 3, Negative.
37	D2P	Data Bit 2, Positive.
38	D2N	Data Bit 2, Negative.
39	D1P	Data Bit 1, Positive.
40	D1N	Data Bit 1, Negative.
41	D0P	Data Bit 0, Positive.
42	D0N	Data Bit 0, Negative.
43	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
44	DVSS	Digital Common.
45	NC/ByteLSBP	This pin is not connected internally (see Figure 3) in word mode. LSB Positive (Data Bit 0) in byte mode.
46	NC/ByteLSBN	This pin is not connected internally (see Figure 3) in word mode. LSB Negative (Data Bit 0) in byte mode.
47	NC	This pin is not connected internally (see Figure 3).
48	NC	This pin is not connected internally (see Figure 3).
49	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
50	SDO	Serial Port Data Output (CMOS Levels with Respect to IOVDD).
51	SDIO	Serial Port Data Input/Output (CMOS Levels with Respect to IOVDD).
52	SCLK	Serial Port Clock Input (CMOS Levels with Respect to IOVDD).
53	$\overline{CS}$	Serial Port Chip Select, Active Low (CMOS Levels with Respect to IOVDD).
54	$\overline{RESET}$	Reset, Active Low (CMOS Levels with Respect to IOVDD).
55	NC	This pin is not connected internally (see Figure 3).
56	AVSS	Analog Supply Common.
57	AVDD33	3.3 V Analog Supply.
58	IOUT2P	Q DAC Positive Current Output.
59	IOUT2N	Q DAC Negative Current Output.
60	AVDD33	3.3 V Analog Supply.
61	AVSS	Analog Supply Common.
62	REFIO	Voltage Reference. Nominally 1.2 V output. Should be decoupled to AVSS.
63	FSADJ	Full-Scale Current Output Adjust. Place a 10 kΩ resistor from this pin to AVSS.
64	AVSS	Analog Supply Common.
65	AVDD33	3.3 V Analog Supply.
66	IOUT1N	I DAC Negative Current Output.
67	IOUT1P	I DAC Positive Current Output.
68	AVDD33	3.3 V Analog Supply.
69	REFCLKN	PLL Reference Clock Input, Negative. This pin has a secondary function as a synchronization input.
70	REFCLKP	PLL Reference Clock Input, Positive. This pin has a secondary function as a synchronization input.
71	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
72	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
	EPAD	The exposed pad (EPAD) must be soldered to the ground plane (AVSS). The EPAD provides an electrical, thermal, and mechanical connection to the board.

TYPICAL PERFORMANCE CHARACTERISTICS

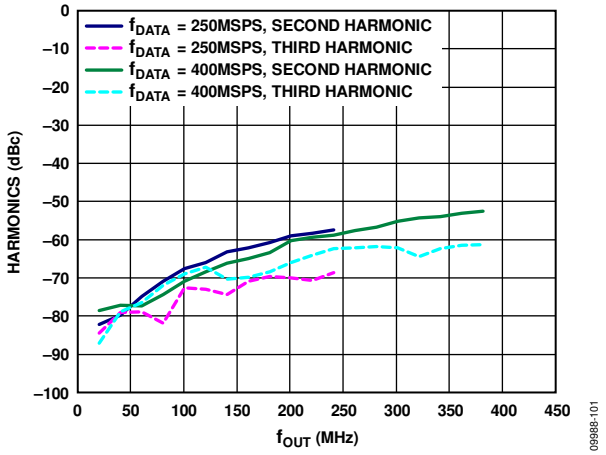


Figure 4. Harmonics vs. f_{OUT} over f_{DATA}, 2× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

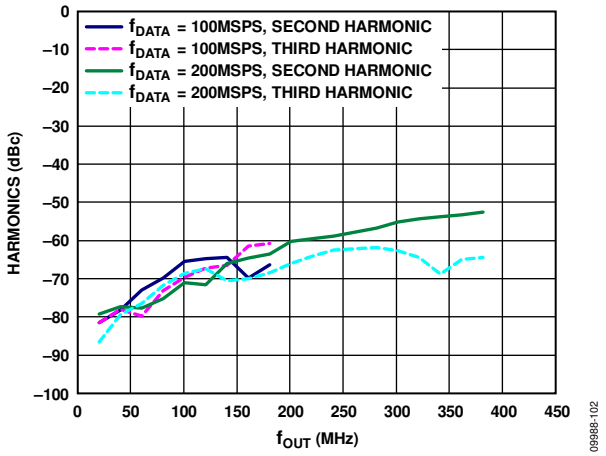


Figure 5. Harmonics vs. f_{OUT} over f_{DATA}, 4× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

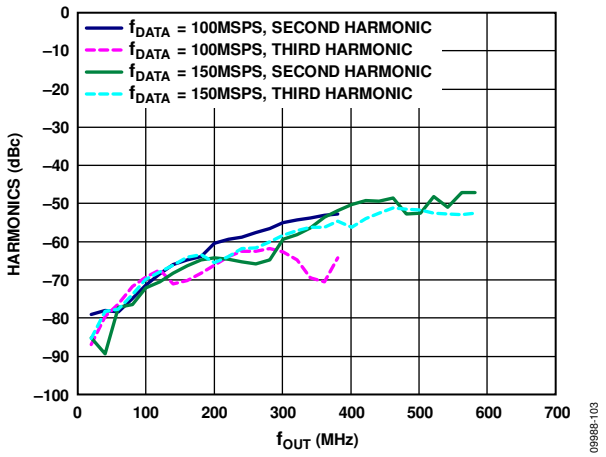


Figure 6. Harmonics vs. f_{OUT} over f_{DATA}, 8× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

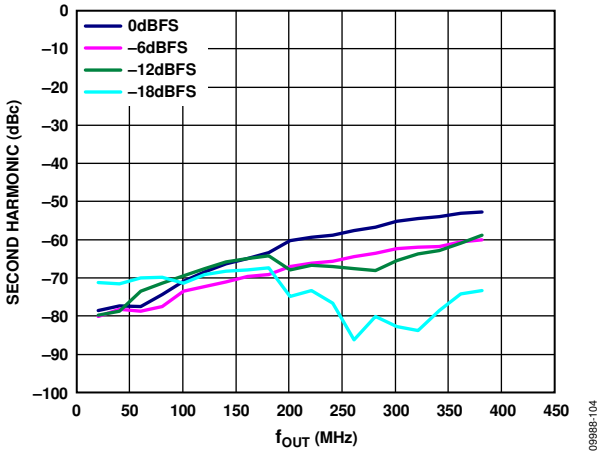


Figure 7. Second Harmonic vs. f_{OUT} over Digital Scale, 2× Interpolation, f_{DATA} = 400 MSPS, I_{FS} = 20 mA

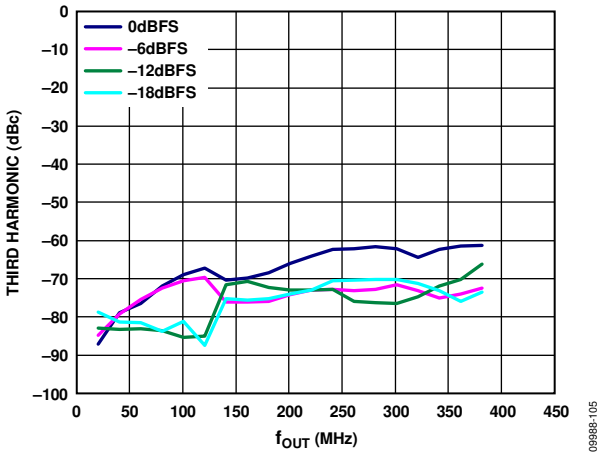


Figure 8. Third Harmonic vs. f_{OUT} over Digital Scale, 2× Interpolation, f_{DATA} = 400 MSPS, I_{FS} = 20 mA

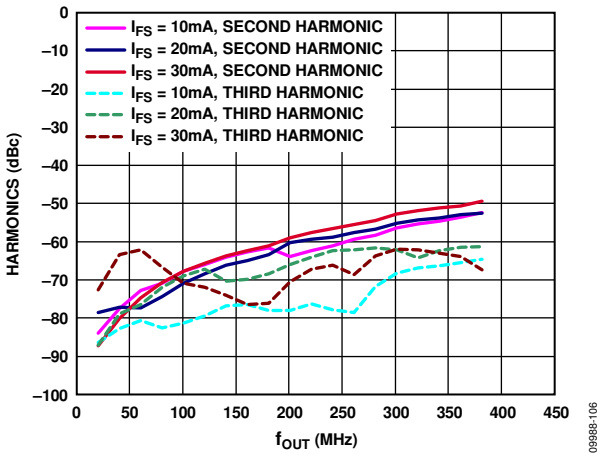


Figure 9. Harmonics vs. f_{OUT} over I_{FS}, 2× Interpolation, f_{DATA} = 400 MSPS, Digital Scale = 0 dBFS

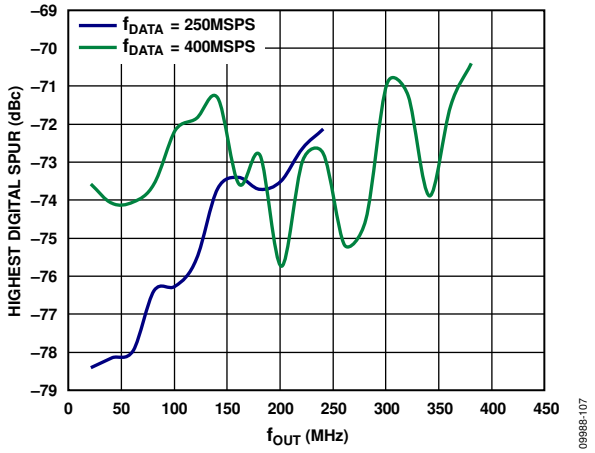


Figure 10. Highest Digital Spur vs. f_{OUT} over f_{DATA}, 2× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

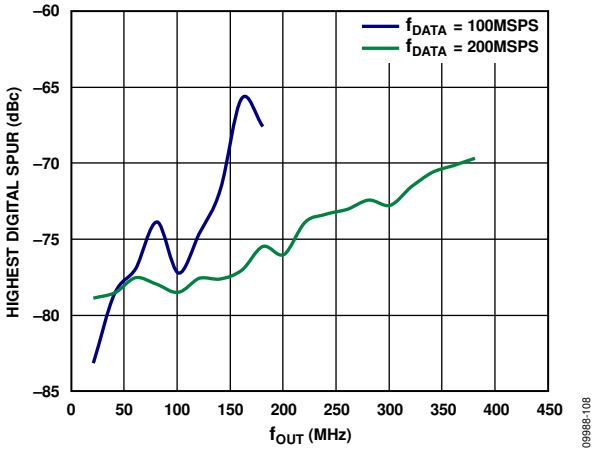


Figure 11. Highest Digital Spur vs. f_{OUT} over f_{DATA}, 4× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

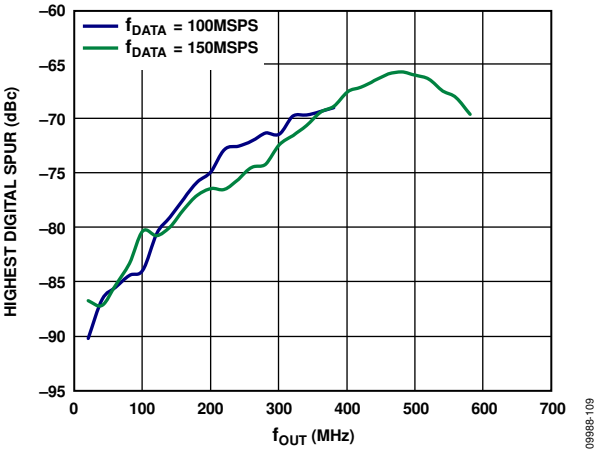


Figure 12. Highest Digital Spur vs. f_{OUT} over f_{DATA}, 8× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

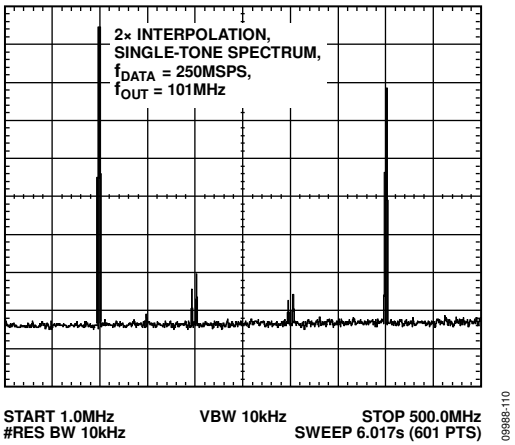


Figure 13. Single-Tone Spectrum, 2× Interpolation, f_{DATA} = 250 MSPS, f_{OUT} = 101 MHz

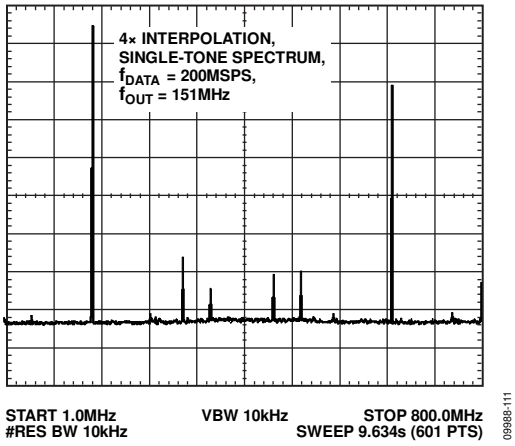


Figure 14. Single-Tone Spectrum, 4× Interpolation, f_{DATA} = 200 MSPS, f_{OUT} = 151 MHz

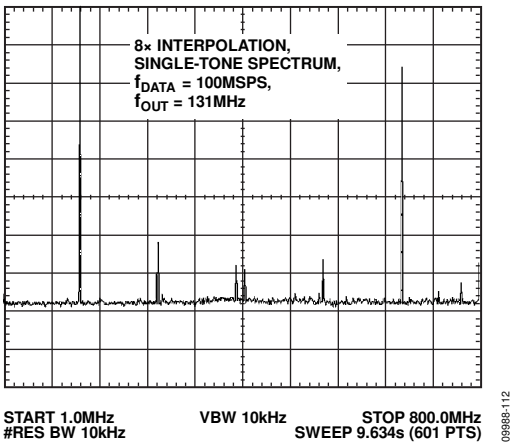


Figure 15. Single-Tone Spectrum, 8× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 131 MHz

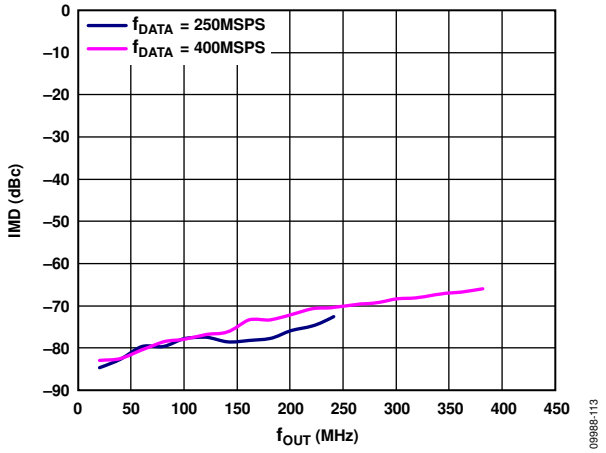


Figure 16. IMD vs. f_{OUT} over f_{DATA}, 2× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

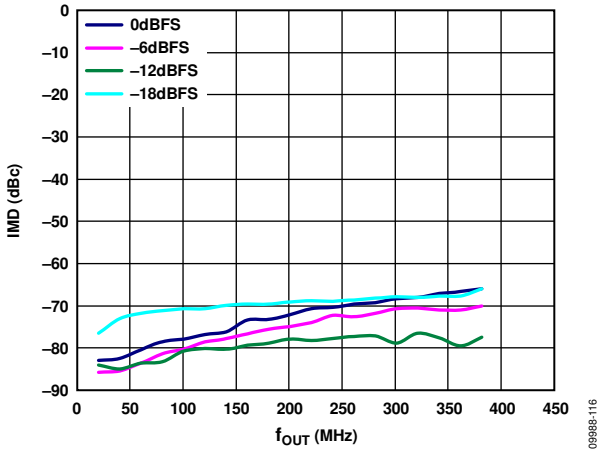


Figure 19. IMD vs. f_{OUT} over Digital Scale, 2× Interpolation, f_{DATA} = 400 MSPS, I_{FS} = 20 mA

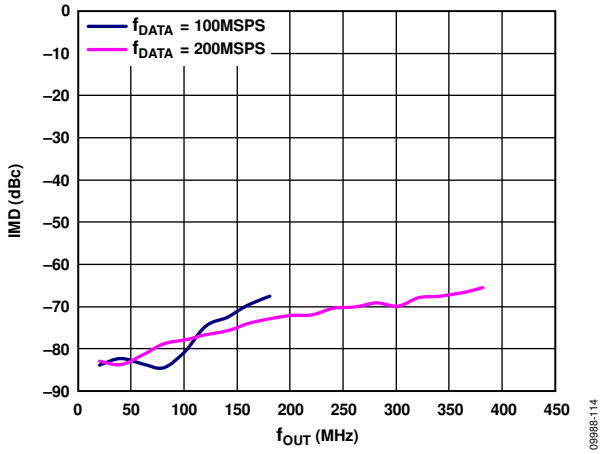


Figure 17. IMD vs. f_{OUT} over f_{DATA}, 4× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

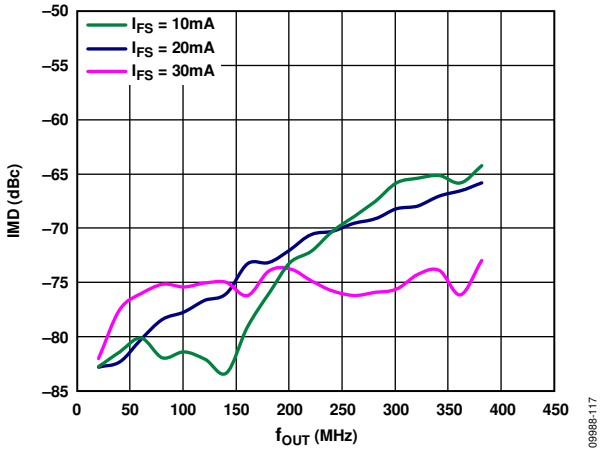


Figure 20. IMD vs. f_{OUT} over I_{FS}, 2× Interpolation, f_{DATA} = 400 MSPS, Digital Scale = 0 dBFS

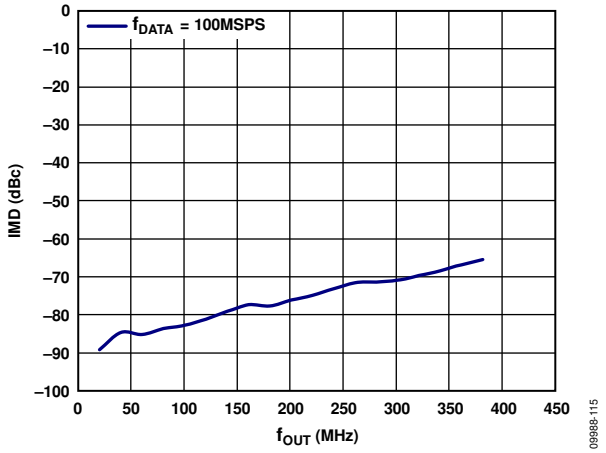


Figure 18. IMD vs. f_{OUT}, 8× Interpolation, f_{DATA} = 100 MSPS, Digital Scale = 0 dBFS, I_{FS} = 20 mA

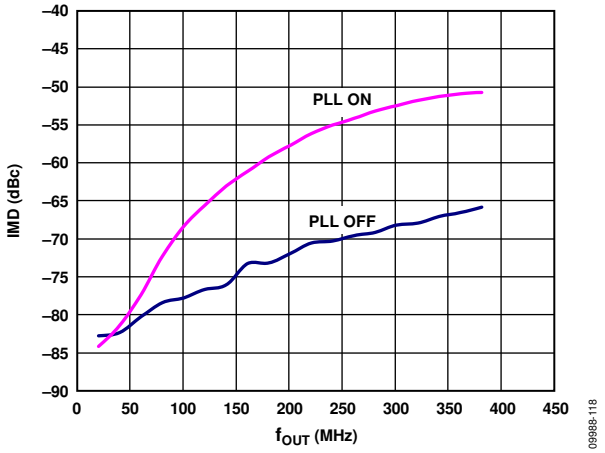


Figure 21. IMD vs. f_{OUT}, 4× Interpolation, f_{DATA} = 200 MSPS, Digital Scale = 0 dBFS, I_{FS} = 20 mA, PLL On and PLL Off

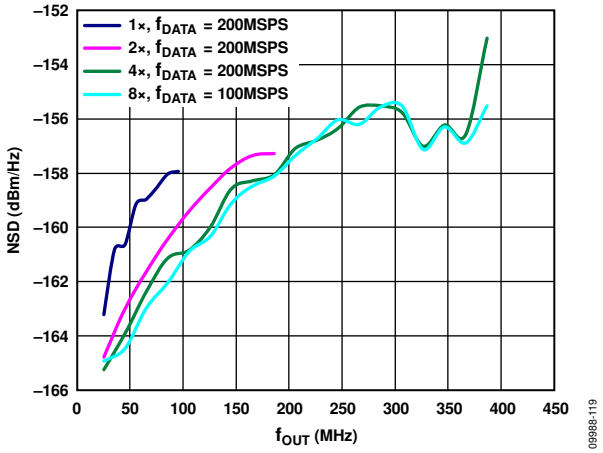


Figure 22. One-Tone NSD vs. f_{OUT} over Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA, PLL Off

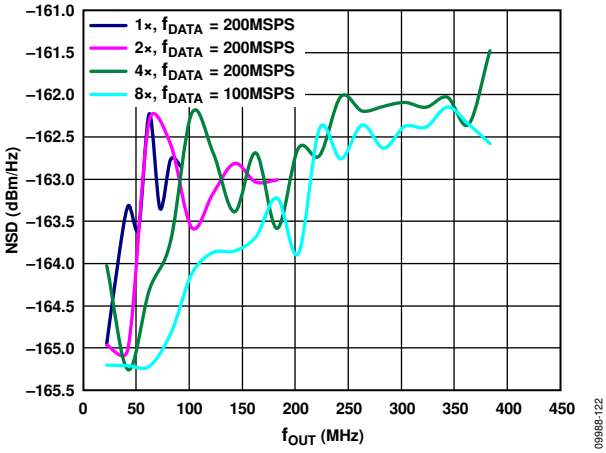


Figure 25. Eight-Tone NSD vs. f_{OUT} over Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA, PLL Off

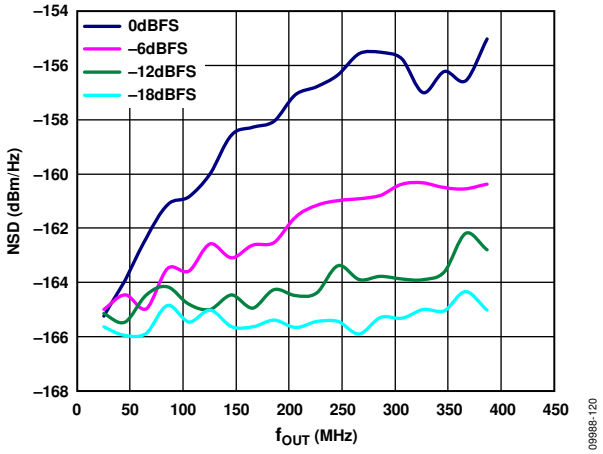


Figure 23. One-Tone NSD vs. f_{OUT} over Digital Scale, 4× Interpolation, f_{DATA} = 200 MSPS, I_{FS} = 20 mA, PLL Off

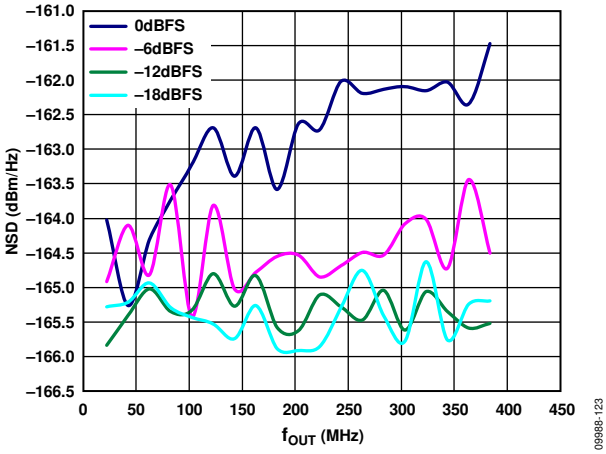


Figure 26. Eight-Tone NSD vs. f_{OUT} over Digital Scale, 4× Interpolation, f_{DATA} = 200 MSPS, I_{FS} = 20 mA, PLL Off

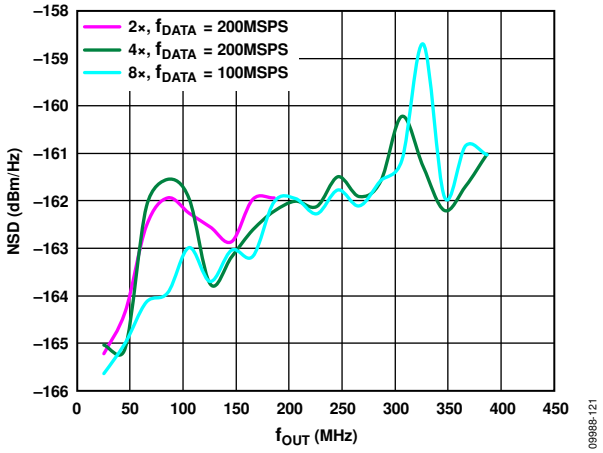


Figure 24. One-Tone NSD vs. f_{OUT} over Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA, PLL On

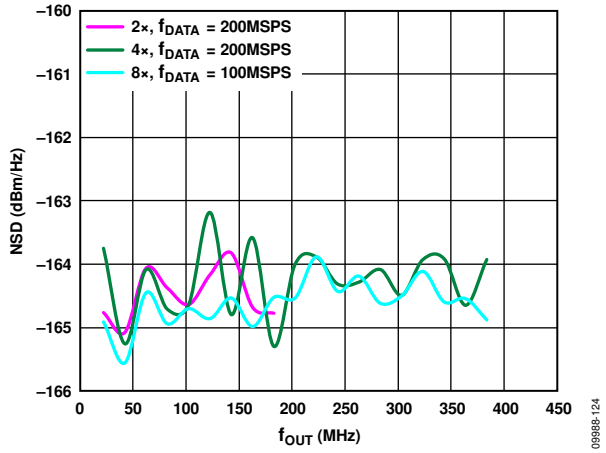


Figure 27. Eight-Tone NSD vs. f_{OUT} over Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA, PLL On

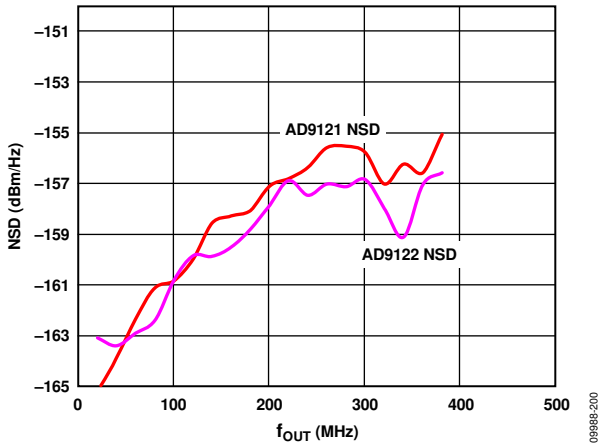


Figure 28. One-Tone NSD vs. f_{OUT}, f_{DATA} = 400 MSPS, 2× Interpolation, PLL Off (Comparison of AD9121 vs. AD9122)

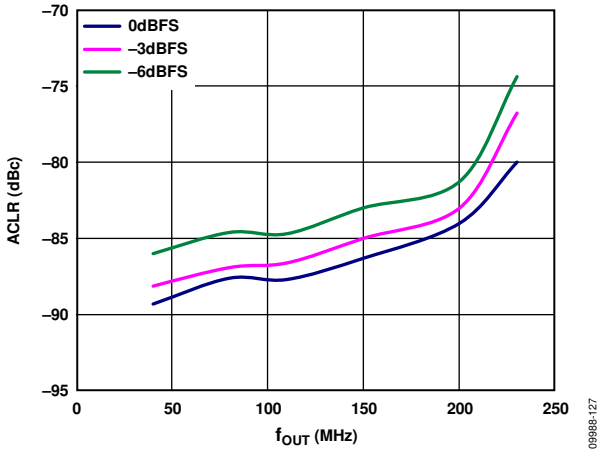


Figure 31. One-Carrier W-CDMA ACLR vs. f_{OUT} over Digital Scale, Second Alternate Channel, PLL Off

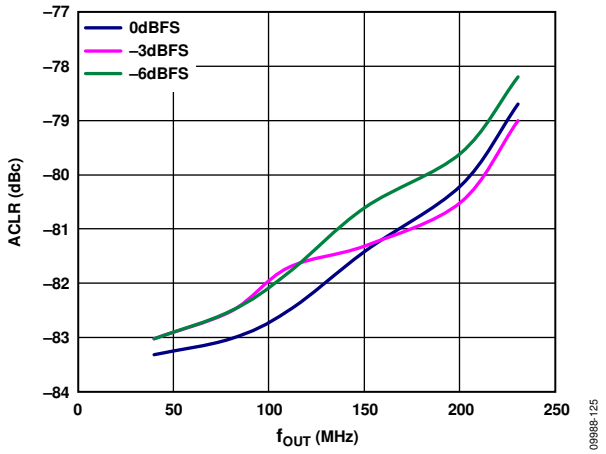


Figure 29. One-Carrier W-CDMA ACLR vs. f_{OUT} over Digital Scale, Adjacent Channel, PLL Off

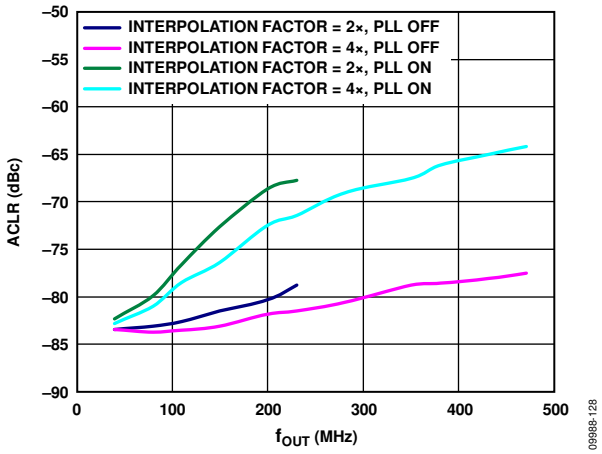


Figure 32. One-Carrier W-CDMA ACLR vs. f_{OUT} over Interpolation, Adjacent Channel, PLL On and PLL Off

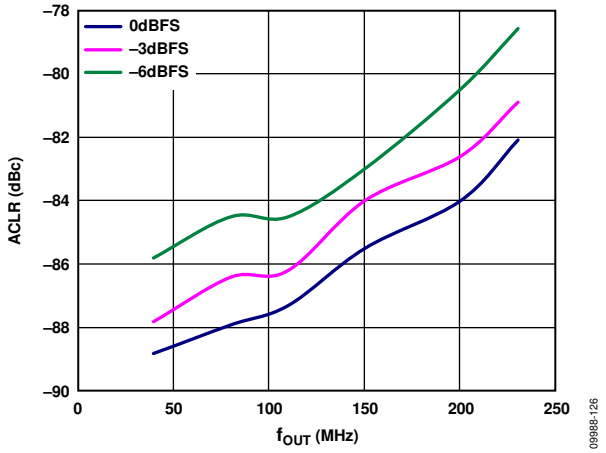


Figure 30. One-Carrier W-CDMA ACLR vs. f_{OUT} over Digital Scale, First Alternate Channel, PLL Off

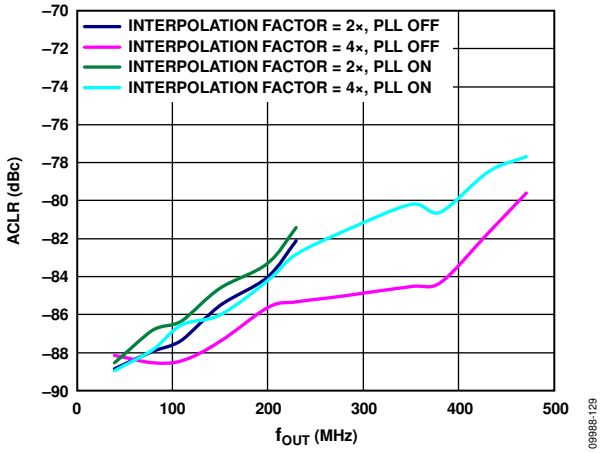


Figure 33. One-Carrier W-CDMA ACLR vs. f_{OUT} over Interpolation, First Alternate Channel, PLL On and PLL Off

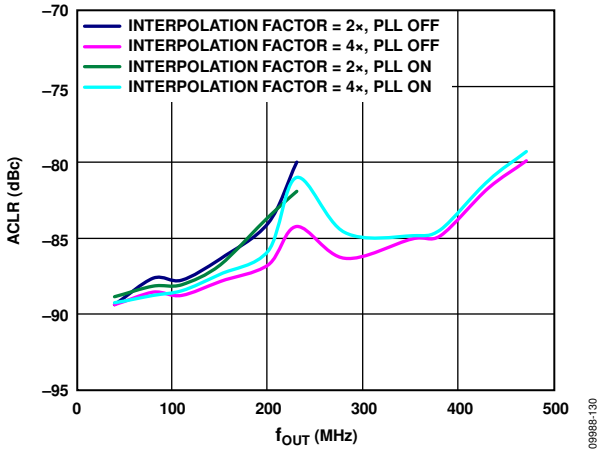


Figure 34. One-Carrier W-CDMA ACLR vs. f_{OUT} over Interpolation, Second Alternate Channel, PLL On and PLL Off

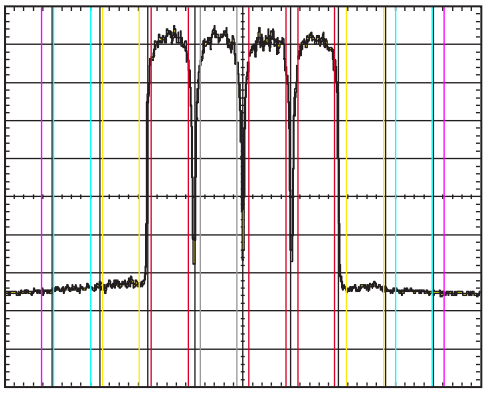


Figure 36. Four-Carrier W-CDMA ACLR Performance, IF = ~150 MHz

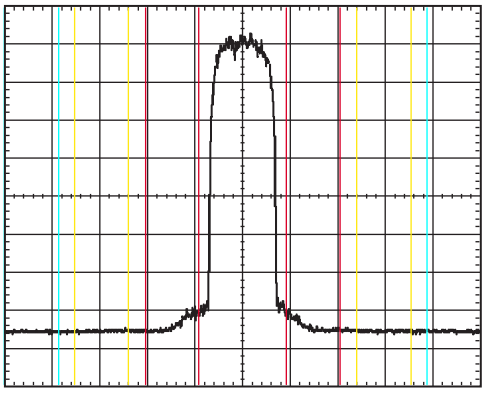


Figure 35. One-Carrier W-CDMA ACLR Performance, IF = ~150 MHz

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error
Offset error is the deviation of the output current from the ideal of 0 mA. For IOUT1P, 0 mA output is expected when all inputs are set to 0. For IOUT1N, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range
The output compliance range is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference voltage drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio, in decibels relative to the carrier (dBc), between the measured power within a channel and that of its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

The AD9121 combines many features that make it a very attractive DAC for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface to common quadrature modulators when designing single sideband (SSB) transmitters. The speed and performance of the AD9121 allow wider bandwidths and more carriers to be synthesized than in previously available DACs. In addition, the AD9121 includes an innovative low power, 32-bit, complex NCO that greatly increases the ease of frequency placement.

The AD9121 offers features that allow simplified synchronization with incoming data and between multiple devices. Auxiliary DACs are also provided on chip. The auxiliary DACs can be used for output dc offset compensation (for LO compensation in SSB transmitters) and for gain matching (for image rejection optimization in SSB transmitters).

SERIAL PORT OPERATION

The serial port is a flexible, synchronous serial communications port that allows easy interfacing to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9121. Single-byte or multiple-byte transfers are supported, as well as MSB first or LSB first transfer formats. The serial port interface can be configured as a single-pin I/O (SDIO) or as two unidirectional pins for input and output (SDIO and SDO).

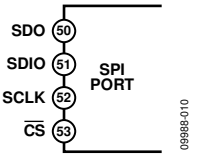


Figure 37. Serial Port Interface Pins

A communication cycle with the AD9121 has two phases. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first eight SCLK rising edges. The instruction byte provides the serial port controller with information regarding the data transfer cycle—Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, along with the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the device.

A logic high on the $\overline{CS}$ pin followed by a logic low resets the serial port timing to the initial state of the instruction cycle. From this state, the next eight rising SCLK edges represent the instruction bits of the current I/O operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one or more data bytes. Registers change immediately upon writing to the last bit of each transfer byte, except for the frequency tuning word and NCO phase offsets, which change only when the frequency tuning word (FTW) update bit (Register 0x36, Bit 0) is set.

DATA FORMAT

The instruction byte contains the information shown in Table 9.

Table 9. Serial Port Instruction Byte

I7 (MSB)	I6	I5	I4	I3	I2	I1	I0 (LSB)
R/W	A6	A5	A4	A3	A2	A1	A0

R/$\overline{W}$, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation, and Logic 0 indicates a write operation.

A6 to A0, Bit 6 to Bit 0 of the instruction byte, determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, A6 is the starting byte address. The remaining register addresses are generated by the device based on the LSB_FIRST bit (Register 0x00, Bit 6).

SERIAL PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

An active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. When the $\overline{CS}$ pin is high, the SDO and SDIO pins go to a high impedance state. During the communication cycle, the $\overline{CS}$ pin should stay low.

Serial Data I/O (SDIO)

Data is always written into the device on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Register 0x00, Bit 7. The default is Logic 0, configuring the SDIO pin as unidirectional.

Serial Data Output (SDO)

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. If the device operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

SERIAL PORT OPTIONS

The serial port can support both MSB first and LSB first data formats. This functionality is controlled by the LSB_FIRST bit (Register 0x00, Bit 6). The default is MSB first (LSB_FIRST = 0).

When LSB_FIRST = 0 (MSB first), the instruction and data bits must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow from high address to low address. In MSB first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When LSB_FIRST = 1 (LSB first), the instruction and data bits must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte. Subsequent data bytes should follow from low address to high address. In LSB first mode, the serial port internal byte address generator increments for each data byte of the multibyte communication cycle.

If the MSB first mode is active, the serial port controller data address decrements from the data address written toward 0x00 for multibyte I/O operations. If the LSB first mode is active, the serial port controller data address increments from the data address written toward 0x7F for multibyte I/O operations.

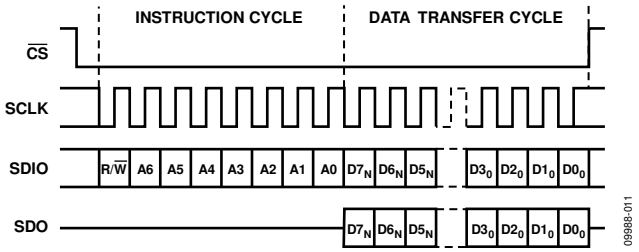


Figure 38. Serial Port Interface Timing, MSB First

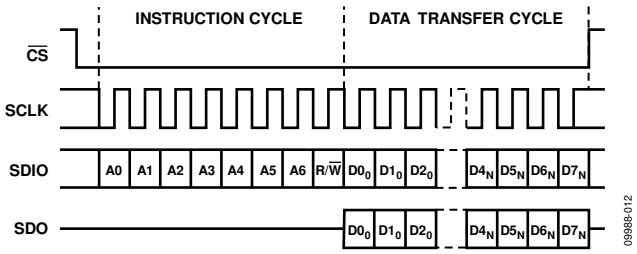


Figure 39. Serial Port Interface Timing, LSB First

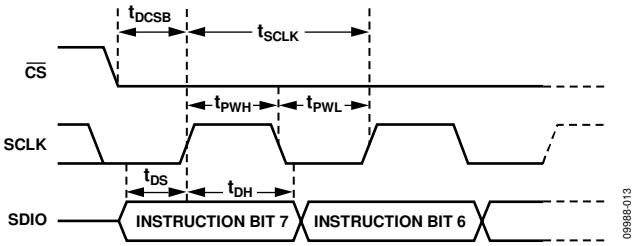


Figure 40. Timing Diagram for Serial Port Register Write

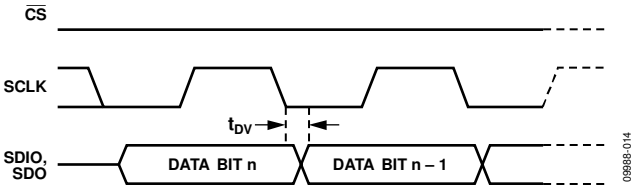


Figure 41. Timing Diagram for Serial Port Register Read

DEVICE CONFIGURATION REGISTER MAP AND DESCRIPTIONS

Table 10. Device Configuration Register Map

Addr (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x00	Comm	SDIO	LSB_FIRST	Reset						0x00
0x01	Power control	Power down I DAC	Power down Q DAC	Power down data receiver	Power down aux ADC					0x10
0x03	Data format	Binary data format	Q data first	MSB swap				Data Bus Width[1:0]		0x00
0x04	Interrupt enable	Enable PLL lock lost	Enable PLL locked	Enable sync signal lost	Enable sync signal locked			Enable FIFO Warning 1	Enable FIFO Warning 2	0x00
0x05	Interrupt enable	0	0	0	Enable AED compare pass	Enable AED compare fail	Enable SED compare fail	0	0	0x00
0x06	Event flag	PLL lock lost	PLL locked	Sync signal lost	Sync signal locked			FIFO Warning 1	FIFO Warning 2	N/A
0x07	Event flag				AED compare pass	AED compare fail	SED compare fail			N/A
0x08	Clock receiver control	DACCLK duty correction	REFCLK duty correction	DACCLK cross-correction	REFCLK cross-correction	1	1	1	1	0x3F
0x0A	PLL control	PLL enable	PLL manual enable	Manual VCO Band[5:0]						0x40
0x0C	PLL control	PLL Loop Bandwidth[1:0]			PLL Charge Pump Current[4:0]					0xD1
0x0D	PLL control	N2[1:0]			PLL cross-control enable	N0[1:0]		N1[1:0]		0xD9
0x0E	PLL status	PLL locked				VCO Control Voltage[3:0]				N/A
0x0F	PLL status			VCO Band Readback[5:0]						N/A
0x10	Sync control	Sync enable	Data/FIFO rate toggle			Rising edge sync	Sync Averaging[2:0]			0x48
0x11	Sync control			Sync Phase Request[5:0]						0x00
0x12	Sync status	Sync lost	Sync locked							N/A
0x13	Sync status	Sync Phase Readback[7:0] (6.2 format)								N/A
0x15	Data receiver status			LVDS FRAME level high	LVDS FRAME level low	LVDS DCI level high	LVDS DCI level low	LVDS data level high	LVDS data level low	N/A
0x16	DCI delay							DCI Delay[1:0]		0x00
0x17	FIFO control						FIFO Phase Offset[2:0]			0x04
0x18	FIFO status	FIFO Warning 1	FIFO Warning 2				FIFO soft align ack	FIFO soft align request		N/A
0x19	FIFO status	FIFO Level[7:0]								N/A
0x1B	Datapath control	Bypass premod	Bypass $sinc^{-1}$	Bypass NCO		NCO gain	Bypass phase comp and dc offset	Select sideband	Send I data to Q data	0xE4

Addr (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x1C	HB1 control						HB1[1:0]		Bypass HB1	0x00
0x1D	HB2 control		HB2[5:0]						Bypass HB2	0x00
0x1E	HB3 control		HB3[5:0]						Bypass HB3	0x00
0x1F	Chip ID	Chip ID[7:0]								0x08
0x30	FTW LSB	FTW[7:0]								0x00
0x31	FTW	FTW[15:8]								0x00
0x32	FTW	FTW[23:16]								0x00
0x33	FTW MSB	FTW[31:24]								0x00
0x34	NCO phase offset LSB	NCO Phase Offset[7:0]								0x00
0x35	NCO phase offset MSB	NCO Phase Offset[15:8]								0x00
0x36	NCO FTW update			FRAME FTW ack	FRAME FTW request			Update FTW ack	Update FTW request	0x00
0x38	I phase adj LSB	I Phase Adj[7:0]								0x00
0x39	I phase adj MSB							I Phase Adj[9:8]		0x00
0x3A	Q phase adj LSB	Q Phase Adj[7:0]								0x00
0x3B	Q phase adj MSB							Q Phase Adj[9:8]		0x00
0x3C	I DAC offset LSB	I DAC Offset[7:0]								0x00
0x3D	I DAC offset MSB	I DAC Offset[15:8]								0x00
0x3E	Q DAC offset LSB	Q DAC Offset[7:0]								0x00
0x3F	Q DAC offset MSB	Q DAC Offset[15:8]								0x00
0x40	I DAC FS adjust	I DAC FS Adj[7:0]								0xF9
0x41	I DAC control	I DAC sleep						I DAC FS Adj[9:8]		0x01
0x42	I aux DAC data	I Aux DAC[7:0]								0x00
0x43	I aux DAC control	I aux DAC sign	I aux DAC current direction	I aux DAC sleep				I Aux DAC[9:8]		0x00
0x44	Q DAC FS adjust	Q DAC FS Adj[7:0]								0xF9
0x45	Q DAC control	Q DAC sleep						Q DAC FS Adj[9:8]		0x01
0x46	Q aux DAC data	Q Aux DAC[7:0]								0x00
0x47	Q aux DAC control	Q aux DAC sign	Q aux DAC current direction	Q aux DAC sleep				Q Aux DAC[9:8]		0x00
0x48	Die temp range control		FS Current[2:0]			Reference Current[2:0]			Capacitor value	0x02
0x49	Die temp LSB	Die Temp[7:0]								N/A
0x4A	Die temp MSB	Die Temp[15:8]								N/A
0x67	SED control	SED compare enable		Sample error detected		Autoclear enable		Compare fail	Compare pass	0x00
0x68	Compare I0 LSBs	Compare Value I0[7:0]								0xB6
0x69	Compare I0 MSBs	Compare Value I0[15:8]								0x7A
0x6A	Compare Q0 LSBs	Compare Value Q0[7:0]								0x45
0x6B	Compare Q0 MSBs	Compare Value Q0[15:8]								0xEA

Addr (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x6C	Compare I1 LSBs	Compare Value I1[7:0]								0x16
0x6D	Compare I1 MSBs	Compare Value I1[15:8]								0x1A
0x6E	Compare Q1 LSBs	Compare Value Q1[7:0]								0xC6
0x6F	Compare Q1 MSBs	Compare Value Q1[15:8]								0xAA
0x70	SED I LSBs	Errors Detected I_BITS[7:0]								0x00
0x71	SED I MSBs	Errors Detected I_BITS[15:8]								0x00
0x72	SED Q LSBs	Errors Detected Q_BITS[7:0]								0x00
0x73	SED Q MSBs	Errors Detected Q_BITS[15:8]								0x00
0x7F	Revision	0	0	Revision[3:0]				0	0	N/A

Table 11. Device Configuration Register Descriptions

Register Name	Address (Hex)	Bits	Name	Description	Default
Comm	0x00	7	SDIO	SDIO pin operation. 0 = SDIO operates as an input only. 1 = SDIO operates as a bidirectional input/output.	0
		6	LSB_FIRST	Serial port communication, LSB or MSB first. 0 = MSB first. 1 = LSB first.	0
		5	Reset	The device is placed in reset when this bit is written high and remains in reset until the bit is written low.	0
Power Control	0x01	7	Power down I DAC	1 = power down I DAC.	0
		6	Power down Q DAC	1 = power down Q DAC.	0
		5	Power down data receiver	1 = power down the input data receiver.	0
		4	Power down auxiliary ADC	1 = power down the auxiliary ADC for temperature sensor.	1
Data Format	0x03	7	Binary data format	0 = input data is in twos complement format. 1 = input data is in binary format.	0
		6	Q data first	Indicates I/Q data pairing on data input. 0 = I data sent to data receiver first. 1 = Q data sent to data receiver first.	0
		5	MSB swap	Swaps the bit order of the data input port. 0 = order of the data bits corresponds to the pin descriptions. 1 = bit designations are swapped; most significant bits become the least significant bits.	0
		[1:0]	Data Bus Width[1:0]	Data receiver interface mode. See the LVDS Input Data Ports section for information about the operation of the different interface modes. 00 = word mode; 14-bit interface bus width. 01 = byte mode; 7-bit interface bus width. 10 = invalid. 11 = invalid.	00
Interrupt Enable	0x04	7	Enable PLL lock lost	1 = enable interrupt for PLL lock lost.	0
		6	Enable PLL locked	1 = enable interrupt for PLL locked.	0
		5	Enable sync signal lost	1 = enable interrupt for sync signal lost.	0
		4	Enable sync signal locked	1 = enable interrupt for sync signal locked.	0
		1	Enable FIFO Warning 1	1 = enable interrupt for FIFO Warning 1.	0
		0	Enable FIFO Warning 2	1 = enable interrupt for FIFO Warning 2.	0

Register Name	Address (Hex)	Bits	Name	Description	Default
Interrupt Enable	0x05	[7:5]	Set to 0	Set these bits to 0.	000
		4	Enable AED compare pass	1 = enable interrupt for AED comparison pass.	0
		3	Enable AED compare fail	1 = enable interrupt for AED comparison fail.	0
		2	Enable SED compare fail	1 = enable interrupt for SED comparison fail.	0
		[1:0]	Set to 0	Set these bits to 0.	00
Event Flag	0x06	7	PLL lock lost	1 = indicates that the PLL, which had been previously locked, has unlocked from the reference signal. This is a latched signal.	N/A
		6	PLL locked	1 = indicates that the PLL has locked to the reference clock input.	N/A
		5	Sync signal lost	1 = indicates that the sync logic, which had been previously locked, has lost alignment. This is a latched signal.	N/A
		4	Sync signal locked	1 = indicates that the sync logic has achieved sync alignment. This is indicated when no phase changes were requested for at least a few full averaging cycles.	N/A
		1	FIFO Warning 1	1 = indicates that the difference between the FIFO read and write pointers is 1.	N/A
		0	FIFO Warning 2	1 = indicates that the difference between the FIFO read and write pointers is 2.	N/A
			Note that all event flags are cleared by writing the respective bit high.		
	0x07	4	AED compare pass	1 = indicates that the SED logic detected a valid input data pattern compared against the preprogrammed expected values. This is a latched signal.	N/A
		3	AED compare fail	1 = indicates that the SED logic detected an invalid input data pattern compared against the preprogrammed expected values. This latched signal is automatically cleared when eight valid I/Q data pairs are received.	N/A
		2	SED compare fail	1 = indicates that the SED logic detected an invalid input data pattern compared against the preprogrammed expected values. This is a latched signal.	N/A
			Note that all event flags are cleared by writing the respective bit high.		
Clock Receiver Control	0x08	7	DACCLK duty correction	1 = enable duty cycle correction on the DACCLK input.	0
		6	REFCLK duty correction	1 = enable duty cycle correction on the REFCLK input.	0
		5	DACCLK cross-correction	1 = enable differential crossing correction on the DACCLK input.	1
		4	REFCLK cross-correction	1 = enable differential crossing correction on the REFCLK input.	1
PLL Control	0x0A	7	PLL enable	1 = enable the PLL clock multiplier. The REFCLK input is used as the PLL reference clock signal.	0
		6	PLL manual enable	1 = enable manual selection of the VCO band. The correct VCO band must be determined by the user and written to Bits[5:0].	1
		[5:0]	Manual VCO Band[5:0]	Selects the VCO band to be used.	000000
	0x0C	[7:6]	PLL Loop Bandwidth[1:0]	Selects the PLL loop filter bandwidth. 00 = widest bandwidth. … 11 = narrowest bandwidth.	11
		[4:0]	PLL Charge Pump Current[4:0]	Sets the nominal PLL charge pump current. 00000 = lowest current setting. … 11111 = highest current setting.	10001

Register Name	Address (Hex)	Bits	Name	Description	Default
PLL Control	0x0D	[7:6]	N2[1:0]	PLL control clock divider. This divider determines the ratio of the REFCLK frequency to the PLL controller clock frequency. f_{PC_CLK} must always be less than 75 MHz. 00 = f_{REFCLK}/f_{PC_CLK} = 2. 01 = f_{REFCLK}/f_{PC_CLK} = 4. 10 = f_{REFCLK}/f_{PC_CLK} = 8. 11 = f_{REFCLK}/f_{PC_CLK} = 16.	11
		4	PLL cross-control enable	1 = enable PLL cross-point controller.	1
		[3:2]	N0[1:0]	PLL VCO divider. This divider determines the ratio of the VCO frequency to the DACCLK frequency. 00 = f_{VCO}/f_{DACCLK} = 1. 01 = f_{VCO}/f_{DACCLK} = 2. 10 = f_{VCO}/f_{DACCLK} = 4. 11 = f_{VCO}/f_{DACCLK} = 4.	10
		[1:0]	N1[1:0]	PLL loop divider. This divider determines the ratio of the DACCLK frequency to the REFCLK frequency. 00 = f_{DACCLK}/f_{REFCLK} = 2. 01 = f_{DACCLK}/f_{REFCLK} = 4. 10 = f_{DACCLK}/f_{REFCLK} = 8. 11 = f_{DACCLK}/f_{REFCLK} = 16.	01
PLL Status	0x0E	7	PLL locked	1 = the PLL-generated clock is tracking the REFCLK input signal.	N/A
		[3:0]	VCO Control Voltage[3:0]	VCO control voltage readback. See Table 24.	N/A
	0x0F	[5:0]	VCO Band Readback[5:0]	Indicates the VCO band currently selected.	N/A
Sync Control	0x10	7	Sync enable	1 = enable the synchronization logic.	0
		6	Data/FIFO rate toggle	0 = operate the synchronization at the FIFO reset rate. 1 = operate the synchronization at the data rate.	1
		3	Rising edge sync	0 = sync is initiated on the falling edge of the sync input. 1 = sync is initiated on the rising edge of the sync input.	1
		[2:0]	Sync Averaging[2:0]	Sets the number of input samples that are averaged in determining the sync phase. 000 = 1. 001 = 2. 010 = 4. 011 = 8. 100 = 16. 101 = 32. 110 = 64. 111 = 128.	000
	0x11	[5:0]	Sync Phase Request[5:0]	This register sets the requested clock phase offset after sync. The offset unit is in DACCLK cycles. This register enables repositioning of the DAC output with respect to the sync input. The offset can also be used to skew the DAC outputs between the synchronized DACs. 000000 = 0 DACCLK cycles. 000001 = 1 DACCLK cycle. … 111111 = 63 DACCLK cycles.	000000