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11-/14-Bit, 5.7 GSPS, RF Digital-to-Analog Converter

Data Sheet

AD9119/AD9129

FEATURES

- DAC update rate: up to 5.7 GSPS
- Direct RF synthesis at 2.85 GSPS data rate
  - DC to 1.425 GHz in baseband mode
  - DC to 1.0 GHz in 2× interpolation mode
  - 1.425 GHz to 4.2 GHz in Mix-Mode
- Bypassable 2× interpolation
- Excellent dynamic performance
- Supports DOCSIS 3.0 wideband ACLR/harmonic performance
  - 8 QAM carriers: ACLR > 65 dBc
- Industry-leading single/multicarrier IF or RF synthesis
  - 4-carrier W-CDMA ACLR at 2457.6 MSPS
    - f_{OUT} = 900 MHz, ACLR = 71 dBc (baseband mode)
    - f_{OUT} = 2100 MHz, ACLR = 68 dBc (Mix-Mode)
    - f_{OUT} = 2700 MHz, ACLR = 67 dBc (Mix-Mode)
- Dual-port LVDS and DHSTL data interface
  - Up to 1.425 GSPS operation
  - Source synchronous DDR clocking with parity bit
- Low power: 1.0 W at 2.85 GSPS (1.3 W at 5.7 GSPS)

APPLICATIONS

- Broadband communications systems
  - CMTS/VOD
  - Wireless infrastructure: W-CDMA, LTE, point-to-point
- Instrumentation, automatic test equipment (ATE)
- Radar, jammers

FUNCTIONAL BLOCK DIAGRAM

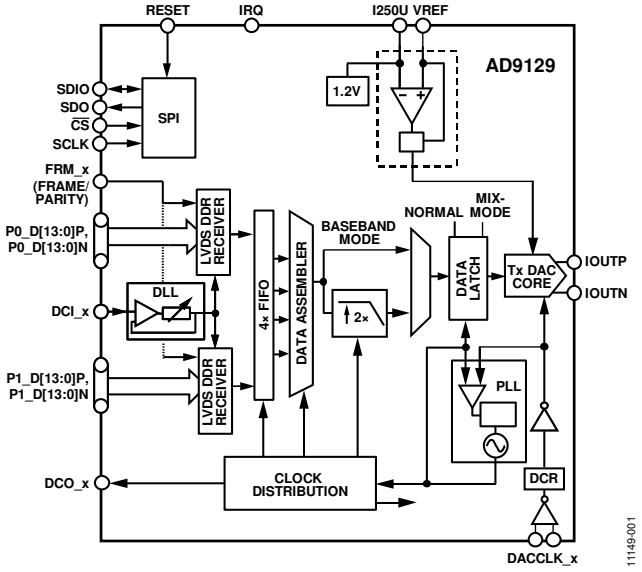

Figure 1.

GENERAL DESCRIPTION

The AD9119/AD9129 are high performance, 11-/14-bit RF digital-to-analog converters (DACs) supporting data rates up to 2.85 GSPS. The DAC core is based on a quad-switch architecture that enables dual-edge clocking operation, effectively increasing the DAC update rate to 5.7 GSPS when configured for Mix-Mode™ or 2× interpolation. The high dynamic range and bandwidth enable multicarrier generation up to 4.2 GHz.

In baseband mode, wide bandwidth capability combines with high dynamic range to support from 1 to 158 contiguous carriers for CATV infrastructure applications. A choice of two optional 2× interpolation filters is available to simplify the postreconstruction filter by effectively increasing the DAC update rate by a factor of 2. In Mix-Mode operation, the AD9119/AD9129 can reconstruct RF carriers in the second and third Nyquist zone while still maintaining exceptional dynamic range up to 4.2 GHz. The high performance NMOS DAC core features a quad-switch architecture that enables industry-leading direct RF synthesis performance with minimal loss in output power. The output current can be programmed over a range of 9.5 mA to 34.4 mA.

The AD9119/AD9129 include several features that may further simplify system integration. A dual-port, source synchronous LVDS interface simplifies the data interface to a host FPGA/ASIC. A differential frame/parity bit is also included to monitor the integrity of the interface. On-chip delay locked loops (DLLs) are used to optimize timing between different clock domains.

A serial peripheral interface (SPI) is used to configure the AD9119/AD9129 and monitor the status of readback registers. The AD9119/AD9129 is manufactured on a 0.18 µm CMOS process and operates from +1.8 V and −1.5 V supplies. It is supplied in a 160-ball chip scale package ball grid array.

PRODUCT HIGHLIGHTS

1. High dynamic range and signal reconstruction bandwidth support RF signal synthesis of up to 4.2 GHz.
2. Dual-port interface with double data rate (DDR) LVDS data receivers supports 2850 MSPS maximum conversion rate.
3. Manufactured on a CMOS process; a proprietary switching technique enhances dynamic performance.

Rev. A
Document Feedback

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SPECIFICATIONS

DC SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = −1.5 V, I_{OUTFS} = 33 mA, T_A = −40°C to +85°C.

Table 1.

	AD9119			AD9129			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		11			14		Bits
ACCURACY							
Integral Nonlinearity (INL)		0.2			1.4		LSB
Differential Nonlinearity (DNL)		0.15			1.1		LSB
ANALOG OUTPUTS							
Gain Error (with Internal Reference)		+2.5			+2.5		%
Full-Scale Output Current Maximum	33.4	34.2	34.9	33.4	34.2	34.9	mA
Full-Scale Output Current Minimum	9.1	9.4	9.6	9.1	9.4	9.6	mA
Output Compliance Range	1.5		2.5	1.5		2.5	V
Output Impedance[1]							
DAC CLOCK INPUT (DACCLK_P, DACCLK_N)							
Differential Peak-to-Peak Voltage	0.4	1	2	0.4	1	2	V
Common-Mode Voltage		1.2			1.2		V
TEMPERATURE DRIFT							
Gain		60			60		ppm/°C
Reference Voltage		20			20		ppm/°C
REFERENCE							
Internal Reference Voltage		1.0			1.0		V
Output Resistance		5			5		kΩ
ANALOG SUPPLY VOLTAGES							
VDDA	1.70	1.80	1.90	1.70	1.80	1.90	V
FIR40 Enabled, DACCLK > 2600 MSPS	1.8	1.9	2.0	1.8	1.9	2.0	V
VSSA	−1.4	−1.5	−1.6	−1.4	−1.5	−1.6	V
DIGITAL SUPPLY VOLTAGES							
VDD	1.70	1.8	1.90	1.70	1.8	1.90	V
FIR40 Enabled, DACCLK > 2600 MSPS	1.8	1.9	2.0	1.8	1.9	2.0	V
SUPPLY CURRENTS AND POWER DISSIPATION, 2.3 GSPS (NORMAL MODE)							
I_{VDDA}		202	209		202	209	mA
I_{VSSA}		53	54		53	54	mA
I_{DVDD}		307	327		307	327	mA
Power Dissipation							
Normal Mode		1.0	1.05		1.0	1.05	W
FIR25 Enabled		1.17	1.24		1.17	1.24	W
FIR40 Enabled		1.3	1.4		1.3	1.4	W
Reduced Power Mode, Power-Down Enabled (Register 0x01 = 0xEF)							
I_{VDDA}		7.6			7.6		mA
I_{VSSA}		6			6		µA
I_{VDD}		0.4			0.4		mA
SUPPLY CURRENTS AND POWER DISSIPATION, 2.8 GSPS (NORMAL MODE)							
I_{VDDA}		230			230		mA
I_{VSSA}		53			53		mA
I_{DVDD}		336			336		mA
Power Dissipation (Normal Mode)		1.1			1.1		W

[1] For more information about output impedance, see the Output Stage Configuration section.

LVDS DIGITAL SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = −1.5 V, I_{OUTFS} = 33 mA, T_A = −40°C to +85°C. LVDS drivers and receivers are compatible with the IEEE Standard 1596.3-1996, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LVDS DATA INPUTS (P1_D[13:0]P, P1_D[13:0]N, P0_D[13:0]P, P0_D[13:0]N, FRM_P, FRM_N)		Px_DxP = V_{IA}, Px_DxN = V_{IB}				
Input Voltage Range	V_{IA}, V_{IB}		825		1575	mV
Input Differential Threshold	V_{IDTH}		−100		+100	mV
Input Differential Hysteresis	$V_{IDTHH} - V_{IDTHL}$			20		mV
Receiver Differential Input Impedance	R_{IN}		80		120	Ω
LVDS Input Rate			1425			MSPS
Input Capacitance				1.2		pF
LVDS CLOCK INPUTS (DCI_P, DCI_N)		DCI_P = V_{IA}, DCI_N = V_{IB}				
Input Voltage Range	V_{IA}, V_{IB}		825		1575	mV
Input Differential Threshold	V_{IDTH}		−225		+225	mV
Input Differential Hysteresis	$V_{IDTHH} - V_{IDTHL}$			20		mV
Receiver Differential Input Impedance	R_{IN}		80		120	Ω
Maximum Clock Rate			712.5			MHz
LVDS CLOCK OUTPUTS (DCO_P, DCO_N)		DCO_P = V_{OA}, DCO_N = V_{OB}, 100 Ω termination				
Output Voltage High	V_{OA}, V_{OB}				1375	mV
Output Voltage Low	V_{OA}, V_{OB}		1025			mV
Output Differential Voltage	$\|V_{OA}\|$, $\|V_{OB}\|$	Register 0x7C[7:6] = 01b (default)	200	225	250	mV
Output Offset Voltage	V_{OS}		1150		1250	mV
Output Impedance, Single-Ended	R_O		80	100	120	Ω
R_O Mismatch Between A and B	ΔR_O				10	%
Change in $\|V_{OD}\|$ Between Setting 0 and Setting 1	$\|\Delta V_{OD}\|$				25	mV
Change in V_{OS} Between Setting 0 and Setting 1	ΔV_{OS}				25	mV
Output Current						
Driver Shorted to Ground	I_{SA}, I_{SB}				20	mA
Drivers Shorted Together	I_{SAB}				4	mA
Power-Off Output Leakage	$\|I_{XA}\|$, $\|I_{XB}\|$				10	µA
Maximum Clock Rate			712.5			MHz

HSTL DIGITAL SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = −1.5 V, I_{OUTFS} = 33 mA, T_A = −40°C to +85°C. HSTL receiver levels are compatible with the EIA/JEDEC JESD8-6 standard, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Comments/Conditions	Min	Typ	Max	Unit
HSTL DATA INPUTS (P1_D[13:0]P, P1_D[13:0]N, P0_D[13:0]P, P0_D[13:0]N, FRM_P, FRM_N)		Px_DxP = V_{IA}, Px_DxN = V_{IB}				
Common-Mode Input Voltage Range	V_{IA}, V_{IB}		0.68		0.9	V
Differential Input Voltage			200			mV
Receiver Differential Input Impedance	R_{IN}		80		120	Ω
HSTL Input Rate			1425			MSPS
Input Capacitance				1.2		pF
HSTL CLOCK INPUT (DCI_P, DCI_N)		DCI_P = V_{IA}, DCI_N = V_{IB}				
Common-Mode Input Voltage Range	V_{IA}, V_{IB}		0.68		0.9	mV
Differential Input Voltage			450			mV
Receiver Differential Input Impedance	R_{IN}		80		120	Ω
Maximum Clock Rate			712.5			MHz

SERIAL PORT AND CMOS PIN SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = −1.5 V, I_{OUTFS} = 33 mA, T_A = −40°C to +85°C.

Table 4.

Parameter	Symbol	Test Comments/Conditions	Min	Typ	Max	Unit
WRITE OPERATION		See Figure 126				
SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$				20	MHz
SCLK Clock High	t_{HIGH}		20			ns
SCLK Clock Low	t_{LOW}		20			ns
SDIO to SCLK Setup Time	t_{DS}		10			ns
SCLK to SDIO Hold Time	t_{DH}		5			ns
$\overline{CS}$ to SCLK Setup Time	t_S		10			ns
SCLK to $\overline{CS}$ Hold Time	t_H		5			ns
READ OPERATION		See Figure 127				
SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$				20	MHz
SCLK Clock High	t_{HIGH}		20			ns
SCLK Clock Low	t_{LOW}		20			ns
SDIO to SCLK Setup Time	t_{DS}		10			ns
SCLK to SDIO Hold Time	t_{DH}		5			ns
$\overline{CS}$ to SCLK Setup Time	t_S		10			ns
SCLK to SDIO (or SDO) Data Valid Time	t_{DV}				10	ns
$\overline{CS}$ to SDIO (or SDO) Output Valid to High-Z	t_{EZ}			2		
INPUTS (SDI, SDIO, SCLK, $\overline{CS}$)						
Voltage In High	V_{IH}		1.2	1.8		V
Voltage In Low	V_{IL}			0	0.4	V
Current In High	I_{IH}				+75	µA
Current In Low	I_{IL}		−150			µA
OUTPUTS (SDIO, SYNC)						
Voltage Out High	V_{OH}		1.3		2.0	V
Voltage Out Low	V_{OL}		0		0.3	V
Current Out High	I_{OH}			4		mA
Current Out Low	I_{OL}			4		mA

AC SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = −1.5 V, I_{OUTFS} = 33 mA, T_A = −40°C to +85°C, unless otherwise noted.

Table 5.

	AD9119			AD9129			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE							
DAC Update Rate (DACCLK_x Inputs)							
Normal Mode, FIR25 Enabled, or FIR40 Enabled with VDD = 1.9 V	1400		2850	1400		2850	MSPS
FIR40 Filter Enabled, VDD = 1.8 V	1400		2600	1400		2600	MSPS
Adjusted DAC Update Rate[1]	1400		2850	1400		2850	MSPS
Output Settling Time to 0.1%		13			13		ns
SPURIOUS-FREE DYNAMIC RANGE (SFDR)							
f_{DAC} = 2600 MSPS							
f_{OUT} = 100 MHz		−76			−76		dBc
f_{OUT} = 350 MHz		−65			−65		dBc
f_{OUT} = 550 MHz		−63			−64		dBc
f_{OUT} = 950 MHz		−55			−55		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)							
f_{DAC} = 2600 MSPS, $f_{OUT2} = f_{OUT1}$ + 1.4 MHz							
f_{OUT} = 100 MHz		−82			−86		dBc
f_{OUT} = 350 MHz		−78			−85		dBc
f_{OUT} = 550 MHz		−73			−83		dBc
f_{OUT} = 950 MHz		−67			−76		dBc
NOISE SPECTRAL DENSITY (NSD)							
Single Tone, f_{DAC} = 2800 MSPS							
f_{OUT} = 100 MHz		−157			−166		dBm/Hz
f_{OUT} = 350MHz		−157			−162		dBm/Hz
f_{OUT} = 550 MHz		−155			−158		dBm/Hz
f_{OUT} = 850 MHz		−154			−157		dBm/Hz
DOCSIS ACLR PERFORMANCE (50 MHz to 1000 MHz) at ≥6 MHz OFFSET							
f_{DAC} = 2782 MSPS							
8 Contiguous Carriers		64			64		dBc
16 Contiguous Carriers		62			63		dBc
32 Contiguous Carriers		60			61		dBc
W-CDMA ACLR (SINGLE CARRIER)							
Adjacent Channel							
f_{DAC} = 2605.056 MSPS, f_{OUT} = 750 MHz		75			75		dBc
f_{DAC}= 2605.056 MSPS, f_{OUT} = 950 MHz		74			74		dBc
f_{DAC} = 2605.056 MSPS, f_{OUT} = 1700 MHz (Mix-Mode)		73.5			73.5		dBc
f_{DAC} = 2605.056 MSPS, f_{OUT} = 2100 MHz (Mix-Mode)		69			69		dBc
Alternate Adjacent Channel							
f_{DAC} = 2605.056 MSPS, f_{OUT} = 750 MHz		80			80		dBc
f_{DAC} = 2605.056 MSPS, f_{OUT} = 950 MHz		78			78		dBc
f_{DAC} = 2605.056 MSPS, f_{OUT} = 1700 MHz (Mix-Mode)		74			74		dBc
f_{DAC} = 2605.056 MSPS, f_{OUT} = 2100 MHz (Mix-Mode)		72			72		dBc

[1] Adjusted DAC update rate is calculated as f_{DAC} divided by the minimum required interpolation factor. For the AD9119/AD9129, the minimum interpolation factor is 1. Thus, with f_{DAC} = 2850 MSPS, f_{DAC} adjusted = 2850 MSPS.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
DCI, DCO to VSS	−0.3 V to VDD + 0.3 V
LVDS Data Inputs to VSS	−0.3 V to VDD + 0.3 V
IOUTP, IOUTN to VSSA	VSSA − 0.3V to +2.5V
I250U, VREF to VSSA	VSSA − 0.3 V to VDDA + 0.3 V
IRQ, $\overline{CS}$, SCLK, SDO, SDIO, RESET, SYNC to VSS	−0.3 V to VDD + 0.3 V
Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
160-Ball CSP_BGA	31.2	7.0	°C/W[1]

[1] With no airflow movement.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

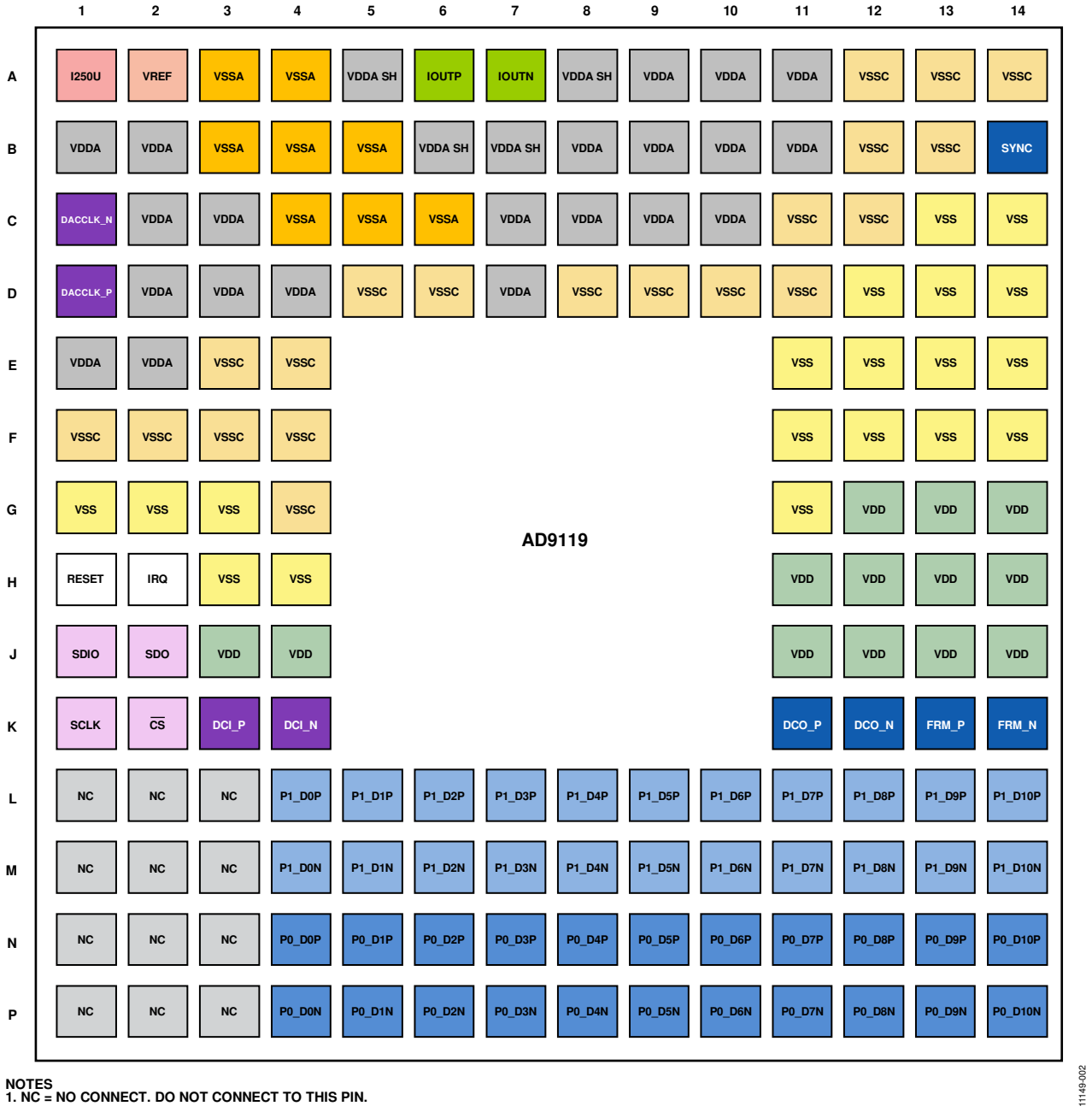


Figure 2. AD9119 Pin Configuration

Table 8. AD9119 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	I250U	Nominal 1.0 V Reference. Tie this pin to VSSA via a 4.0 kΩ resistor to generate a 250 µA reference current.
A2	VREF	Voltage Reference Input/Output. Decouple to VSSA with a 1 nF capacitor.
A3, A4, B3, B4, B5, C4, C5, C6	VSSA	−1.5 V Analog Supply Voltage Input.
A5, A8, B6, B7	VDDA SH	+1.8 V Analog Supply Shield. Tie these pins to VDDA at the DAC.
A9, A10, A11, B1, B2, B8, B9, B10, B11, C2, C3, C7, C8, C9, C10, D2, D3, D4, D7, E1, E2	VDDA	+1.8 V Analog Supply Voltage Input.

Pin No.	Mnemonic	Description
G12, G13, G14, H11, H12, H13, H14, J3, J4, J11, J12, J13, J14	VDD	+1.8 V Digital Supply Voltage Input.
C13, C14, D12, D13, D14, E11, E12, E13, E14, F11, F12, F13, F14, G1, G2, G3, G11, H3, H4	VSS	+1.8 V Digital Supply Return.
A12, A13, A14, B12, B13, C11, C12, D5, D6, D8, D9, D10, D11, E3, E4, F1, F2, F3, F4, G4	VSSC	Analog Supply Return.
A6	IOUTP	DAC Positive Current Output Source.
A7	IOUTN	DAC Negative Current Output Source.
B14	SYNC	Synchronization Signal Output.
C1, D1	DACCLK_N, DACCLK_P	Negative/Positive DAC Clock Input.
H1	RESET	Reset Input. Active high. If unused, tie this pin to VSS.
H2	IRQ	Interrupt Request Open Drain Output. Active high. Pull up this pin to VDD with a 1 kΩ resistor.
J1	SDIO	Serial Port Data Input/Output.
J2	SDO	Serial Port Data Output.
K1	SCLK	Serial Port Clock Input.
K2	$\overline{CS}$	Serial Port Enable Input.
K3, K4	DCI_P, DCI_N	Positive, Negative Data Clock Input (DCI).
K11, K12	DCO_P, DCO_N	Positive, Negative Data Clock Output (DCO).
K13, K14	FRM_P, FRM_N	Positive, Negative Data Frame/Parity Signal (FRAME/PARITY).
L1, M1	NC, NC	No Connect. Do not connect to this pin.
L2, M2	NC, NC	No Connect. Do not connect to this pin.
L3, M3	NC, NC	No Connect. Do not connect to this pin.
L4, M4	P1_D0P, P1_D0N	Data Port 1 Positive/Negative Data Input Bit 0.
L5, M5	P1_D1P, P1_D1N	Data Port 1 Positive/Negative Data Input Bit 1.
L6, M6	P1_D2P, P1_D2N	Data Port 1 Positive/Negative Data Input Bit 2.
L7, M7	P1_D3P, P1_D3N	Data Port 1 Positive/Negative Data Input Bit 3.
L8, M8	P1_D4P, P1_D4N	Data Port 1 Positive/Negative Data Input Bit 4.
L9, M9	P1_D5P, P1_D5N	Data Port 1 Positive/Negative Data Input Bit 5.
L10, M10	P1_D6P, P1_D6N	Data Port 1 Positive/Negative Data Input Bit 6.
L11, M11	P1_D7P, P1_D7N	Data Port 1 Positive/Negative Data Input Bit 7.
L12,M12	P1_D8P, P1_D8N	Data Port 1 Positive/Negative Data Input Bit 8.
L13, M13	P1_D9P, P1_D9N	Data Port 1 Positive/Negative Data Input Bit 9.
L14, M14	P1_D10P, P1_D10N	Data Port 1 Positive/Negative Data Input Bit 10.
N1, P1	NC, NC	No Connect. Do not connect to this pin.
N2, P2	NC, NC	No Connect. Do not connect to this pin.
N3, P3	NC, NC	No Connect. Do not connect to this pin.
N4, P4	P0_D0P, P0_D0N	Data Port 0 Positive/Negative Data Input Bit 0.
N5, P5	P0_D1P, P0_D1N	Data Port 0 Positive/Negative Data Input Bit 1.
N6, P6	P0_D2P, P0_D2N	Data Port 0 Positive/Negative Data Input Bit 2.
N7, P7	P0_D3P, P0_D3N	Data Port 0 Positive/Negative Data Input Bit 3.
N8, P8	P0_D4P, P0_D4N	Data Port 0 Positive/Negative Data Input Bit 4.
N9, P9	P0_D5P, P0_D5N	Data Port 0 Positive/Negative Data Input Bit 5.
N10, P10	P0_D6P, P0_D6N	Data Port 0 Positive/Negative Data Input Bit 6.
N11, P11	P0_D7P, P0_D7N	Data Port 0 Positive/Negative Data Input Bit 7.
N12, P12	P0_D8P, P0_D8N	Data Port 0 Positive/Negative Data Input Bit 8.
N13, P13	P0_D9P, P0_D9N	Data Port 0 Positive/Negative Data Input Bit 9.
N14, P14	P0_D10P, P0_D10N	Data Port 0 Positive/Negative Data Input Bit 10.

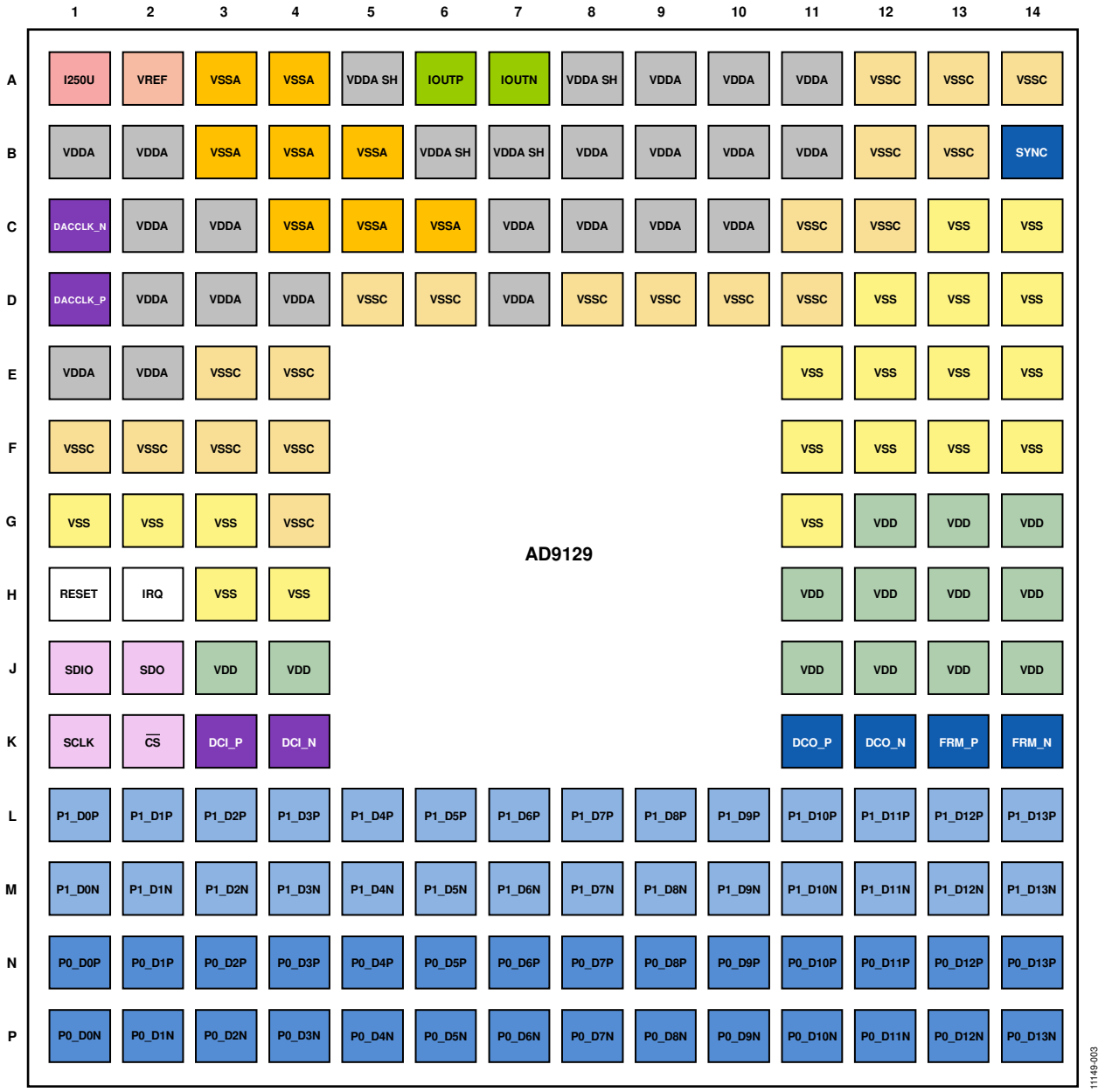


Figure 3. AD9129 Pin Configuration

Table 9. AD9129 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	I250U	Nominal 1.0 V Reference. Tie this pin to VSSA via a 4.0 kΩ resistor to generate a 250 µA reference current.
A2	VREF	Voltage Reference Input/Output. Decouple to VSSA with a 1 nF capacitor.
A3, A4, B3, B4, B5, C4, C5, C6	VSSA	−1.5 V Analog Supply Voltage Input.
A5, A8, B6, B7	VDDA SH	+1.8 V Analog Supply Shield. Tie these pins to VDDA at the DAC.
A9, A10, A11, B1, B2, B8, B9, B10, B11, C2, C3, C7, C8, C9, C10, D2, D3, D4, D7, E1, E2	VDDA	+1.8 V Analog Supply Voltage Input.
G12, G13, G14, H11, H12, H13, H14, J3, J4, J11, J12, J13, J14	VDD	+1.8 V Digital Supply Voltage Input.
C13, C14, D12, D13, D14, E11, E12, E13, E14, F11, F12, F13, F14, G1, G2, G3, G11, H3, H4	VSS	+1.8 V Digital Supply Return.

Pin No.	Mnemonic	Description
A12, A13, A14, B12, B13, C11, C12, D5, D6, D8, D9, D10, D11, E3, E4, F1, F2, F3, F4, G4	VSSC	Analog Supply Return.
A6	IOUTP	DAC Positive Current Output Source.
A7	IOUTN	DAC Negative Current Output Source.
B14	SYNC	Synchronization Signal Output.
C1, D1	DACCLK_N, DACCLK_P	Negative/Positive DAC Clock Input.
H1	RESET	Reset Input. Active high. If unused, tie this pin to VSS.
H2	IRQ	Interrupt Request Open-Drain Output. Active high. Pull up this pin to VDD with a 1 kΩ resistor.
J1	SDIO	Serial Port Data Input/Output.
J2	SDO	Serial Port Data Output.
K1	SCLK	Serial Port Clock Input.
K2	$\overline{CS}$	Serial Port Enable Input.
K3, K4	DCI_P, DCI_N	Positive, Negative Data Clock Input (DCI).
K11, K12	DCO_P, DCO_N	Positive, Negative Data Clock Output (DCO).
K13, K14	FRM_P, FRM_N	Positive, Negative Data Frame/Parity Signal (FRAME/PARITY).
L1, M1	P1_D0P, P1_D0N	Data Port 1 Positive/Negative Data Input Bit 0.
L2, M2	P1_D1P, P1_D1N	Data Port 1 Positive/Negative Data Input Bit 1.
L3, M3	P1_D2P, P1_D2N	Data Port 1 Positive/Negative Data Input Bit 2.
L4, M4	P1_D3P, P1_D3N	Data Port 1 Positive/Negative Data Input Bit 3.
L5, M5	P1_D4P, P1_D4N	Data Port 1 Positive/Negative Data Input Bit 4.
L6, M6	P1_D5P, P1_D5N	Data Port 1 Positive/Negative Data Input Bit 5.
L7, M7	P1_D6P, P1_D6N	Data Port 1 Positive/Negative Data Input Bit 6.
L8, M8	P1_D7P, P1_D7N	Data Port 1 Positive/Negative Data Input Bit 7.
L9, M9	P1_D8P, P1_D8N	Data Port 1 Positive/Negative Data Input Bit 8.
L10, M10	P1_D9P, P1_D9N	Data Port 1 Positive/Negative Data Input Bit 9.
L11, M11	P1_D10P, P1_D10N	Data Port 1 Positive/Negative Data Input Bit 10.
L12,M12	P1_D11P, P1_D11N	Data Port 1 Positive/Negative Data Input Bit 11.
L13, M13	P1_D12P, P1_D12N	Data Port 1 Positive/Negative Data Input Bit 12.
L14, M14	P1_D13P, P1_D13N	Data Port 1 Positive/Negative Data Input Bit 13.
N1, P1	P0_D0P, P0_D0N	Data Port 0 Positive/Negative Data Input Bit 0.
N2, P2	P0_D1P, P0_D1N	Data Port 0 Positive/Negative Data Input Bit 1.
N3, P3	P0_D2P, P0_D2N	Data Port 0 Positive/Negative Data Input Bit 2.
N4, P4	P0_D3P, P0_D3N	Data Port 0 Positive/Negative Data Input Bit 3.
N5, P5	P0_D4P, P0_D4N	Data Port 0 Positive/Negative Data Input Bit 4.
N6, P6	P0_D5P, P0_D5N	Data Port 0 Positive/Negative Data Input Bit 5.
N7, P7	P0_D6P, P0_D6N	Data Port 0 Positive/Negative Data Input Bit 6.
N8, P8	P0_D7P, P0_D7N	Data Port 0 Positive/Negative Data Input Bit 7.
N9, P9	P0_D8P, P0_D8N	Data Port 0 Positive/Negative Data Input Bit 8.
N10, P10	P0_D9P, P0_D9N	Data Port 0 Positive/Negative Data Input Bit 9.
N11, P11	P0_D10P, P0_D10N	Data Port 0 Positive/Negative Data Input Bit 10.
N12, P12	P0_D11P, P0_D11N	Data Port 0 Positive/Negative Data Input Bit 11.
N13, P13	P0_D12P, P0_D12N	Data Port 0 Positive/Negative Data Input Bit 12.
N14, P14	P0_D13P, P0_D13N	Data Port 0 Positive/Negative Data Input Bit 13.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9119

Static Linearity

I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

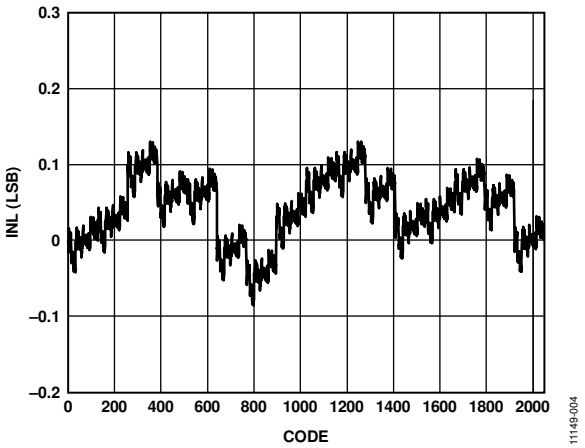


Figure 4. Typical INL, 11 mA at 25°C

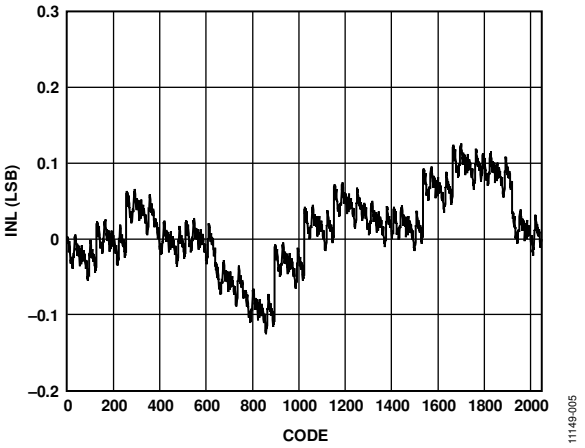


Figure 5. Typical INL, 22 mA at 25°C

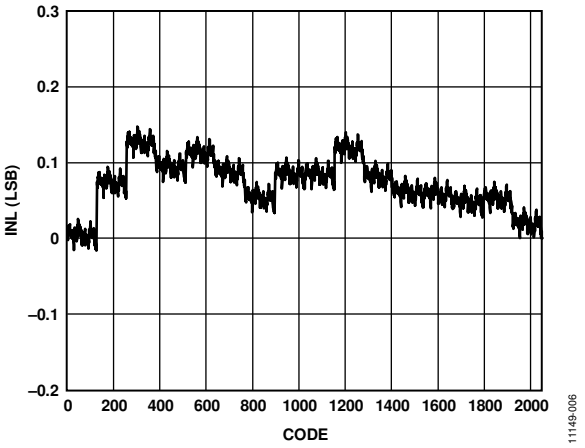


Figure 6. Typical INL, 33 mA at 25°C

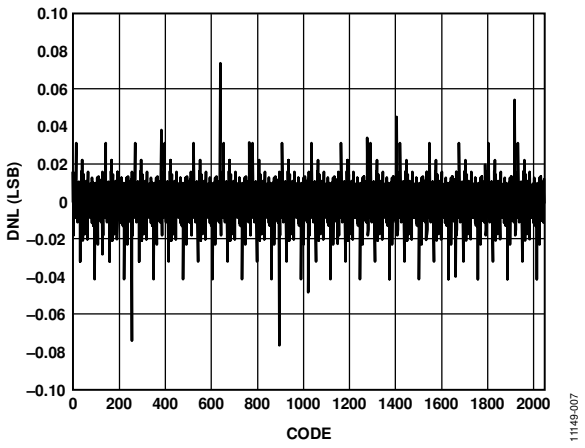


Figure 7. Typical DNL, 11 mA at 25°C

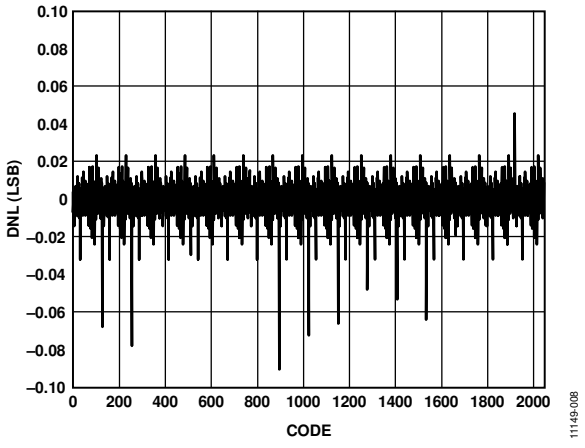


Figure 8. Typical DNL, 22 mA at 25°C

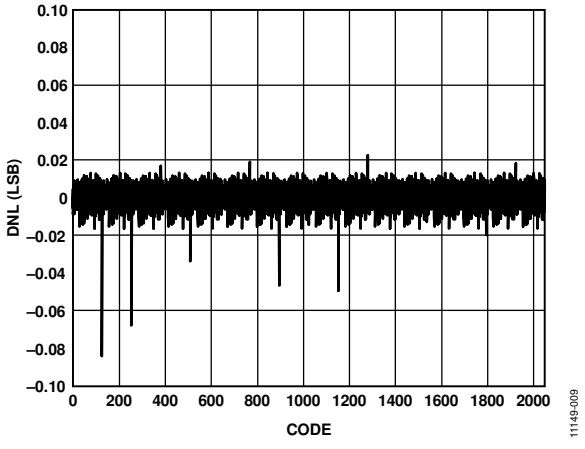


Figure 9. Typical DNL, 33 mA at 25°C

AC (Normal Mode)

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

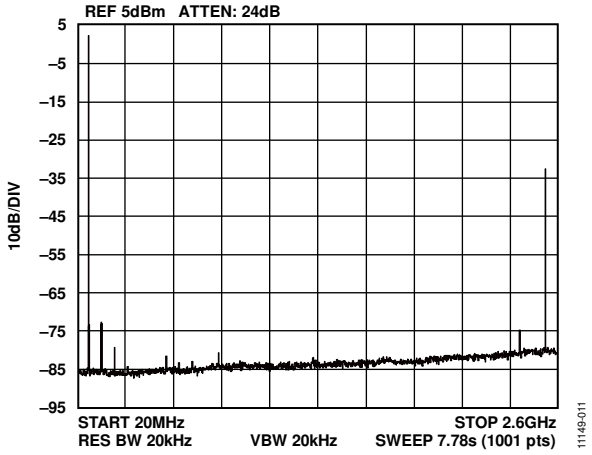


Figure 10. Single-Tone Spectrum at f_{OUT} = 70 MHz

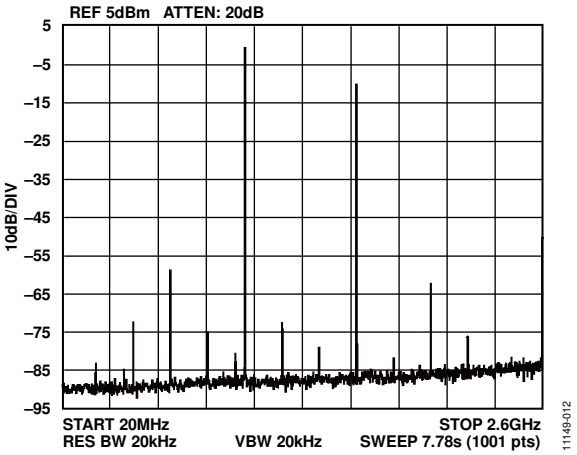


Figure 13. Single-Tone Spectrum at f_{OUT} = 1000 MHz

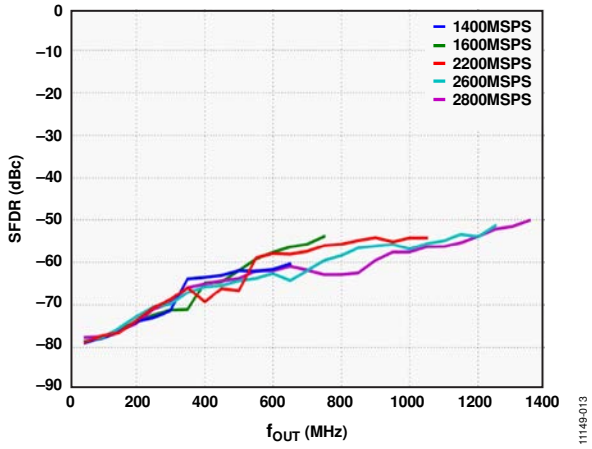


Figure 11. SFDR vs. f_{OUT} over f_{DAC}

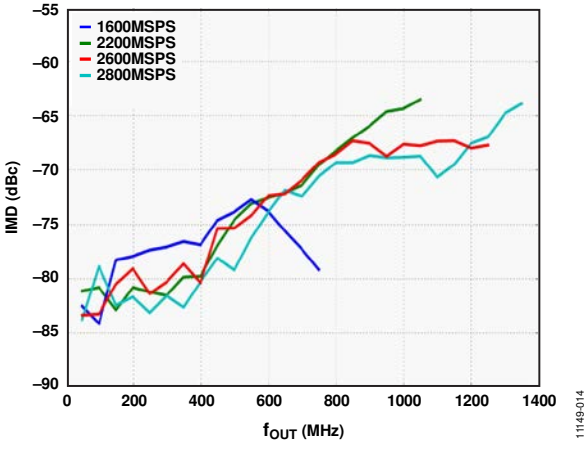


Figure 14. IMD vs. f_{OUT} over f_{DAC}

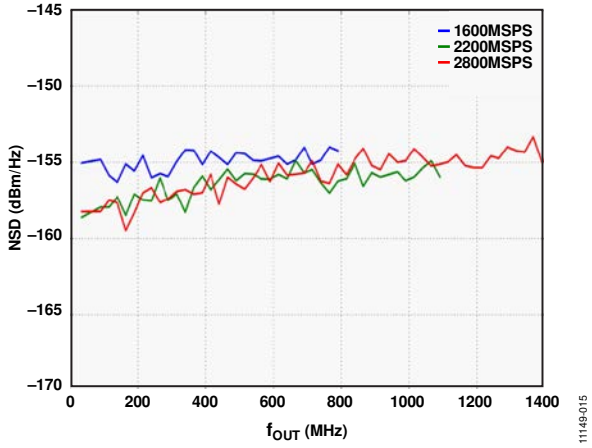


Figure 12. Single-Tone NSD vs. f_{OUT}

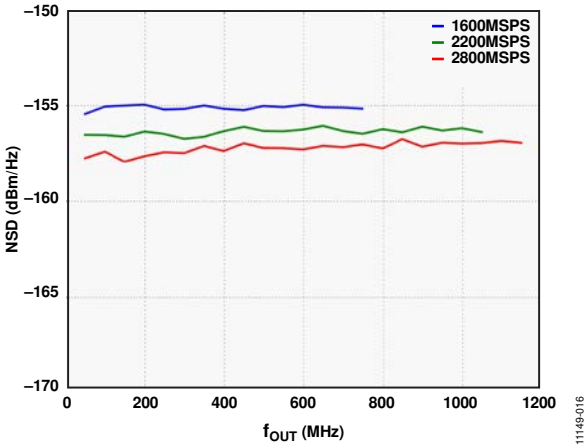


Figure 15. W-CDMA NSD vs. f_{OUT}

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

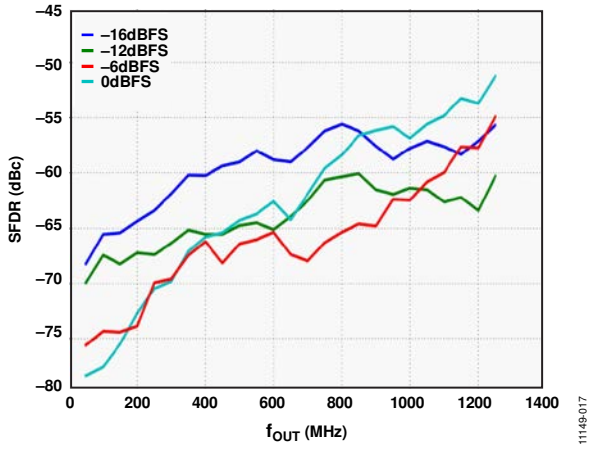


Figure 16. SFDR vs. f_{OUT} over Digital Full Scale

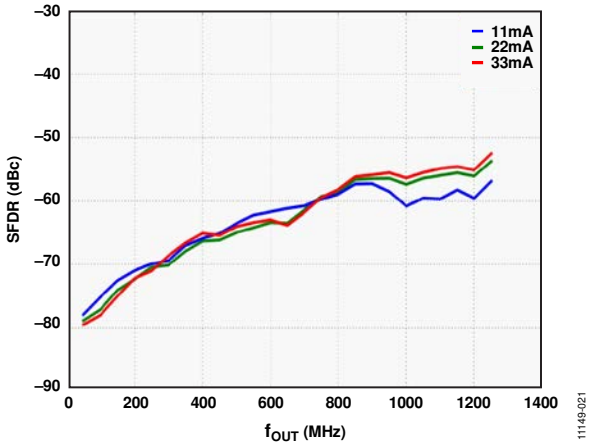


Figure 18. SFDR vs. f_{OUT} over DAC I_{OUTFS}

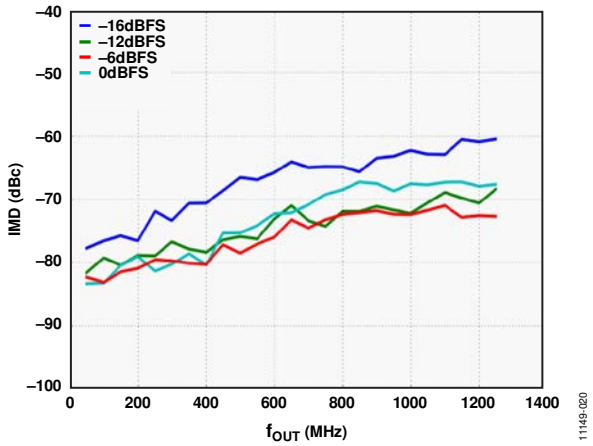


Figure 17. IMD vs. f_{OUT} over Digital Full Scale

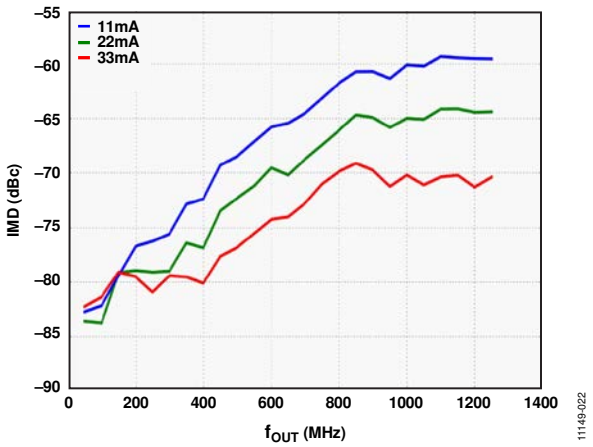


Figure 19. IMD vs. f_{OUT} over DAC I_{OUTFS}

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

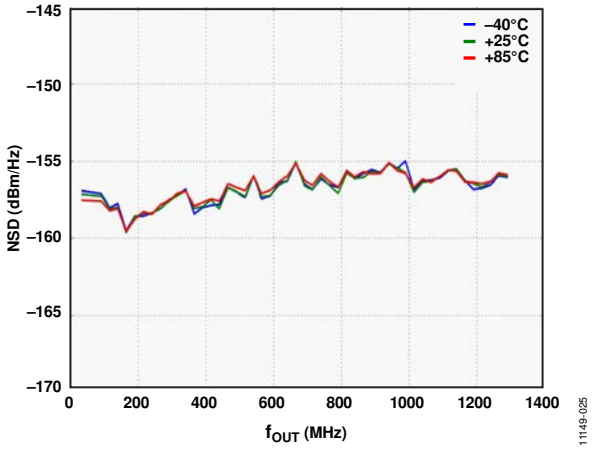


Figure 20. Single-Tone NSD vs. f_{OUT} over Temperature

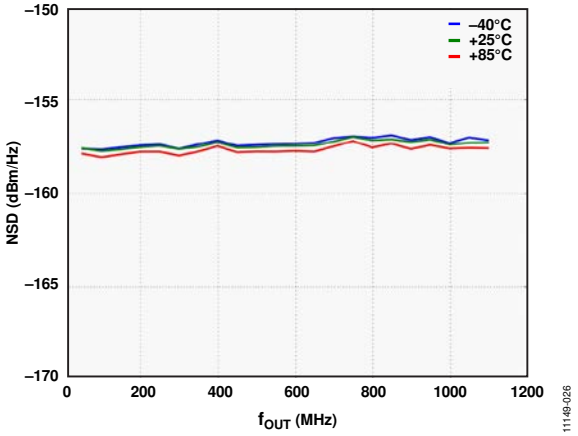
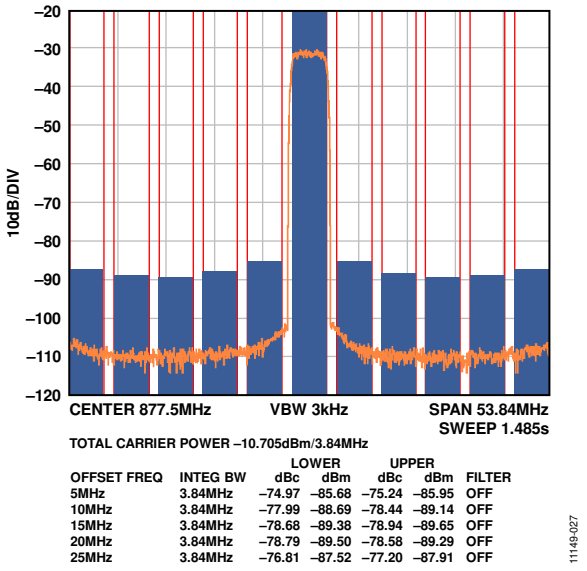
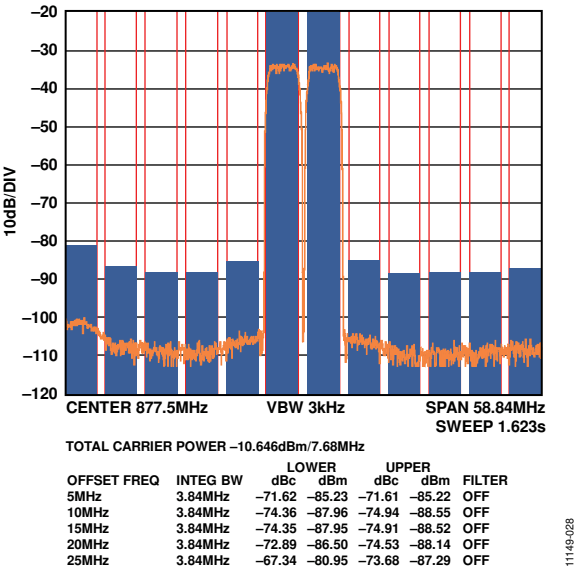


Figure 22. W-CDMA NSD vs. f_{OUT} over Temperature



		LOWER		UPPER		
OFFSET FREQ	INTEG BW	dBc	dBm	dBc	dBm	FILTER
5MHz	3.84MHz	–74.97	–85.68	–75.24	–85.95	OFF
10MHz	3.84MHz	–77.99	–88.69	–78.44	–89.14	OFF
15MHz	3.84MHz	–78.68	–89.38	–78.94	–89.65	OFF
20MHz	3.84MHz	–78.79	–89.50	–78.58	–89.29	OFF
25MHz	3.84MHz	–76.81	–87.52	–77.20	–87.91	OFF

Figure 21. Single-Carrier W-CDMA at 877.5 MHz



		LOWER		UPPER		
OFFSET FREQ	INTEG BW	dBc	dBm	dBc	dBm	FILTER
5MHz	3.84MHz	–71.62	–85.23	–71.61	–85.22	OFF
10MHz	3.84MHz	–74.36	–87.96	–74.94	–88.55	OFF
15MHz	3.84MHz	–74.35	–87.95	–74.91	–88.52	OFF
20MHz	3.84MHz	–72.89	–86.50	–74.53	–88.14	OFF
25MHz	3.84MHz	–67.34	–80.95	–73.68	–87.29	OFF

Figure 23. Two-Carrier W-CDMA at 877.5 MHz

AC (Mix-Mode)

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

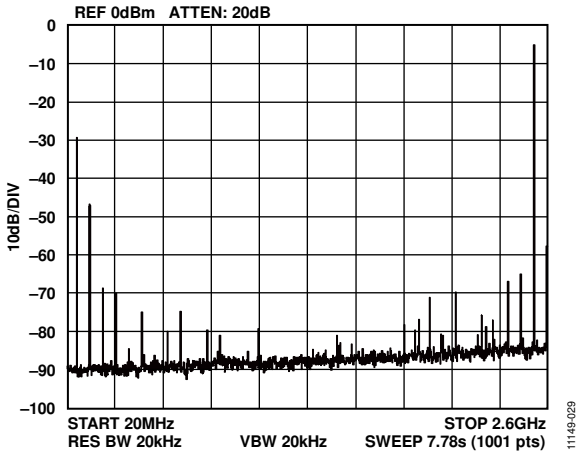


Figure 24. Single Tone Spectrum at f_{OUT} = 2350 MHz

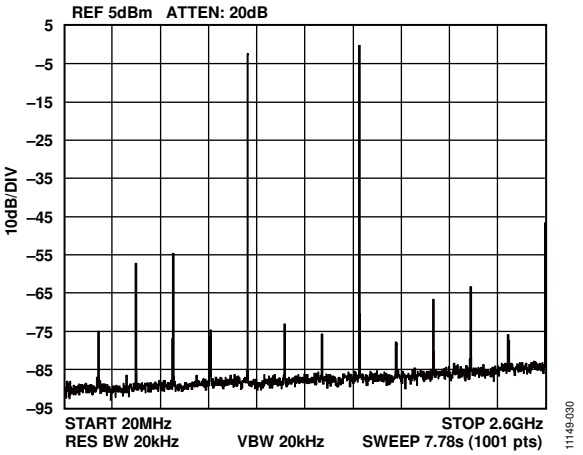


Figure 27. Single-Tone Spectrum at f_{OUT} = 1600 MHz

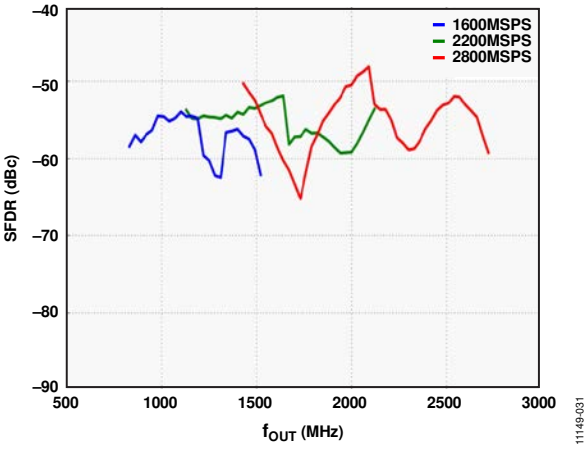


Figure 25. SFDR vs. f_{OUT} over f_{DAC}

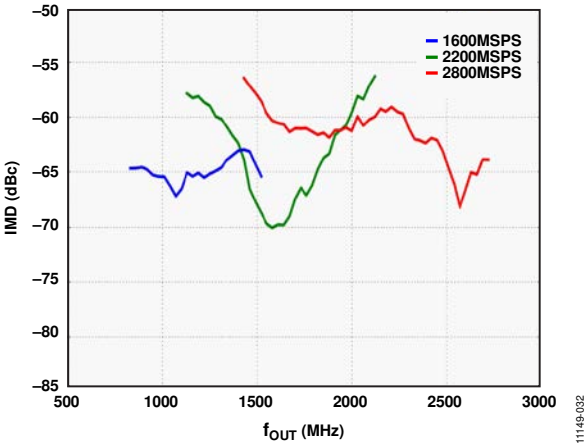


Figure 28. IMD vs. f_{OUT} over f_{DAC}

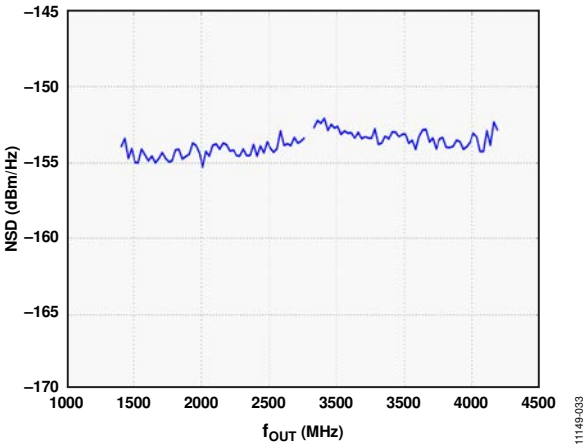


Figure 26. Single-Tone NSD vs. f_{OUT}

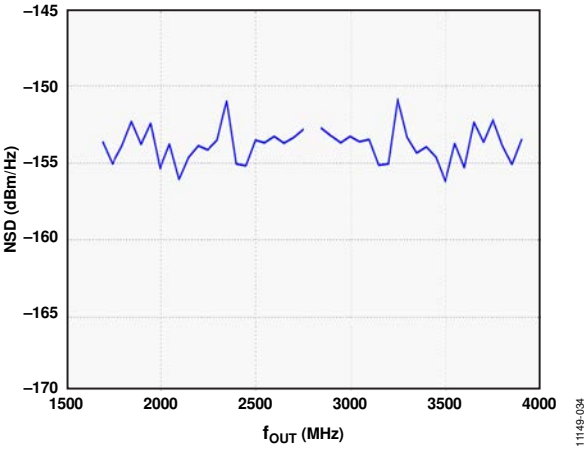


Figure 29. W-CDMA NSD vs. f_{OUT}

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

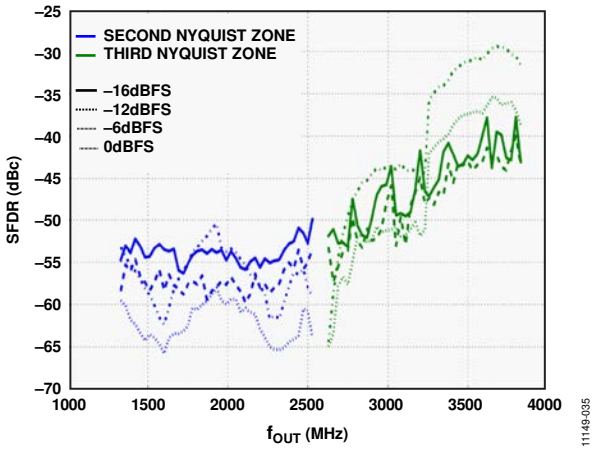


Figure 30. SFDR vs. f_{OUT} over Digital Full Scale

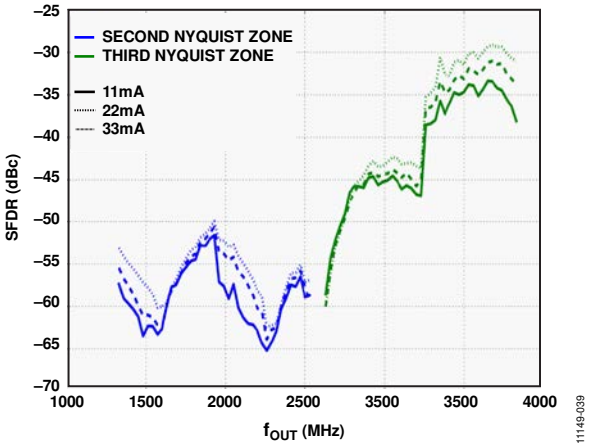


Figure 32. SFDR vs. f_{OUT} over DAC I_{OUTFS}

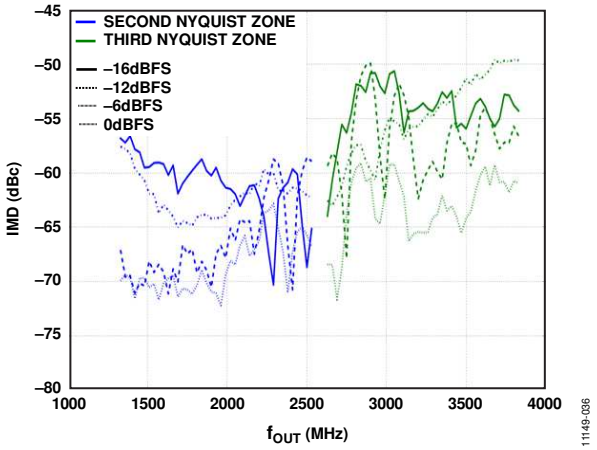


Figure 31. IMD vs. f_{OUT} over Digital Full Scale

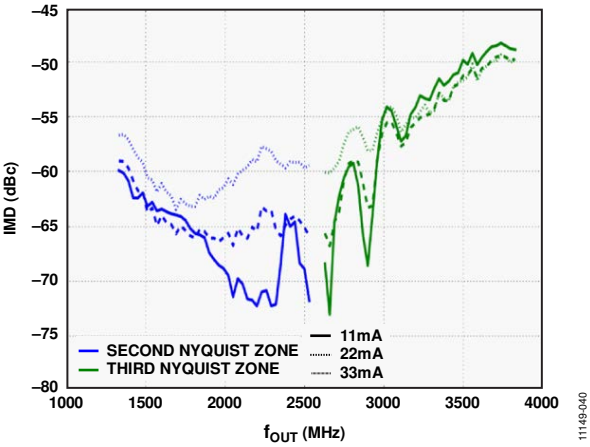


Figure 33. IMD vs. f_{OUT} over DAC I_{OUTFS}

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

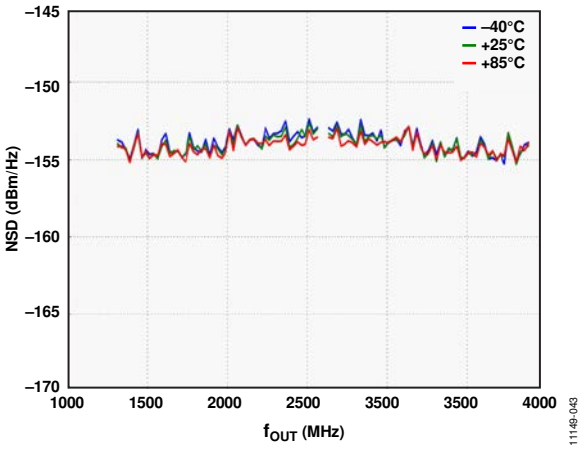


Figure 34. Single-Tone NSD vs. f_{OUT} over Temperature

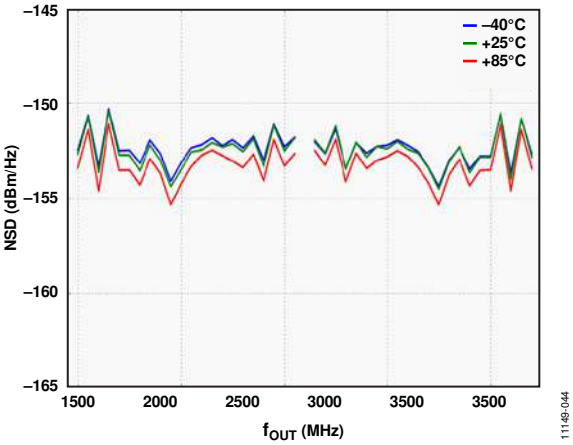


Figure 36. W-CDMA NSD vs. f_{OUT} over Temperature

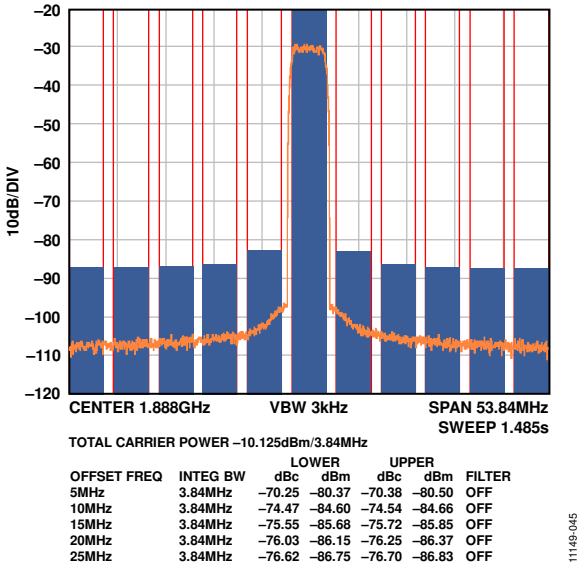


Figure 35. Single-Carrier W-CDMA at 1887.5 MHz

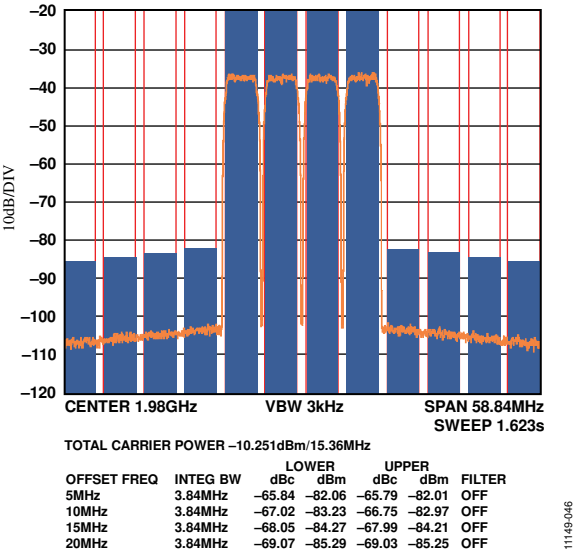


Figure 37. Four-Carrier W-CDMA at 1980 MHz

DOCSIS Performance (Normal Mode)

I_{OUTFS} = 33 mA, f_{DAC} = 2.782 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

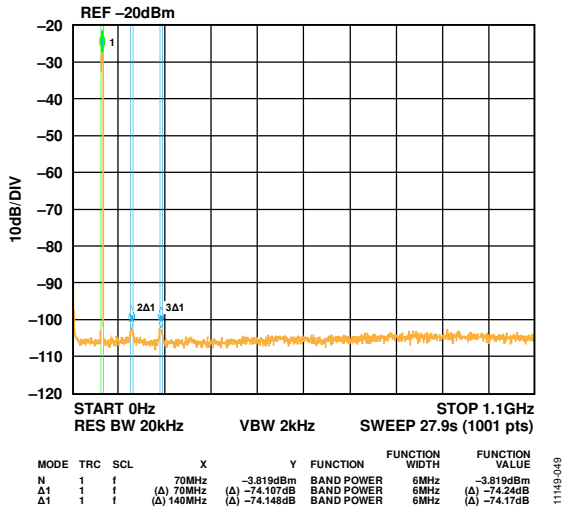


Figure 38. Single Carrier at 70 MHz Output

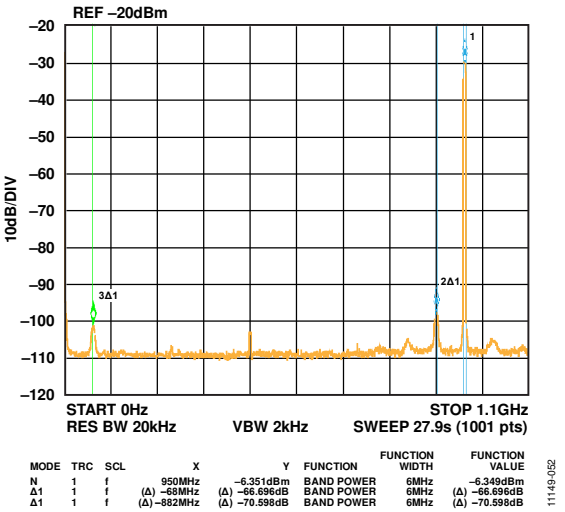


Figure 41. Single Carrier at 950 MHz Output

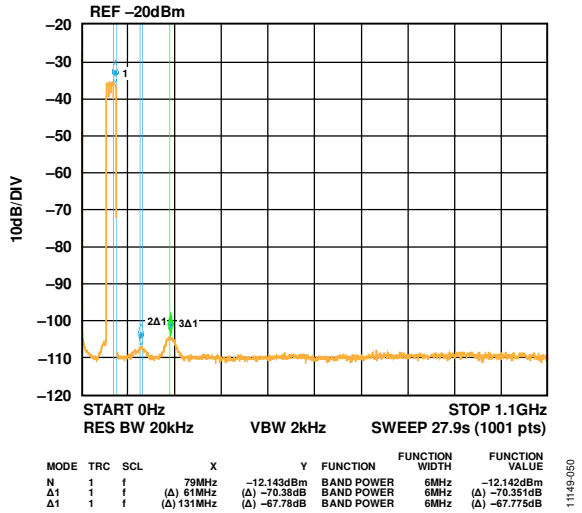


Figure 39. Four Carrier at 70 MHz Output

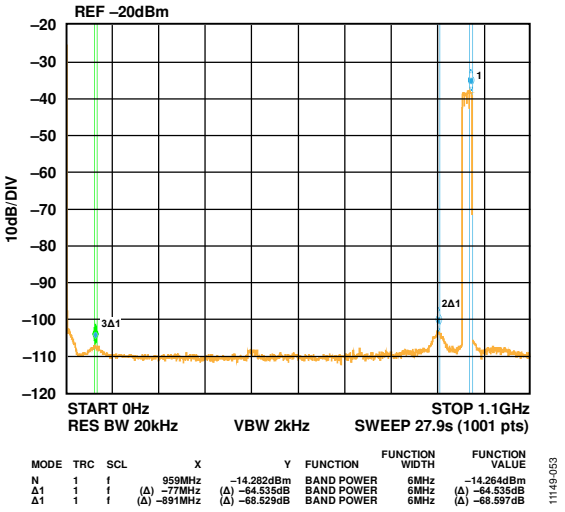


Figure 42. Four Carrier at 950 MHz Output

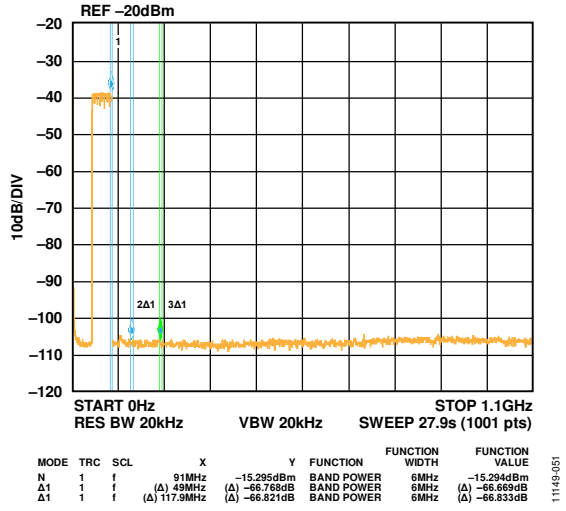


Figure 40. Eight Carrier at 70 MHz Output

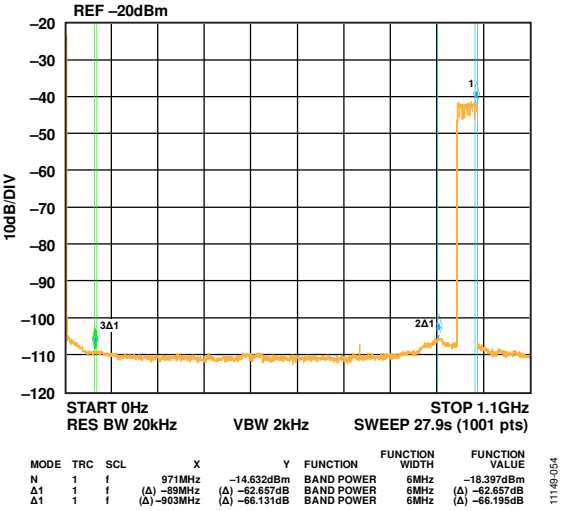


Figure 43. Eight Carrier at 950 MHz Output

I_{OUTFS} = 33 mA, f_{DAC} = 2.782 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

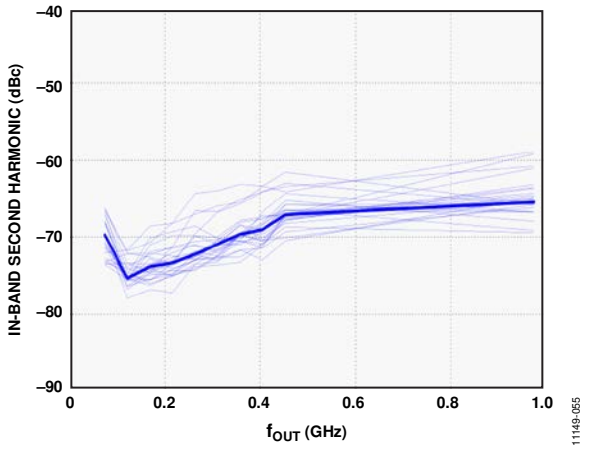


Figure 44. Second Harmonic vs. f_{OUT} Performance for One DOCSIS Carrier

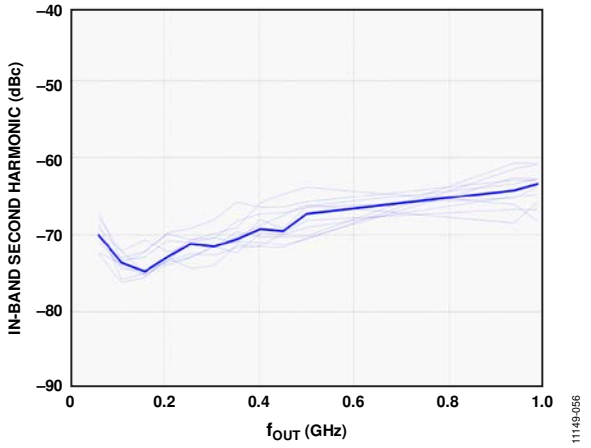


Figure 45. Second Harmonic vs. f_{OUT} Performance for Four DOCSIS Carriers

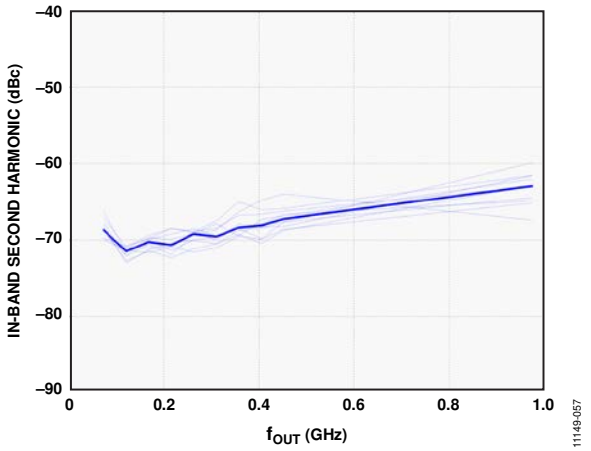


Figure 46. Second Harmonic vs. f_{OUT} Performance for Eight DOCSIS Carriers

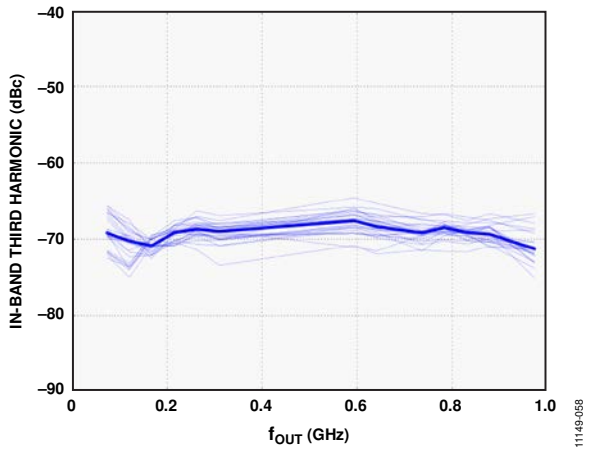


Figure 47. Third Harmonic vs. f_{OUT} Performance for One DOCSIS Carrier

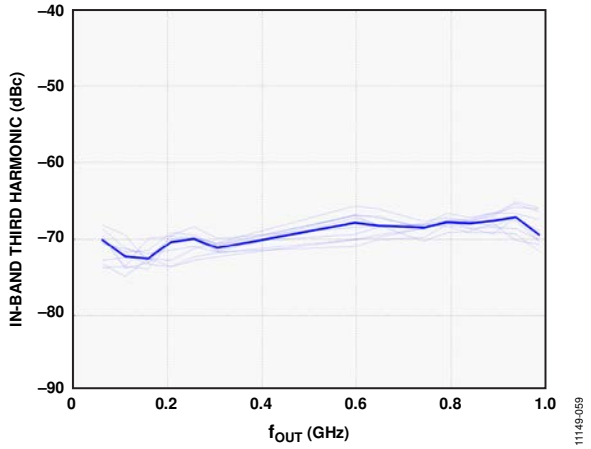


Figure 48. Third Harmonic vs. f_{OUT} Performance for Four DOCSIS Carriers

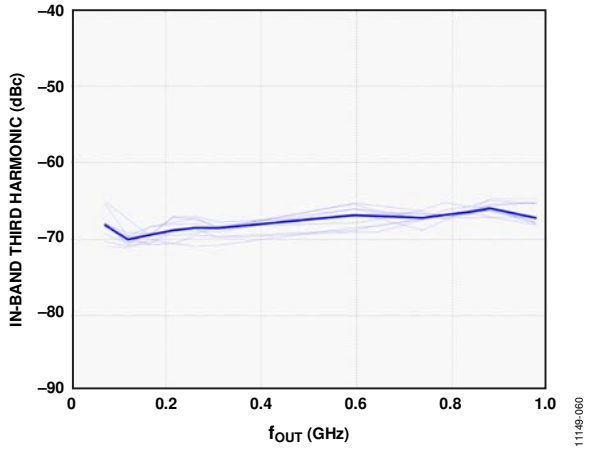


Figure 49. Third Harmonic vs. f_{OUT} Performance for Eight DOCSIS Carriers

I_{OUTFS} = 33 mA, f_{DAC} = 2.782 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

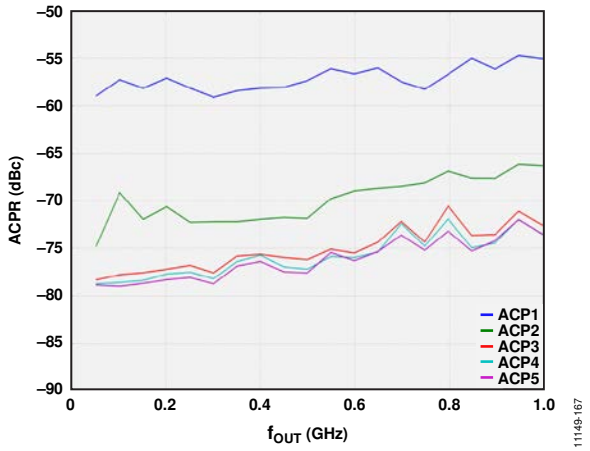


Figure 50. Single-Carrier ACPR vs. f_{OUT}

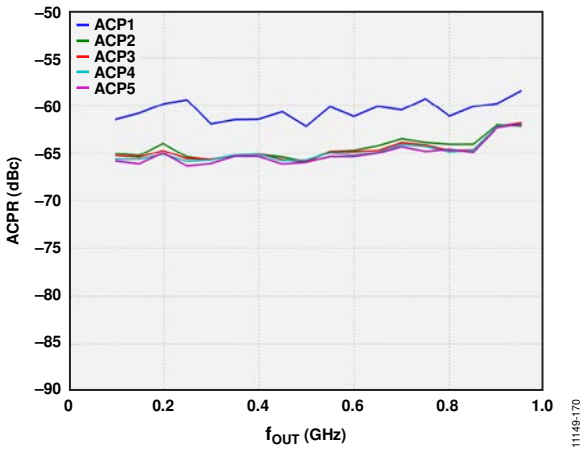


Figure 53. 16-Carrier ACPR vs. f_{OUT}

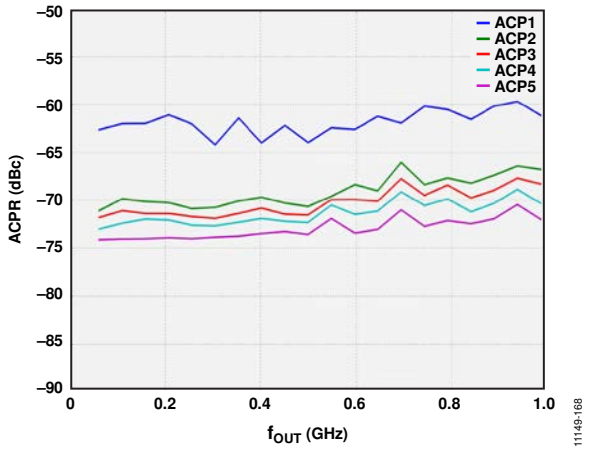


Figure 51. Four-Carrier ACPR vs. f_{OUT}

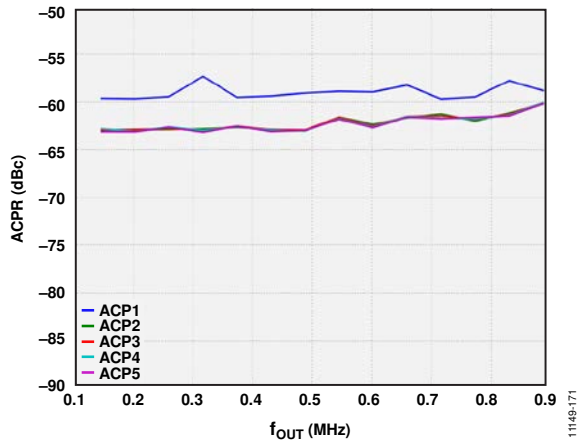


Figure 54. 32-Carrier ACPR vs. f_{OUT}

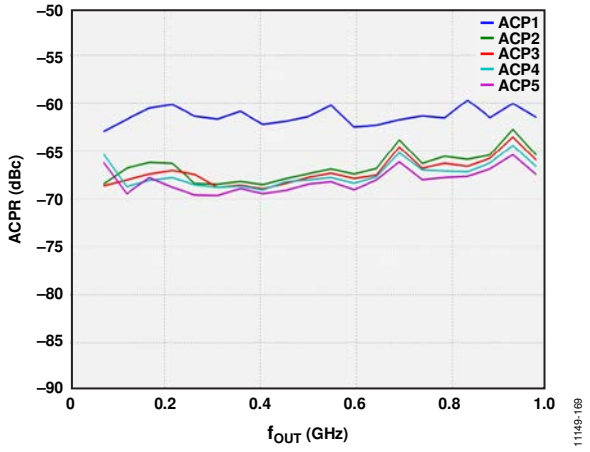


Figure 52. Eight-Carrier ACPR vs. f_{OUT}

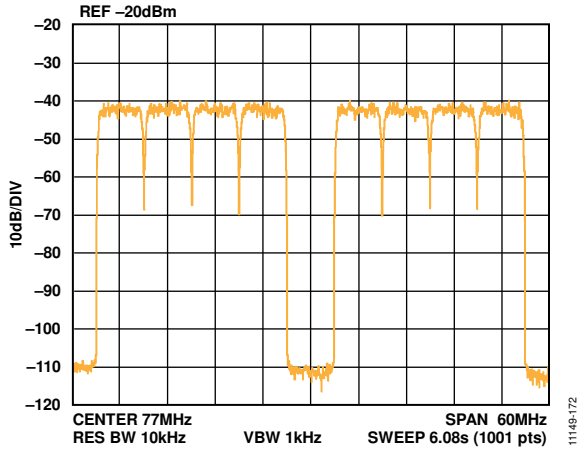


Figure 55. Gap Channel ACPR at 77 MHz

AD9129

Static Linearity

I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

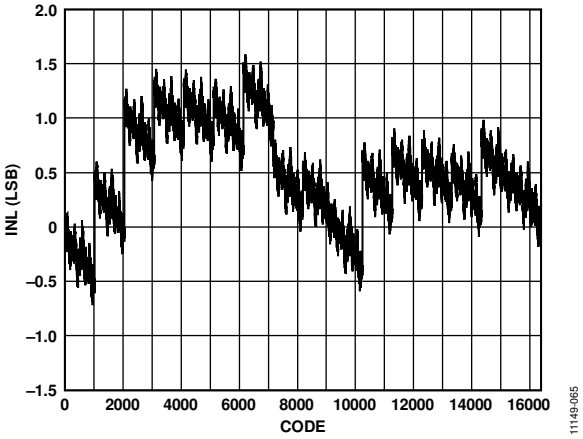


Figure 56. Typical INL, 11 mA at 25°C

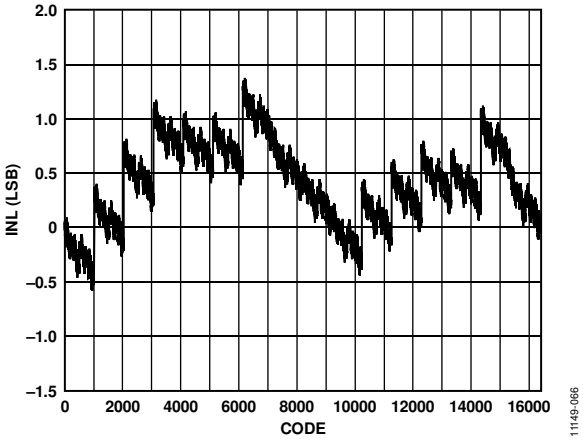


Figure 57. Typical INL, 22 mA at 25°C

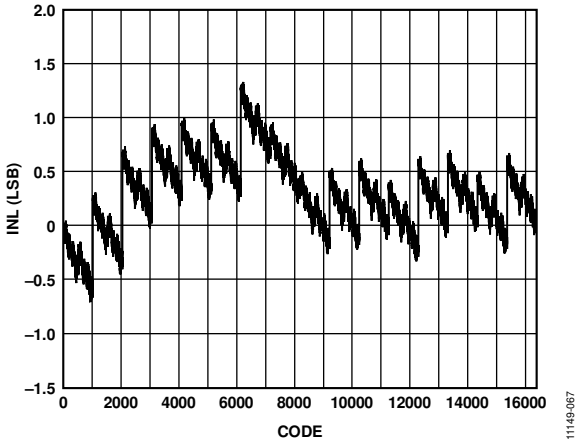


Figure 58. Typical INL, 33 mA at 25°C

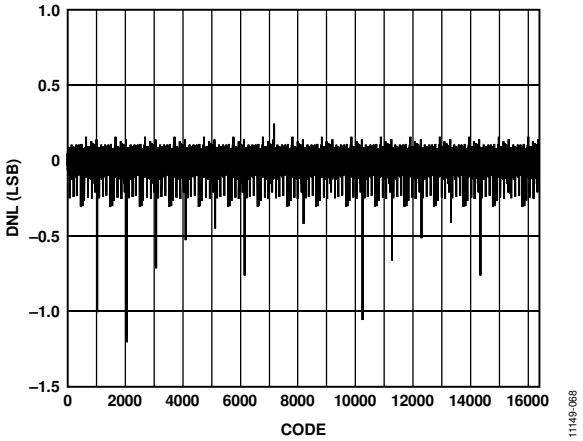


Figure 59. Typical DNL, 11 mA at 25°C

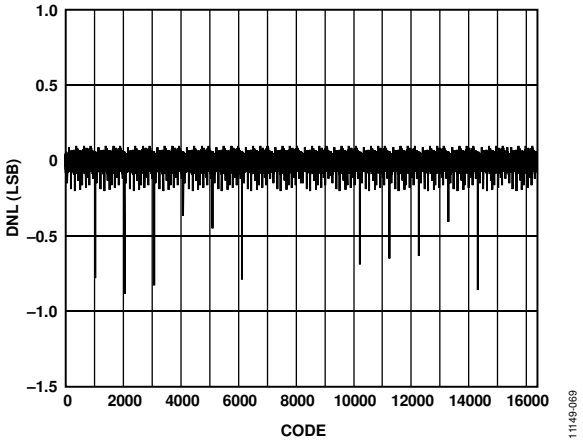


Figure 60. Typical DNL, 22 mA at 25°C

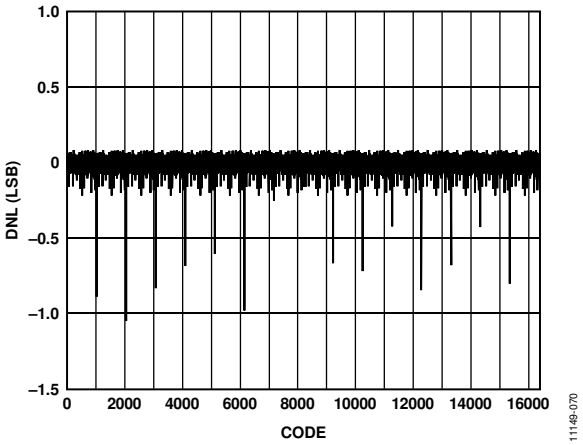


Figure 61. Typical DNL, 33 mA at 25°C

AC (Normal Mode)

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

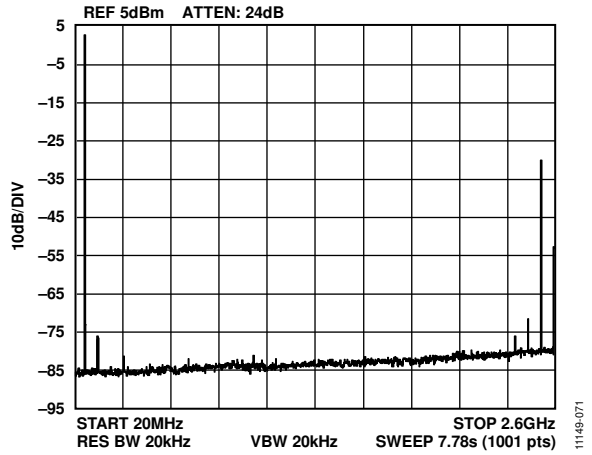


Figure 62. Single-Tone Spectrum at f_{OUT} = 70 MHz

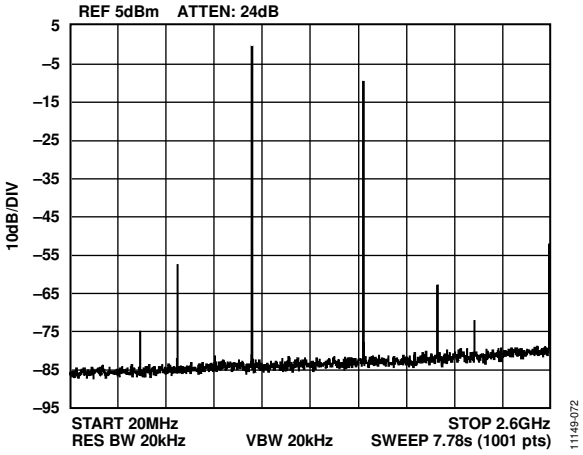


Figure 65. Single-Tone Spectrum at f_{OUT} = 1000 MHz

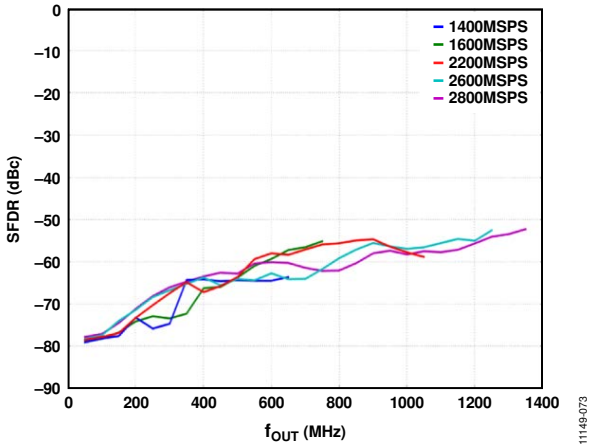


Figure 63. SFDR vs. f_{OUT} over f_{DAC}

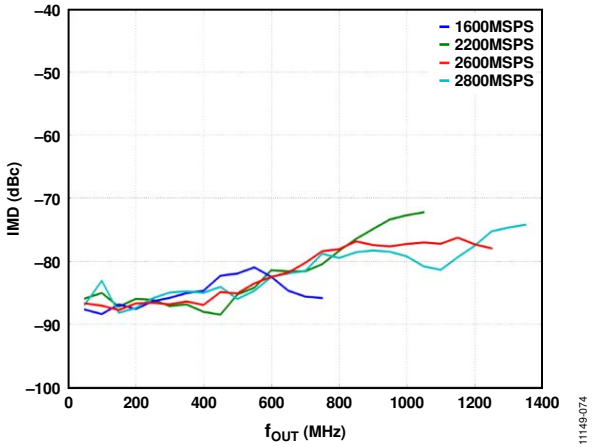


Figure 66. IMD vs. f_{OUT} over f_{DAC}

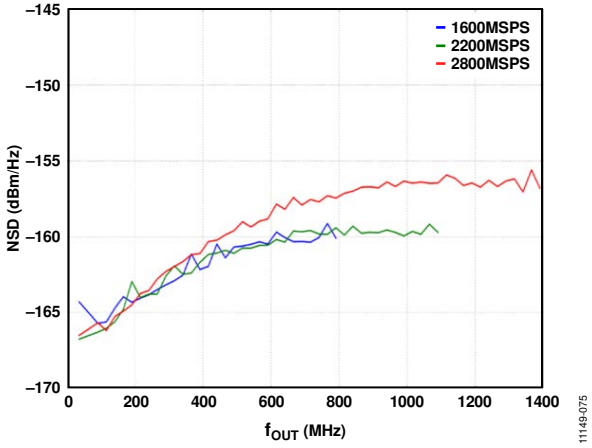


Figure 64. Single-Tone NSD vs. f_{OUT}

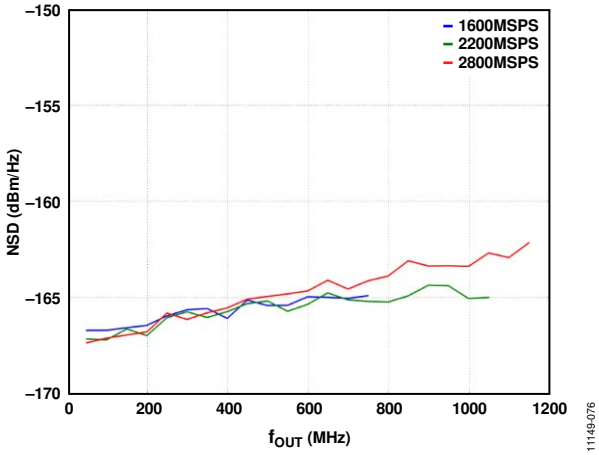


Figure 67. W-CDMA NSD vs. f_{OUT}

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

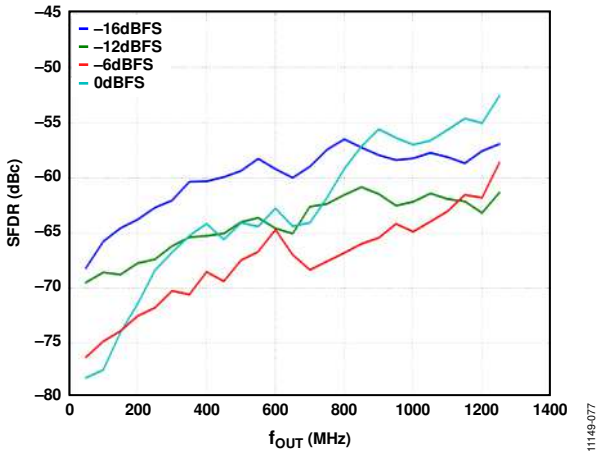


Figure 68. SFDR vs. f_{OUT} over Digital Full Scale

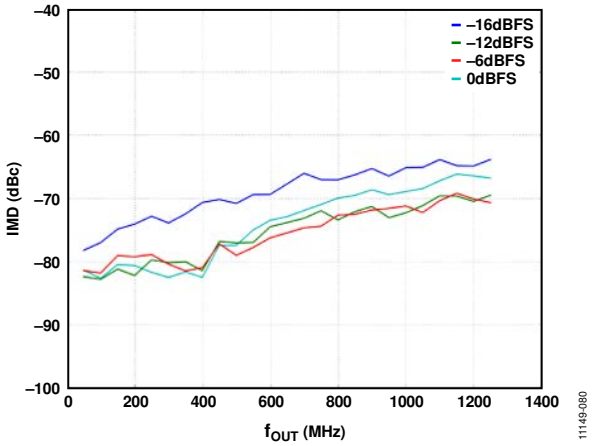


Figure 71. IMD vs. f_{OUT} over Digital Full Scale

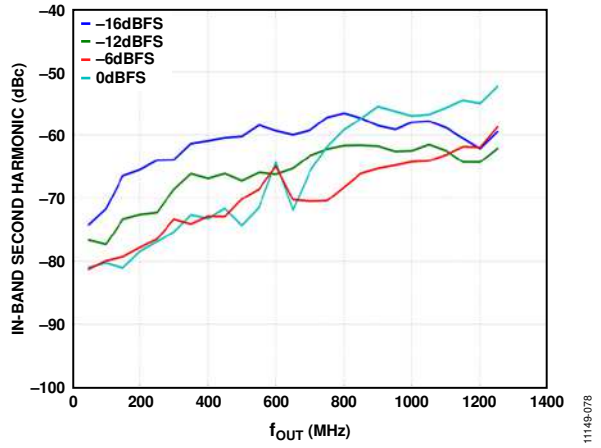


Figure 69. SFDR for Second Harmonic vs. f_{OUT} over Digital Full Scale

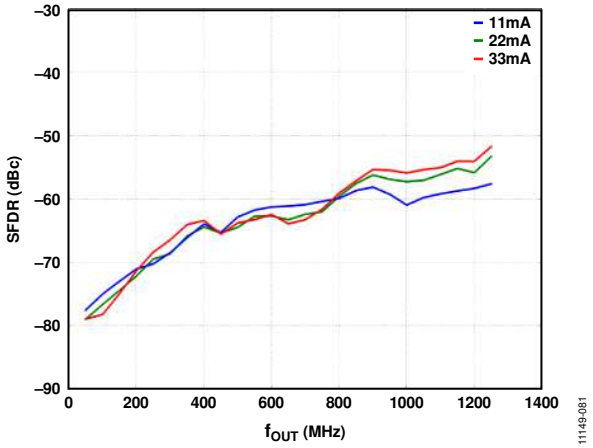


Figure 72. SFDR vs. f_{OUT} over DAC I_{OUTFS}

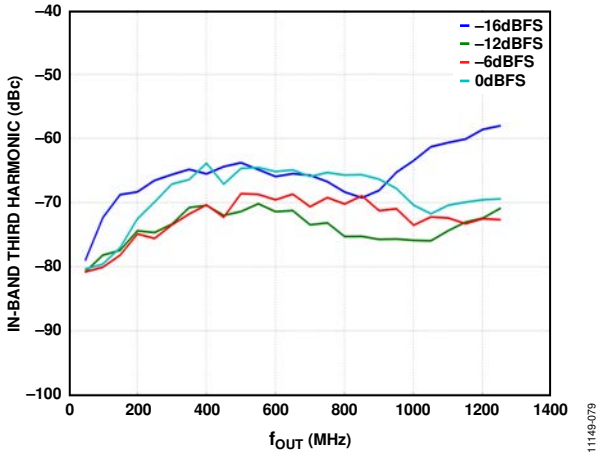


Figure 70. SFDR for Third Harmonic vs. f_{OUT} over Digital Full Scale

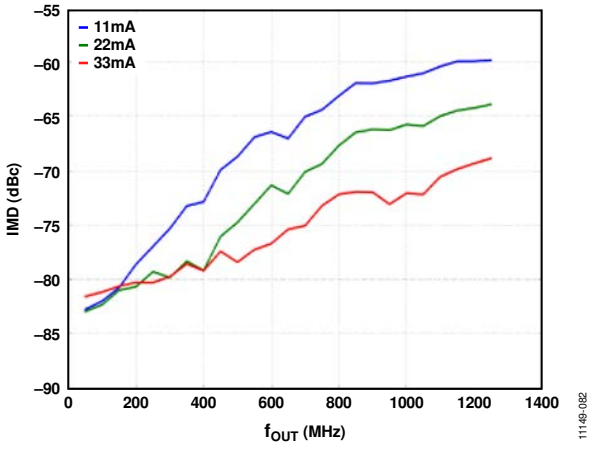


Figure 73. IMD vs. f_{OUT} over DAC I_{OUTFS}

I_{OUTFS} = 28 mA, f_{DAC} = 2.6 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

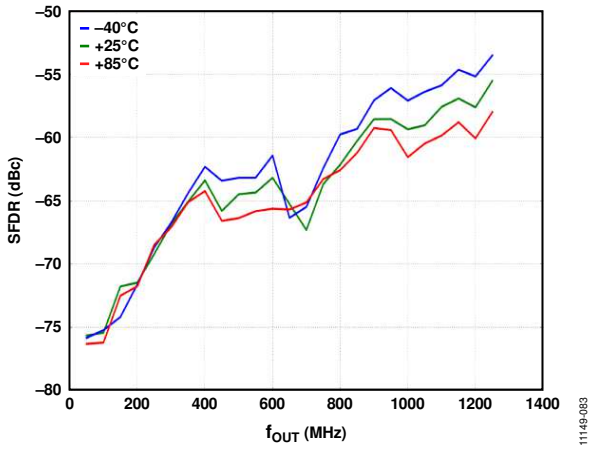


Figure 74. SFDR vs. f_{OUT} over Temperature

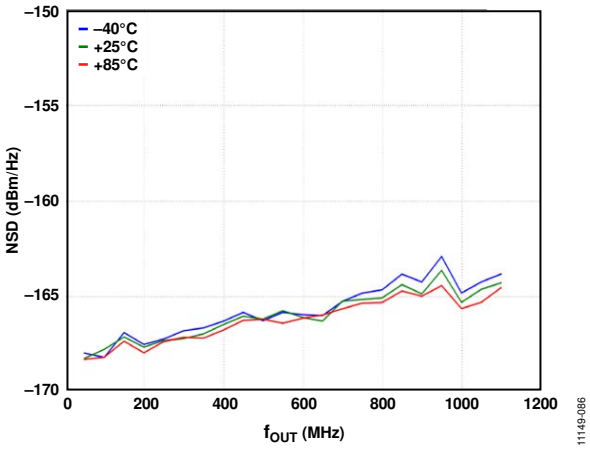


Figure 77. W-CDMA NSD vs. f_{OUT} over Temperature

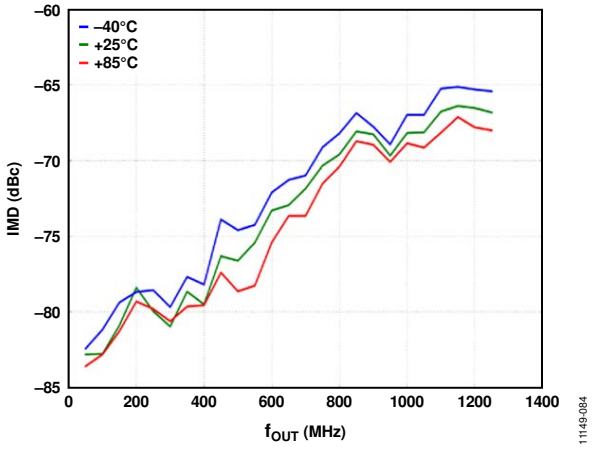


Figure 75. IMD vs. f_{OUT} over Temperature

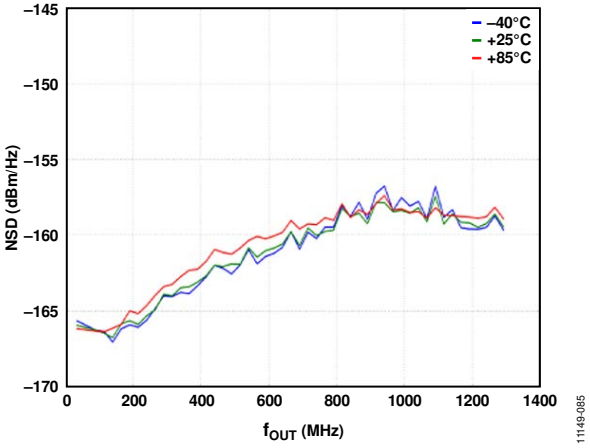


Figure 78. Single-Tone NSD vs. f_{OUT} over Temperature

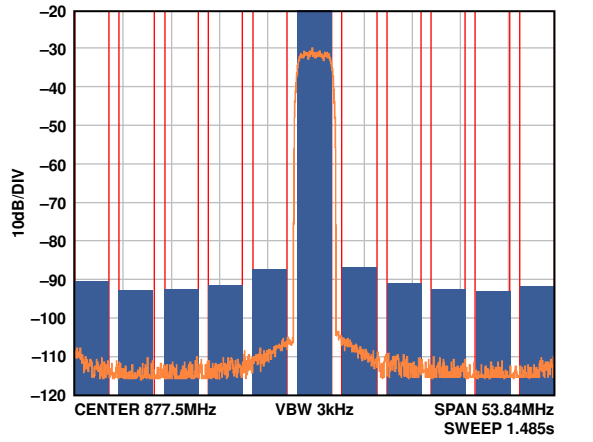


Figure 76. Single-Carrier W-CDMA at 877.5 MHz

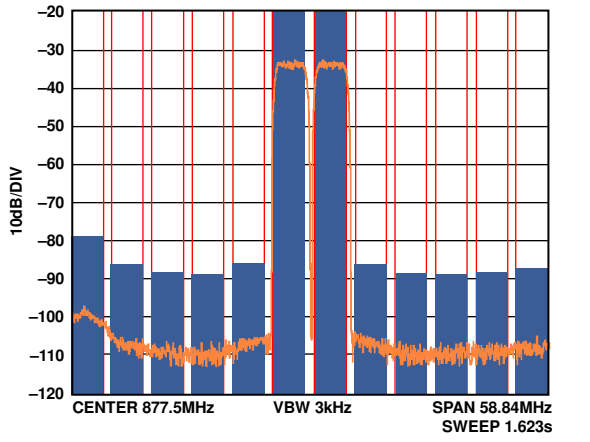


Figure 79. Two-Carrier W-CDMA at 875 MHz