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Dual, 11-/16-Bit, 2.8 GSPS, TxDAC+® Digital-to-Analog Converters

Data Sheet **AD9135/AD9136**

FEATURES

- Support input data rate >2 GSPS
- Proprietary low spurious and distortion design
  - SFDR = 82 dBc at dc IF, −9 dBFS
  - Flexible 8-lane JESD204B interface
- Multiple chip synchronization
  - Fixed latency
  - Data generator latency compensation
- Selectable 1×, 2×, 4×, or 8× interpolation filter
  - Low power architecture
- Transmit enable function allows extra power saving and instant control of the output status
- High performance, low noise phase-locked loop (PLL) clock multiplier
- Digital inverse sinc filter
- Low power: 1.42 W at 1.6 GSPS full operating conditions
- 88-lead LFCSP with exposed pad

APPLICATIONS

- Wireless communications
  - 3G/4G W-CDMA base stations
  - Wideband repeaters
  - Software defined radios
- Wideband communications
  - Point to point
  - Local multipoint distribution service (LMDS) and multichannel multipoint distribution service (MMDS)
- Transmit diversity, multiple input/multiple output (MIMO)
- Instrumentation
- Automated test equipment

TYPICAL APPLICATION CIRCUIT

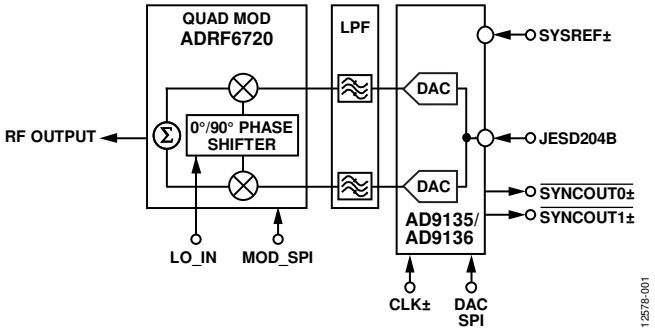

Figure 1.

GENERAL DESCRIPTION

The AD9135/AD9136 are dual, 11-/16-bit, high dynamic range digital-to-analog converters (DACs) that provide a maximum sample rate of 2800 MSPS, permitting a multicarrier generation over a very wide bandwidth. The DAC outputs are optimized to interface seamlessly with the ADRF6720, as well as other analog quadrature modulators (AQMs) from Analog Devices, Inc. An optional 3-wire or 4-wire serial port interface (SPI) provides for programming/readback of many internal parameters. The full-scale output current can be programmed over a typical range of 13.9 mA to 27.0 mA. The AD9135/AD9136 are available in an 88-lead LFCSP.

PRODUCT HIGHLIGHTS

1. Greater than 2 GHz, ultrawide complex signal bandwidth enables emerging wideband and multiband wireless applications.
2. Advanced low spurious and distortion design techniques provide high quality synthesis of wideband signals from baseband to high intermediate frequencies.
3. JESD204B Subclass 1 support simplifies multichip synchronization in software and hardware design.
4. Fewer pins for data interface width with a serializer/deserializer (SERDES) JESD204B eight-lane interface.
5. Programmable transmit enable function allows easy design balance between power consumption and wake-up time.
6. Small package size with 12 mm × 12 mm footprint.

Rev. B

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FUNCTIONAL BLOCK DIAGRAM

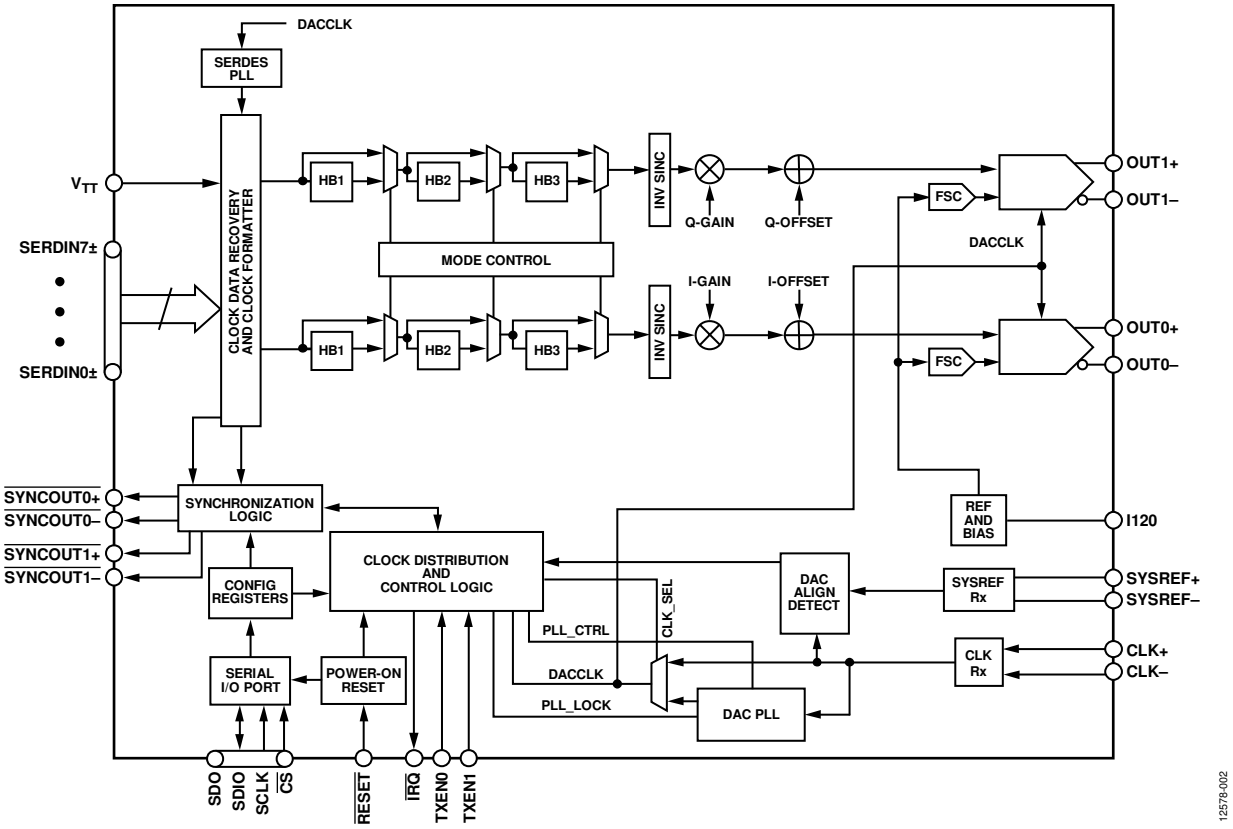


Figure 2.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 1.

		AD9135			AD9136			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION			11			16		Bits
ACCURACY	With calibration							
Differential Nonlinearity (DNL)			±0.175			±1.0		LSB
Integral Nonlinearity (INL)			±0.35			±2.0		LSB
MAIN DAC OUTPUTS								
Gain Error	With internal reference	−2.5	+2	+5.5	−2.5	+2	+5.5	% FSR
I/Q Gain Mismatch		−0.6		+0.6	−0.6		+0.6	% FSR
Full-Scale Output Current (I_{OUTFS})	Based on a 4 kΩ external resistor between I120 and GND							
Maximum Setting		25.5	27.0	28.6	25.5	27.0	28.6	mA
Minimum Setting		13.1	13.9	14.8	13.1	13.9	14.8	mA
Output Compliance Range		−250		+750	−250		+750	mV
Output Resistance			0.2			0.2		MΩ
Output Capacitance			3.0			3.0		pF
Gain DAC Monotonicity			Guaranteed			Guaranteed		
Settling Time	To within ±0.5 LSB		20			20		ns
MAIN DAC TEMPERATURE DRIFT								
Offset			0.04			0.04		ppm
Gain			32			32		ppm/°C
REFERENCE								
Internal Reference Voltage			1.2			1.2		V
ANALOG SUPPLY VOLTAGES								
AVDD33		3.13	3.3	3.47	3.13	3.3	3.47	V
PVDD12		1.14	1.2	1.26	1.14	1.2	1.26	V
CVDD12		1.14	1.2	1.26	1.14	1.2	1.26	V
DIGITAL SUPPLY VOLTAGES								
SIOVDD33		3.13	3.3	3.47	3.13	3.3	3.47	V
V_{TT}		1.1	1.2	1.37	1.1	1.2	1.37	V
DVDD12	1.2 V nominal supply voltage	1.14	1.2	1.26	1.14	1.2	1.26	V
	1.3 V nominal supply voltage	1.274	1.3	1.326	1.274	1.3	1.326	V
SVDD12	1.2 V nominal supply voltage	1.14	1.2	1.26	1.14	1.2	1.26	V
	1.3 V nominal supply voltage	1.274	1.3	1.326	1.274	1.3	1.326	V
IOVDD		1.71	1.8	3.47	1.71	1.8	3.47	V
POWER CONSUMPTION								
1× Interpolation Mode, JESD Mode 8, 8 SERDES Lanes	f_{DAC} = 1.6 GSPS, IF = 40 MHz, PLL on, digital gain on, inverse sinc on, DAC full-scale current (I_{OUTFS}) = 20 mA		1.42	1.74		1.42	1.74	W
AVDD33			68	73		68	73	mA
PVDD12			100	113.4		100	113.4	mA
CVDD12			101	112		101	112	mA
SVDD12	Includes V_{TT}		554	665		554	665	mA
DVDD12			196	224		196	224	mA
SIOVDD33			11	12		11	12	mA
IOVDD			36	50		36	50	µA

DIGITAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL						
Input Voltage (V_{IN}) Logic						
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.7 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.3 × IOVDD	V
CMOS OUTPUT LOGIC LEVEL						
Output Voltage (V_{OUT}) Logic						
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.75 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.25 × IOVDD	V
MAXIMUM DAC UPDATE RATE[1]						
		1× interpolation[2] (see Table 4)	2120			MSPS
		2× interpolation[2]	2120			MSPS
		4× interpolation[3]	2800			MSPS
		8× interpolation[3]	2800			MSPS
ADJUSTED DAC UPDATE RATE						
		1× interpolation	2120			MSPS
		2× interpolation	1060			MSPS
		4× interpolation	700			MSPS
		8× interpolation	350			MSPS
INTERFACE[4]						
Number of JESD204B Lanes				8		Lanes
JESD204B Serial Interface Speed						
Minimum		Per lane			1.44	Gbps
Maximum		Per lane, SVDD12 = 1.3 V ± 2%	12.4			Gbps
DAC CLOCK INPUT (CLK+, CLK−)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage		Self biased input, ac-coupled		600		mV
Maximum Clock Rate			2800			MHz
REFCLK[5] Frequency (PLL Mode)		6.0 GHz ≤ f_{VCO} ≤ 12.0 GHz	35		1000	MHz
SYSTEM REFERENCE INPUT (SYSREF+, SYSREF−)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage			0		2000	mV
SYSREF± Frequency[6]					$f_{DATA}/(K \times S)$	Hz
SYSREF SIGNAL TO DAC CLOCK[7]		SYSREF differential swing = 0.4 V, slew rate = 1.3 V/ns, common modes tested: ac-coupled, 0 V, 0.6 V, 1.25 V, 2.0 V				
Setup Time	t_{SSD}		131			ps
Hold Time	t_{HSD}		119			ps
Keep Out Window	KOW			20		ps
SPI						
Maximum Clock Rate	SCLK	IOVDD = 1.8 V	10			MHz
Minimum SCLK Pulse Width						
High	t_{PWH}				8	ns
Low	t_{PWL}				12	ns
SDIO to SCLK						
Setup Time	t_{DS}		5			ns
Hold Time	t_{DH}		2			ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SDO to SCLK						
Data Valid Window	t_{DV}		25			ns
$\overline{CS}$ to SCLK						
Setup Time	$t_{S\overline{CS}}$		5			ns
Hold Time	$t_{H\overline{CS}}$		2			ns

[1] See Table 3 for detailed specifications for DAC update rate conditions.
[2] The maximum speed for 1× and 2× interpolation is limited by the JESD204B interface with increased supply levels. See Table 4 for details.
[3] The maximum speed for 4× and 8× interpolation is limited by the DAC core. See Table 4 for details.
[4] See Table 4 for detailed specifications for JESD204B speed conditions.
[5] REFCLK is the reference clock.
[6] K, F, and S are JESD204B transport layer parameters. See Table 43 for the full definitions.
[7] See Table 5 for detailed specifications for SYSREF signal to DAC clock timing conditions.

MAXIMUM DAC UPDATE RATE SPEED SPECIFICATIONS BY SUPPLY

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DAC UPDATE RATE					
2×, 4×, and 8× Interpolation					
	DVDD12, CVDD12 = 1.2 V ± 5%	2.23			GSPS
	DVDD12, CVDD12 = 1.2 V ± 2%	2.41			GSPS
	DVDD12, CVDD12 = 1.3 V ± 2%	2.80			GSPS
1× Interpolation					
	DVDD12, CVDD12 = 1.2 V ± 5%	1.81			GSPS
	DVDD12, CVDD12 = 1.2 V ± 2%	1.93			GSPS
	DVDD12, CVDD12 = 1.3 V ± 2%	2.21			GSPS

JESD204B SERIAL INTERFACE SPEED SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
HALF RATE	SVDD12 = 1.2 V ± 5%	5.75		11.4	Gbps
	SVDD12 = 1.2 V ± 2%	5.75		12.0	Gbps
	SVDD12 = 1.3 V ± 2%	5.75		12.4	Gbps
FULL RATE	SVDD12 = 1.2 V ± 5%	2.88		5.98	Gbps
	SVDD12 = 1.2 V ± 2%	2.88		6.06	Gbps
	SVDD12 = 1.3 V ± 2%	2.88		6.2	Gbps
OVERSAMPLING	SVDD12 = 1.2 V ± 5%	1.44		3.0	Gbps
	SVDD12 = 1.2 V ± 2%	1.44		3.04	Gbps
	SVDD12 = 1.3 V ± 2%	1.44		3.1	Gbps

SYSREF SIGNAL TO DAC CLOCK TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, SYSREF± common-mode voltages = 0.0 V, 0.6 V, 1.25 V, and 2.0 V, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSREF DIFFERENTIAL SWING = 0.4 V, SLEW RATE = 1.3 V/ns					
Setup Time	AC-coupled		126		ps
	DC-coupled		131		ps
Hold Time	AC-coupled		92		ps
	DC-coupled		119		ps
SYSREF DIFFERENTIAL SWING = 0.7 V, SLEW RATE = 2.28 V/ns					
Setup Time	AC-coupled		96		ps
	DC-coupled		104		ps
Hold Time	AC-coupled		77		ps
	DC-coupled		95		ps
SYSREF SWING = 1.0 V, SLEW RATE = 3.26 V/ns					
Setup Time	AC-coupled		83		ps
	DC-coupled		90		ps
Hold Time	AC-coupled		68		ps
	DC-coupled		84		ps

DIGITAL INPUT DATA TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 6.

Parameter	Min	Typ	Max	Unit
LATENCY				
Interface		17		PClock[1] cycles
Interpolation				
1×		66		DAC clock cycles
2×		137		DAC clock cycles
4×		251		DAC clock cycles
8×		484		DAC clock cycles
Inverse Sinc		17		DAC clock cycles
Digital Gain Adjust		12		DAC clock cycles
POWER-UP TIME		60		µs

[1] PClock is the AD9135/AD9136 internal processing clock and equals the lane rate ÷ 40.

LATENCY VARIATION SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 7.

Parameter	Min	Typ	Max	Unit
DAC LATENCY VARIATION				
SYNC On				
PLL Off		0	1	DAC clock cycles
PLL On	−1		+1	DAC clock cycles

JESD204B INTERFACE ELECTRICAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 8.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B DATA INPUTS						
Input Leakage Current		T_A = 25°C				
Logic High		Input level = 1.2 V ± 0.25 V, V_{TT} = 1.2 V		10		µA
Logic Low		Input level = 0 V		−4		µA
Unit Interval	UI		94		714	ps
Common-Mode Voltage	V_{RCM}	AC-coupled, V_{TT} = SVDD12[1]	−0.05		+1.85	V
Differential Voltage	R_V_{DIFF}		110		1050	mV
V_{TT} Source Impedance	Z_{TT}	At dc			30	Ω
Differential Impedance	Z_{RDIFF}	At dc	80	100	120	Ω
Differential Return Loss	RL_{RDIF}			8		dB
Common-Mode Return Loss	RL_{RCM}			6		dB
DIFFERENTIAL OUTPUTS ($\overline{SYNCOUTx\pm}$)[2]						
Output Differential Voltage	V_{OD}					
Normal Swing Mode		Register 0x2A5[0] = 0	192		235	mV
High Swing Mode		Register 0x2A5[0] = 1	341		394	mV
Output Offset Voltage	V_{OS}		1.19		1.27	V
DETERMINISTIC LATENCY						
Fixed					17	PClock[3] cycles
Variable					2	PClock[3] cycles
SYSREF± to LOCAL MULTIFRAME COUNTER (LMFC) DELAY				4		DAC clock cycles

[1] As measured on the input side of the ac coupling capacitor.
[2] IEEE Standard 1596.3 LVDS compatible.
[3] PClock is an AD9135/AD9136 internal processing clock and equals the lane rate ÷ 40.

AC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V,[1] V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 9.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	−9 dBFS single-tone				
f_{DAC} = 983.04 MSPS	f_{OUT} = 20 MHz		82		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		76		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 20 MHz		81		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 170 MHz		69		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)	−9 dBFS				
f_{DAC} =983.04 MSPS	f_{OUT} = 20 MHz		90		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		82		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 20 MHz		90		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 170 MHz		81		dBc
NOISE SPECTRAL DENSITY (NSD), SINGLE-TONE	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		−162		dBm/Hz
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		−163		dBm/Hz
W-CDMA FIRST ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE-CARRIER	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 30 MHz		82		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		80		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		80		dBc
W-CDMA SECOND ACLR, SINGLE-CARRIER	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 30 MHz		84		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		85		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		85		dBc

[1] SVDD12 = 1.3 V for all f_{DAC} = 1966.08 MSPS conditions in Table 9.

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
I120 to Ground	−0.3 V to AVDD33 + 0.3 V
SERDINx±, V_{TT}, SYNCOUT1±/ SYNCOUT0±, TXENx	−0.3 V to SIOVDD33 + 0.3 V
OUTx±	−0.3 V to AVDD33 + 0.3 V
SYSREF±	GND − 0.5 V to +2.5 V
CLK± to Ground	−0.3 V to PVDD12 + 0.3 V
RESET, IRQ, CS, SCLK, SDIO, SDO to Ground	−0.3 V to IOVDD + 0.3 V
LDO_BYP1	−0.3 V to SVDD12 + 0.3 V
LDO_BYP2	−0.3 V to PVDD12 + 0.3 V
LDO24	−0.3 V to AVDD33 + 0.3 V
Ambient Operating Temperature (T_A)	−40°C to +85°C
Operating Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The exposed pad (EPAD) must be soldered to the ground plane for the 88-lead LFCSP. The EPAD provides an electrical, thermal, and mechanical connection to the board.

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer JESD51-7 high effective thermal conductivity test board for leaded surface-mount packages. θ_{JA} is obtained in still air conditions (JESD51-2). Airflow increases heat dissipation, effectively reducing θ_{JA}. θ_{JB} is obtained following double-ring cold plate test conditions (JESD51-8). θ_{JC} is obtained with the test case temperature monitored at the bottom of the exposed pad.

Ψ_{JT} and Ψ_{JB} are thermal characteristic parameters obtained with θ_{JA} in still air test conditions.

Junction temperature (T_J) can be estimated using the following equations:

$$T_J = T_T + (\Psi_{JT} \times P)$$

or

$$T_J = T_B + (\Psi_{JB} \times P)$$

where:
T_T is the temperature measured at the top of the package.
P is the total device power dissipation.
T_B is the temperature measured at the board.

Table 11. Thermal Resistance

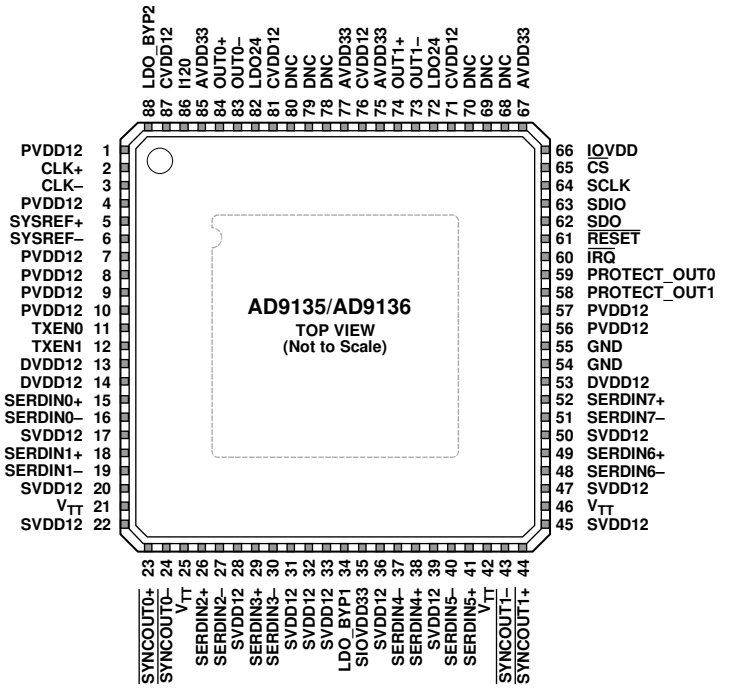
Package	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
88-Lead LFCSP[1]	22.6	5.59	1.17	0.1	5.22	°C/W

[1] The exposed pad must be securely connected to the ground plane.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD MUST BE SECURELY CONNECTED TO THE GROUND PLANE.

Figure 3. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
2	CLK+	PLL Reference/Clock Input, Positive. When the PLL is used, this pin is the positive reference clock input. When the PLL is not used, this pin is the positive device clock input. This pin is self biased and must be ac-coupled.
3	CLK–	PLL Reference/Clock Input, Negative. When the PLL is used, this pin is the negative reference clock input. When the PLL is not used, this pin is the negative device clock input. This pin is self biased and must be ac-coupled.
4	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
5	SYSREF+	Positive Reference Clock for Deterministic Latency. This pin is self biased for ac coupling. It can be ac-coupled or dc-coupled.
6	SYSREF–	Negative Reference Clock for Deterministic Latency. This pin is self biased for ac coupling. It can be ac-coupled or dc-coupled.
7	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
8	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
9	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
10	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
11	TXEN0	Transmit Enable for DAC0. CMOS levels are determined with respect to IOVDD.
12	TXEN1	Transmit Enable for DAC1. CMOS levels are determined with respect to IOVDD.
13	DVDD12	1.2 V Digital Supply.
14	DVDD12	1.2 V Digital Supply.
15	SERDIN0+	Serial Channel Input 0, Positive. CML compliant. SERDIN0+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
16	SERDIN0–	Serial Channel Input 0, Negative. CML compliant. SERDIN0– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
17	SVDD12	1.2 V JESD204B Receiver Supply.
18	SERDIN1+	Serial Channel Input 1, Positive. CML compliant. SERDIN1+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.

Pin No.	Mnemonic	Description
19	SERDIN1−	Serial Channel Input 1, Negative. CML compliant. SERDIN1− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
20	SVDD12	1.2 V JESD204B Receiver Supply.
21	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
22	SVDD12	1.2 V JESD204B Receiver Supply.
23	$\overline{\text{SYNCOUT0+}}$	Positive LVDS Sync (Active Low) Output Signal Channel Link 0.
24	$\overline{\text{SYNCOUT0−}}$	Negative LVDS Sync (Active Low) Output Signal Channel Link 0.
25	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
26	SERDIN2+	Serial Channel Input 2, Positive. CML compliant. SERDIN2+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
27	SERDIN2−	Serial Channel Input 2, Negative. CML compliant. SERDIN2− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
28	SVDD12	1.2 V JESD204B Receiver Supply.
29	SERDIN3+	Serial Channel Input 3, Positive. CML compliant. SERDIN3+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
30	SERDIN3−	Serial Channel Input 3, Negative. CML compliant. SERDIN3− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
31	SVDD12	1.2 V JESD204B Receiver Supply.
32	SVDD12	1.2 V JESD204B Receiver Supply.
33	SVDD12	1.2 V JESD204B Receiver Supply.
34	LDO_BYP1	LDO SERDES Bypass. This pin requires a 1 Ω resistor in series with a 1 µF capacitor to ground.
35	SIOVDD33	3.3 V Supply for SERDES.
36	SVDD12	1.2 V JESD204B Receiver Supply.
37	SERDIN4−	Serial Channel Input 4, Negative. CML compliant. SERDIN4− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
38	SERDIN4+	Serial Channel Input 4, Positive. CML compliant. SERDIN4+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
39	SVDD12	1.2 V JESD204B Receiver Supply.
40	SERDIN5−	Serial Channel Input 5, Negative. CML compliant. SERDIN5− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
41	SERDIN5+	Serial Channel Input 5, Positive. CML compliant. SERDIN5+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
42	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
43	$\overline{\text{SYNCOUT1−}}$	Negative LVDS Sync (Active Low) Output Signal Channel Link 1.
44	$\overline{\text{SYNCOUT1+}}$	Positive LVDS Sync (Active Low) Output Signal Channel Link 1.
45	SVDD12	1.2 V JESD204B Receiver Supply.
46	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
47	SVDD12	1.2 V JESD204B Receiver Supply.
48	SERDIN6−	Serial Channel Input 6, Negative. CML compliant. SERDIN6− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
49	SERDIN6+	Serial Channel Input 6, Positive. CML compliant. SERDIN6+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
50	SVDD12	1.2 V JESD204B Receiver Supply.
51	SERDIN7−	Serial Channel Input 7, Negative. CML compliant. SERDIN7− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
52	SERDIN7+	Serial Channel Input 7, Positive. CML compliant. SERDIN7+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
53	DVDD12	1.2 V Digital Supply.
54	GND	Ground. Connect GND to the ground plane.
55	GND	Ground. Connect GND to the ground plane.
56	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
57	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
58	PROTECT_OUT1	Power Detection and Protection Pin Output for DAC1. Pin 58 is high when power protection is in process.
59	PROTECT_OUT0	Power Detection and Protection Pin Output for DAC0. Pin 59 is high when power protection is in process.
60	$\overline{\text{IRQ}}$	Interrupt Request (Active Low, Open Drain).

Pin No.	Mnemonic	Description
61	$\overline{\text{RESET}}$	Reset. This pin is active low. CMOS levels are determined with respect to IOVDD.
62	SDO	Serial Port Data Output. CMOS levels are determined with respect to IOVDD.
63	SDIO	Serial Port Data Input/Output. CMOS levels are determined with respect to IOVDD.
64	SCLK	Serial Port Clock Input. CMOS levels are determined with respect to IOVDD.
65	$\overline{\text{CS}}$	Serial Port Chip Select. This pin is active low. CMOS levels are determined with respect to IOVDD.
66	IOVDD	IOVDD Supply for CMOS Input/Output and SPI. Operational for 1.8 V ≤ IOVDD ≤ 3.3 V.
67	AVDD33	3.3 V Analog Supply for DAC Cores.
68	DNC	Do not connect to this pin.
69	DNC	Do not connect to this pin.
70	DNC	Do not connect to this pin.
71	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 71.
72	LDO24	2.4 V LDO. Requires a 1 µF capacitor to ground.
73	OUT1−	DAC1 Negative Current Output.
74	OUT1+	DAC1 Positive Current Output.
75	AVDD33	3.3 V Analog Supply for DAC Cores.
76	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 76.
77	AVDD33	3.3 V Analog Supply for DAC Cores.
78	DNC	Do not connect to this pin.
79	DNC	Do not connect to this pin.
80	DNC	Do not connect to this pin.
81	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 81.
82	LDO24	2.4 V LDO. Requires a 1 µF capacitor to ground.
83	OUT0−	DAC0 Negative Current Output.
84	OUT0+	DAC0 Positive Current Output.
85	AVDD33	3.3 V Analog Supply for DAC Cores.
86	I120	Output Current Generation Pin for DAC Full-Scale Current. Tie a 4 kΩ resistor from the I120 pin to ground.
87	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 87.
88	LDO_BYP2	LDO Clock Bypass for DAC PLL. This pin requires a 1 Ω resistor in series with a 1 µF capacitor to ground.
	EPAD	Exposed Pad. The exposed pad must be securely connected to the ground plane.

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error
Offset error is the deviation of the output current from the ideal of 0 mA. For OUTx+, 0 mA output is expected when all inputs are set to 0. For OUTx−, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when the input is at its minimum code and the output when the input is at its maximum code.

Output Compliance Range
The output compliance range is the range of allowable voltages at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Offset drift is a measure of how far from full-scale range (FSR) the DAC output current is at 25°C (in ppm). Gain drift is a measure of the slope of the DAC output current across its full ambient operating temperature range, T_A (in ppm/°C).

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

Adjusted DAC Update Rate
The adjusted DAC update rate is defined as the DAC update rate divided by the smallest interpolating factor. For clarity on DACs with multiple interpolating factors, the adjusted DAC update rate for each interpolating factor may be given.

Physical Lane
Physical Lane x refers to SERDINx±.

Logical Lane
Logical Lane x refers to physical lanes after optionally being remapped by the crossbar block (Register 0x308 to Register 0x30B).

Link Lane
Link Lane x refers to logical lanes considered per link. When paging Link 0 (Register 0x300[2] = 0), Link Lane x = Logical Lane x. When paging Link 1 (Register 0x300[2] = 1, dual link only), Link Lane x = Logical Lane x + 4.

TYPICAL PERFORMANCE CHARACTERISTICS

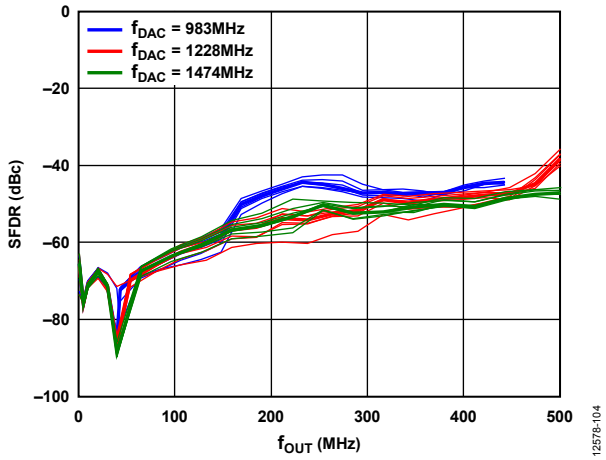


Figure 4. Single-Tone SFDR vs. f_{OUT} in the First Nyquist Zone, f_{DAC} = 983 MHz, 1228 MHz, and 1474 MHz

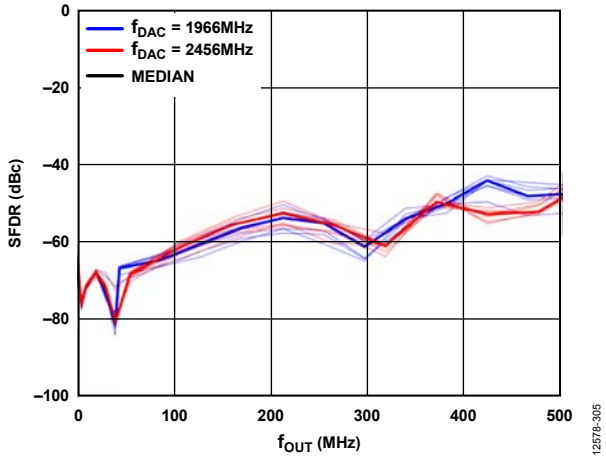


Figure 5. Single-Tone SFDR vs. f_{OUT} in the First Nyquist Zone, f_{DAC} = 1966 MHz and 2456 MHz

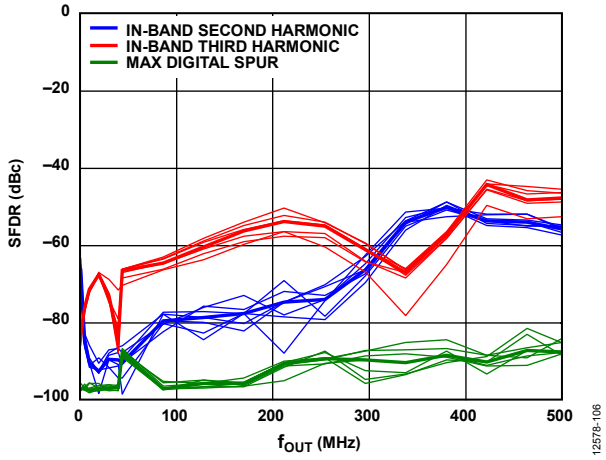


Figure 6. Single-Tone Second and Third Harmonics and Maximum Digital Spur in the First Nyquist Zone, f_{DAC} = 1966 MHz, 0 dB Back Off

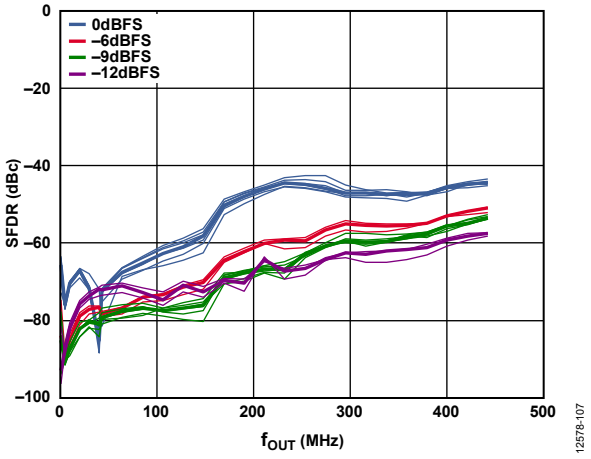


Figure 7. Single-Tone SFDR vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 983 MHz

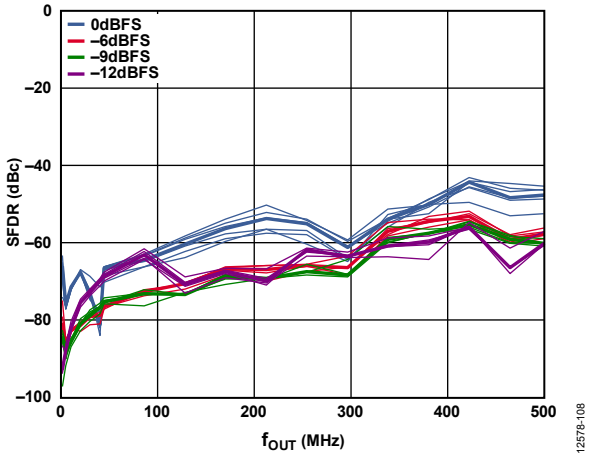


Figure 8. Single-Tone SFDR vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 1966 MHz

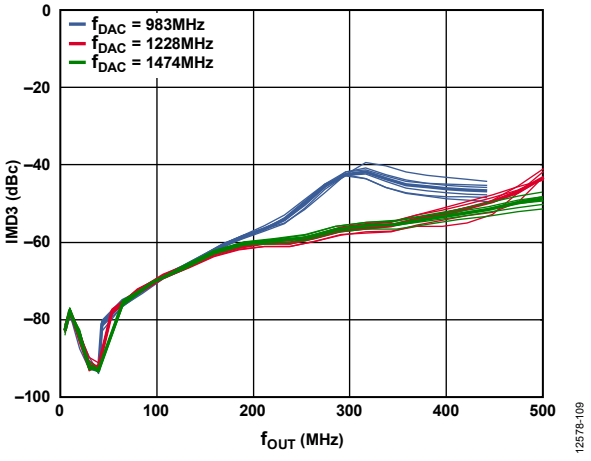


Figure 9. Two-Tone Third IMD (IMD3) vs. f_{OUT}, f_{DAC} = 983 MHz, 1228 MHz, and 1474 MHz

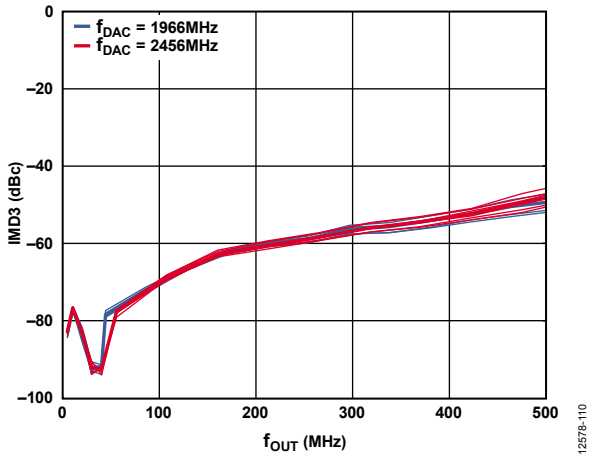


Figure 10. Two-Tone Third IMD (IMD3) vs. f_{OUT}, f_{DAC} = 1966 MHz and 2456 MHz

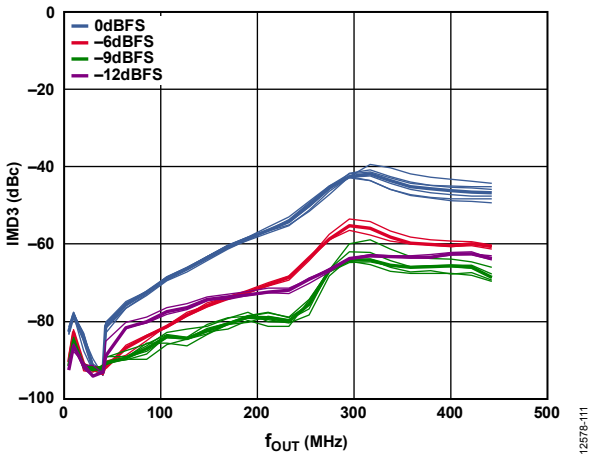


Figure 11. Two-Tone Third IMD (IMD3) vs. f_{OUT} over Digital Back Off, f_{DAC} = 983 MHz, Each Tone Is at –6 dBFS

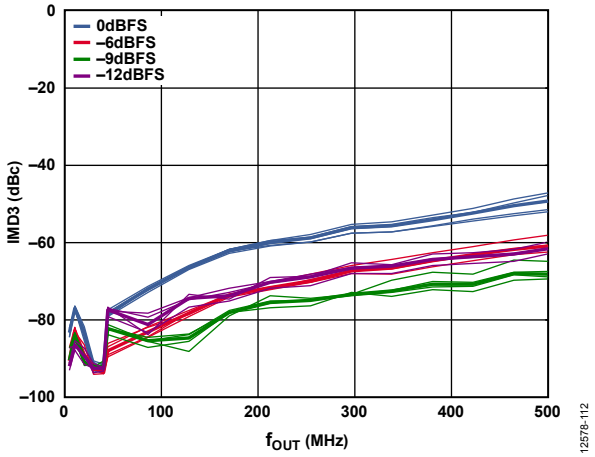


Figure 12. Two-Tone Third IMD (IMD3) vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966 MHz, Each Tone Is at –6 dBFS

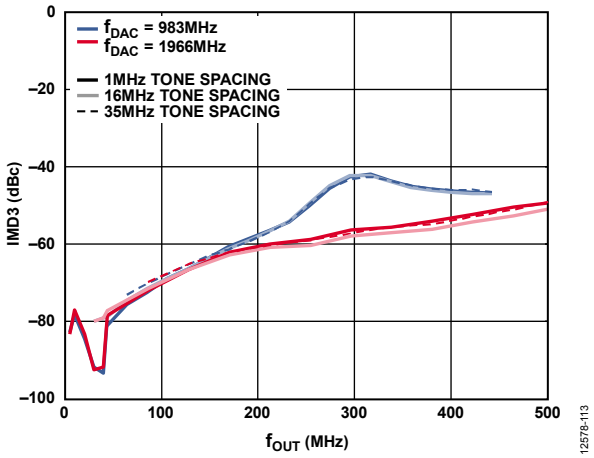


Figure 13. Two-Tone Third IMD (IMD3) vs. f_{OUT} over Tone Spacing at 0 dB Back Off, f_{DAC} = 983 MHz and 1966 MHz

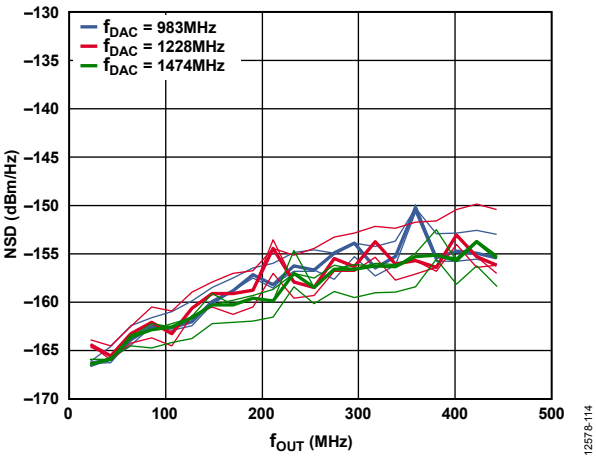


Figure 14. AD9136 Single-Tone (0 dBFS) NSD vs. f_{OUT}, f_{DAC} = 983 MHz, 1228 MHz, and 1474 MHz

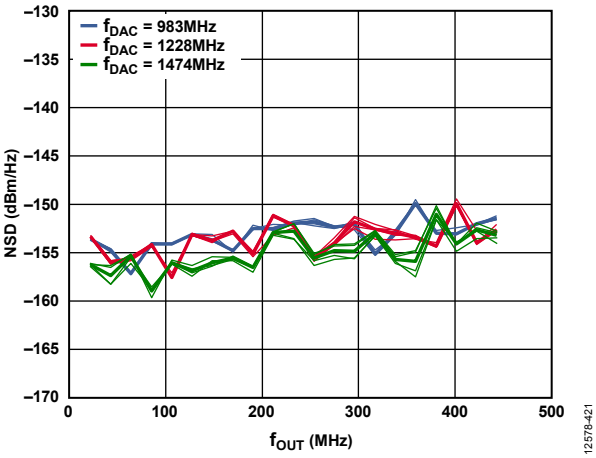


Figure 15. AD9135 Single-Tone (0 dBFS) NSD vs. f_{OUT}, f_{DAC} = 983 MHz, 1228 MHz, and 1474 MHz

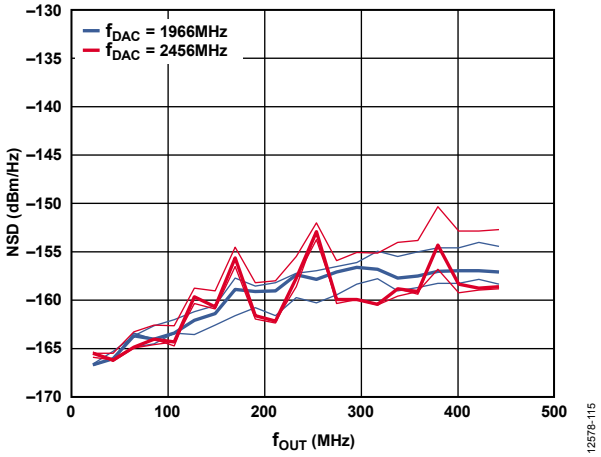


Figure 16. AD9136 Single-Tone (0 dBFS) NSD vs. f_{OUT}, f_{DAC} = 1966 MHz and 2456 MHz

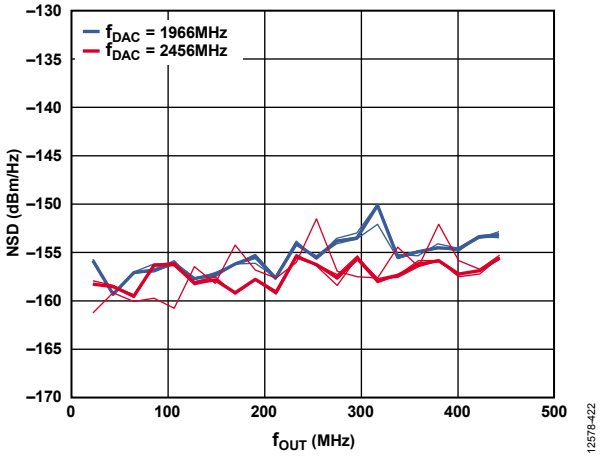


Figure 17. AD9135 Single-Tone (0 dBFS) NSD vs. f_{OUT}, f_{DAC} = 1966 MHz and 2456 MHz

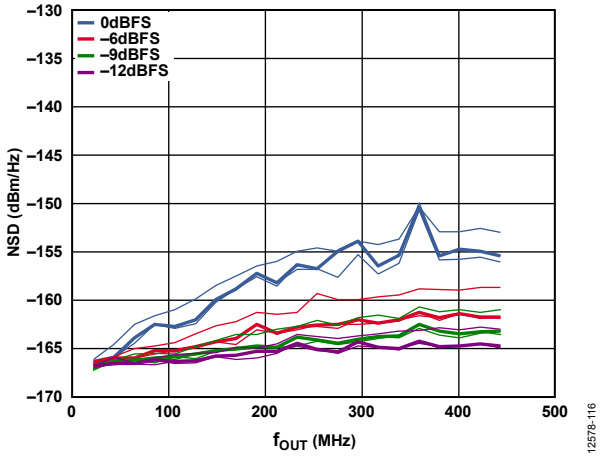


Figure 18. AD9136 Single-Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 983 MHz

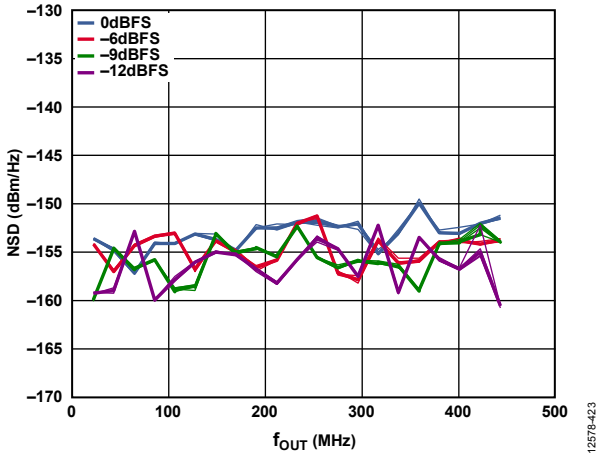


Figure 19. AD9135 Single-Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 983 MHz

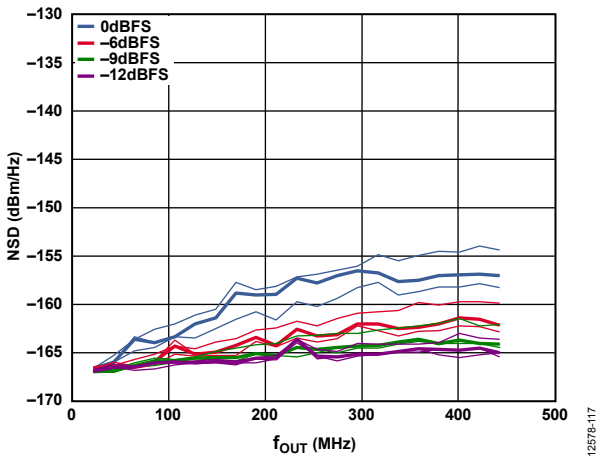


Figure 20. AD9136 Single-Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966 MHz

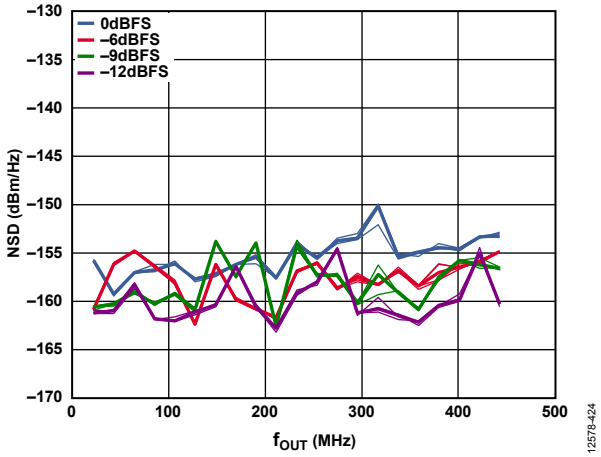


Figure 21. AD9135 Single-Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966 MHz

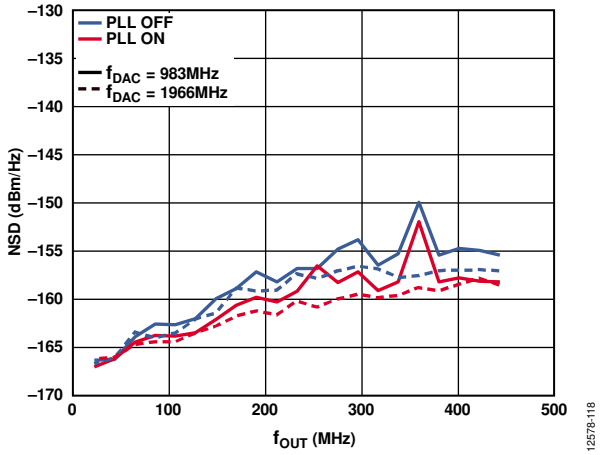


Figure 22. AD9136 Single-Tone NSD (0 dBFS) vs. f_{OUT}, f_{DAC} = 983 MHz and 1966 MHz, PLL On and Off

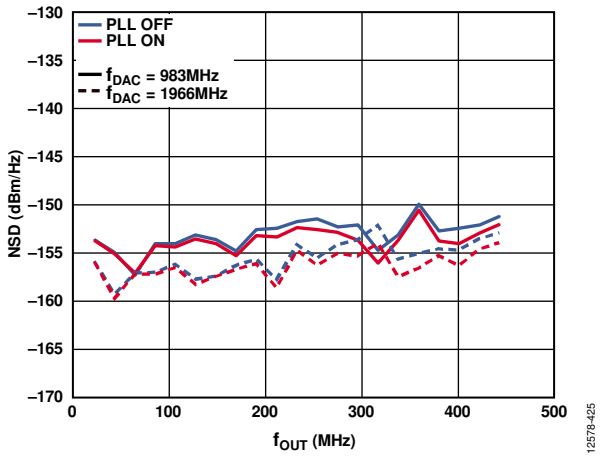


Figure 23. AD9135 Single-Tone NSD (0 dBFS) vs. f_{OUT}, f_{DAC} = 983 MHz and 1966 MHz, PLL On and Off

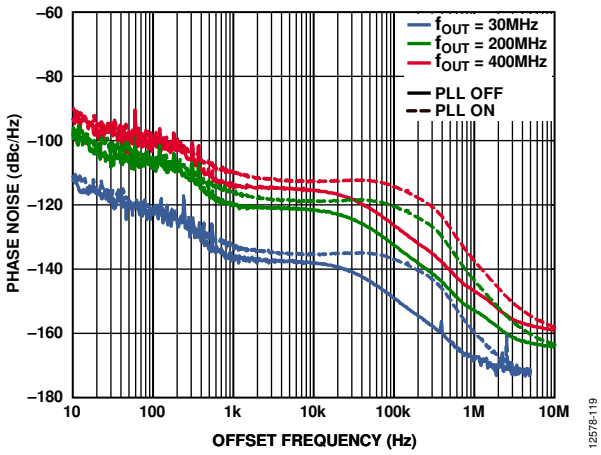


Figure 24. AD9136 Single-Tone Phase Noise vs. Offset Frequency over f_{OUT}, f_{DAC} = 2.0 GHz, PLL On and Off

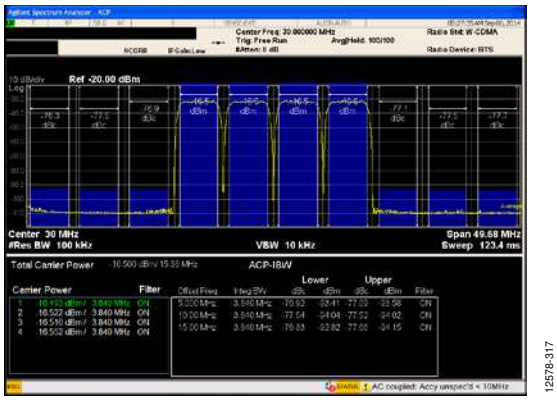


Figure 25. AD9136 Four-Carrier W-CDMA ACLR, f_{OUT} = 30 MHz, f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz

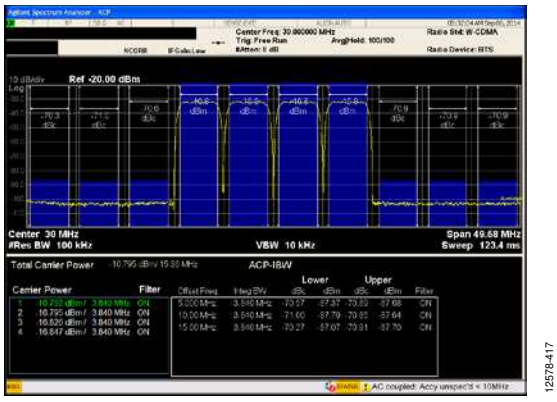


Figure 26. AD9135 Four-Carrier W-CDMA ACLR, f_{OUT} = 30 MHz, f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz

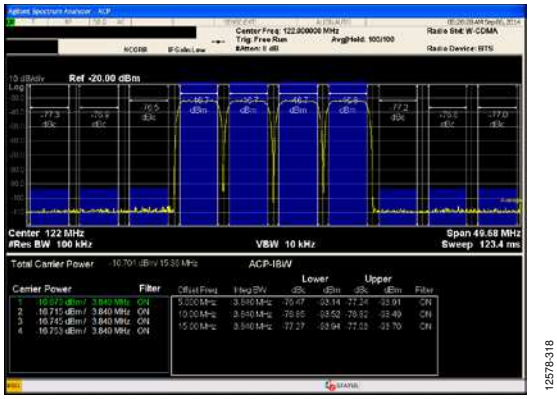


Figure 27. AD9136 Four-Carrier W-CDMA ACLR, f_{OUT} = 122 MHz, f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz

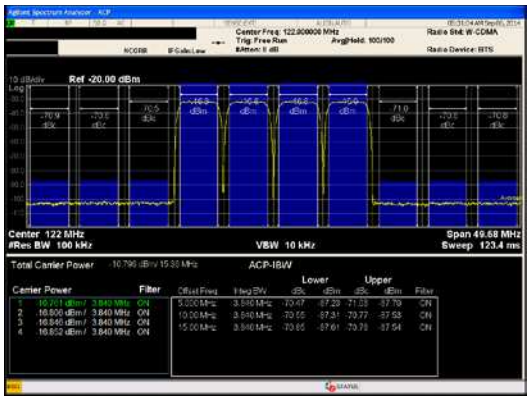


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Figure 28. AD9135 Four-Carrier W-CDMA ACLR, f_{OUT} = 122 MHz, f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz

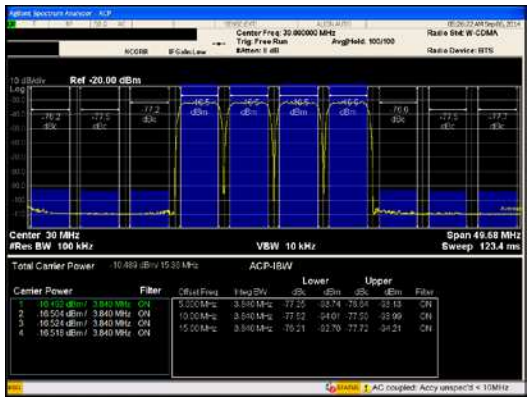

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Figure 29. AD9136 Four-Carrier W-CDMA ACLR, f_{OUT} = 30 MHz, f_{DAC} = 1966 MHz, 4× Interpolation, PLL Frequency = 245 MHz

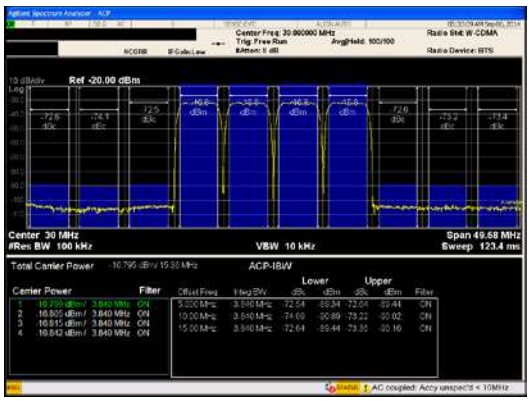

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Figure 30. AD9135 Four-Carrier W-CDMA ACLR, f_{OUT} = 30 MHz, f_{DAC} = 1966 MHz, 4× Interpolation, PLL Frequency = 245 MHz

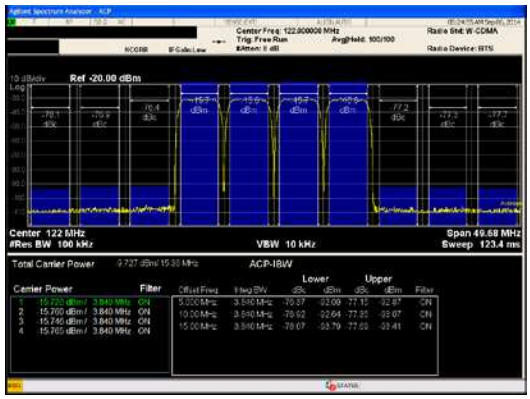

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Figure 31. AD9136 Four-Carrier W-CDMA ACLR, f_{OUT} = 122 MHz, f_{DAC} = 1966 MHz, 4× Interpolation, PLL Frequency = 122 MHz

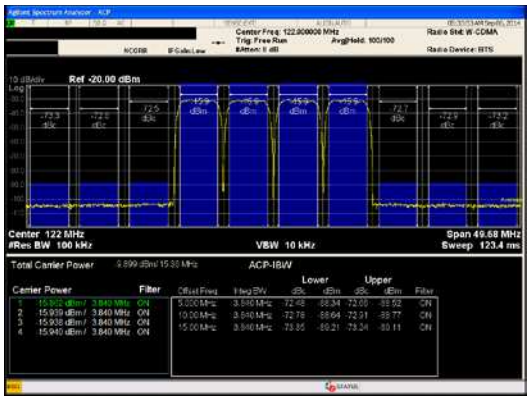

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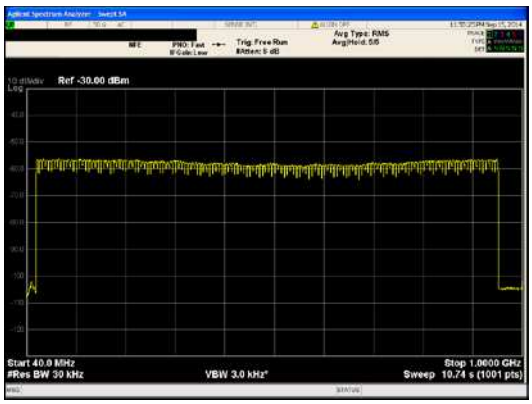
Figure 32. AD9135 Four-Carrier W-CDMA ACLR, f_{OUT} = 122 MHz, f_{DAC} = 1966 MHz, 4× Interpolation, PLL Frequency = 122 MHz



12578-433

Figure 33. AD9136 Output Performance of an Ultra Wideband (900 MHz) QAM Signal, f_{DAC} = 2 GHz, 1× Interpolation, Inverse sinc On, JESD204B Mode 11

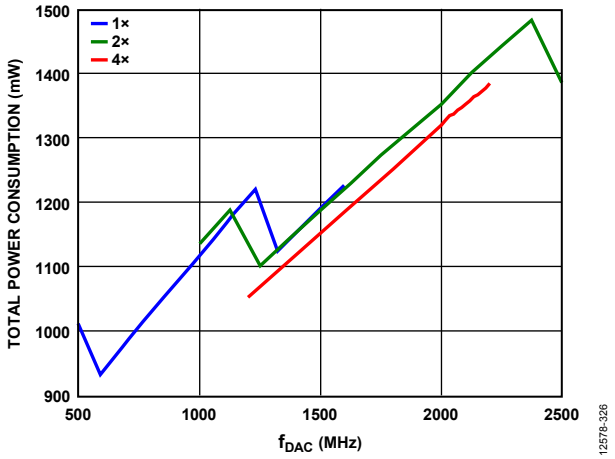


Figure 34. Total Power Consumption vs. f_{DAC} over Interpolation, 8 SERDES Lanes Enabled, 2 DACs Enabled, Digital Gain, Inverse Sinc and DAC PLL Disabled

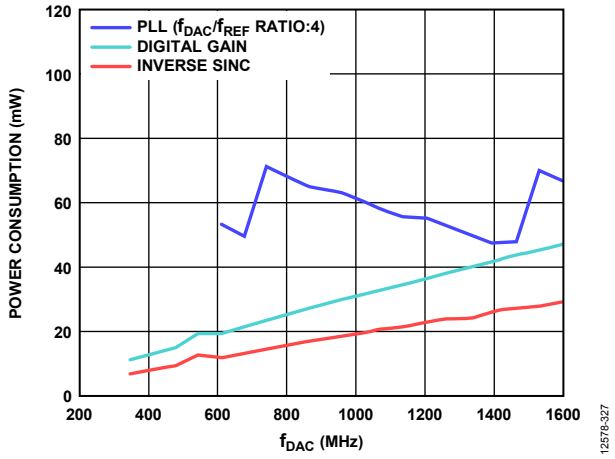


Figure 35. Power Consumption vs. f_{DAC} over Digital Functions

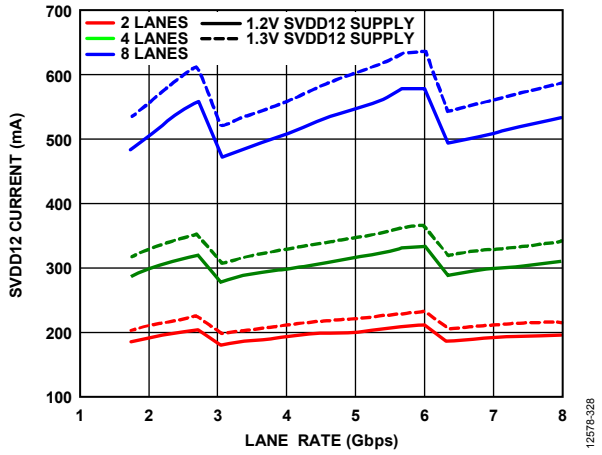


Figure 36. SVDD12 Current vs. Lane Rate over Number of SERDES Lanes and Supply Voltage Setting

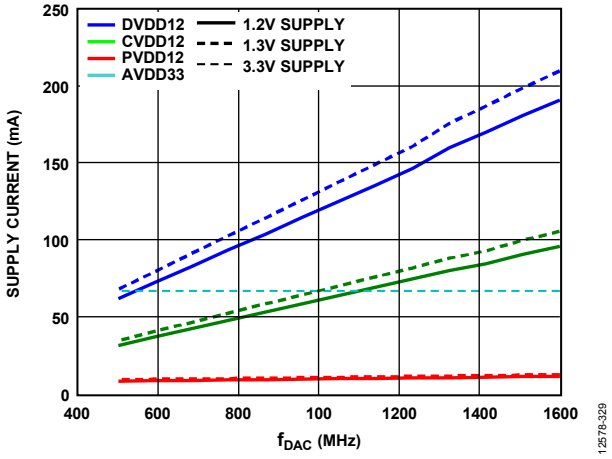


Figure 37. DVDD12, CVDD12, PVDD12, and AVDD33 Supply Currents vs. f_{DAC} over Supply Voltage Setting, 2 DACs Enabled

THEORY OF OPERATION

The AD9135/AD9136 are 11-/16-bit, dual DACs with a SERDES interface. Figure 2 shows a detailed functional block diagram of the AD9135/AD9136. Eight high speed serial lanes carry data at a maximum speed of 12.4 Gbps, and a 2120 MSPS input data rate to each DAC. Compared to either LVDS or CMOS interfaces, the SERDES interface simplifies pin count, board layout, and input clock requirements to the device.

The clock for the input data is derived from the device clock (required by the JESD204B specification). This device clock can be sourced with a PLL reference clock used by the on-chip PLL to generate a DAC clock or a high fidelity direct external DAC sampling clock. The device can be configured to operate in one-, two-, four-, or eight-lane modes, depending on the required input data rate.

The digital datapath of the AD9135/AD9136 offers four interpolation modes (1×, 2×, 4×, and 8×) through three half-band filters with a maximum DAC sample rate of 2.8 GSPS. An inverse sinc filter is provided to compensate for sinc related roll-off.

The AD9135/AD9136 DAC cores provide a fully differential current output with a nominal full-scale current of 20 mA. The full-scale current, I_{OUTFS}, is user adjustable to between 13.9 mA and 27.0 mA, typically. The differential current outputs are complementary and are optimized for easy integration with the Analog Devices the ADRF6720 AQM. The AD9135/AD9136 are capable of multichip synchronization that can both synchronize multiple DACs and establish a constant and deterministic latency (latency locking) path for the DACs. The latency for each of the DACs remains constant from link establishment to link establishment. An external alignment (SYSREF±) signal makes the AD9135/AD9136 Subclass 1 compliant. Several modes of SYSREF± signal handling are available for use in the system.

An SPI configures the various functional blocks and monitors their statuses. The various functional blocks and the data interface must be set up in a specific sequence for proper operation (see the Device Setup Guide section). Simple SPI initialization routines set up the JESD204B link and are included in the evaluation board package. The following sections describe the various blocks of the AD9135/AD9136 in greater detail. Descriptions of the JESD204B interface, control parameters, and various registers to set up and monitor the device are provided. The recommended start-up routine reliably sets up the data link.

SERIAL PORT OPERATION

The serial port is a flexible, synchronous serial communications port that allows easy interfacing with many industry-standard microcontrollers and microprocessors. The serial input/output (I/O) is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9135/AD9136. MSB first or LSB first transfer formats are supported. The serial port interface can be configured as a 4-wire interface or a 3-wire interface in which the input and output share a single-pin I/O (SDIO).

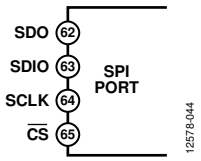


Figure 38. Serial Port Interface Pins

There are two phases to a communication cycle with the AD9135/AD9136. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first 16 SCLK rising edges. The instruction word provides the serial port controller with information regarding the data transfer cycle, Phase 2 of the communication cycle. The Phase 1 instruction word defines whether the upcoming data transfer is a read or write, along with the starting register address for the following data transfer.

A logic high on the $\overline{CS}$ pin followed by a logic low resets the serial port timing to the initial state of the instruction cycle. From this state, the next 16 rising SCLK edges represent the instruction bits of the current I/O operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one or more data bytes. Eight × N SCLK cycles are needed to transfer N bytes during the transfer cycle. Registers change immediately upon writing to the last bit of each transfer byte.

DATA FORMAT

The instruction byte contains the information shown in Table 13.

Table 13. Serial Port Instruction Word

I[15] (MSB)	I[14:0]
R/$\overline{W}$	A[14:0]

R/$\overline{W}$, Bit 15 of the instruction word, determines whether a read or a write data transfer occurs after the instruction word write. Logic 1 indicates a read operation, and Logic 0 indicates a write operation.

A14 to A0, Bit 14 to Bit 0 of the instruction word, determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, A[14:0] is the starting address. The remaining register addresses are generated by the device based on the address increment bits. If the address increment bits are set high (Register 0x000, Bit 5 and Bit 2), multibyte SPI writes start at A[14:0] and increment by 1 every 8 bits sent/received. If the address increment bits are set to 0, the address decrements by 1 every 8 bits.

SERIAL PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is 10 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

An active low input starts and gates a communication cycle. $\overline{CS}$ allows more than one device to be used on the same serial communications lines. The SDIO pin goes to a high impedance state when this input is high. During the communication cycle, chip select must stay low.

Serial Data I/O (SDIO)

This pin is a bidirectional data line. In 4-wire mode, this pin acts as the data input, and SDO acts as the data output.

SERIAL PORT OPTIONS

The serial port can support both MSB first and LSB first data formats. This functionality is controlled by the LSB first bits (Register 0x000, Bit 6 and Bit 1). The default is MSB first (LSBFIRST/LSBFIRST_M = 0).

When the LSB first bits = 0 (MSB first), the instruction and data bits must be written from MSB to LSB. R/$\overline{W}$ is followed by A[14:0] as the instruction word, and D[7:0] is the data-word. When the LSB first bits = 1 (LSB first), the opposite is true. A[0:14] is followed by R/$\overline{W}$, which is subsequently followed by D[0:7].

The serial port supports a 3-wire or 4-wire interface. When the SDO active bits = 1 (Register 0x000, Bit 4 and Bit 3), a 4-wire interface with a separate input pin (SDIO) and output pin (SDO) is used. When the SDO active bits = 0, the SDO pin is unused and the SDIO pin is used for both input and output.

Multibyte data transfers can be performed as well. This is done by holding the $\overline{CS}$ pin low for multiple data transfer cycles (eight SCLKs) after the first data transfer word following the instruction cycle. The first eight SCLKs following the instruction cycle read from or write to the register provided in the instruction cycle. For each additional eight SCLK cycles, the address is either incremented or decremented and the read/write occurs on the new register. The direction of the address can be set using the address increment bits (Register 0x000, Bit 5 and Bit 2). When the address increment bits is 1, the multicycle addresses are incremented. When the address increment bits is 0, the addresses are decremented. A new write cycle can always be initiated by bringing $\overline{CS}$ high and then low again.

To prevent confusion and to ensure consistency between devices, the chip tests the first nibble following the address phase, ignoring the second nibble. This test is completed independently from the LSB first bit and ensures that there are extra clock cycles following the soft reset bits (Register 0x000, Bit 0 and Bit 7). This only applies when writing to Register 0x000.

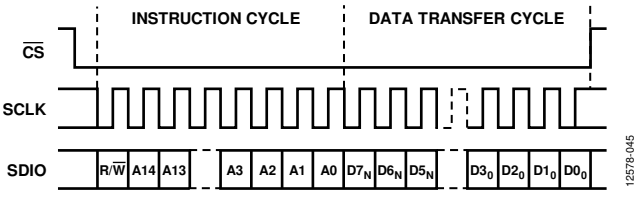


Figure 39. Serial Register Interface Timing, MSB First, ADDRINC = 0

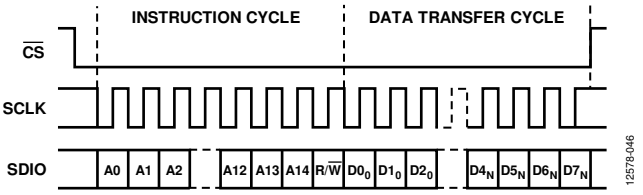


Figure 40. Serial Register Interface Timing, LSB First, ADDRINC = 1

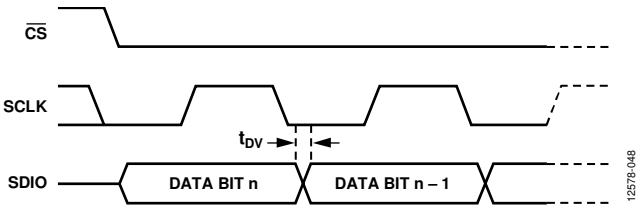


Figure 41. Timing Diagram for Serial Port Register Read

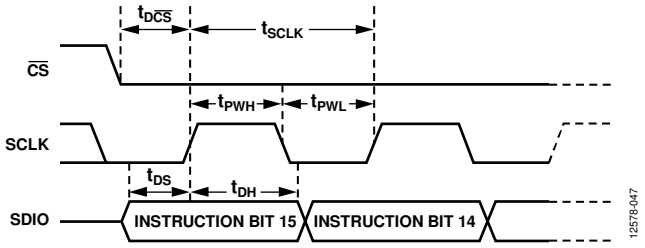


Figure 42. Timing Diagram for Serial Port Register Write

CHIP INFORMATION

Register 0x003 to Register 0x006 contain chip information, as shown in Table 14.

Table 14. Chip Information

Information	Description
Chip Type	The product type is high speed DAC, which is represented by a code of 0x04 in Register 0x003.
Product ID	Eight MSBs in Register 0x005 and eight LSBs in Register 0x004. The product ID is 0x9144.
Product Grade	Register 0x006[7:4]. The product grade is 0x6 for the AD9136 and 0x4 for the AD9135.
Device Revision	Register 0x006[3:0]. The device revision is 0x08.