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Dual, 16-Bit, 1600 MSPS, TxDAC+ Digital-to-Analog Converter

Data Sheet **AD9142A**

FEATURES

- Supports input data rate up to 575 MHz
- Very small inherent latency variation: <2 DAC clock cycles
- Proprietary low spurious and distortion design
  - 6-carrier GSM ACLR = 79 dBc at 200 MHz IF
  - SFDR > 85 dBc (bandwidth = 300 MHz) at ZIF
- Flexible 16-bit LVDS interface
  - Supports word and byte load
  - Data interface DLL
  - Sample error detection and parity
- Multiple chip synchronization
  - Fixed latency and data generator latency compensation
- Selectable 2×, 4×, 8× interpolation filter
  - Low power architecture
  - $f_S/4$ power saving coarse mixer
- Input signal power detection
  - Emergency stop for downstream analog circuitry protection
  - FIFO error detection
- On-chip numeric control oscillator allows carrier placement anywhere in the DAC Nyquist bandwidth
- Transmit enable function for extra power saving
- High performance, low noise PLL clock multiplier
- Digital gain and phase adjustment for sideband suppression
- Digital inverse sinc filter
- Low power: 1.8 W at 1.6 GSPS, 1.5 W at 1.25 GSPS, full operating conditions
- 72-lead LFCSP

APPLICATIONS

- Wireless communications: 3G/4G and MC-GSM base stations, wideband repeaters, software defined radios
- Wideband communications: point-to-point, LMDS/MMDS
- Transmit diversity/MIMO
- Instrumentation
- Automated test equipment

GENERAL DESCRIPTION

The AD9142A is a dual, 16-bit, high dynamic range digital-to-analog converter (DAC) that provides a sample rate of 1600 MSPS, permitting a multicarrier generation up to the Nyquist frequency. The AD9142A TxDAC+® includes features optimized for direct conversion transmit applications, including complex digital modulation, input signal power detection, and gain, phase, and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators, such as the ADL537x F-MOD series and the ADRF670x series from Analog Devices, Inc. A 3-wire serial port interface provides for the programming/readback of many internal parameters. Full-scale output current can be programmed over a range of 9 mA to 33 mA. The AD9142A is available in a 72-lead LFCSP.

PRODUCT HIGHLIGHTS

1. Wide signal bandwidth (BW) enables emerging wideband and multiband wireless applications.
2. Advanced low spurious and distortion design techniques provide high quality synthesis of wideband signals from baseband to high intermediate frequencies.
3. Very small inherent latency variation simplifies both software and hardware design in the system. It allows easy multichip synchronization for most applications.
4. New low power architecture improves power efficiency (mW/MHz/channel) by 30%.
5. Input signal power and FIFO error detection simplify designs for downstream analog circuitry protection.
6. Programmable transmit enable function allows easy design balance between power consumption and wakeup time.

Rev. A

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Technical Support www.analog.com

AD9142A* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9142A Evaluation Board

DOCUMENTATION

Application Notes

- AN-1342: AD9142 to AD9142A Migration

Data Sheet

- AD9142A: Dual, 16-Bit, 1600 MSPS, TxDAC+ Digital-to-Analog Converter Data Sheet

TOOLS AND SIMULATIONS

- AD9142A IBIS Model

REFERENCE DESIGNS

- CN0375

REFERENCE MATERIALS

Press

- Analog Devices Introduces High-Performance RF ICs for Multi-band Base Stations and Microwave Point-to-Point Radios

DESIGN RESOURCES

- AD9142A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9142A EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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12/13—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

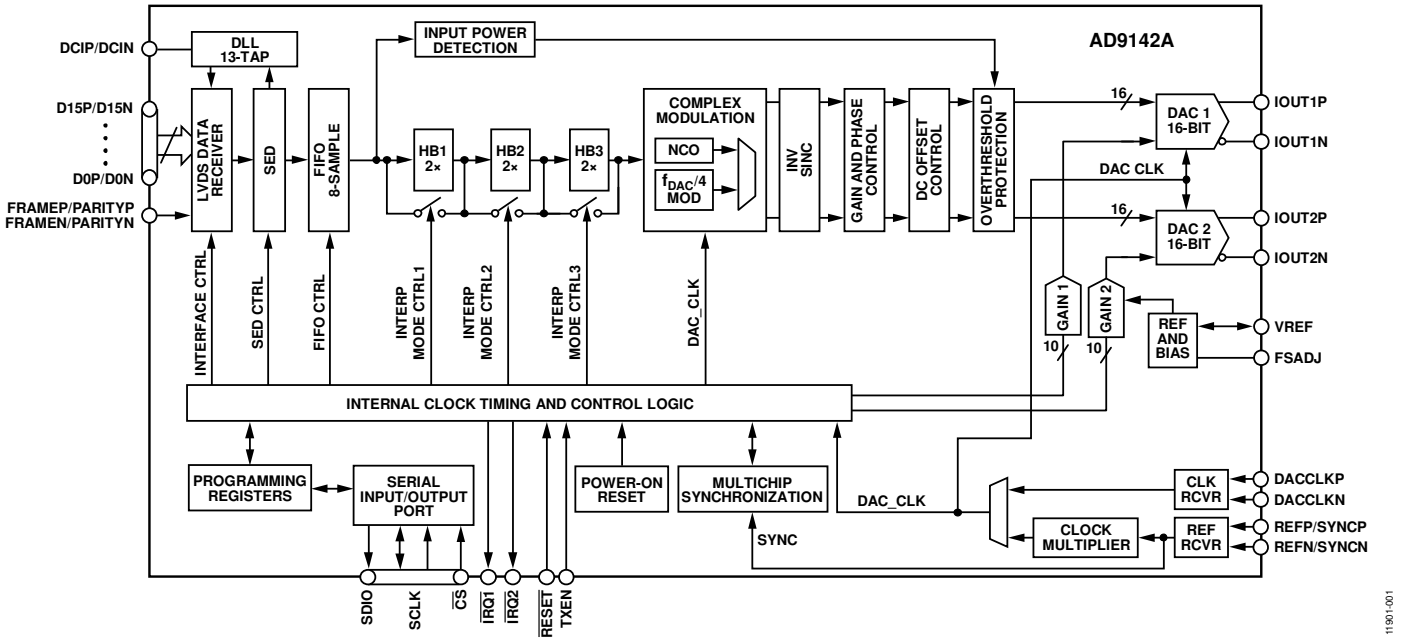

Figure 1.

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION			16		Bits
ACCURACY					
Differential Nonlinearity (DNL)			±2.1		LSB
Integral Nonlinearity (INL)			±3.7		LSB
MAIN DAC OUTPUTS					
Offset Error		−0.001	0	+0.001	% FSR
Gain Error	With internal reference	−3.2	+2	+4.7	% FSR
Full-Scale Output Current	Based on a 10 kΩ external resistor between FSADJ and AVSS	19.06	19.8	20.6	mA
Output Compliance Range		−1.0		+1.0	V
Output Resistance			10		MΩ
Gain DAC Monotonicity			Guaranteed		
Settling Time to Within ±0.5 LSB			20		ns
MAIN DAC TEMPERATURE DRIFT					
Offset			0.04		ppm/°C
Gain			100		ppm/°C
Reference Voltage			30		ppm/°C
REFERENCE					
Internal Reference Voltage		1.17		1.19	V
Output Resistance			5		kΩ
ANALOG SUPPLY VOLTAGES					
AVDD33		3.13	3.3	3.47	V
CVDD18		1.7	1.8	1.9	V
DIGITAL SUPPLY VOLTAGES					
DVDD18		1.7	1.8	1.9	V
DVDD18 Variation over Operating Conditions[1]		−2.5%		+2.5%	V
POWER CONSUMPTION					
2× Mode	f_{DAC} = 737.28 MSPS				
NCO OFF			925		mW
NCO ON			1217		mW
2× Mode	f_{DAC} = 983.04 MSPS				
NCO OFF			1135		mW
NCO ON			1520		mW
4× Mode	f_{DAC} = 737.28 MSPS				
NCO OFF			852		mW
NCO ON			1144		mW
4× Mode	f_{DAC} = 983.04 MSPS				
NCO OFF			1040		mW
NCO ON			1425		mW
4× Mode	f_{DAC} = 1228.8 MSPS				
NCO OFF			1230		mW
NCO ON			1725		mW
4× Mode	f_{DAC} = 1474.56 MSPS				
NCO OFF			1405		mW
NCO ON			1990		mW

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
8× Mode	f_{DAC} = 1600 MSPS				
NCO OFF			1350		mW
NCO ON			1984		mW
Phase-Lock Loop (PLL)			70		mW
Inverse Sinc	f_{DAC} = 1474.56 MSPS		113		mW
Reduced Power Mode (Power-Down)				96.6	mW
AVDD33				1.5	mA
CVDD18				42.3	mA
DVDD18				8.6	mA
OPERATING RANGE		−40	+25	+85	°C

[1] This term specifies the maximum allowable variation of DVDD18 over operating conditions compared with the DVDD18 presented to the device at the time the data interface DLL is enabled.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL						
Input						
Logic High		DVDD18 = 1.8 V	1.2			V
Logic Low		DVDD18 = 1.8 V			0.6	V
CMOS OUTPUT LOGIC LEVEL						
Output						
Logic High		DVDD18 = 1.8 V	1.4			V
Logic Low		DVDD18 = 1.8 V			0.4	V
LVDS RECEIVER INPUTS		Data, frame signal, and DCI inputs				
Input Voltage Range	V_{IA} or V_{IB}		825		1675	mV
Input Differential Threshold	V_{IDTH}		−175		+175	mV
Input Differential Hysteresis	V_{IDTHH} to V_{IDTHL}			20		mV
Receiver Differential Input Impedance	R_{IN}			100		Ω
DLL SPEED RANGE			250		575	MHz
DAC UPDATE RATE					1600	MSPS
DAC Adjusted Update Rate		2× interpolation			575	MSPS
DAC CLOCK INPUT (DACCLKP, DACCLKN)						
Differential Peak-to-Peak Voltage			100	500	2000	mV
Common-Mode Voltage		Self biased input, ac-coupled		1.25		V
REFCLK/SYNCCLK INPUT (REFP/SYNCP, REFN/SYNCN)						
Differential Peak-to-Peak Voltage			100	500	2000	mV
Common-Mode Voltage				1.25		V
Input Clock Frequency		1.03 GHz ≤ f_{VCO} ≤ 2.07 GHz			450	MHz
SERIAL PORT INTERFACE						
Maximum Clock Rate	SCLK		40			MHz
Minimum Pulse Width						
High	t_{PWH}				12.5	ns
Low	t_{PWL}				12.5	ns
SDIO to SCLK Setup Time	t_{DS}		1.5			ns
SDIO to SCLK Hold Time	t_{DH}		0.68			ns
$\overline{CS}$ to SCLK Setup Time	t_{DCSB}		2.38	1.4		ns
$\overline{CS}$ to SCLK Hold Time	t_{DCSB}		9.6			ns
SDIO to SCLK Delay	t_{DV}	Wait time for valid output from SDIO	11			ns
SDIO High-Z to $\overline{CS}$		Time for SDIO to relinquish the output bus	8.5			ns
SDIO LOGIC LEVEL						
Voltage Input High	V_{IH}		1.2	1.8		V
Voltage Input Low	V_{IL}			0	0.5	V
Voltage Output High	I_{IH}	With 2 mA loading	1.36		2	V
Voltage Output Low	I_{IL}	With 2 mA loading	0		0.45	V

DAC LATENCY SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, FIFO level is set to 4 (half of the FIFO depth), unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
WORD INTERFACE MODE	Fine/coarse modulation, inverse sinc, gain/phase compensation off				
2× Interpolation			134		DACCLK cycles
4× Interpolation			244		DACCLK cycles
8× Interpolation			481		DACCLK cycles
BYTE INTERFACE MODE	Fine/coarse modulation, inverse sinc, gain/phase compensation off				
2× Interpolation			145		DACCLK cycles
4× Interpolation			271		DACCLK cycles
8× Interpolation			506		DACCLK cycles
INDIVIDUAL FUNCTION BLOCKS					
Modulation					
Fine			17		DACCLK cycles
Coarse			10		DACCLK cycles
Inverse Sinc			20		DACCLK cycles
Phase Compensation			12		DACCLK cycles
Gain Compensation			16		DACCLK cycles

LATENCY VARIATION SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit
DAC LATENCY VARIATION[1]				
SYNC Off		1	2	DACCLK cycles
SYNC On		0	1	DACCLK cycles

[1] DAC latency is defined as the elapsed time from a data sample clocked at the input to the AD9142A until the analog output begins to change.

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	−14 dBFS single tone				
f_{DAC} = 737.28 MSPS	f_{OUT} = 200 MHz				
BW = 125 MHz			85		dBc
BW = 270 MHz			80		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 200 MHz				
BW = 360 MHz			85		dBc
f_{DAC} = 1228.8 MSPS	f_{OUT} = 280 MHz				
BW = 200 MHz			85		dBc
BW = 500 MHz			75		dBc
f_{DAC} = 1474.56 MSPS					
BW = 737 MHz	f_{OUT} = 10 MHz		85		dBc
BW = 400 MHz	f_{OUT} = 280 MHz		80		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)	−12 dBFS each tone				
f_{DAC} = 737.28 MSPS	f_{OUT} = 200 MHz		80		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 200 MHz		82		dBc
f_{DAC} = 1228.8 MSPS	f_{OUT} = 280 MHz		80		dBc
f_{DAC} = 1474.56 MSPS	f_{OUT} = 10 MHz		85		dBc
	f_{OUT} = 280 MHz		79		dBc
NOISE SPECTRAL DENSITY (NSD)	Eight-tone, 500 kHz tone spacing				
f_{DAC} = 737.28 MSPS	f_{OUT} = 200 MHz		−160		dBm/Hz
f_{DAC} = 983.04 MSPS	f_{OUT} = 200 MHz		−161.5		dBm/Hz
f_{DAC} = 1228.8 MSPS	f_{OUT} = 280 MHz		−164.5		dBm/Hz
f_{DAC} = 1474.56 MSPS	f_{OUT} = 10 MHz		−166		dBm/Hz
	f_{OUT} = 280 MHz		−162.5		dBm/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR)	Single carrier				
f_{DAC} = 983.04 MSPS	f_{OUT} = 200 MHz		81		dBc
f_{DAC} = 1228.8 MSPS	f_{OUT} = 20 MHz		83		dBc
	f_{OUT} = 280 MHz		80		dBc
f_{DAC} = 1474.56 MSPS	f_{OUT} = 20 MHz		81		dBc
	f_{OUT} = 280 MHz		80		dBc
W-CDMA SECOND (ACLR)	Single carrier				
f_{DAC} = 983.04 MSPS	f_{OUT} = 200 MHz		85		dBc
f_{DAC} = 1228.8 MSPS	f_{OUT} = 20 MHz		86		dBc
	f_{OUT} = 280 MHz		86		dBc
f_{DAC} = 1474.56 MSPS	f_{OUT} = 20 MHz		86		dBc
	f_{OUT} = 280 MHz		85		dBc

OPERATING SPEED SPECIFICATIONS

Table 6.

	DVDD18, CVDD18 = 1.8 V ± 5%		DVDD18, CVDD18 = 1.9 V ± 5% or 1.8 V ± 2%		DVDD18, CVDD18 = 1.9 V ± 2%	
Interpolation Factor	f_{DCI} (MSPS) Maximum	f_{DAC} (MSPS) Maximum	f_{DCI} (MSPS) Maximum	f_{DAC} (MSPS) Maximum	f_{DCI} (MSPS) Maximum	f_{DAC} (MSPS) Maximum
2×	575	1150	575	1150	575	1150
4×	350	1400	375	1500	400	1600
8×	175	1400	187.5	1500	200	1600

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
AVDD33 to GND	−0.3 V to +3.6 V
DVDD18, CVDD18 to GND	−0.3 V to +2.1 V
FSADJ, VREF, IOUT1P, IOUT1N, IOUT2P, IOUT2N to GND	−0.3 V to AVDD33 + 0.3 V
D15P to D0P, D15N to D0N, FRAMEP/PARITYP, FRAMEN/PARITYN, DCIP, DCIN to GND	−0.3 V to DVDD18 + 0.3 V
DACCLKP, DACCLKN, REFP, SYNCP, REFN, SYNCN to GND	−0.3 V to CVDD18 + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, $\overline{\text{CS}}$, SCLK, SDIO to GND	−0.3 V to DVDD18 + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed pad (EPAD) must be soldered to the ground plane (AVSS) for the 72-lead LFCSP. The EPAD provides an electrical, thermal, and mechanical connection to the board.

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA} and θ_{JB}.

Table 8. Thermal Resistance

Package	θ_{JA}	θ_{JB}	θ_{JC}	Unit	Conditions
72-Lead LFCSP	20.7	10.9	1.1	°C/W	EPAD soldered to ground plane

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

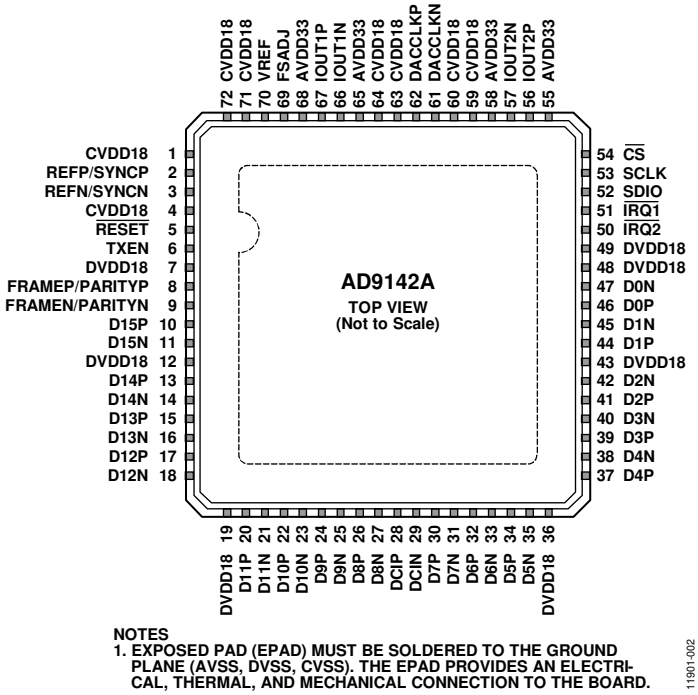

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V PLL Supply. CVDD18 supplies the clock receivers, clock multiplier, and clock distribution.
2	REFP/SYNCP	PLL Reference Clock/Synchronization Clock Input, Positive.
3	REFN/SYNCN	PLL Reference Clock/Synchronization Clock Input, Negative.
4	CVDD18	1.8 V PLL Supply. CVDD18 supplies the clock receivers, clock multiplier, and clock distribution.
5	$\overline{\text{RESET}}$	Reset, Active Low. CMOS levels with respect to DVDD18. Recommended reset pulse length is 1 µs.
6	TXEN	Active High Transmit Path Enable. CMOS levels with respect to DVDD18. A low level on this pin triggers three selectable actions in the DAC. See Table 87 for details.
7	DVDD18	1.8 V Digital Supply. Pin 7 supplies power to the digital core, digital data ports, serial port input/output pins, $\overline{\text{RESET}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$.
8	FRAMEP/PARITYP	Frame/Parity Input, Positive.
9	FRAMEN/PARITYN	Frame/Parity Input, Negative.
10	D15P	Data Bit 15 (MSB), Positive.
11	D15N	Data Bit 15 (MSB), Negative.
12	DVDD18	1.8 V Digital Supply. Pin 12 supplies the power to the digital core and digital data ports, serial port input/output pins, $\overline{\text{RESET}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$.
13	D14P	Data Bit 14, Positive.
14	D14N	Data Bit 14, Negative.
15	D13P	Data Bit 13, Positive.
16	D13N	Data Bit 13, Negative.
17	D12P	Data Bit 12, Positive.
18	D12N	Data Bit 12, Negative.
19	DVDD18	1.8 V Digital Supply. Pin 19 supplies power to the digital core, digital data ports, serial port input/output pins, $\overline{\text{RESET}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$.
20	D11P	Data Bit 11, Positive.
21	D11N	Data Bit 11, Negative.
22	D10P	Data Bit 10, Positive.
23	D10N	Data Bit 10, Negative.

Pin No.	Mnemonic	Description
24	D9P	Data Bit 9, Positive.
25	D9N	Data Bit 9, Negative.
26	D8P	Data Bit 8, Positive.
27	D8N	Data Bit 8, Negative.
28	DCIP	Data Clock Input, Positive.
29	DCIN	Data Clock Input, Negative.
30	D7P	Data Bit 7, Positive.
31	D7N	Data Bit 7, Negative.
32	D6P	Data Bit 6, Positive.
33	D6N	Data Bit 6, Negative.
34	D5P	Data Bit 5, Positive.
35	D5N	Data Bit 5, Negative.
36	DVDD18	1.8 V Digital Supply. Pin 36 supplies power to the digital core, digital data ports, serial port input/output pins, RESET, IRQ1, and IRQ2.
37	D4P	Data Bit 4, Positive.
38	D4N	Data Bit 4, Negative.
39	D3P	Data Bit 3, Positive.
40	D3N	Data Bit 3, Negative.
41	D2P	Data Bit 2, Positive.
42	D2N	Data Bit 2, Negative.
43	DVDD18	1.8 V Digital Supply. Pin 43 supplies power to the digital core, digital data ports, serial port input/output pins, RESET, IRQ1, and IRQ2.
44	D1P	Data Bit 1, Positive.
45	D1N	Data Bit 1, Negative.
46	D0P	Data Bit 0, Positive.
47	D0N	Data Bit 0, Negative.
48	DVDD18	1.8 V Digital Supply. Pin 48 supplies power to the digital core, digital data ports, serial port input/output pins, RESET, IRQ1, and IRQ2.
49	DVDD18	1.8 V Digital Supply. Pin 49 supplies power to the digital core, digital data ports, serial port input/output pins, RESET, IRQ1, and IRQ2.
50	$\overline{\text{IRQ2}}$	Second Interrupt Request. Open-drain, active low output. Connect an external pull-up to DVDD18 through a 10 kΩ resistor.
51	$\overline{\text{IRQ1}}$	First Interrupt Request. Open-drain, active low output. Connect an external pull-up to DVDD18 through a 10 kΩ resistor.
52	SDIO	Serial Port Data Input/Output. CMOS levels with respect to DVDD18.
53	SCLK	Serial Port Clock Input. CMOS levels with respect to DVDD18.
54	$\overline{\text{CS}}$	Serial Port Chip Select. Active low (CMOS levels with respect to DVDD18).
55	AVDD33	3.3 V Analog Supply.
56	IOUT2P	QDAC Positive Current Output.
57	IOUT2N	QDAC Negative Current Output.
58	AVDD33	3.3 V Analog Supply.
59	CVDD18	1.8 V Clock Supply. Supplies clock receivers and clock distribution.
60	CVDD18	1.8 V Clock Supply. Supplies clock receivers and clock distribution.
61	DACCLKN	DAC Clock Input, Negative.
62	DACCLKP	DAC Clock Input, Positive.
63	CVDD18	1.8 V Clock Supply. Supplies clock receivers and clock distribution.
64	CVDD18	1.8 V Clock Supply. Supplies clock receivers and clock distribution.
65	AVDD33	3.3 V Analog Supply.
66	IOUT1N	IDAC Negative Current Output.
67	IOUT1P	IDAC Positive Current Output.
68	AVDD33	3.3 V Analog Supply.
69	FSADJ	Full-Scale Current Output Adjust. Place a 10 kΩ resistor from this pin to GND.
70	VREF	Voltage Reference. Nominally 1.2 V output. Decouple VREF to GND.

Pin No.	Mnemonic	Description
71	CVDD18	1.8 V Clock Supply. Pin 71 supplies the clock receivers, clock multiplier, and clock distribution.
72	CVDD18	1.8 V Clock Supply. Pin 72 supplies the clock receivers, clock multiplier, and clock distribution.
	EPAD	Exposed Pad. The exposed pad (EPAD) must be soldered to the ground plane (AVSS, DVSS, CVSS). The EPAD provides an electrical, thermal, and mechanical connection to the board.

TYPICAL PERFORMANCE CHARACTERISTICS

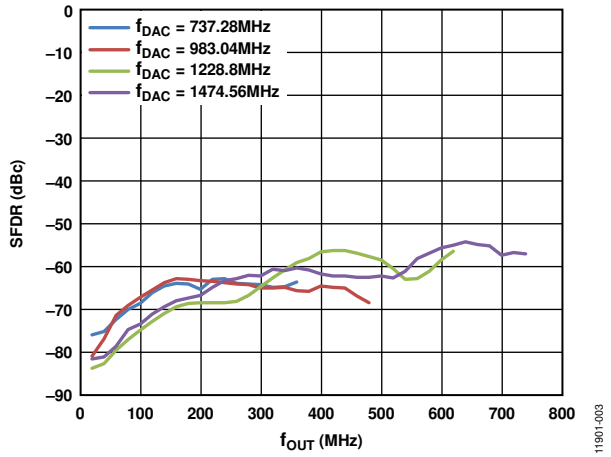

Figure 3. Single Tone (0 dBFS) SFDR vs. f_{OUT} in the First Nyquist Zone over f_{DAC}

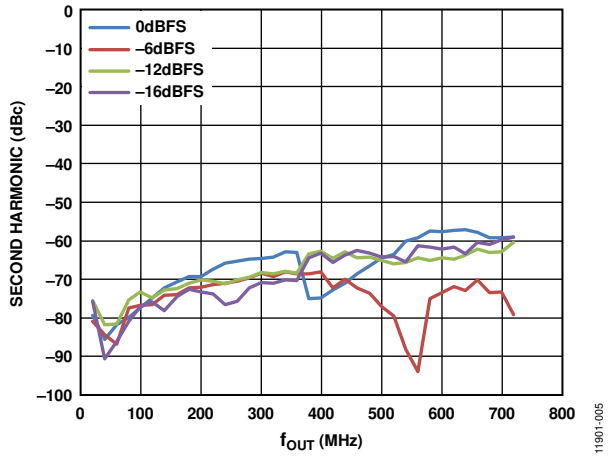

Figure 4. Single Tone Second Harmonic vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 1474.56 MHz

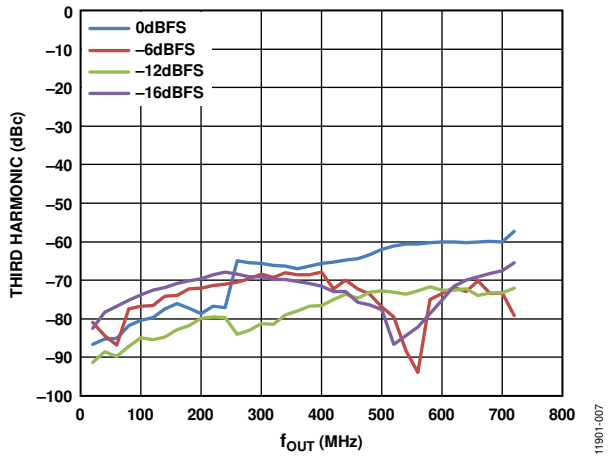

Figure 5. Single Tone Third Harmonic vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 1474.56 MHz

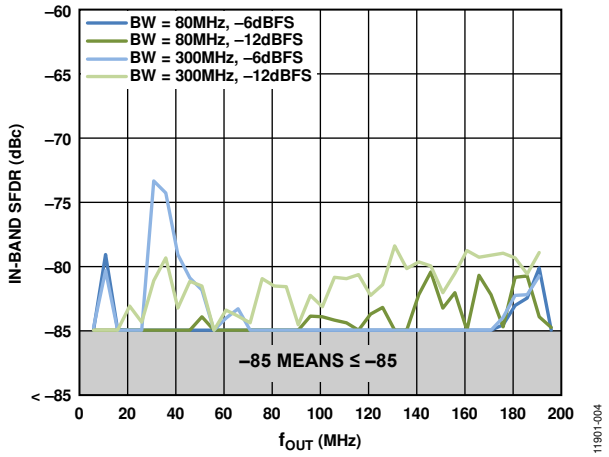

Figure 6. In-Band, Single Tone SFDR (Excluding Second Harmonic) vs. f_{OUT} in 80 MHz and 300 MHz Bandwidths, f_{DAC} = 737.28 MHz

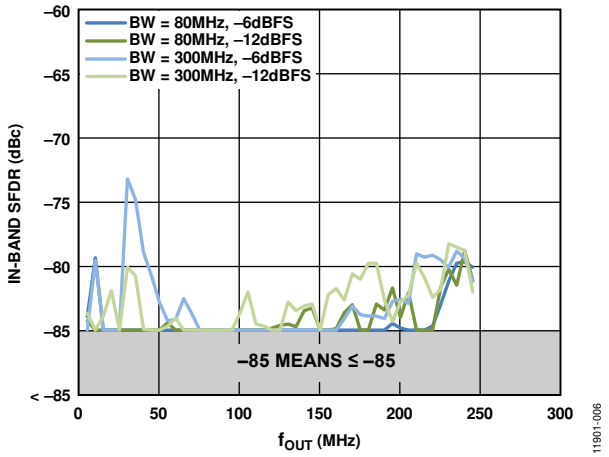

Figure 7. In-Band, Single Tone SFDR (Excluding Second Harmonic) vs. f_{OUT} in 80 MHz and 300 MHz BW, f_{DAC} = 983.04 MHz

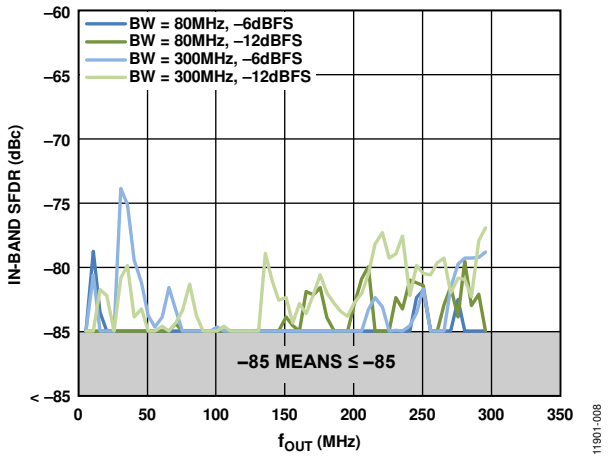

Figure 8. In-Band, Single Tone SFDR (Excluding Second Harmonic) vs. f_{OUT} in 80 MHz and 300 MHz Bandwidths, f_{DAC} = 1228.8 MHz

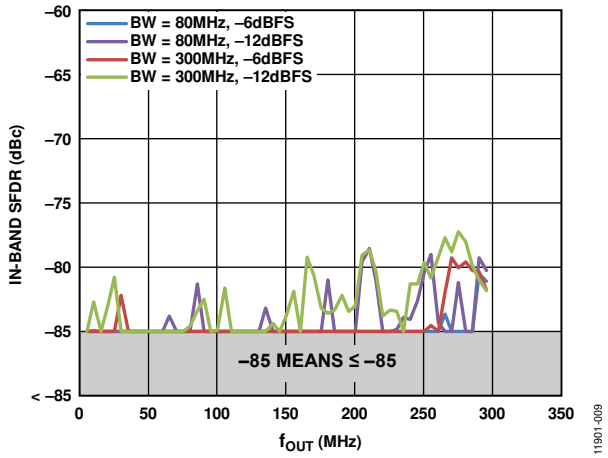

Figure 9. In-Band, Single Tone SFDR (Excluding Second Harmonic) vs. f_{OUT} in 80 MHz and 300 MHz Bandwidths, f_{DAC} = 1474.56 MHz

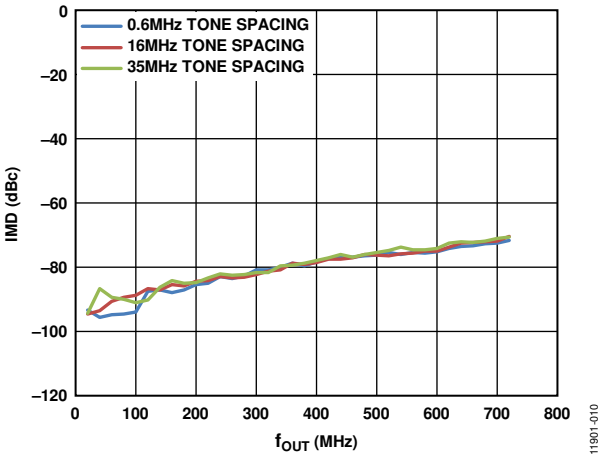

Figure 12. Two Tone, Third IMD vs. f_{OUT} over Tone Spacing, f_{DAC} = 1474.56 MHz

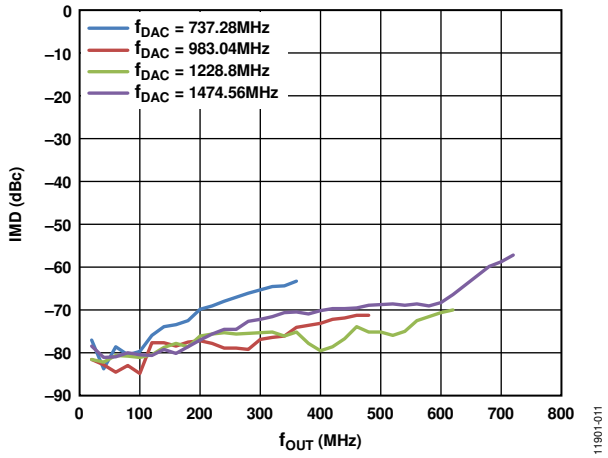

Figure 10. Two Tone, Third IMD vs. f_{OUT} over f_{DAC}

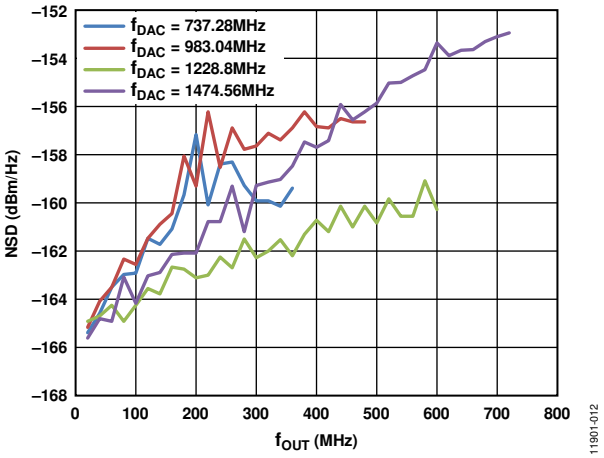

Figure 13. Single Tone (0 dBFS) NSD vs. f_{OUT} over f_{DAC}

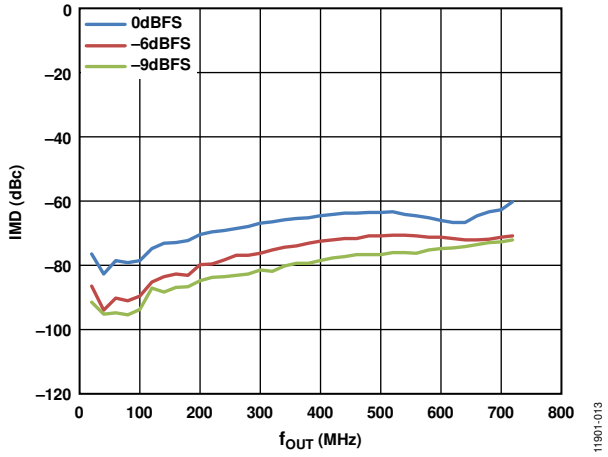

Figure 11. Two Tone, Third IMD vs. f_{OUT} over Digital Back Off, f_{DAC} = 1474.56 MHz

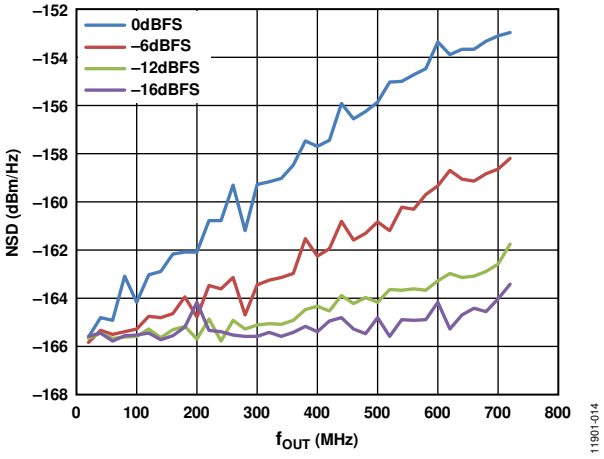

Figure 14. Single Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 1474.56 MHz

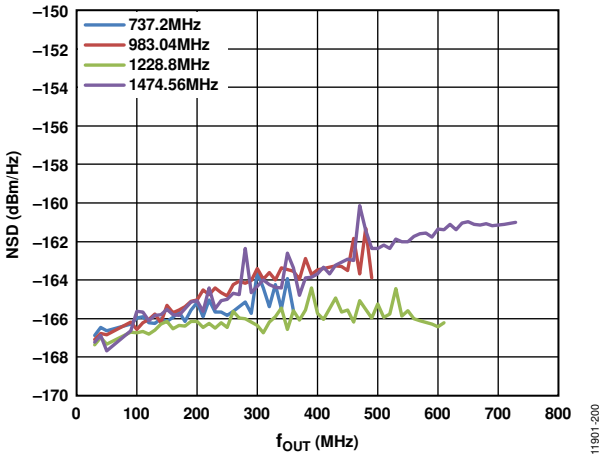

Figure 15. 1C WCDMA NSD vs. f_{OUT}, over f_{DAC}

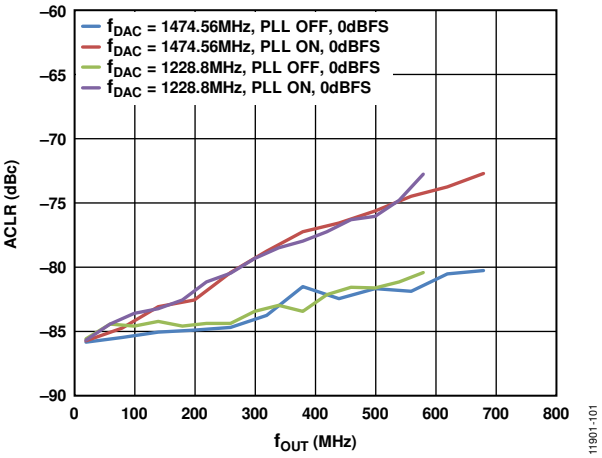

Figure 18. 1C WCDMA, Second Adjacent ACLR vs. f_{OUT}, PLL On and Off

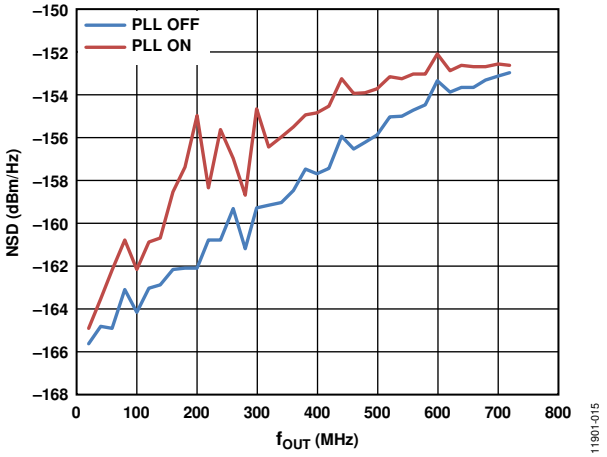

Figure 16. Single Tone NSD vs. f_{OUT}, f_{DAC} = 1474.28 MHz, PLL On and Off

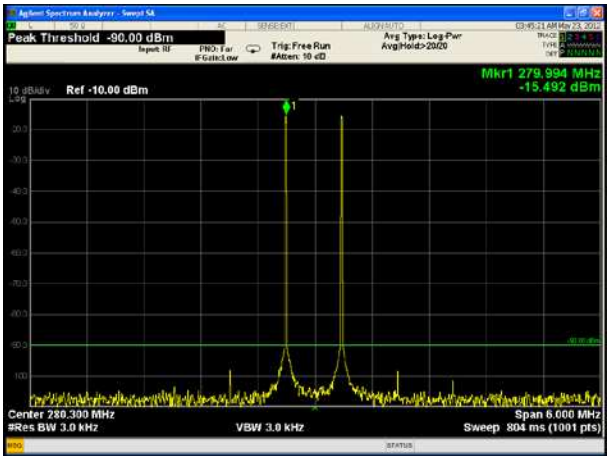

Figure 19. Two Tone, Third IMD Performance, IF = 280 MHz, f_{DAC} = 1474.28 MHz

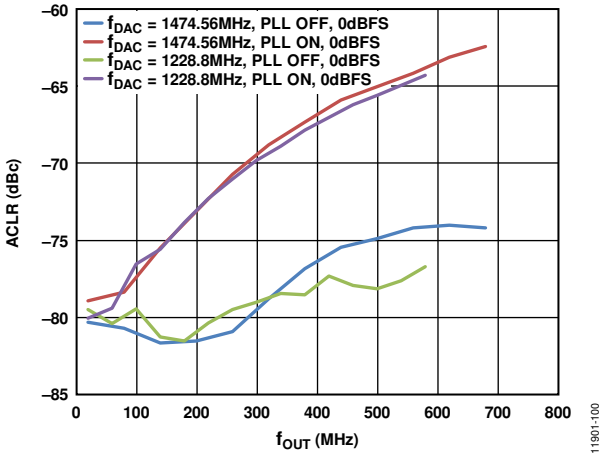

Figure 17. 1C WCDMA, First Adjacent ACLR vs. f_{OUT}, PLL On and Off

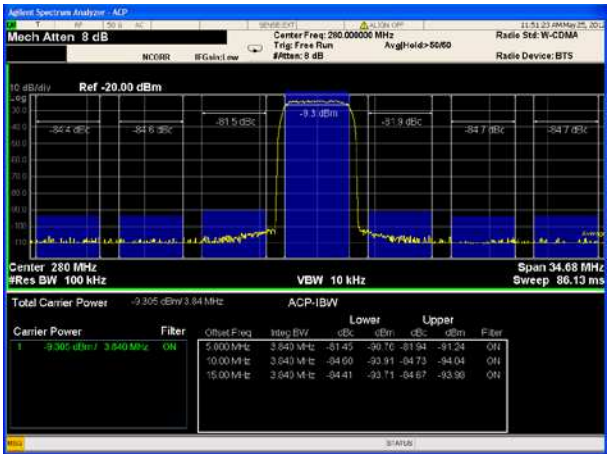

Figure 20. 1C WCDMA ACLR Performance, IF = 280 MHz, f_{DAC} = 1474.28 MHz

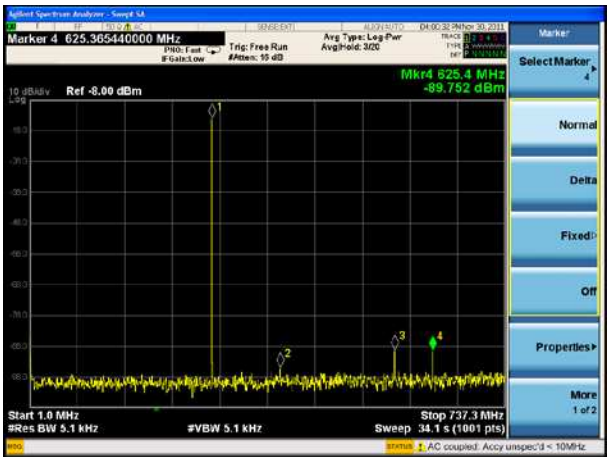

Figure 21. Single Tone f_{DAC} = 1474.56 MHz, f_{OUT} = 280 MHz, −14 dBFS

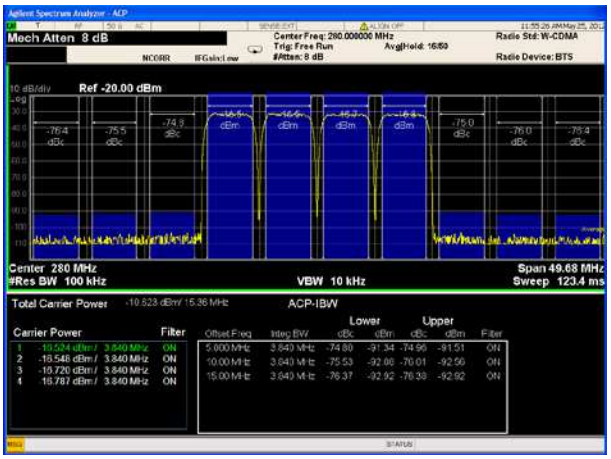

Figure 22. 4C WCDMA ACLR Performance, IF = 280 MHz, f_{DAC} = 1474.28 MHz

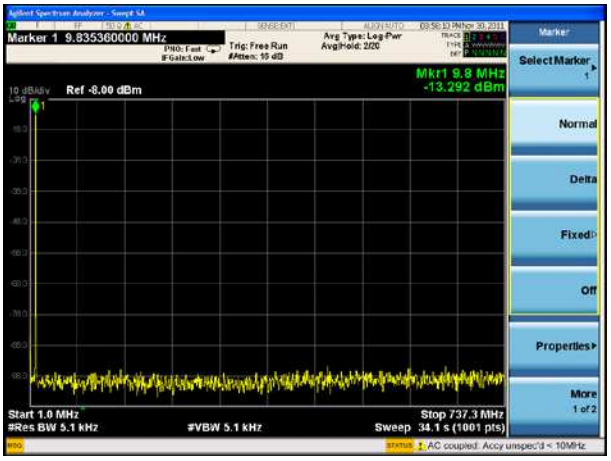

Figure 23. Single Tone SFDR f_{DAC} = 1474.56 MHz, 4× Interpolation, f_{OUT} = 10 MHz, −14 dBFS

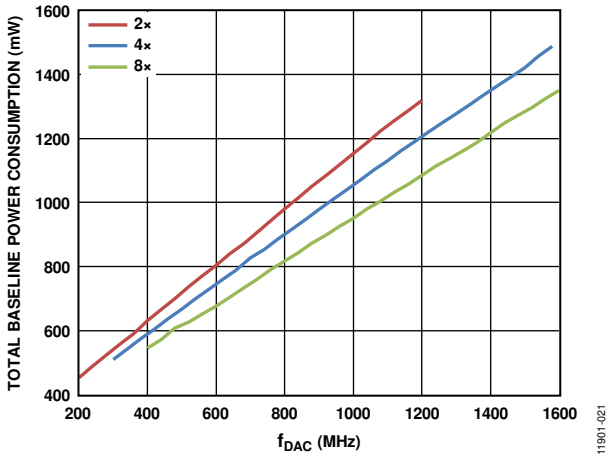

Figure 24. Total Power Baseline Consumption vs. f_{DAC} over Interpolation

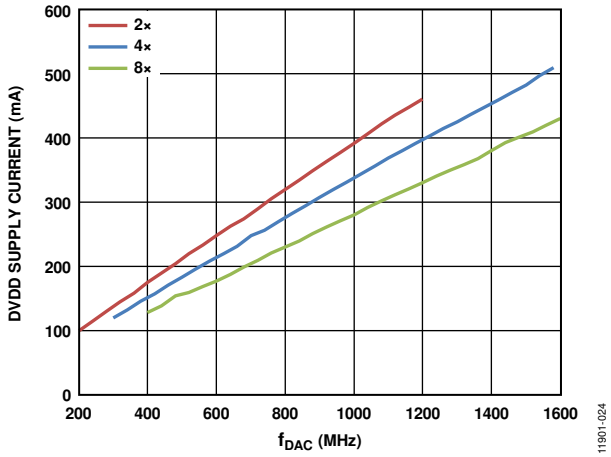

Figure 25. DVDD18 Supply Current vs. f_{DAC} over Interpolation

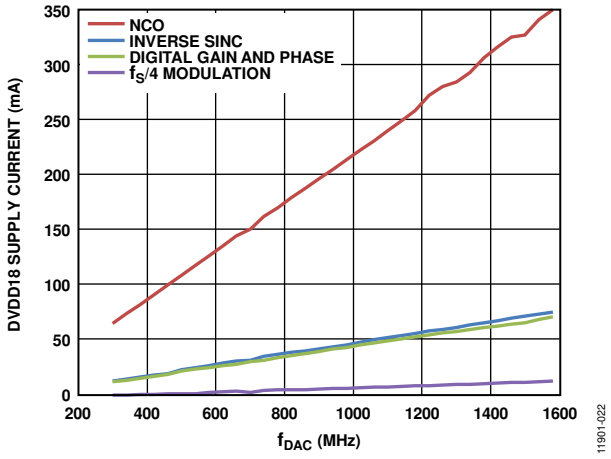

Figure 26. DVDD18 Supply Current vs. f_{DAC} over Digital Functions

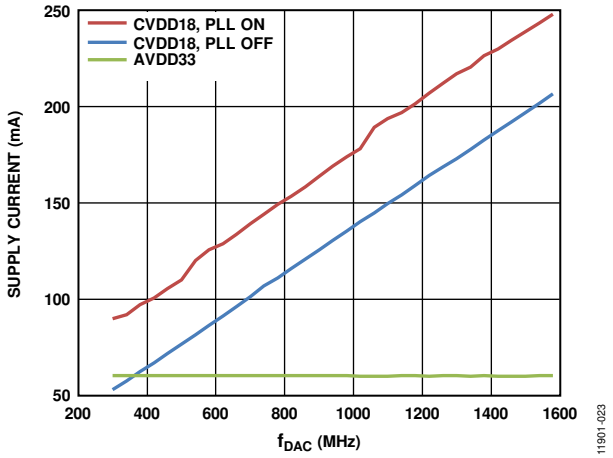

Figure 27. CVDD18, AVDD33 Supply Current vs. f_{DAC}

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error
Offset error is the deviation of the output current from the ideal of 0 mA. For IOUT1P, 0 mA output is expected when all inputs are set to 0. For IOUT1N, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range
The output compliance range is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, the interpolation filters reject energy in this band. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

SERIAL PORT OPERATION

The serial port is a flexible, synchronous serial communications port that allows easy interfacing to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola® SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9142A. MSB-first or LSB-first transfer formats are supported. The serial port interface is a 3-wire only interface. The input and output share a single pin input/output (SDIO).

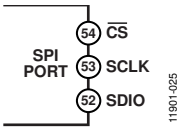

Figure 28. Serial Port Interface Pins

There are two phases to a communication cycle with the AD9142A. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first 16 SCLK rising edges. The instruction word provides the serial port controller with information regarding the data transfer cycle, Phase 2, of the communication cycle. The Phase 1 instruction word defines whether the upcoming data transfer is a read or write, along with the starting register address for the next data transfer in the cycle.

A logic high on the $\overline{CS}$ pin, followed by a logic low, resets the serial port timing to the initial state of the instruction cycle. From this state, the next 16 rising SCLK edges represent the instruction bits of the current I/O operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one data byte. Registers change immediately upon writing to the last bit of each transfer byte, except for the frequency tuning word and NCO phase offsets, which change only when the frequency tuning word (FTW) update bit is set.

DATA FORMAT

The instruction byte contains the information shown in Table 10.

Table 10. Serial Port Instruction Word

I15 (MSB)	I[14:0]
R/$\overline{W}$	A[14:0]

R/$\overline{W}$ (Bit 15 of the instruction word) determines whether a read or a write data transfer occurs after the instruction word write. Logic 1 indicates a read operation and Logic 0 indicates a write operation.

A14 to A0 (Bit 14 to Bit 0 of the instruction word) determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, A14 is the starting address; the device generates the remaining register addresses based on the SPI_LSB_FIRST bit.

SERIAL PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

$\overline{CS}$ is an active low input that starts and gates a communication cycle. It allows more than one device to be used on the same serial communications line. The SDIO pins enter a high impedance state when the $\overline{CS}$ input is high. During the communication cycle, $\overline{CS}$ should stay low.

Serial Data I/O (SDIO)

The SDIO pin is a bidirectional data line.

SERIAL PORT OPTIONS

The serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by the SPI_LSB_FIRST bit (Register 0x00, Bit 6). The default is MSB first (LSB_FIRST = 0).

When SPI_LSB_FIRST = 0 (MSB first), the instruction and data bits must be written from MSB to LSB. Multibyte data transfers in MSB-first format start with an instruction word that includes the register address of the most significant data byte. Subsequent data bytes must follow from high address to low address. In MSB-first mode, the serial port internal word address generator decrements for each data byte of the multibyte communication cycle.

When SPI_LSB_FIRST = 1 (LSB first), the instruction and data bits must be written from LSB to MSB. Multibyte data transfers in LSB-first format start with an instruction word that includes the register address of the least significant data byte. Subsequent data bytes must follow from low address to high address. In LSB-first mode, the serial port internal word address generator increments for each data byte of the multibyte communication cycle.

If the MSB-first mode is active, the serial port controller data address decrements from the data address written toward 0x00 for multibyte I/O operations. If the LSB-first mode is active, the serial port controller data address increments from the data address written toward 0xFF for multibyte I/O operations.

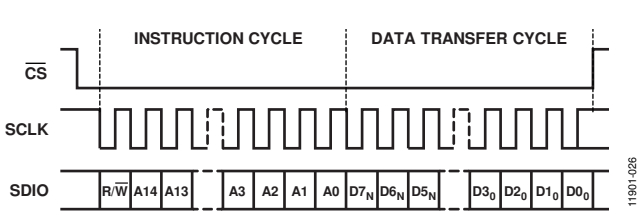

Figure 29. Serial Register Interface Timing, MSB First

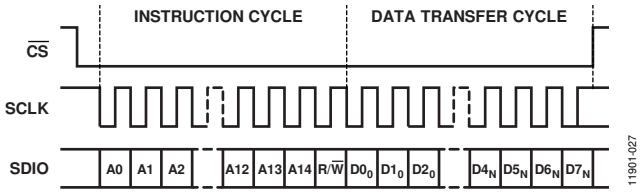

Figure 30. Serial Register Interface Timing, LSB First

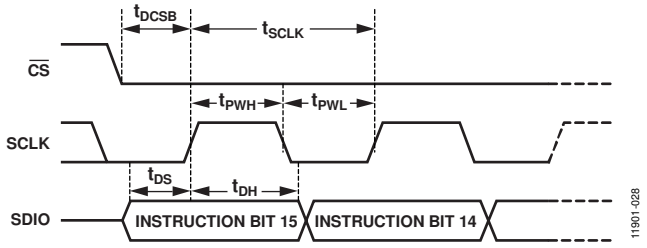

Figure 31. Timing Diagram for Serial Port Register Write

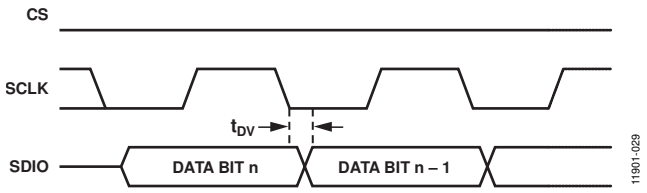

Figure 32. Timing Diagram for Serial Port Register Read

DATA INTERFACE

LVDS INPUT DATA PORTS

The AD9142A has a 16-bit LVDS bus that accepts 16-bit I and Q data either in word (16-bit) or byte (8-bit) formats. In the word interface mode, the data is sent over the entire 16-bit data bus. In the byte interface mode, the data is sent over the lower 8-bit (D7 to D0) LVDS bus. Table 11 lists the pin assignment of the bus and the SPI register configuration for each mode.

Table 11. LVDS Input Data Modes

Interface Mode	Pin Assignment	SPI Register Configuration
Word	D15 to D0	Register 0x26, Bit 0 = 0
Byte	D7 to D0	Register 0x26, Bit 0 = 1

WORD INTERFACE MODE

In word interface mode, the digital clock input (DCI) signal is a reference bit that generates a double data rate (DDR) data sampling clock. Time align the DCI signal with the data. The IDAC data follows the rising edge of the DCI, and the QDAC data follows the falling edge of the DCI, as shown in Figure 33.

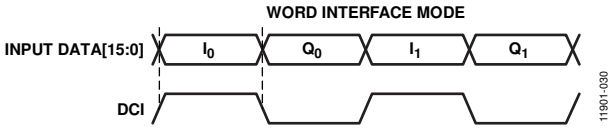

Figure 33. Timing Diagram for Word Interface Mode

BYTE INTERFACE MODE

In byte interface mode, the required sequence of the input data stream is I[15:8], I[7:0], Q[15:8], Q[7:0]. A frame signal is required to align the order of input data bytes properly. Time align both the DCI signal and frame signal with the data. The rising edge of the frame indicates the start of the sequence. The frame can be either a one shot or periodical signal as long as its first rising edge is correctly captured by the device. For a one shot frame, the frame pulse must be held at high for at least one DCI cycle. For a periodical frame, the frequency needs to be

$$f_{DCI}/(2 \times n)$$

where n is a positive integer, that is, 1, 2, 3, …

Figure 34 is an example of signal timing in byte mode.

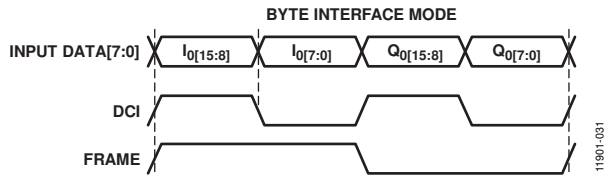

Figure 34. Timing Diagram for Byte Interface Mode

DATA INTERFACE CONFIGURATION OPTIONS

To provide more flexibility for the data interface, some additional options are listed in Table 12.

Table 12. Data Interface Configuration Options

Register 0x26	Description
DATA_FORMAT (Bit 7)	Select between binary and twos complement formats.
DATA_PAIRING (Bit 6)	Indicate I/Q data pairing on data input. This allows the I and Q data that is received to be paired in various ways.
DATA_BUS_INVERT (Bit 5)	Swaps the bit order of the data input port. Remaps the input data from D[15:0] to D[0:15].

DLL INTERFACE MODE

A source synchronous LVDS interface is used between the data host and AD9142A to achieve high data rates while simplifying the interface. The FPGA or ASIC feeds the AD9142A with 16-bit input data. Along with the input data, the FPGA or ASIC provides a DDR (double data rate) data clock input (DCI).

A delay locked loop (DLL) circuit designed to operate with DCI clock rates between 250 and 575 MHz is used to generate a phase-shifted version of the DCI, called DSC (data sampling clock), to register the input data on both the rising and falling edges.

As shown in Figure 35, the DCI clock edges must be coincident with the data bit transitions with minimum skew and jitter. The nominal sampling point of the input data occurs in the middle of the DCI clock edges because this point corresponds to the center of the data eye. This is also equivalent to a nominal phase shift of 90°of the DCI clock.

The data timing requirements are defined by a data valid window (DVW) that is dependent on the data clock input skew, input data jitter, and the variations of the DLL delay line across delay settings. The DVW is defined as

$$DVW = t_{DATA\ PERIOD} - t_{DATA\ SKEW} - t_{DATA\ JITTER}$$

The available margin for data interface timing is given by

$$t_{MARGIN} = DVW - (t_S + t_H)$$

The difference between the setup and hold times, which is also called the keep out window, or KOW, is the area where data transitions should not happen. The timing margin allows tuning of the DLL delay setting by the user, see Figure 36.

From the figure, it can be seen that the ideal location for the DSC signal is 90° out of phase from the DCI input. However, due to skew of the DCI relative to the data, it may be necessary to change the DSC phase offset to sample the data at the center of its eye diagram. The sampling instance can be varied in discrete increments by offsetting the nominal DLL phase shift value of 90° via Register 0x0A, Bits[3:0]. This register is a signed value. The MSB is the sign and the LSBs are the magnitude. The following equation defines the phase offset relationship:

$$Phase\ Offset = 90° \pm n \times 11.25°,\ |n| < 7$$

where n is the DLL phase offset setting.

Figure 35 shows the DSC setup and hold times with respect to the DCI signal and data signals.

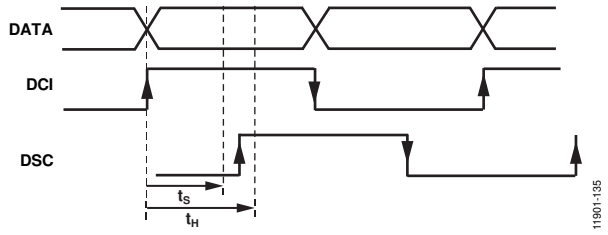

Figure 35. LVDS Data Port Setup and Hold Times

Table 13 lists the values that are guaranteed over the operating conditions. These values were taken with a 50% duty cycle and a DCI swing of 450 mV p-p. For best performance, the duty cycle variation should be kept below ±5%, and the DCI input should be as high as possible, up to 1200 mV p-p.

Table 13. DLL Phase Setup and Hold Times (Guaranteed)

Frequency, f_{DCI} (MHz)	Time (ps)	Data Port Setup and Hold Times (ps) at DLL Phase		
		−3	0	+3
307	t_S	−125	−385	−695
	t_H	834	1120	1417
368	t_S	−70	−305	−534
	t_H	753	967	1207
491	t_S	−81	−245	−402
	t_H	601	762	928

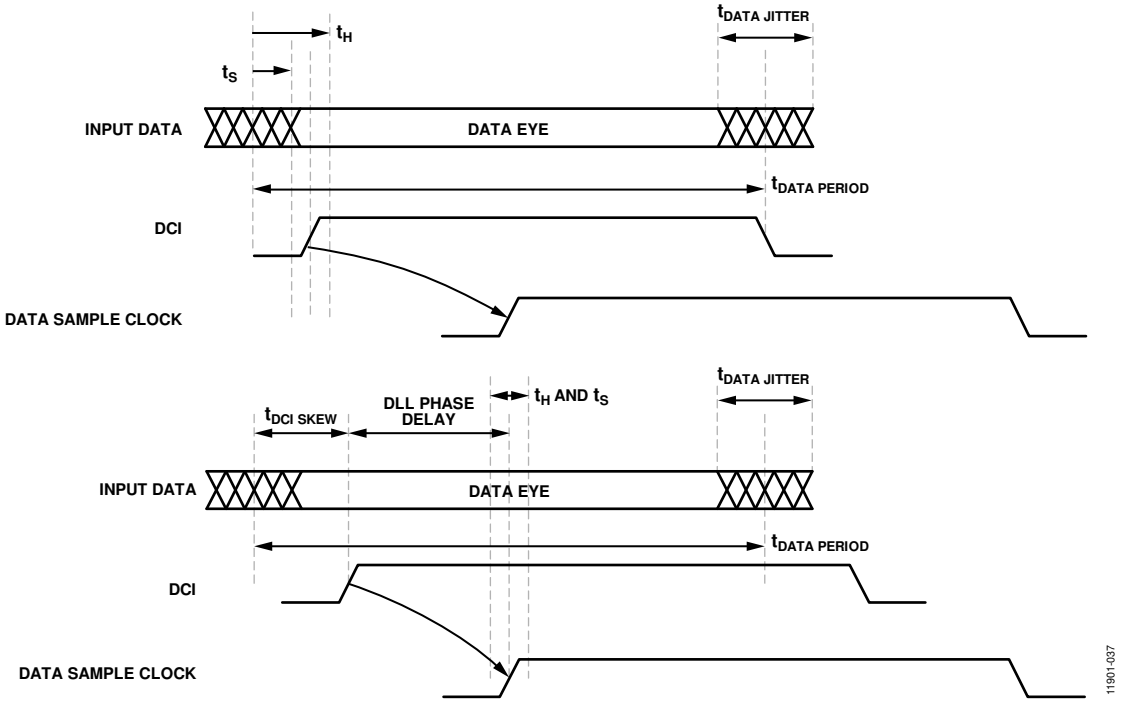

Figure 36. LVDS Data Port Timing Requirements