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AD9146-EBZ
Quick Start Guide

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Getting Started with the AD9146-EBZ Evaluation Board

WHAT'S IN THE BOX

AD9146-EBZ Evaluation Board
Evaluation Board CD
Mini-USB Cable

RECOMMENDED EQUIPMENT

Sinusoidal Clock Source
Spectrum Analyzer
Data Pattern Generator Series 2 (DPG2)

INTRODUCTION

The AD9146-EBZ Evaluation Board pairs up to a DPG2 to quickly evaluate the AD9146. The SPI port is controlled through USB along with the included PC software used to configure the AD9146 with desired settings for evaluation.

Additionally, a clock distribution chip (AD9516) and quadrature modulator (ADL5375-05) are included on this evaluation board to facilitate the subsystem evaluation.

SOFTWARE

The AD9146-EBZ receives data from a Data Pattern Generator 2 (DPG2). The DAC Software Suite with the AD9146 Update, included on the Evaluation Board CD or online at http://www.analog.com/dpg, is needed for evaluation. The DPGDownloader program will install to allow for easy loading and playing of vectors into the DPG2. The AD9146 SPI application is also included for communication with the part.

HARDWARE SETUP

Connect a +5.0V DC power supply to the banana jacks (P5 and P6). A clock source signal generator should be connected to the SMA connector J1 (AD9516_CLKIN). This is the clock supply for the clock distribution chip to provide both DAC clocks and DPG2 DCO signals to properly clock the part. The DPG2 connects to the connector (P1 & P2) along the left side of the board, and the USB cable connects the PC computer to the mini-USB connector (XP2 USB) along the bottom edge of the board. **Note the PC software must be installed before connecting the USB cable to the computer.**

This evaluation board allows evaluation of both the DAC IF outputs as well as the modulator RF outputs. By default, the solder jumpers are configured to look at the DAC output. Below is a table listing the jumper configurations and SMA connector connections needed to view either output on a spectrum analyzer.

JUMPERS

Table 1: Evaluation Board Output Path Configurations

Output Viewed	*SMA Connector*	*Jumper Configurations*
I DAC Output (P-side)	J5 ("IOUT")	JP4 & JP5 Pins 2-3 (outer pads)
Q DAC Output (P-side)	J9 ("QOUT")	JP6 & JP7 Pins 2-3 (outer pads)

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Quadrature Modulator RF Output*	J6 (“MOD_OUT”)	JP4 & JP5 Pins 1-2 (inner pads) JP6 & JP7 Pins 1-2 (inner pads)

*When viewing the modulator output, a local oscillator (LO) must be connected to J15 (”LO_IN”) to properly modulate the signals.

POWER SUPPLIES

The AD9146-EBZ has five two-pin jumpers for each of the different power supplies on the board. By default, all of these jumpers should be populated and their respective supplies are listed in the table below and the locations shown in red in **Figure 1**.

Table 2: Power Supply Jumpers

Power Supply	*Pin Jumper*
DVDD 1.8V Supply (DUT Digital Supply)	JP3
XCVDD 3.3V Supply (Clock Chip Supply)	JP9
CVDD 1.8V Supply (DUT Clock Supply)	JP2
AVDD 3.3V Supply (DUT Analog Supply)	JP8
5V Modulator Supply	JP11

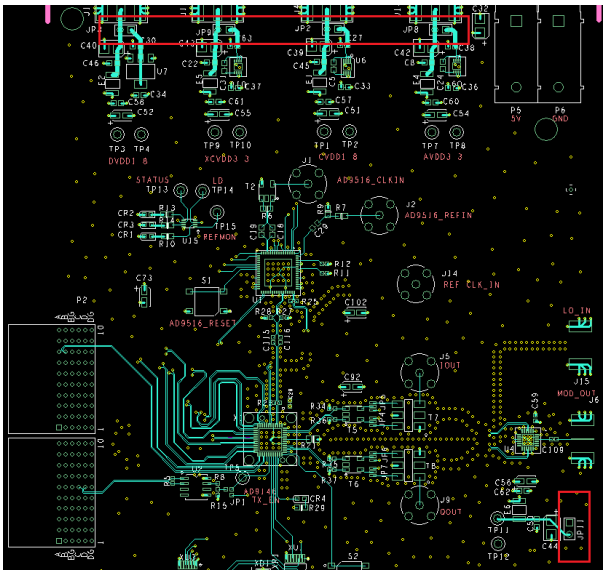

Figure 1: Power Supply Jumper Locations

OUTPUT CONFIGURATIONS

This evaluation board has four three-pad solder jumpers on the top of the board, two for each DAC (P and N side each). These solder jumpers, JP4-JP7, are used to choose between viewing the DAC output or the modulator output. As mentioned previously, by default the jumpers are configured for viewing the DAC output (outer pads soldered). For the modulator, the inner pads should be soldered, which jumps to the back of the evaluation board for the modulator path. These traces go through a 5th-order Butterworth filter before entering the modulator inputs. These different options and configurations are listed in the previous section in Table 1 and shown in red below in **Figure 2** and **Figure 3**.

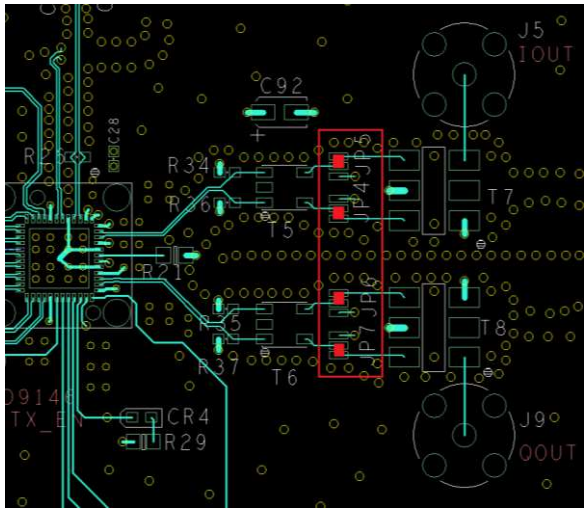

Figure 2: DAC Output Solder Jumper Configuration

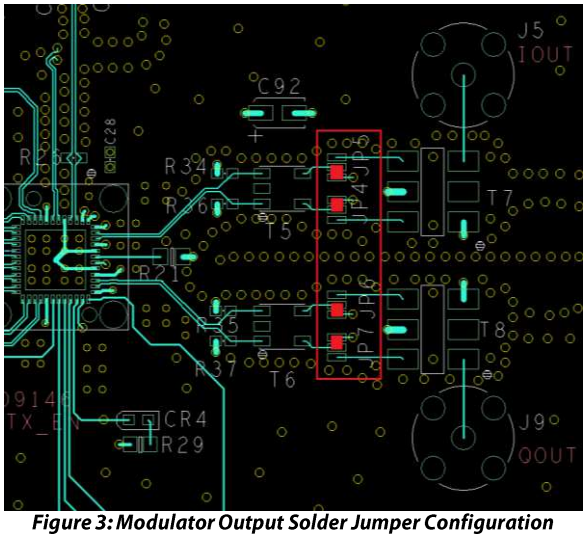

Figure 3: Modulator Output Solder Jumper Configuration

REFERENCE CLOCK

The AD9146 has an on-chip PLL that uses the SYNCP/SYNCN pins to supply the reference clock to the chip. The AD9146-EBZ evaluation board allows the option to supply this clock either from the AD9516 clock chip or from an additional external signal generator by connecting to J14 ("REF CLK_IN"). Solder jumpers JP10 and JP15 on the back of the board can be changed according to the desired option. Connecting the inner pads selects the option to use the AD9516 by default (**Figure 4**), whereas soldering the outer pads chooses the external option to drive from a sine source (**Figure 5**).

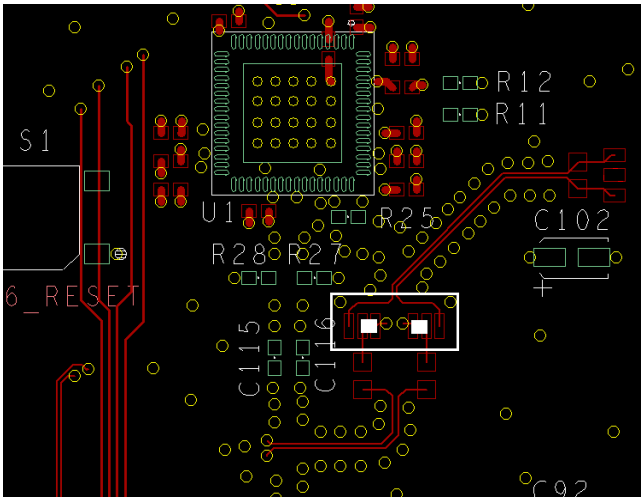

Figure 4: AD9516 Reference Clock Jumper Configuration

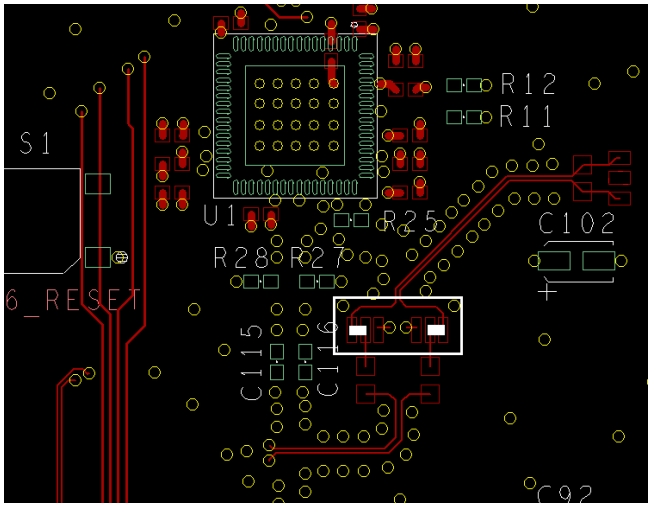

Figure 5: External Reference Clock Jumper Configuration

TX ENABLE

The AD9146 product has a TX Enable feature (active low) that allows the user to toggle the level of the TX enable pin to control when the DACs are transmitting and when the outputs are clamped to mid-scale and stop passing data through. The evaluation board allows for control of this through the DPGDownloader or by forcing a voltage on the pin via a test point. By default, this pin is set by the DPG2 and JP1 should be connected horizontally, as shown in Figure 6. To drive the pin manually via TP5 ("AD9146 TX_EN"), leave the jumper unsoldered. A description of how to use the TX Enable control via the DPG2 is given in a later section.

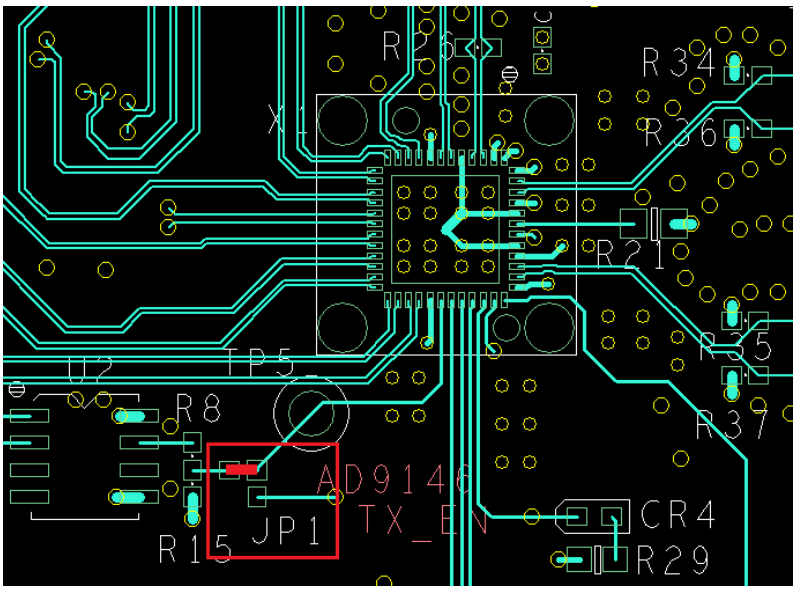

Figure 6: TX Enable to DPG Jumper Configuration

GETTING STARTED

Single-Tone Test

These settings configure the AD9146 to output a sine wave using the DPG2 and allows the user to view the single-tone AC performance of the DAC output (or modulator output depending on jumper settings).

Procedure:

- Install the software as described in the *Software Setup* section above.
- Connect all necessary cables to the evaluation board as listed in the *Hardware Setup* section above. Turn on the power supply and reset the part by pressing the *DUT_Reset* pushbutton (S2).
- Set the clock signal generator to output a 500MHz tone at 0dB.
- Open the AD9146 SPI application via the button available on the DPGDownloader.
    - Select the 2nd tab and choose "2x Interpolation" from the drop-down menu and check that the "Run Clock Chip" button is selected. Run the controller by clicking on the arrow ( ) at the top of the window.
- With a 500MHz sampling rate and 2x interpolation selected, the real data rate is 250MHz. However since this part runs in byte mode, the necessary clocking frequency to clock in the data is twice the data rate. Therefore, the DPGDownloader *DCO Frequency* readback should read ~500MHz. The "Evaluation Board" dropdown menu should reflect that the board was recognized and automatically displays *AD9146* when the USB cable is connected.
- To load and play a single-tone vector, select the "Add Generated Waveform" drop-down menu at the top of the DPGDownloader program and choose "Single Tone".
    - Set the *Sample Rate* to 250MHz, *Desired Frequency* to 21MHz, check the *Generate Complex Data (I&Q)*, and uncheck the *Unsigned Data* checkbox to select 2's compliment data format.
    - Select the "1I: Single-Tone…" vector from the *I Data Vector* drop-down menu, and choose "1Q: Single-Tone.." vector from the *Q Data Vector* menu.
    - Choose "Byte Mode" from the *Data* Width drop-down menu and "DCI/16" from the *Frame* Sync drop-down menu.
    - Click Download ( ) and Play ( ).
- The spectrum should display a 21MHz single-tone (or f_{LO}±21MHz single-tone depending on the sideband select setting if using the modulator and LO), as show in the figures below. The current on the 5V supply should read about 663mA (854mA with the modulator).

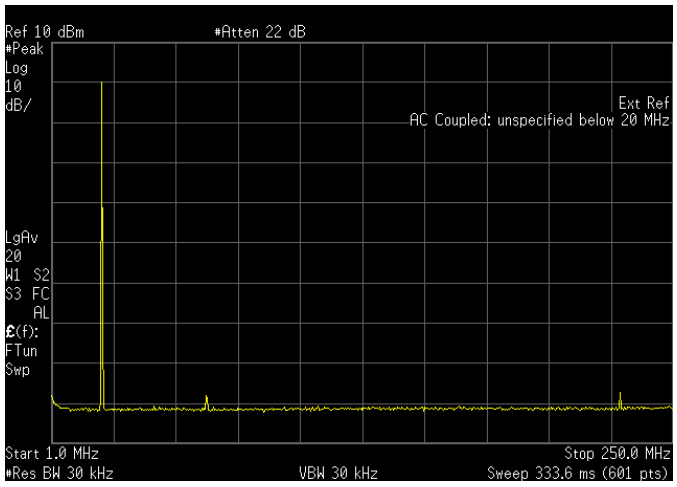

Figure 7: Single-Tone Test Spectrum at DAC Output

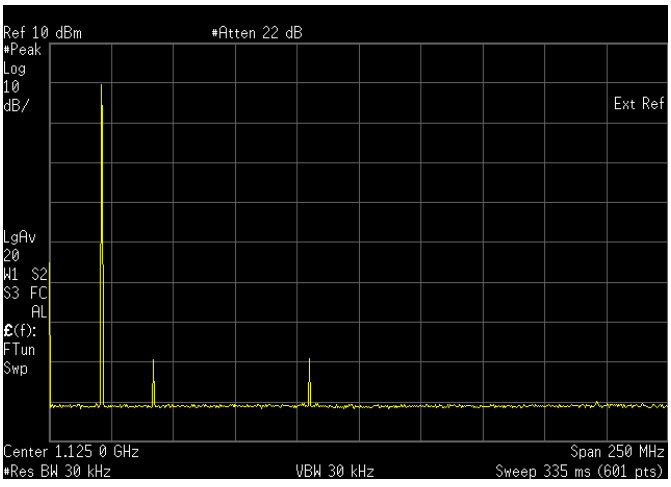

Figure 8: Single-Tone Test Spectrum at Modulator Output (f_{LO}=1GHz, Upper-Sideband Selected)

DPG2 TX ENABLE CONTROL

The TX Enable pin can be controlled with the DPG by enabling the checkbox and clicking on the "TX ENABLE Waveform Designer", both shown in **Figure 9**. The Waveform Designer window will pop up and allow the user to enter in transitions as desired based on the data being inputted. If a vector is loaded and padded so that it allows for time to have the DAC transmit and then stop transmitting using the TX Enable pin, this can be detected by the waveform designer by clicking the "Auto-Detect" button in this window. This will automatically create a signal for the TX Enable based on when transmission is desired and when the DAC can be turned off.

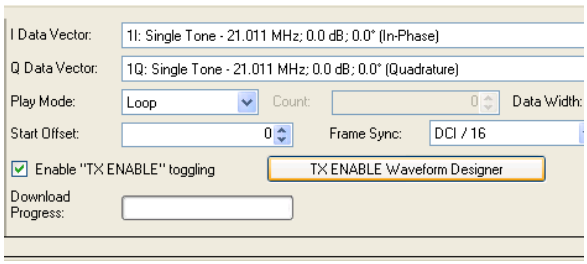

Figure 9: DPGDownloader Panel, TX Enable Section

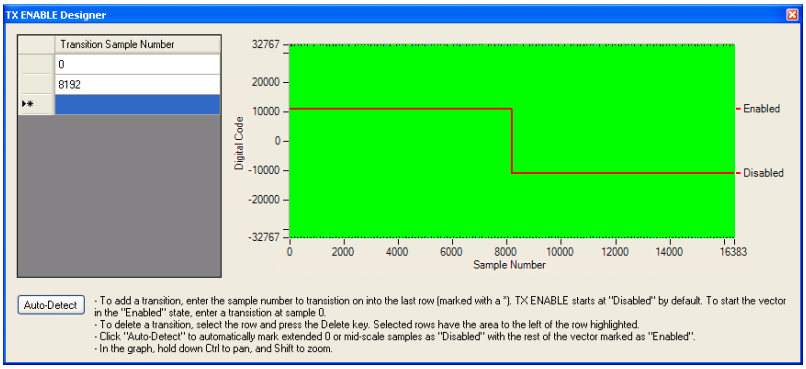

Figure 10: TX Enable Waveform Designer Window

SPI APPLICATION

The SPI application is separated into multiple tabs relating to the different functionality controls of the part. Most of the controls are described in this section as each relate to the evaluation board. For a complete list and description of all the control registers, refer to the AD9146 Datasheet, also included in the software package and available through its respective button in the DPGDownloader.

Running the SPI Application

To execute the SPI application with its current settings, click the "Run" arrow ( ) and all of the selected functions will be written to the part once. To perform writes to the part continuously, click the "Run Continuously" button ( ); to stop, click the "Run Continuously" button again to allow for the controller to properly finish the last write and close the communication. If only a readback is desired, click the *Read Only* button, shown in **Figure 11**, before selecting the "Run" arrow. This will only execute a readback of the current settings. The indicators next to the controls will read back the selections as well as the *SPI Map* tab will be updated with the current SPI settings. When writing to the clock chip is desired, the *Run Clock Chip* button should be pressed (shown in **Figure 12**); turning this button off will not execute any write commands to the AD9516 and settings will not be changed.

Figure 11: Readback Only

Figure 12: Run AD9516 Clock Chip

Data Clock Control

This section, shown in Figure 13, controls the Interpolation Rate and Coarse Modulation. The *Modulation Description* field will readback the controls selected. Additionally, the individual half-band filter stages will also update in the respective fields. If an improper selection of these controls is chosen, the *Modulation Description* indicator will read *Invalid*. By default, the AD9516 will automatically update the proper dividers for the clocks based on the chosen interpolation from the drop-down menu. To disable this feature, select the *AD9516* tab and uncheck the *Sync with Interpolation* box near the *Data Clock* controls.

An advanced filter control option is available to manually control the stages of each of the filters. To access this, the *Enable Advanced Filter Control* should be turned on. Each of the half-band filters are turned on by their respective enable controls, and the modes for each filter are set in the corresponding field selections. Note that if the *Sync with Interpolation* checkbox is selected, the clock dividers will still be updated according to the interpolation rate selected from the menu, even when using the advanced control.

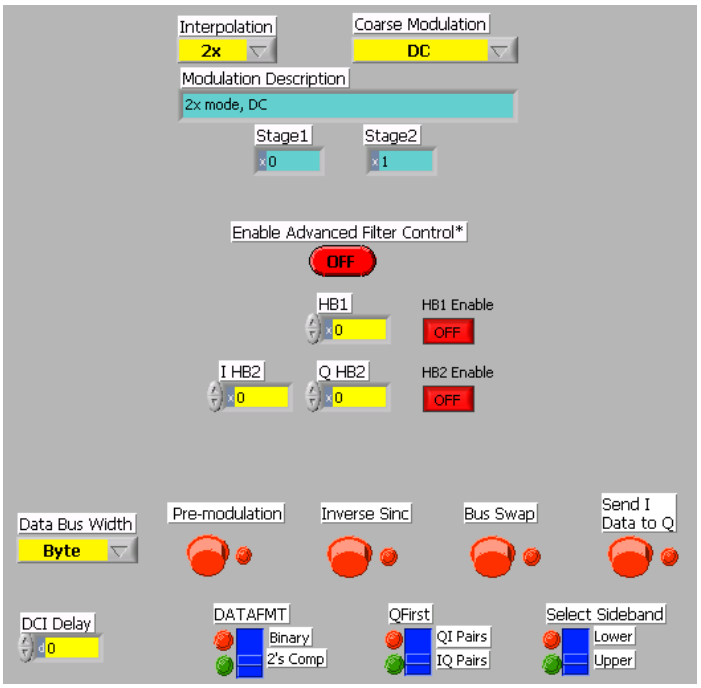

Figure 13: Data Clock Controls

The interface control section of Figure 13 allows for easy control of the different features of the AD9146. *DataFMT* controls the number format for the incoming data with a choice between unsigned/binary and signed/2's complement. *Inverse Sinc* is used to obtain flatness across the band and to counter the sinc roll-off effect. The *QFirst* control is available to swap whether the I or Q data is transmitted first. The *Send I Data to Q* sends the same data being fed to the I DAC to the Q DAC as well. The supported *Data Bus Width* for this part is "Byte" (8-bits) and "Nibble" (4-bits) and the DPGDownloader panel *Interface Mode* and necessary *Frame* signal must be set to the corresponding modes for proper execution. The clock chip divider will update appropriately to set the necessary DCO and DAC clock signals if *Sync With Interpolation* is selected (*AD9516* tab). For example, for 4x interpolation using byte mode, the *DCO Clk Div Ratio* is set to "Divide-by-2" and the *DAC Clk Div Ratio* is set to "Bypass". However, for 4x interpolation using nibble mode, the *DCO Clk Div Ratio* should be set to "Bypass", and the same for *DAC Clk Div Ratio*. Note that the *Bus Swap* control is not supported with the DPG2.

PLL Control

The AD9146 has an on-chip PLL. When *PLL_Enable* is turned on, the PLL starts an auto-search mode to determine the best PLL band to use, including over temperature, based on the *Divider1* and *Divider0* values. This tab calculates the DAC frequency and VCO frequency based on the *Reference Clock* value and the dividers being set. For proper and stable locking of the PLL, the VCO frequency should be within the 1GHz to 2GHz range. To override the auto-band search, enable the *PLL_Manual* button and enter the desired band for the conditions used, in addition to having the proper divider settings. To ensure that the PLL locks properly, the recommended startup sequence is to enable the PLL in manual mode first (*PLL_Enable* and *PLL_Manual* are set; the band setting is not important). Then disable *PLL_Manual* to start the auto-search mode for the PLL and the lock indicators should show a lock has been achieved.

Interrupts

This tab provides a visual indication of the state of each interrupt. Enabling the button to the left of each interrupt with enable the interrupt. A green indicator to the right of the button will light when the interrupt is asserted. Once asserted, the interrupt can be acknowledged by pressing the *Clear* button.

Main DAC Control

This tab controls the two main DACs in the AD9146. The Full-Scale Current of each DAC can be set with the *I DAC Gain* and *Q DAC Gain* controls. The *I Sleep* and *Q Sleep* controls put their respective DAC into a low-power sleep state. When the AD9146 is used with a modulator, the *Phase Compensation/DC Offset* controls can be used to correct any mismatches between the two DACs.

AUX DAC Control

As with the main DACs, the full-scale current of the auxiliary DACs can be set over the SPI port. Each DAC can also be powered down as well as providing the option to source or sink the current for either the P-side or N-side.

Sample Error Detection

The Sampling Error Detection (SED) checks the data inputs. An 8-byte signature is handed to the AD9146. The controller can automatically generate and load the vectors using the DPG2 device. Indicators display the result of the comparison between the input data and the expected signature, noting which of the bits contain the errors.

SPI Map

The SPI Map tab provides an overview of all the settings currently written to the part. The individual register values are indicated graphically (with red and green boxes) and numerically. The numeric results can be used in whatever system the AD9146 connects to, to duplicate the current settings in the end system.

AD9516 Control

The evaluation board contains its own clock chip. The AD9516 has an optional on-chip PLL. The top half of the control tab helps the user select the appropriate control values for the PLL controller. If the PLL is bypassed, the DAC Clock has the same frequency as the input to the AD9516, unless when using conditions where the DCO needs to run at higher speeds than the DAC (ie. 1x interpolation in byte mode requires a DCO of 2×DAC for proper clocking). Two additional clocks, Ref Clk and DCO Clk, are generated from the DAC Clock/input clock. The DCO Clock controlling the data frequency can be synchronized with the interpolation rate and interface bus width listed on the Data Clock Control tab. If this is enabled, changing the interpolation rate or data bus width will automatically update the AD9516 to have the appropriate DCO and DAC Clock Divider Ratio.

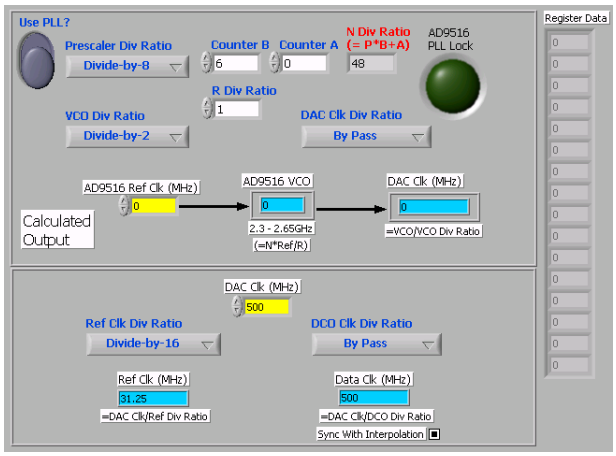

Figure 14: AD9516 Control

Save & Load

The SPI application has options to save and load all the control registers. The save takes place after the controller is run once and the load happens before any of the read or writes to the evaluation board.

NOTES:

D00000-0-1/0

ANALOG DEVICES