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AD9148(-M5372/5)-EBZ Quick Start Guide

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Getting Started with the AD9148(-M5372/5)-EBZ Evaluation Board

WHAT'S IN THE BOX

AD9148(-M5372/5)-EBZ Evaluation Board
Evaluation Board CD
Mini-USB Cable

RECOMMENDED EQUIPMENT

Sinusoidal Clock Source (at least 1.2GHz)
Sinusoidal Clock Source (for modulator LO)
Spectrum Analyzer
DC Power Supply
Data Pattern Generator Series 2 (DPG2)

INTRODUCTION

The AD9148 Evaluation Board connects to a DPG2 to allow for quick evaluation of the AD9148. Control of the SPI port in the AD9148 is available through USB with accompanying PC software.

To ease the subsystem evaluation, a clock distribution chip (AD9516) and a quadrature modulator are also designed into this evaluation board.

SOFTWARE

The AD9148 Evaluation board is designed to receive data from a Data Patten Generator 2 (DPG2). The DAC Software Suite, plus the AD9148 Update, is required for evaluation. The DAC Software Suite is included on the Evaluation Board CD, or can be downloaded from the DPG web site at http://www.analog.com/dpg. This will install DPGDownloader (for loading vectors into the DPG2) and the AD9148 SPI application.

HARDWARE SETUP

Connect a +5V DC power supply to the banana jacks (P5 and P6). A clock source should be connected to the SMA jack labeled J1 (CLKIN). The AD9516 buffers this clock and distributes clock signals with proper frequencies to the AD9148 and the DPG2. In order to monitor the desired outputs, a spectrum analyzer should be connected:

- To the SMA jack labeled J3 (OUT1) for DAC1 output or J8 (OUT2), J16 (OUT3), J9 (OUT4) for DAC2, DAC3, DAC4 output respectively if the evaluation board you ordered is **AD9148-EBZ**.
- To the SMA jack labeled J3 (TX_MOD OUT1) for TX channel1 output or J4 (TX_MOD OUT2) for TX channel2 output if the evaluation board you ordered is **AD9148-M5372-EBZ** or **AD9148-M5375-EBZ**.

If the evaluation board you ordered is **AD9148-M5372-EBZ** or **AD9148-M5375-EBZ** a clock source must be supplied to J5 (LO_IN) for the LO. The levels of the single need to be 10dBm and 7dBm, respectively.

DPG2 connects through connector P1 and P2 on the left edge of the evaluation board, and the USB cable should be connected to the mini USB connector labeled XP2 USB SPI on the top side of the board. Note that the PC software needs to be installed before connecting the USB cable to your computer.

JUMPER CONFIGURATIONS

There are 6 (on the **AD9148-EBZ**) and 7 (on the **AD9148-M5372/5-EBZ)** pin jumpers and 2 solder jumpers on the evaluation board. The pin jumpers are corresponding to the 6 supplies, i.e., AVDD3.3, DVDD1.8, CVDD1.8 and etc, on the board. They serve as 'switches' that determine if the LDOs on board or external supplies are used for each individual supply. Most of the pin jumpers, except JP1, are 2

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pin jumpers. They are shunted by default, which means on board LDOs are used. When an external supply is necessary, pull off the shunt from the corresponding supply and connect the external supply to the test points close to the jumper. JP1 selects the supply voltage level of IOVDD. When pin 1 and 2 are connected, IOVDD = 3.3V. When pin 2 and 3 are connected, IOVDD = 1.8V. The default configuration is 3.3V.

The solder jumpers JP15 and JP18 on the back side of the board determines whether the ref/sync clock of the AD9148 is from the AD9516 or an external source through the SMA jack J2 (REF_IN). When the AD9516 is used for the clock source, the jumpers should be configured so that the center pad is connected to the inner pad. When an external source is used, the center pad should be connected to the outer pad.

For AD9148-M5372/5-EBZ, a LO signal is needed to drive the modulators. The LO signal is fed through the SMA connector J5 (LO_IN) and shared between the two modulators.

GETTING STARTED

Single Tone Test

This setup configures the AD9148 to generate a sine wave by using the DPG2 as a data source. This allows the user to measure the single-tone AC performance at the DAC output or the modulator output. Install the software as described in the *Software* section, and connect all the required cables as described in the *Hardware Setup* section. Turn on the power supply.

For this setup, the clock source is set to generate a 500MHz tone at 0dBFS. Using 2x interpolation and two port mode, the data clock should be running at 250MHz. Open the AD9148 SPI software and go to the 2nd tab (data). Set the interpolation rate to 2X. Hit 'run' button. This will set the part to 2x interpolation mode and configure the clock going into the DPG2 to half of the DAC rate.

In DPG2 Downloader software, the 'DCO frequency' shown should be 250MHz. (Due to the resolution of the DPG frequency counter, the measured frequency could be a little off). In the 'evaluation board' drop down menu, the selection should be shown as 'AD9148'. This selection is automatically done when you plug the USB cable into the evaluation board.

Select 'Single Tone' in the 'Add Generated Waveform' drop down menu in the DPG2 Downloader. Set the sample rate to 250MHz and the desired frequency to 31MHz. Check the box of 'Generate Complex Data (I&Q)'. Uncheck the box of 'Unsigned Data'. Pick the generated I waveform in the 'Data Vector 1' and 'Data Vector 3'. Pick the generated Q waveform in the 'Data Vector 2' and 'Data Vector 4'. Click Download ( ) and Play ( ). This results in a single-tone centered at 31MHz at the DAC output or LO+31MHz at the modulator output. The current on the 5V supply should be approximately 920mA for **AD9148-EBZ** and 1240mA for **AD9148-M5372/5-EBZ**.

SPI APPLICATION

The SPI application is divided into multiple tabs pertaining to different functionality controls. Several of the controls and functions are described in this section as they relate to the evaluation board. For a comprehensive list and description of all the control registers, refer to the AD9148 datasheet. In the interest of continuous quality improvements, the images below may not exactly match your version of the software.

Running the SPI Controller

To run the SPI controller once, simply click the run arrow ( ) as normal in LabVIEW. In order to properly run the controller continuously, turn the *Run Continuously* button ON before clicking the run button (Figure 1). When only a readback of the indicators is necessary and no writes are to be executed, select the *Read Only* button before running the controller, also depicted in Figure 1. By default, the clock chip (AD9516) updates every time the SPI controller runs, including when *Run Continuously* is selected. For each run, the *Update AD9516* button correspondingly changes status to indicate the AD9516 SPI has executed, shown in Figure 1. To prevent the clock chip from constantly being updated, select the "AD9516" tab and turn off the *AD9516 Control*, shown in Figure 2. When the *AD9516 Control* is turned off, the next time the SPI controller is executed the status button will appear on and remain instead of clearing itself, but the clock chip controls will not have been altered.

Figure 1

Figure 2

Data Clock Control

This section, shown in

Figure 3, controls the Interpolation Rate and Coarse Modulation. The *Modulation Description* field will readback the controls selected. Additionally, the individual half-band filter stages will also update in the respective fields. If an improper selection of these controls is chosen, the *Modulation Description* indicator will read *Invalid*. By default, the AD9516 will automatically update the proper dividers for the clocks based on the chosen interpolation from the drop-down menu. To disable this feature, select the *AD9516* tab and uncheck the *Sync with Interpolation* box near the *Data Clock* controls.

An advanced filter control option is available to manually control the stages of each of the filters. To access this, the *Enable Advanced Filter Control* should be turned on. Each of the half-band filters are turned on by their respective enable controls, and the modes for each filter are set in the corresponding field selections. Note that if the *Sync with Interpolation* checkbox is selected, the clock dividers will still be updated according to the interpolation rate selected from the menu, even when using the advanced control.

The Interface Control section of

Figure 3 allows for easy control of the different features that the AD9148 has to offer. *Binary Enable* controls the number format for the incoming data with a choice between unsigned/binary, when enabled, and signed/2's compliment, when disabled. When using the DPG2, the *All Ports Enable* and *One DCI* controls should be selected. Note that the *Bus Swap, Byte Swap,* and *Q First Enable* controls are not supported features with the DPG2. *Byte Mode* is supported and the DPGDownloader panel *Interface Mode* must be set to "Byte Mode" for proper execution. When implementing *Byte Mode*, the *All Ports Enable* control must be disabled (single-port mode selected) and *One DCI* must be enabled. Additionally, the clock chip divider must be set appropriately to allow for a DCO that is twice the rate of what the setting would be in word mode for a particular interpolation. Note that byte mode cannot be used in 1x interpolation mode. For example, for 2x interpolation using word mode, the *DCO Clk Div Ratio* is set to "Divide-by-2". However, for 2x interpolation using byte mode, the *DCO Clk Div Ratio* should be set to "Bypass". Also, note that the *Sync with Interpolation* box for the clock divider will not adjust when byte mode is selected and therefore should be unchecked and the divider set manually in this mode.

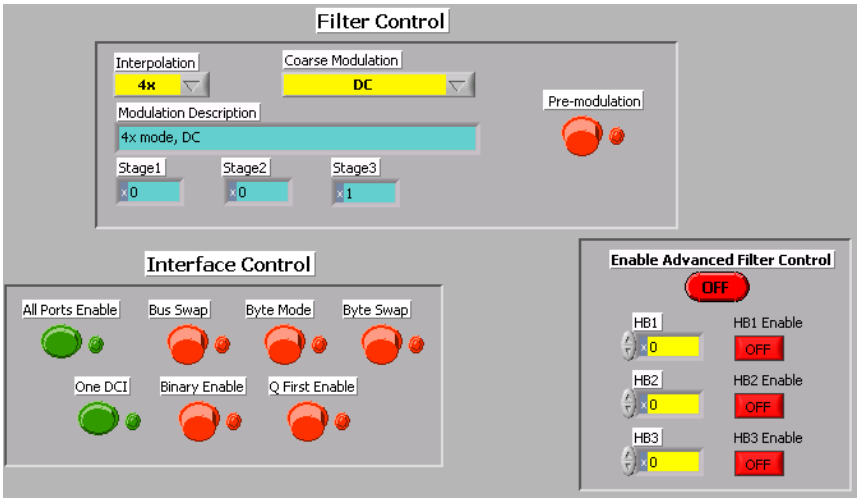

Figure 3

NCO Control

The NCO controls shown in Figure 4 are listed at the bottom of the "Data" tab, listed previously. When using the NCO, turn the *Fine Modulation* control ON and input the *DAC Clock* rate as well as the *NCO Freq Shift* (up to ± $F_{dac/2}$ allowable) and the desired sideband using *Sideband Select*. A readback of the calculated FTW written will appear in the indicator field. Also available is a phase offset feature for the NCO, which is set through the *NCO Phase Offset Word*. For a higher degree of control, select the *Enable Advanced NCO Control* while keeping *Fine Modulation* ON as well, and use the FTW control to input

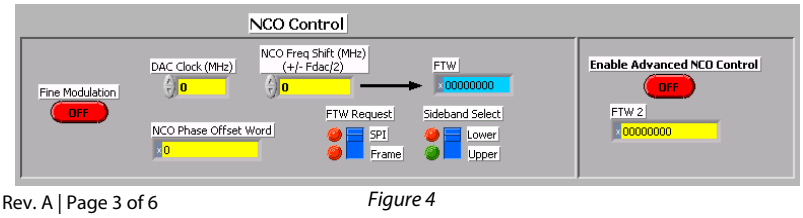

Figure 4

the desired tuning word. This will bypass the other control values on the left and directly write the FTW to the SPI.

Inverse Sinc Control

The AD9148 has a programmable Inverse Sinc filter. The coefficients are ten 2's complement numbers for each of the two sets of DACs as described in the datasheet. In order to program the coefficients using the DAC software, the *Bypass Inv Sinc* control needs to be set to the off position. The coefficients can either be entered manually or generated from the DAC rate and center frequencies of both DAC sets. Enter the coefficients, in decimal form, into the blue boxes of Figure 5 for manual setup. In order to use the built-in coefficient calculator, enter the DAC rate and Center Frequencies in the yellow boxes. Enable the *Run InvSinc Simulation* control and run the software for the calculation of the coefficients.

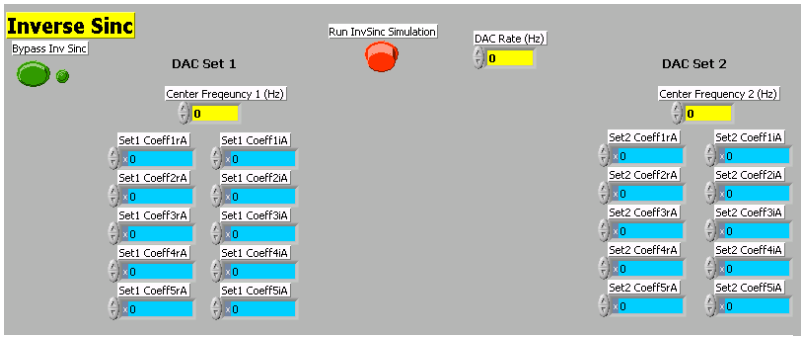

Figure 5

PLL Control

The AD9148 has an on-chip PLL, with controls shown in Figure . In order to ensure that the PLL will lock on the correct band using the auto-search mode, the part must first be enabled in manual mode by selecting the *PLL_Enable* and *PLL Manual* controls. From here, the part can be taken out of manual mode by disabling the *PLL Manual* control. The PLL will start an auto-search to determine the best band based on the Divider1 and Divider0 values selected. Included in this tab is the calculation for the DAC Freq and VCO Freq based on the reference clock (*Ref Clk* control) and the value of the dividers. The VCO Frequency must be between 1 and 2 GHz for proper operation. The auto-band select can be bypassed by enabling *PLL MANUAL* and entering a band in *PLL Band Select*. *Divider1* and *Divider0* must still be chosen appropriately in this mode of operation.

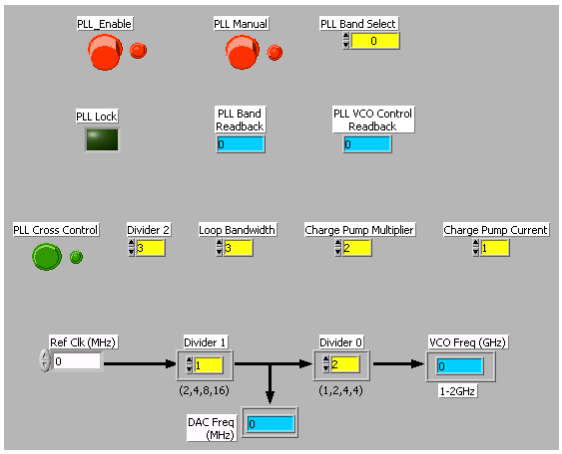

Figure 6

Interrupts

This tab provides a visual indication of the state of each interrupt. Enabling the button to the left of each interrupt with enable the interrupt. A green indicator to the right of the button will light when the interrupt is asserted. Once asserted, the interrupt can be acknowledged by pressing the *Clear* button.

Main DAC Control

This tab, shown in Figure , controls the four main DACs in the AD9148. The Full-Scale Current of each DAC can be set with the *I[1/2] DAC Gain* and *Q[1/2] DAC Gain* controls. The output current setting is calculated and displayed for each DAC based on the inputted code for the DAC Gains. The *I[1/2] Sleep* and *Q[1/2] Sleep* controls put their respective DAC into a low-power sleep state. When the AD9148 is used with a modulator, the phase compensation (*I/Q Phase Word*) and DC offset controls (*I/Q DC Offset Code*) can be used to correct any mismatches between the two DAC sets. Also available are the *I[1/2] Digital Gain* and *Q[1/2] Digital Gain* which scale the samples written to each individual DAC, yielding a multiplier range of 0 to 3.984375.

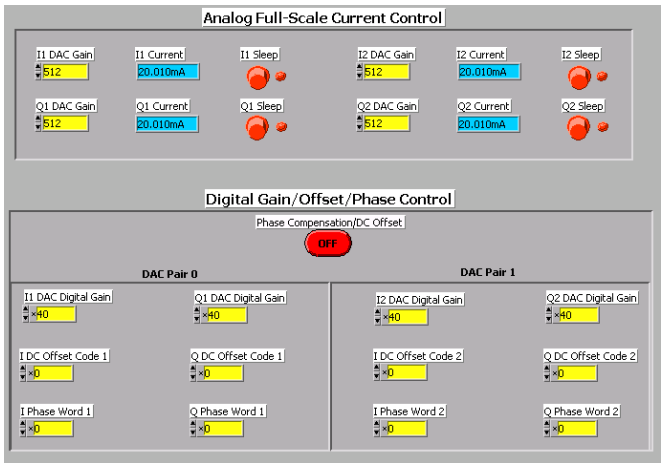

Figure 7

AUX DAC Control

As with the main DACs, the full-scale current of the auxiliary DACs can be set over the SPI port. Each DAC can also be powered down as well as providing the option to source or sink the current for either the P-side or N-side.

Sampling Error Detection

The Sampling Error Detection (SED) checks the data inputs. An 8-byte signature is handed to the AD9148. The controller can automatically generate and load the vectors using the DPG2 device. Indicators display the result of the comparison between the input data and the expected signature, noting which of the bits contain the errors.

SPI Map

The SPI Map tab provides an overview of all the settings currently written to the part. The individual register values are indicated graphically (with red and green boxes) and numerically. The numeric results can be used in whatever system the AD9148 connects to, to duplicate the current settings in the end system. The *SPI Map Read* button must be on in order to reflect the current readback of all the registers. The *Read DAC Select* control chooses which DAC set values (DAC Set0: DAC1, DAC2 ; DAC Set1: DAC3, DAC4) will appear in the readback arrays for the duplicated registers.

AD9516 Control

The evaluation board contains its own clock chip. The AD9516 has an optional on-chip PLL. The top half of the control tab helps the user select the appropriate control values for the PLL controller. If the PLL is bypassed, the DAC Clock has the same frequency as the input to the AD9516. Two additional clocks, Ref Clk and DCO Clk, are generated based off of the DAC Clock. The DCO Clock controlling the data frequency can be synced with the interpolation rate on the Data Clock Control tab. If this is enabled, changing the interpolation rate will automatically update the AD9516 to have the appropriate DCO Clock Divider Ratio. Note: This is true only for word mode and is not supported in byte mode, as mentioned previously.

Save and Load

The SPI controller has options to save and load all the control registers. The save takes place after the controller is run once and the load happens before any of the read or writes to the evaluation board.

NOTES

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