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Dual, 16-Bit, 2.25 GSPS, TxDAC+ Digital-to-Analog Converter

Data Sheet **AD9152**

FEATURES

- Supports input data rates up to 1.125 GSPS
- Proprietary low spurious and distortion design
  - Single carrier LTE 20 MHz bandwidth (BW), ACLR = 77 dBc at 180 MHz IF
  - SFDR = 72 dBc at 150 MHz IF, −6 dBFS
- Flexible 4-lane JESD204B interface
- Multiple chip synchronization
  - Fixed latency
  - Data generator latency compensation
- Selectable 1×, 2×, 4×, and 8× interpolation filter
  - Low power architecture
- Input signal power detection
  - Emergency stop for downstream analog circuitry protection
- Transmit enable function allows extra power saving
- High performance, low noise, phase-locked loop (PLL) clock multiplier
- Digital inverse sinc filter and programmable finite impulse response (FIR) filter
- Low power: 1223 mW at 1.5 GSPS, 1406 mW at 2.0 GSPS, full operating conditions
- 56-lead LFCSP with exposed pad

APPLICATIONS

- Wireless communications
  - Multicarrier LTE and GSM base stations
  - Wideband repeaters
  - Software defined radios
- Wideband communications
  - Point to point microwave radios
  - LMDS/MMDS
- Transmit diversity, multiple input/multiple output (MIMO)
- Instrumentation
- Automated test equipment

GENERAL DESCRIPTION

The AD9152 is a dual, 16-bit, high dynamic range digital-to-analog converter (DAC) that provides a maximum sample rate of 2.25 GSPS, permitting a multicarrier generation up to the Nyquist frequency. The DAC outputs are optimized to interface seamlessly with the ADRF6720 analog quadrature modulator (AQM) from Analog Devices, Inc. An optional 3-wire or 4-wire serial port interface (SPI) provides for programming/readback of many internal parameters. The full-scale output current can be programmed over a range of 4 mA to 20 mA. The AD9152 is available in a 56-lead LFCSP. The AD9152 is a member of the TxDAC+® family.

PRODUCT HIGHLIGHTS

1. Ultrawide signal bandwidth enables emerging wideband and multiband wireless applications.
2. Advanced low spurious and distortion design techniques provide high quality synthesis of wideband signals from baseband to high intermediate frequencies.
3. JESD204B Subclass 1 support simplifies multichip synchronization in software and hardware design.
4. Fewer pins for data interface width with the serializer/deserializer (SERDES) JESD204B four-lane interface.
5. Programmable transmit enable function allows easy design balance between power consumption and wake-up time.
6. Small package size with an 8 mm × 8 mm footprint.

FUNCTIONAL BLOCK DIAGRAM

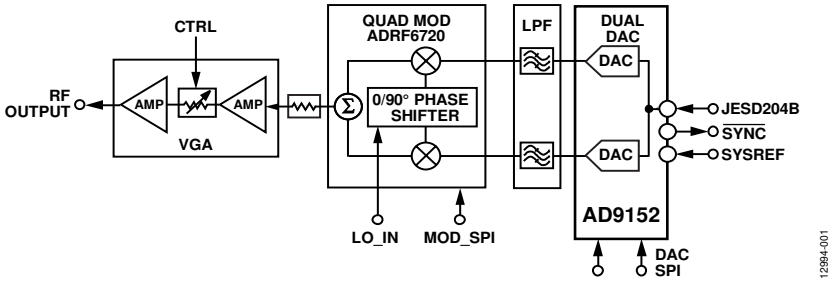

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD9152* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9152 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9152: Dual, 16-Bit, 2.25 GSPS, TxDAC+ Digital-to-Analog Converter Data Sheet

TOOLS AND SIMULATIONS

- AD9144/AD9152/AD9154/AD9135/AD9136 AMI Model Download
- AD9152 IBIS Model

DESIGN RESOURCES

- AD9152 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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4/2015—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

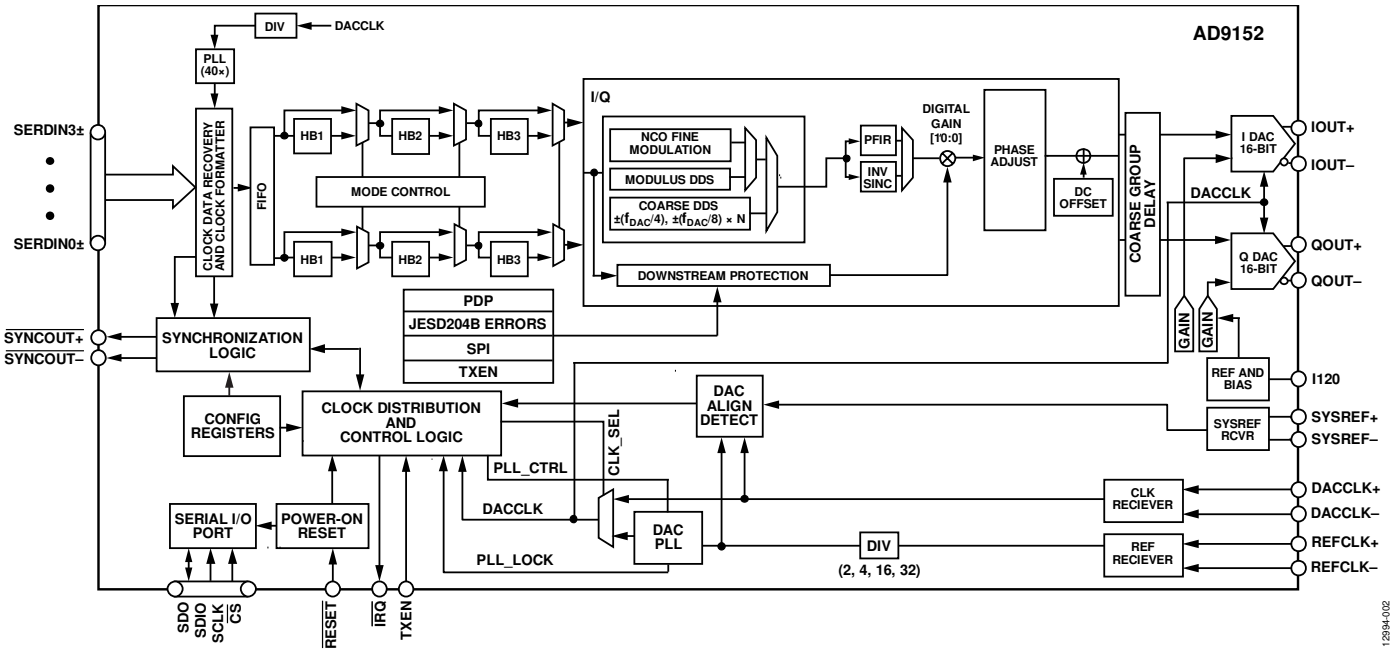

Figure 2. Detailed Functional Block Diagram

SPECIFICATIONS

DC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, PLLVDD12 = 1.2 V, SVDD12 = 1.2 V, SDVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION			16		Bits
ACCURACY					
Differential Nonlinearity (DNL)			±5.0		LSB
Integral Nonlinearity (INL)			±10.0		LSB
MAIN DAC OUTPUTS					
Gain Error	With internal reference	−5.5	−1.3	+5.5	% FSR
I/Q Gain Mismatch		−4.5		+4.5	% FSR
Full-Scale Output Current (I_{OUTFS})	Based on a 4 kΩ external resistor between I120 and ground				
Maximum Setting		19.1	20.22	21.4	mA
Minimum Setting		3.8	4.04	4.3	mA
Output Compliance Range		2.3		3.47	mV
Output Resistance			15		MΩ
Output Capacitance			3.0		pF
Gain DAC Monotonicity			Guaranteed		
MAIN DAC TEMPERATURE DRIFT					
Offset			0.1		ppm/°C
Gain			35		ppm/°C
Reference Voltage			25		ppm/°C
REFERENCE					
Internal Reference Voltage			0.5		V
ANALOG SUPPLY VOLTAGES					
AVDD33	±5%	3.13	3.3	3.47	V
PVDD12, CVDD12	±5%	1.14	1.2	1.26	V
	±2%	1.274	1.3	1.326	V
SVDD12, PLLVDD12, V_{TT}	±5%	1.14	1.2	1.26	V
	±2%	1.274	1.3	1.326	V
DIGITAL SUPPLY VOLTAGES					
DVDD12, SDVDD12	±5%	1.14	1.2	1.26	V
	±2%	1.274	1.3	1.326	V
SIOVDD33	±5%	3.13	3.3	3.47	V
IOVDD	±5%	1.71	1.8	3.47	V
POWER CONSUMPTION					
Total Power	2× interpolation mode, f_{DAC} = 1.5 GSPS, IF = 70 MHz, PLL off, INVSINC on, digital gain on, NCO on, JESD204B Mode 4, four SERDES lanes with 7.5 Gbps lane rate, I_{OUTFS} = 20 mA		1223		mW
AVDD33			87		mA
PVDD12			11		mA
CVDD12			179		mA
SDVDD12 and SVDD12 (Includes PLLVDD12 and V_{TT})			328		mA
DVDD12			246		mA
SIOVDD33 and IOVDD			5.7		mA
OPERATING TEMPERATURE RANGE		−40	+25	+85	°C

DIGITAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, PLLVDD12 = 1.2 V, SVDD12 = 1.2 V, SDVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL						
Input Voltage Logic	V_{IN}					
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.7 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.3 × IOVDD	V
CMOS OUTPUT LOGIC LEVEL						
Output Voltage Logic	V_{OUT}					
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.7 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.3 × IOVDD	V
MAXIMUM DAC UPDATE RATE[1]		DVDD12 = CVDD12 = PVDD12 = 1.3 V ± 2%				
		1× interpolation[2]	1238			MSPS
		2× interpolation	2250			MSPS
		4× interpolation	2250			MSPS
		8× interpolation	2250			MSPS
ADJUSTED DAC UPDATE RATE		DVDD12 = CVDD12 = PVDD12 = 1.3 V ± 2%				
		1× interpolation	1238			MSPS
		2× interpolation	1125			MSPS
		4× interpolation	562.5			MSPS
		8× interpolation	281.25			MSPS
INTERFACE[3]						
Number of JESD204B Lanes				4		Lanes
JESD204B Serial Interface Speed		SVDD12 = SDVDD12 = PLLVDD12 = 1.3 V ± 2%				
Minimum		Per lane			1.44	Gbps
Maximum		Per lane	12.38			Gbps
DAC CLOCK INPUT (DACCLK±)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage		Self biased input, ac-coupled		600		mV
Maximum Clock Rate		DVDD12 = CVDD12 = PVDD12 = 1.3 V ± 2%	2250			MHz
REFERENCE CLOCK INPUT (REFCLK±)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage		Self biased input, ac-coupled		600		mV
Input Clock Frequency (PLL Mode)		6 GHz ≤ f_{VCO} ≤ 12 GHz	70		1000	MHz
SYSTEM REFERENCE INPUT (SYSREF±)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage			0		2000	mV
SYSREF± Frequency[4]					$f_{DATA}/(K \times S)$	Hz
SYSREF± TO DAC CLOCK[5]		SYSREF± differential swing = 1.2 V, slew rate = 6.3 V/ns, hysteresis off (ac-coupled, and 0 V, 0.6 V, 1.25 V, 2.0 V dc-coupled common-mode voltages)				
Setup Time	t_{SSD}		−6			ps
Hold Time	t_{HSD}		224			ps
Keep Out Window	KOW			218		ps

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SPI						
Maximum Clock Rate	SCLK	IOVDD = 1.8 V	10			MHz
Minimum SCLK Pulse Width						
High	t_{PWH}				8	ns
Low	t_{PWL}				12	ns
SDIO to SCLK						
Setup Time	t_{DS}		5			ns
Hold Time	t_{DH}		2			ns
SDO to SCLK						
Data Valid Window	t_{DV}		26			ns
$\overline{CS}$ to SCLK						
Setup Time	$t_{S\overline{CS}}$		5			ns
Hold Time	$t_{H\overline{CS}}$		2			ns

[1] See Table 3 and Table 4 for detailed specifications for the DAC update rate conditions.
[2] The maximum speed for 1× interpolation is limited by the JESD2040B interface. See Table 4 for details.
[3] See Table 4 for detailed specifications for JESD2040B speed conditions.
[4] K and S are JESD204B transport layer parameters. See Table 41 for the full definitions.
[5] See Table 5 for detailed specifications for SYSREF± to DAC clock timing conditions.

MAXIMUM DAC UPDATE RATE SPEED SPECIFICATIONS BY SUPPLY

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, PLLVDD12 = 1.2 V, SVDD12 = 1.2 V, SDVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DAC UPDATE RATE	DVDD12, CVDD12 = 1.2 V ± 5%	1.85			GSPS
	DVDD12, CVDD12 = 1.3 V ± 2%	2.25			GSPS

JESD204B SERIAL INTERFACE SPEED SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, PLLVDD12 = 1.2 V, SVDD12 = 1.2 V, SDVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
HALF RATE	SVDD12, SDVDD12, PLLVDD12 = 1.2 V ± 5%	5.75		11.00	Gbps
	SVDD12, SDVDD12, PLLVDD12 = 1.3 V ± 2%	5.75		12.38	Gbps
FULL RATE	SVDD12, SDVDD12, PLLVDD12 = 1.2 V ± 5%	2.88		5.53	Gbps
	SVDD12, SDVDD12, PLLVDD12 = 1.3 V ± 2%	2.88		6.19	Gbps
OVERSAMPLING	SVDD12, SDVDD12, PLLVDD12 = 1.2 V ± 5%	1.44		2.69	Gbps
	SVDD12, SDVDD12, PLLVDD12 = 1.3 V ± 2%	1.44		3.09	Gbps

SYSREF± TO DAC CLOCK TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, PLLVDD12 = 1.2 V, SVDD12 = 1.2 V, SDVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, SYSREF± common-mode voltages = 0.0 V, 0.6 V, 1.25 V, and 2.0 V, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSREF	Differential swing = 1.2 V, slew rate = 6.3 V/ns				
Hysteresis Off					
Setup Time	AC-coupled	−9			ps
	DC-coupled	−6			ps
Hold Time	AC-coupled	199			ps
	DC-coupled	224			ps
Hysteresis On (HYS_CNTRL = 0x3FF)					
Setup Time	AC-coupled	143			ps
	DC-coupled	145			ps
Hold Time	AC-coupled	97			ps
	DC-coupled	123			ps

DIGITAL INPUT DATA TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, PLLVDD12 = 1.2 V, SVDD12 = 1.2 V, SDVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LATENCY					
Interface			17		PClock[1] cycles
Interpolation					
1×			143		DAC clock cycles
2×			163		DAC clock cycles
4×			287		DAC clock cycles
8×			557		DAC clock cycles
Inverse Sinc			17		DAC clock cycles
Fine Modulation			20		DAC clock cycles
Coarse Modulation					
$f_S/8$			8		DAC clock cycles
$f_S/4$			4		DAC clock cycles
Digital Phase Adjust			12		DAC clock cycles
Digital Gain Adjust			12		DAC clock cycles
Power-Up Time	Register 0x011 from 0x60 to 0x00		60		µs

[1] PClock is the AD9152 internal processing clock and equals the lane rate ÷ 40.

LATENCY VARIATION SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, PLLVDD12 = 1.2 V, SVDD12 = 1.2 V, SDVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 7.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC LATENCY VARIATION	Given proper calibration of the local multiframe clock (LMFC) delay				
Subclass 1					DAC clock cycles
PLL Off		−3	0	+3	DAC clock cycles
PLL On		−4		+4	DAC clock cycles

JESD204B INTERFACE ELECTRICAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, PLLVDD12 = 1.2 V, SVDD12 = 1.2 V, SDVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 8.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B DATA INPUTS						
Input Leakage Current		T_A = 25°C				
Logic High		Input level = 1.2 V ± 0.25 V, V_{TT} = 1.2 V		10		µA
Logic Low		Input level = 0 V		−4		µA
Unit Interval	UI		81		694	ps
Common-Mode Voltage	V_{RCM}	AC-coupled V_{TT} = SVDD12[1]	−0.05		+1.85	V
Differential Voltage	R_V_{DIFF}		110		1050	mV
V_{TT} Source Impedance	Z_{TT}	At dc			30	Ω
Differential Impedance	Z_{RDIFF}	At dc	80	100	120	Ω
Differential Return Loss	RL_{RDIF}			8		dB
Common-Mode Return Loss	RL_{RCM}			6		dB
DIFFERENTIAL OUTPUTS ($\overline{\text{SYNCOUT}}$±)[2]						
Output Offset Voltage	V_{OS}		1.15		1.25	V
Output Differential Voltage	V_{OD}	High swing mode: Register 0x230, Bit 0 = 1	350		410	mV
DETERMINISTIC LATENCY						
Fixed					17	PClock[3] cycles
Variable					2	PClock[3] cycles
SYSREF± TO LMFC DELAY				4		DAC clock cycles

[1] As measured on the input side of the ac coupling capacitor.
[2] IEEE Standard 1596.3 LVDS compatible.
[3] PClock is the AD9152 internal processing clock and equals the lane rate ÷ 40.

AC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, PLLVDD12 = 1.2 V, SVDD12 = 1.2 V, SDVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 9.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	−6 dBFS single tone				
f_{DAC} = 1966.08 MSPS	f_{OUT} = 20 MHz		76		dBc
	f_{OUT} = 150 MHz		72		dBc
	f_{OUT} = 180 MHz		68		dBc
TWO-TONE THIRD INTERMODULATION DISTORTION (IMD)	−6 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 30 MHz		86		dBc
	f_{OUT} = 150 MHz		79		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 30 MHz		86		dBc
	f_{OUT} = 180 MHz		78		dBc
NOISE SPECTRAL DENSITY (NSD), SINGLE TONE	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		−162.5		dBm/Hz
f_{DAC} = 1966.08 MSPS	f_{OUT} = 180 MHz		−163		dBm/Hz
5 MHz BW LTE FIRST ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER	0 dBFS, PLL off				
f_{DAC} = 1966.08 MSPS	f_{OUT} = 50 MHz		79		dBc
	f_{OUT} = 150 MHz		77		dBc
	f_{OUT} = 180 MHz		77		dBc
5 MHz BW LTE SECOND ACLR, SINGLE CARRIER	0 dBFS, PLL off				
f_{DAC} = 1966.08 MSPS	f_{OUT} = 50 MHz		82		dBc
	f_{OUT} = 150 MHz		81		dBc
	f_{OUT} = 180 MHz		81		dBc

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
I120 to Ground	−0.3 V to AVDD33 + 0.3 V
SERDINx±, V_{TT}, $\overline{\text{SYNCOUT}}$±, TXEN	−0.3 V to SIOVDD33 + 0.3 V
IOUT±, QOUT±	−0.3 V to AVDD33 + 0.3 V
SYSREF±	GND − 0.5 V to +2.5 V
DACCLK± and REFCLK± to Ground	−0.3 V to PVDD12 + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{CS}}$, SCLK, SDIO, SDO, PROTECT_OUT to Ground	−0.3 V to IOVDD + 0.3 V
LDO_BYP1	−0.3 V to SVDD12 + 0.3 V
LDO_BYP2	−0.3 V to PVDD12 + 0.3 V
Ambient Operating Temperature (T_A)	−40°C to +85°C
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The exposed pad (EPAD) must be soldered to the ground plane for the 56-lead LFCSP. The EPAD provides an electrical, thermal, and mechanical connection to the board.

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer JESD51-7 high effective thermal conductivity test board for leaded surface-mount packages. θ_{JA} is obtained in still air conditions (JESD51-2). Airflow increases heat dissipation, effectively reducing θ_{JA}. θ_{JB} is obtained following double-ring cold plate test conditions (JESD51-8). θ_{JC} is obtained with the test case temperature monitored at the bottom of the exposed pad.

Ψ_{JT} and Ψ_{JB} are thermal characteristic parameters obtained with θ_{JA} in still air test conditions.

Junction temperature (T_J) can be estimated using the following equations:

$$T_J = T_T + (\Psi_{JT} \times P)$$

or

$$T_J = T_B + (\Psi_{JB} \times P)$$

where:
T_T is the temperature measured at the top of the package.
P is the total device power dissipation.
T_B is the temperature measured at the board.

Table 11. Thermal Resistance

Package	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
56-Lead LFCSP[1]	25.5	4.8	1.7	0.1	4.8	°C/W

[1] The exposed pad must be securely connected to the ground plane.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

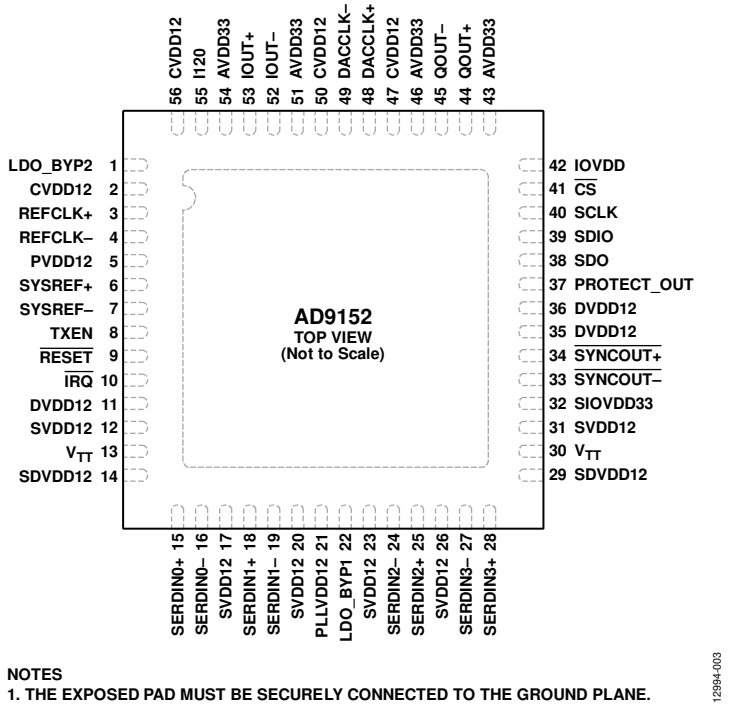

Figure 3. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	LDO_BYP2	LDO Clock Bypass for the DAC PLL. This pin requires a 1 Ω resistor in series with a 1 µF capacitor to ground.
2	CVDD12	1.2 V Clock Supply.
3	REFCLK+	PLL Reference Clock Input, Positive.
4	REFCLK–	PLL Reference Clock Input, Negative.
5	PVDD12	1.2 V Supply. This pin supplies the DAC PLL and clock receiver circuitry.
6	SYSREF+	Positive Reference Clock for Deterministic Latency. This pin is self biased for ac coupling. This pin may be ac-coupled or dc-coupled.
7	SYSREF–	Negative Reference Clock for Deterministic Latency. This pin is self biased for ac coupling. This pin may be ac-coupled or dc-coupled.
8	TXEN	Transmitter (Tx) Enable for I DAC and Q DAC. CMOS levels are determined with respect to IOVDD.
9	$\overline{\text{RESET}}$	Reset (Active Low). CMOS levels are determined with respect to IOVDD.
10	$\overline{\text{IRQ}}$	Interrupt Request (Active Low, Open Drain).
11	DVDD12	1.2 V Digital Supply.
12	SVDD12	1.2 V JESD204B Receiver (Rx) Analog Supply.
13	V_{TT}	1.2 V Termination Voltage. Connect this pin to the SVDD12 pin externally.
14	SDVDD12	1.2 V JESD204B Rx Digital Supply.
15	SERDIN0+	Serial Channel Input 0, Positive. CML compliant. SERDIN0+ is 50 Ω terminated to the V_{TT} pin voltage. This pin is ac-coupled only. Resistance calibrated.
16	SERDIN0–	Serial Channel Input 0, Negative. CML compliant. SERDIN0– is 50 Ω terminated to the V_{TT} pin voltage. This pin is ac-coupled only. Resistance calibrated.
17	SVDD12	1.2 V JESD204B Rx Analog Supply.
18	SERDIN1+	Serial Channel Input 1, Positive. CML compliant. SERDIN1+ is 50 Ω terminated to the V_{TT} pin voltage. This pin is ac-coupled only. Resistance calibrated.
19	SERDIN1–	Serial Channel Input 1, Negative. CML compliant. SERDIN1– is 50 Ω terminated to the V_{TT} pin voltage. This pin is ac-coupled only. Resistance calibrated.
20	SVDD12	1.2 V JESD204B Rx Analog Supply.
21	PLLVDD12	1.2 V SERDES PLL Supply.
22	LDO_BYP1	LDO SERDES Bypass. This pin requires a 1 Ω resistor in series with a 1 µF capacitor to ground.

Pin No.	Mnemonic	Description
23	SVDD12	1.2 V JESD204B Rx Analog Supply.
24	SERDIN2−	Serial Channel Input 2, Negative. CML compliant. SERDIN2− is 50 Ω terminated to the V_{TT} pin voltage. This pin is ac-coupled only. Resistance calibrated
25	SERDIN2+	Serial Channel Input 2, Positive. CML compliant. SERDIN2+ is 50 Ω terminated to the V_{TT} pin voltage. This pin is ac-coupled only. Resistance calibrated.
26	SVDD12	1.2 V JESD204B Rx Analog Supply.
27	SERDIN3−	Serial Channel Input 3, Negative. CML compliant. SERDIN3− is 50 Ω terminated to the V_{TT} pin voltage. This pin is ac-coupled only. Resistance calibrated.
28	SERDIN3+	Serial Channel Input 3, Positive. CML compliant. SERDIN3+ is 50 Ω terminated to the V_{TT} pin voltage. This pin is ac-coupled only. Resistance calibrated.
29	SDVDD12	1.2 V JESD204B Rx Digital Supply.
30	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 pin externally.
31	SVDD12	1.2 V JESD204B Rx Analog Supply.
32	SIOVDD33	3.3 V Supply for Equalizers.
33	$\overline{\text{SYNCOUT}}$−	Negative LVDS Sync Output Signal.
34	$\overline{\text{SYNCOUT}}$+	Positive LVDS Sync Output Signal.
35	DVDD12	1.2 V Digital Supply.
36	DVDD12	1.2 V Digital Supply.
37	PROTECT_OUT	Protection Indicator for I DAC and Q DAC. CMOS levels are determined with respect to IOVDD.
38	SDO	Serial Port Data Output. CMOS levels are determined with respect to IOVDD.
39	SDIO	Serial Port Data Input/Output. CMOS levels are determined with respect to IOVDD.
40	SCLK	Serial Port Clock Input. CMOS levels are determined with respect to IOVDD.
41	$\overline{\text{CS}}$	Serial Port Chip Select, Active Low. CMOS levels are determined with respect to IOVDD.
42	IOVDD	1.8 V IOVDD Supply for CMOS Input/Output and SPI.
43	AVDD33	3.3 V Analog Supply for the DAC Cores.
44	QOUT+	Q DAC Positive Current Output.
45	QOUT−	Q DAC Negative Current Output.
46	AVDD33	3.3 V Analog Supply for the DAC Cores.
47	CVDD12	1.2 V Clock Supply.
48	DACCLK+	Positive Device Clock When PLL Is Not Used.
49	DACCLK−	Negative Device Clock When PLL Is Not Used.
50	CVDD12	1.2 V Clock Supply.
51	AVDD33	3.3 V Analog Supply for the DAC Cores.
52	IOUT−	I DAC Negative Current Output.
53	IOUT+	I DAC Positive Current Output.
54	AVDD33	3.3 V Analog Supply for the DAC Cores.
55	I120	Output Current Generation Pin for the DAC Full-Scale Current. Tie a 4 kΩ resistor from this pin to the ground plane.
56	CVDD12	1.2 V Clock Supply.
	EPAD	Exposed Pad. The exposed pad must be securely connected to the ground plane.

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error
Offset error is the deviation of the output current from the ideal of 0 mA. For IOUT+/QOUT+, 0 mA output is expected when all inputs are set to 0. For IOUT−/QOUT−, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when the input is at its minimum code and the output when the input is at its maximum code.

Output Compliance Range
The output compliance range is the range of allowable voltages at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

Adjusted DAC Update Rate
The adjusted DAC update rate is defined as the DAC update rate divided by the smallest interpolating factor. For clarity on DACs with multiple interpolating factors, the adjusted DAC update rate for each interpolating factor may be given.

Physical Lane
Physical Lane x refers to SERDINx±.

Logical Lane
Logical Lane x refers to physical lanes after optionally being remapped by the crossbar block (Register 0x308 and Register 0x309).

TYPICAL PERFORMANCE CHARACTERISTICS

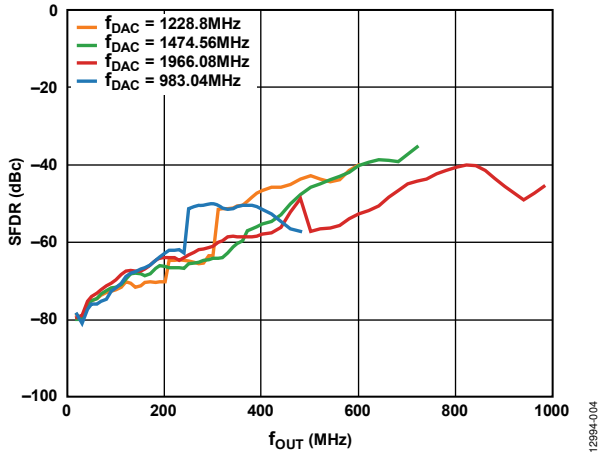

Figure 4. Single Tone (0 dBFS) SFDR vs. f_{OUT} in the First Nyquist Zone over f_{DAC}

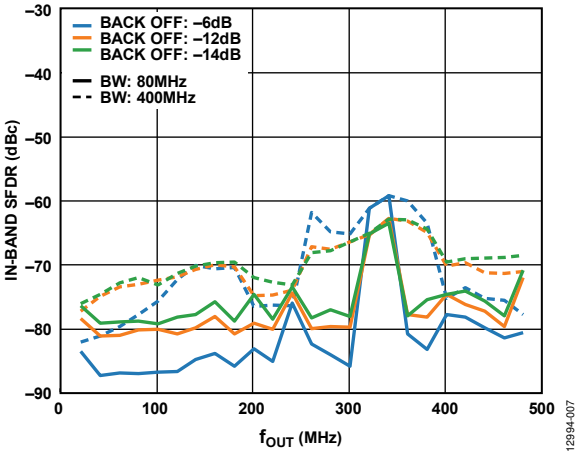

Figure 7. In-Band, Single Tone SFDR vs. f_{OUT} in 80 MHz and 400 MHz Bandwidths, f_{DAC} = 983.04 MHz

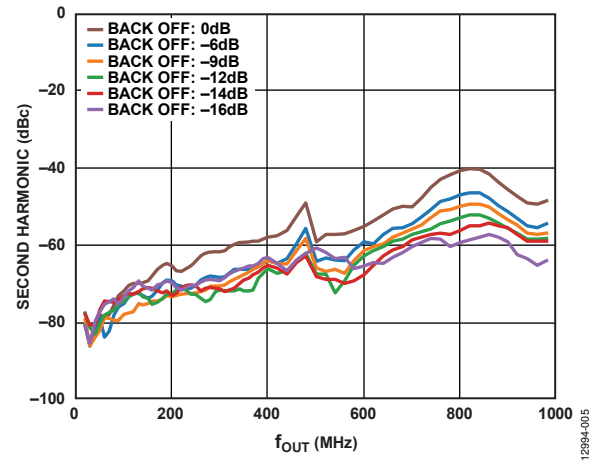

Figure 5. Single Tone Second Harmonic vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 1966.08 MHz

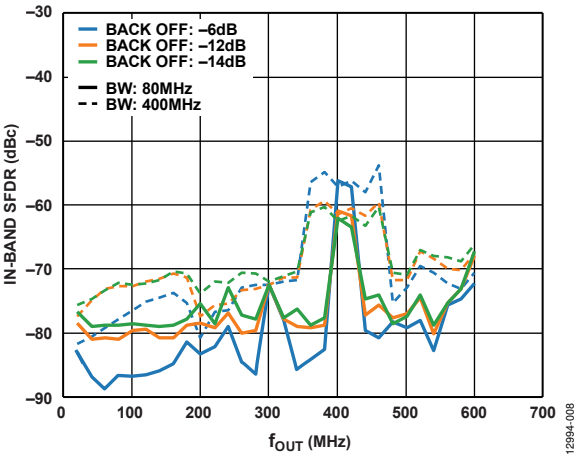

Figure 8. In-Band, Single Tone SFDR vs. f_{OUT} in 80 MHz and 400 MHz Bandwidths, f_{DAC} = 1228.8 MHz

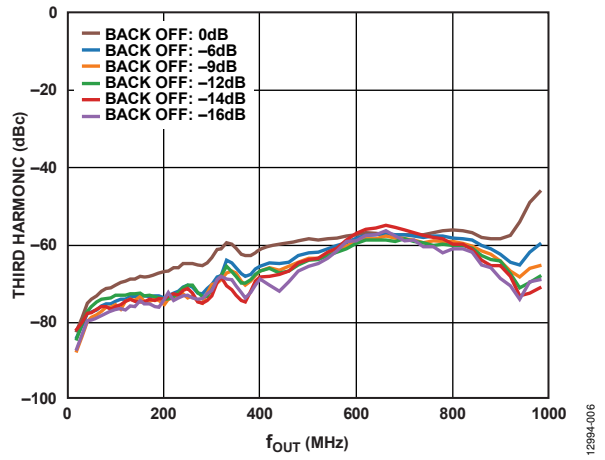

Figure 6. Single Tone Third Harmonic vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 1966.08 MHz

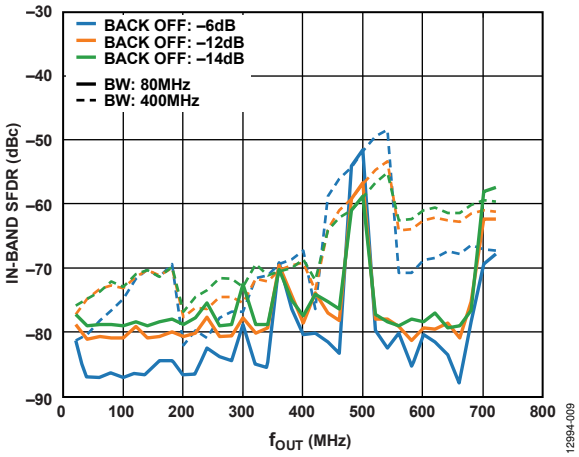

Figure 9. In-Band, Single Tone SFDR vs. f_{OUT} in 80 MHz and 400 MHz Bandwidths, f_{DAC} = 1474.56 MHz

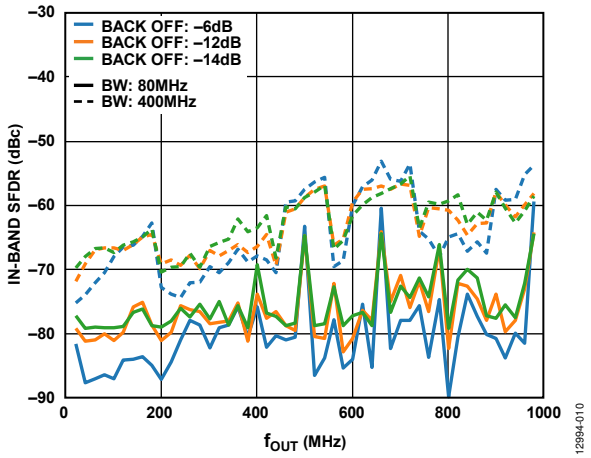

Figure 10. In-Band, Single Tone SFDR vs. f_{OUT} in 80 MHz and 400 MHz Bandwidths, f_{DAC} = 1966.08 MHz

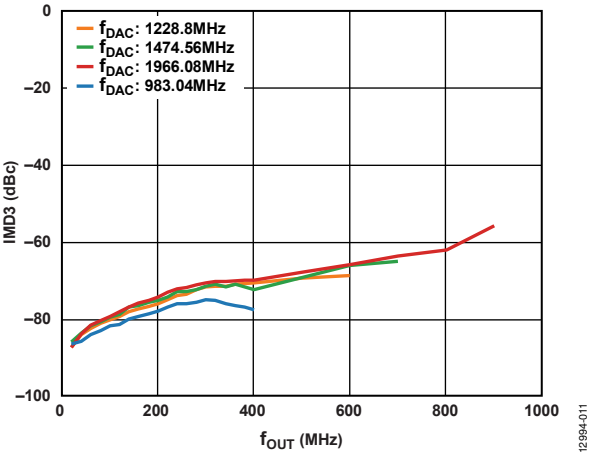

Figure 11. Two-Tone, Third-Order IMD (IMD3) vs. f_{OUT} over f_{DAC}

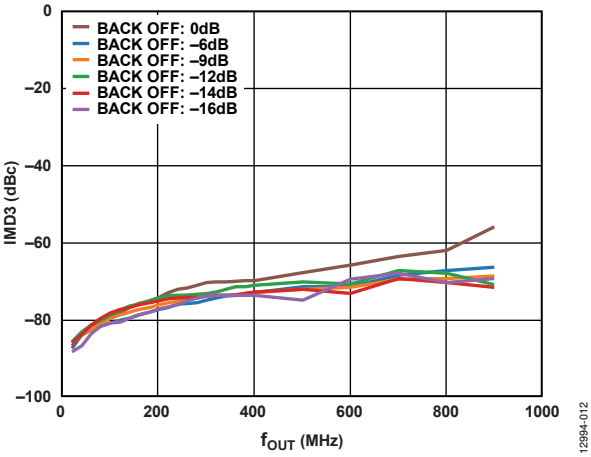

Figure 12. Two-Tone, Third-Order IMD (IMD3) vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966.08 MHz

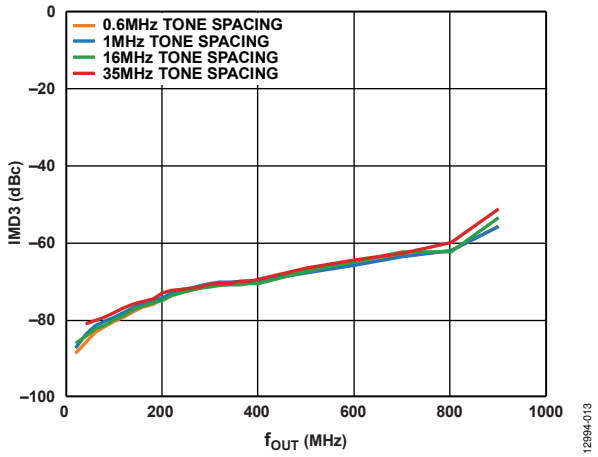

Figure 13. Two-Tone, Third-Order IMD (IMD3) vs. f_{OUT} over Tone Spacing, f_{DAC} = 1966.08 MHz

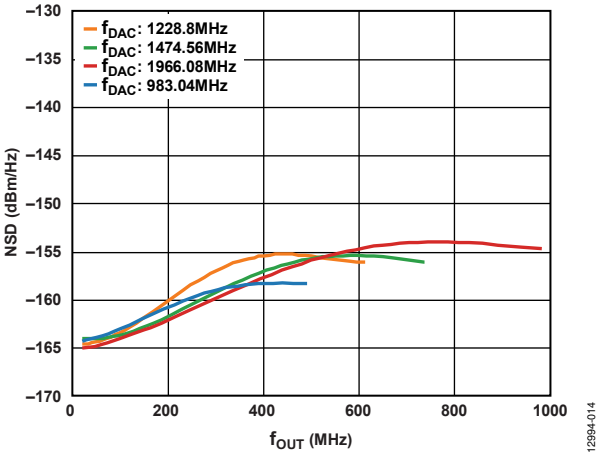

Figure 14. Single Tone (0 dBFS) NSD vs. f_{OUT} over f_{DAC}

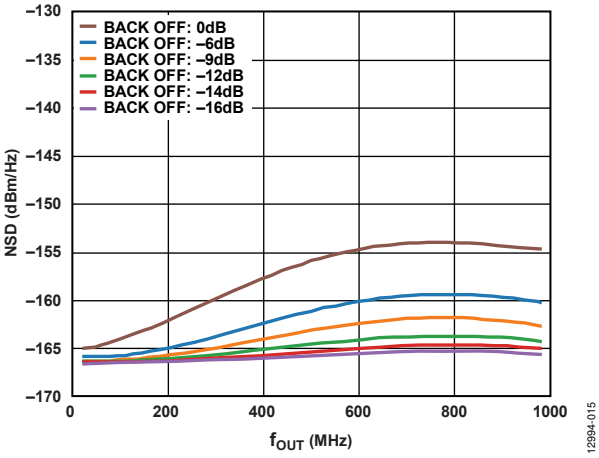

Figure 15. Single Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966.08 MHz

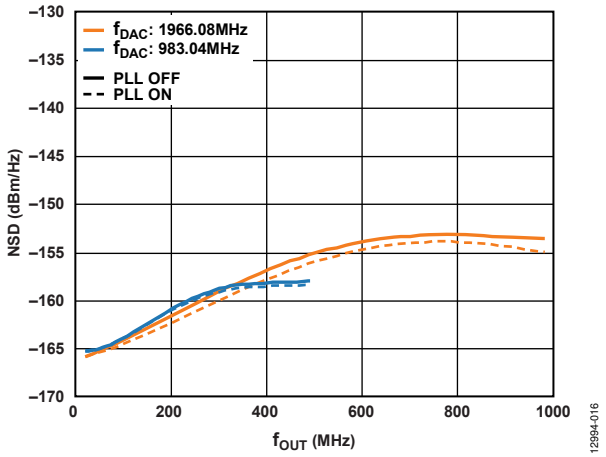

Figure 16. Single Tone NSD vs. f_{OUT}, PLL On and Off

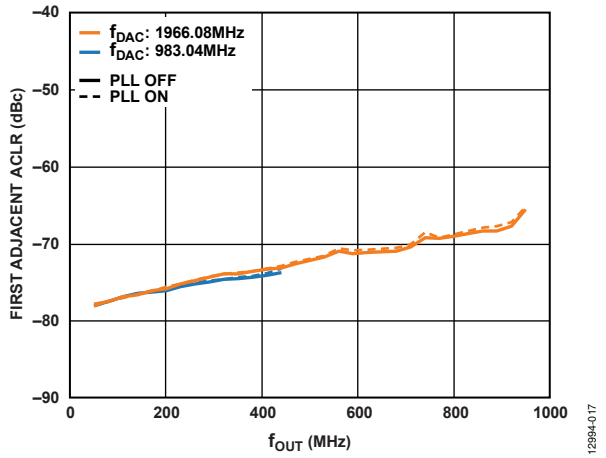

Figure 17. One-Carrier (1C) 5 MHz Bandwidth LTE, First Adjacent ACLR vs. f_{OUT}, PLL On and Off

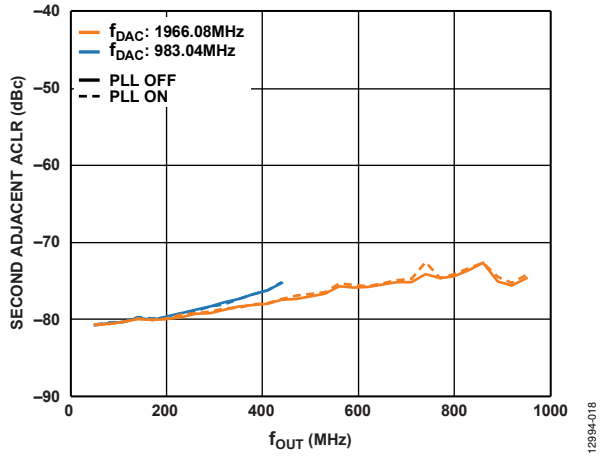

Figure 18. 1C 5 MHz Bandwidth LTE, Second Adjacent ACLR vs. f_{OUT}, PLL On and Off

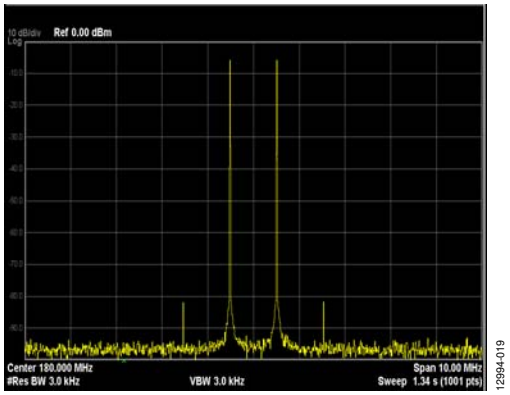

Figure 19. Two-Tone, Third-Order IMD Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

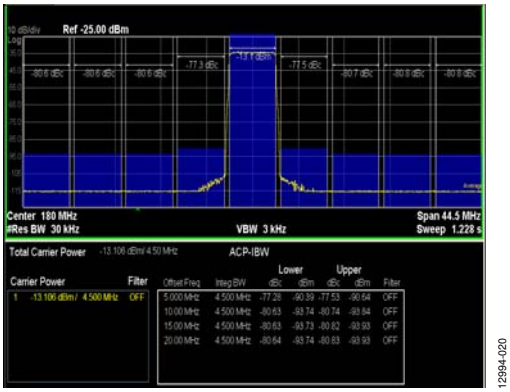

Figure 20. 1C 5 MHz Bandwidth LTE ACLR Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

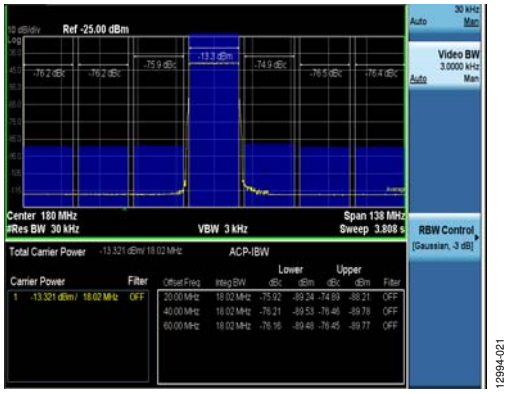

Figure 21. 1C 20 MHz Bandwidth LTE ACLR Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

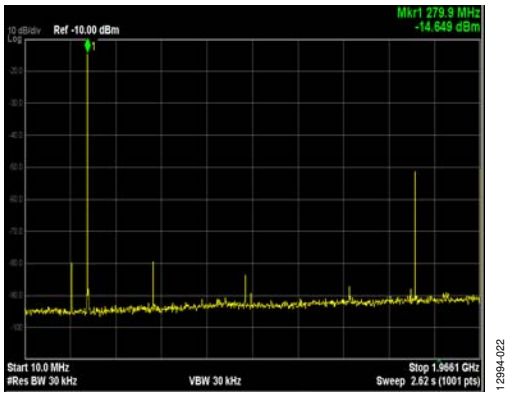

Figure 22. Single Tone, f_{DAC} =1966.08 MHz, f_{OUT} = 280 MHz, −14 dBFS

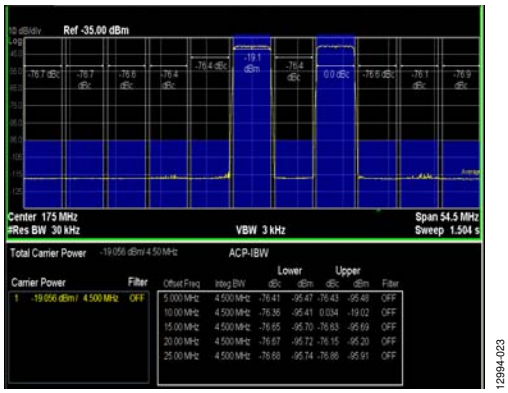

Figure 23. Two-Carrier (2C) 2× 5 MHz Bandwidth with 5 MHz Gap LTE ACLR Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

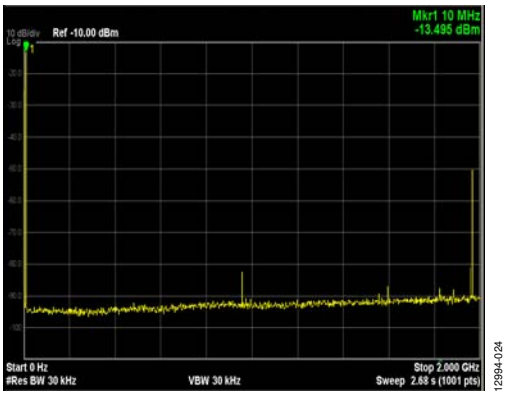

Figure 24. Single Tone SFDR, f_{DAC} =1966.08 MHz, 4× Interpolation, f_{OUT} = 10 MHz, −14 dBFS

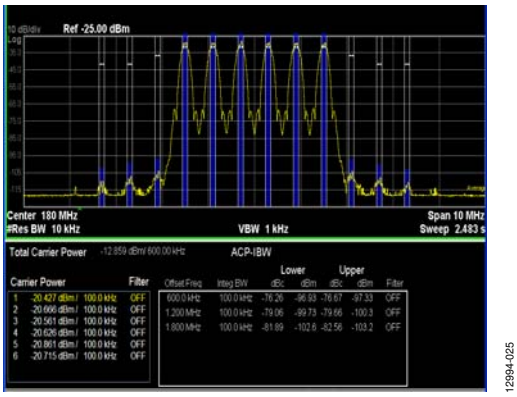

Figure 25. Six-Carrier (6C) Spaced by 600 kHz GSM Edge ACP Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

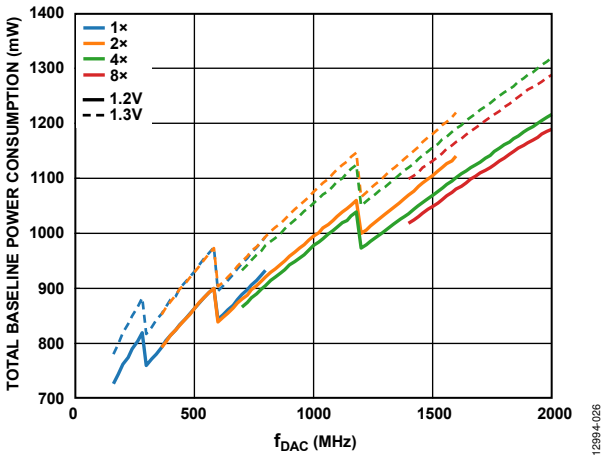

Figure 26. Total Baseline Power Consumption vs. f_{DAC} over Interpolation

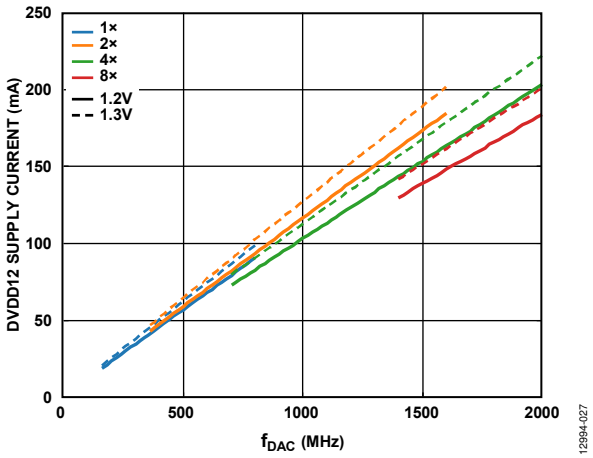

Figure 27. DVDD12 Supply Current vs. f_{DAC} over Interpolation

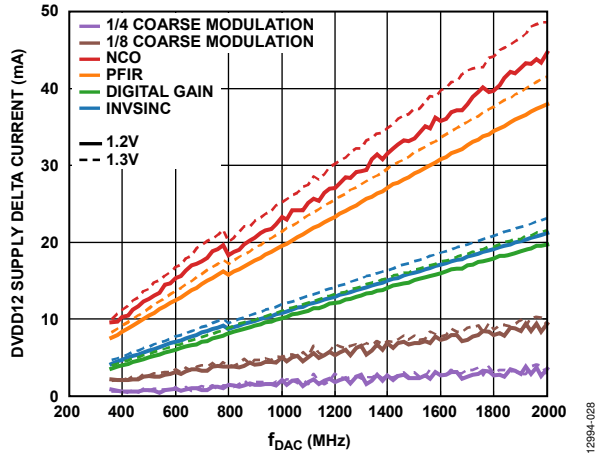

Figure 28. DVDD12 Supply Delta Current vs. f_{DAC} over Digital Functions

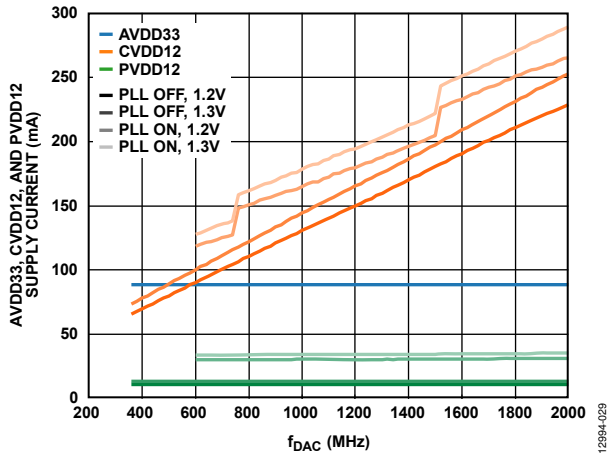

Figure 29. AVDD33, CVDD12, PVDD12 Supply Current vs. f_{DAC}

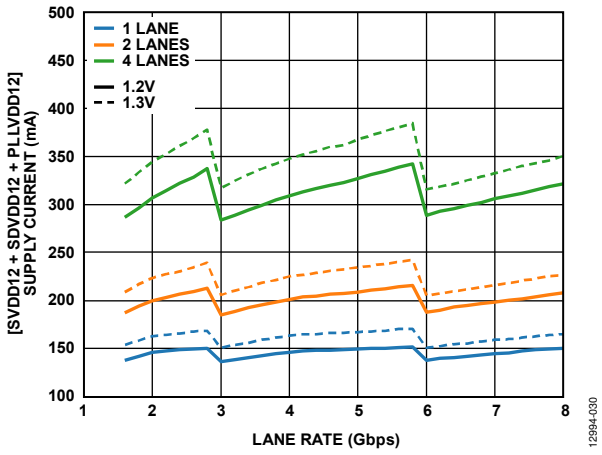

Figure 30. Total SERDES Supply Current (SVDD12, SDVDD12, PLLVDD12) vs. Lane Rate; One, Two, and Four Lanes

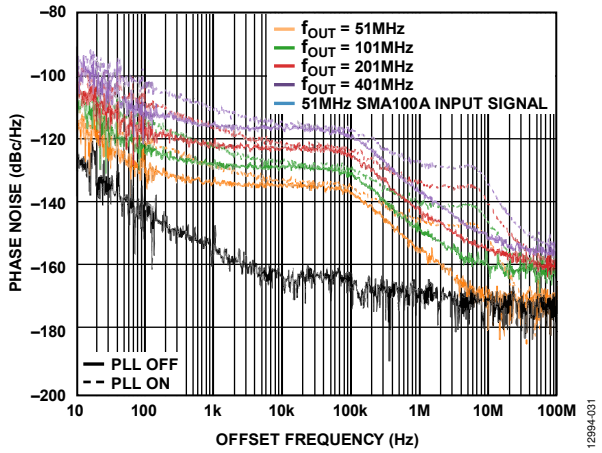

Figure 31. Single Tone Phase Noise vs. Offset Frequency at Four f_{OUT} Values and with an SMA100A Signal Generator, f_{DAC} = 1.96608 GHz, PLL On and Off

THEORY OF OPERATION

The AD9152 is a 16-bit, dual DAC with a SERDES interface. Figure 2 shows a detailed functional block diagram of the AD9152. Four high speed serial lanes carry data at a maximum speed of 12.38 Gbps, and a 1.238 GSPS input data rate to the DACs. Compared to either LVDS or CMOS interfaces, the SERDES interface simplifies pin count, board layout, and input clock requirements to the device.

The clock for the input data is derived from the device clock (required by the JESD204B specification). This device clock can be sourced with a PLL reference clock used by the on-chip PLL to generate a DAC clock, a high fidelity direct external DAC sampling clock, or a 2× DAC frequency RF clock. The device can be configured to operate in one-, two-, or four-lane modes, depending on the required input data rate.

The digital datapath of the AD9152 offers four interpolation modes (1×, 2×, 4×, and 8×) through three half-band filters with a maximum DAC sample rate of 2.25 GSPS. An inverse sinc filter compensates for sinc related roll-off. The PFIR filter compensates the gain over frequency in a more flexible way.

The AD9152 DAC cores provide a fully differential current output with a nominal full-scale current of 20 mA. The full-scale current, I_{OUTFS}, is user adjustable to between 4.04 mA and 20.22 mA, typically. The differential current outputs are complementary and are optimized for easy integration with the Analog Devices ADRF6720 AQM. The AD9152 is capable of multichip synchronization that can both synchronize multiple DACs and establish a constant and deterministic latency (latency locking) path for the DACs. The latency for each of the DACs remains constant from link establishment to link establishment. An external alignment (SYSREF±) signal makes the AD9152 Subclass 1 compliant. Several modes of SYSREF± signal handling are available for use in the system.

An SPI configures the various functional blocks and monitors their statuses. The various functional blocks and the data interface must be set up in a specific sequence for proper operation (see the Device Setup Guide section). Simple SPI initialization routines set up the JESD204B link and are included in the evaluation board package. The following sections describe the various blocks of the AD9152 in greater detail. Descriptions of the JESD204B interface, control parameters, and various registers to set up and monitor the device are provided. The recommended start-up routine reliably sets up the data link.

SERIAL PORT OPERATION

The serial port is a flexible, synchronous serial communications port that allows easy interfacing with many industry-standard microcontrollers and microprocessors. The serial input/output is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9152. MSB first or LSB first transfer formats are supported. The serial port interface is a 4-wire or a 3-wire (by default) interface in which the input and output share a single-pin input/output (SDIO).

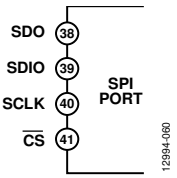

Figure 32. Serial Port Interface Pins

There are two phases to a communication cycle with the AD9152. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first 16 SCLK rising edges. The instruction word provides the serial port controller with information regarding the data transfer cycle, Phase 2 of the communication cycle. The Phase 1 instruction word defines whether the upcoming data transfer is a read or write, along with the starting register address for the following data transfer.

A logic high on the $\overline{CS}$ pin followed by a logic low resets the serial port timing to the initial state of the instruction cycle. From this state, the next 16 rising SCLK edges represent the instruction bits of the current input/output operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one or more data bytes. Eight × N SCLK cycles are needed to transfer N bytes during the transfer cycle. Registers change immediately upon writing to the last bit of each transfer byte, except for the frequency tuning word (FTW) and the numerically controlled oscillator (NCO) phase offsets, which change only when the frequency tuning word (FTW) FTW_UPDATE_REQ bit (Register 0x113, Bit 0) is set.

DATA FORMAT

The instruction byte contains the information shown in Table 13.

Table 13. Serial Port Instruction Word

I15 (MSB)	I[14:0]
R/$\overline{W}$	A[14:0]

R/$\overline{W}$, Bit 15 of the instruction word, determines whether a read or a write data transfer occurs after the instruction word write. Logic 1 indicates a read operation, and Logic 0 indicates a write operation.

A14 to A0, Bit 14 to Bit 0 of the instruction word, determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, [A14:0] is the starting address. The remaining register addresses are generated by the device based on the address increment bits (Register 0x000, Bit 5 and Bit 2). If the address increment bits are set high, multibyte SPI writes start on A[14:0] and increment by 1 every 8 bits sent/received. If the address increment bits are set to 0, the address decrements by 1 every 8 bits.

SERIAL PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is 10 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

An active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDIO pin goes to a high impedance state when this input is high. During the communication cycle, chip select must stay low.

Serial Data Input/Output (SDIO)

This pin is a bidirectional data line. In 4-wire mode, this pin acts as the data input and SDO acts as the data output.

SERIAL PORT OPTIONS

The serial port can support both MSB first and LSB first data formats. This functionality is controlled by the LSB first bits (Register 0x000, Bit 6 and Bit 1). The default is MSB first (the LSB first bits = 0).

When the LSB first bits = 0 (MSB first), the instruction and data bits are written from MSB to LSB. R/$\overline{W}$ is followed by A[14:0] as the instruction word, and D[7:0] is the data-word. When the LSB first bits = 1 (LSB first), the opposite is true. A[0:14] is followed by R/$\overline{W}$, which is subsequently followed by D[0:7].

The serial port supports a 3-wire or 4-wire interface. When the SDO active bits = 1 (Register 0x000, Bit 4 and Bit 3), a 4-wire interface with a separate input pin (SDIO) and output pin (SDO) is used. When the SDO active bits = 0, the SDO pin is unused and the SDIO pin is used for both input and output.

Multibyte data transfers can be performed as well. This is achieved by holding the $\overline{CS}$ pin low for multiple data transfer cycles (eight SCLKs) after the first data transfer word following the instruction cycle. The first eight SCLKs following the instruction cycle read from or write to the register provided in the instruction cycle. For each additional eight SCLK cycles, the address is either incremented or decremented and the read/write occurs on the new register. The direction of the address can be set using the address increment bits (Register 0x000, Bit 5 and Bit 2). When the address increment bits are 1, the multicycle addresses are incremented. When the address increment bits are 0, the addresses are decremented. A new write cycle can always be initiated by bringing $\overline{CS}$ high and then low again.

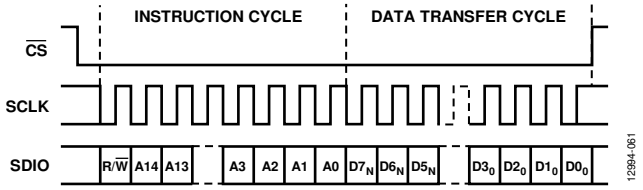

Figure 33. Serial Register Interface Timing, MSB First, Register 0x000, Bit 5 and Bit 2 = 0

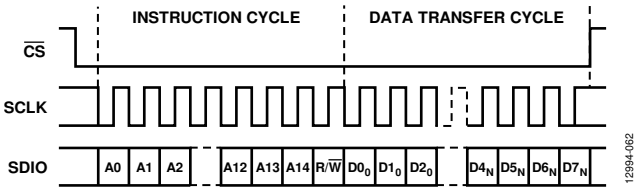

Figure 34. Serial Register Interface Timing, LSB First, Register 0x000, Bit 5 and Bit 2 = 1

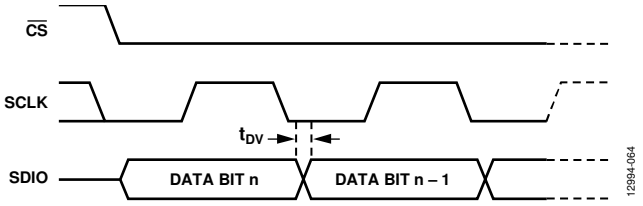

Figure 35. Timing Diagram for Serial Port Register Read

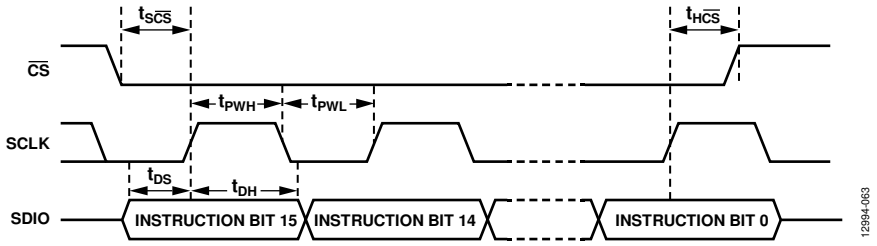

Figure 36. Timing Diagram for Serial Port Register Write

CHIP INFORMATION

Register 0x003 to Register 0x006 contain chip information, as shown in Table 14.

Table 14. Chip Information

Information	Description
Chip Type	Register 0x003. The product type is high speed DAC, which is represented by a code of 0x04.
Product ID	8 MSBs in Register 0x005 and 8 LSBs in Register 0x004. The product ID is 0x9152.
Device Revision	Register 0x006, Bits[4:0]. The device revision is 0x8.

DEVICE SETUP GUIDE

OVERVIEW

The sequence of steps to properly set up the AD9152 is as follows:

1. Set up the SPI interface, power up necessary circuit blocks, make the required writes to the configuration registers, and set up the DAC clocks (see Step 1: Start Up the DAC).
2. Set the digital features (see Step 2: Digital Datapath).
3. Set up the JESD204B links (see Step 3: Transport Layer).
4. Set up the physical layer of the SERDES interface (see Step 4: Physical Layer).
5. Set up the data link layer of the SERDES interface (see Step 5: Data Link Layer).
6. Check for errors (see Step 6: Optional Error Monitoring).
7. Optionally, enable any needed features as described in Step 7: Optional Features.

A specific working start-up sequence example is given in the Example Start-Up Sequence section.

The register writes listed in Table 15 to Table 23 give the register writes necessary to set up the AD9152. Consider printing this setup guide and filling in the Value column with appropriate variable values for the conditions of the desired application.

The notation 0x indicates register settings that the user must fill in. To fill in the unknown register values, select the correct settings for each variable listed in the Variable column. The Description column describes how to set variables or provides a link to a section where this is described. Register settings with specified values are fixed settings to be used in all cases. A variable is noted by concatenating multiple terms. For example, PdDACs is a variable that corresponds to the value determined for Register 0x011, Bits[6:5].

STEP 1: START UP THE DAC

This section describes how to set up the SPI interface, power up necessary circuit blocks, write to the required configuration registers, and set up the DAC clocks.

Table 15. Power-Up and DAC Initialization Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x000		0xBD		Soft reset.
0x000		0x3C		Deassert reset, set 4-wire SPI.
0x011		0x		
	7	0		Power up band gap.
	[6:5]		PdDACs	PdDACs = 0 if both DACs are used. If not, see the DAC Power-Down Setup section.
	4	0		Power up digital clocks.
	[3:2]		PdCLKs	PdCLKs = 0 if both DACs are used.
	1	0		Power up the PCLK.
	0	0		Power up the clock receiver.
0x080		0x		
	2		DUTY_EN	DUTY_EN = 1 if using the duty function.
0x081		0x		
	4		PdSysref	PdSysref = 0x0 for Subclass 1. PdSysref = 0x1 for Subclass 0. See the Subclass Setup section.
0x1CD[2]		0xD8		Band gap configuration.

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.
[2] Register 0x1CD must be set to the recommended value and does not appear in the register map.

The following registers must be written to and values changed from default for the device to work correctly and must be written after any soft reset, hard reset, or power-up occurs. All registers in Table 16 do not appear in the register map.

Table 16. Required SERDES PLL Register Settings

Address	Value[1]	Description
0x284	0x62	SERDES PLL configuration
0x285	0xC9	SERDES PLL configuration
0x286	0xE	SERDES PLL configuration
0x287	0x12	SERDES PLL configuration
0x28A	0x	See Table 36
0x28B	0x0	SERDES PLL configuration
0x290	0x89	SERDES PLL configuration
0x291	0x	See Table 36
0x294	0x24	SERDES PLL configuration
0x296	0x	See Table 36
0x297	0xD	SERDES PLL configuration
0x299	0x2	SERDES PLL configuration
0x29A	0x8E	SERDES PLL configuration
0x29C	0x2A	SERDES PLL configuration
0x29F	0x7E	SERDES PLL configuration
0x2A0	0x6	SERDES PLL configuration

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

If using the optional DAC PLL, also set the registers in Table 17 and Table 18. The registers in Table 17 optimize the performance of the SERDES PLL and must be set to the fixed value as required. Some registers in Table 17 do not appear in the register map.