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Quad, 16-Bit, 2.4 GSPS, TxDAC+® Digital-to-Analog Converter

Data Sheet **AD9154**

FEATURES

- Supports input data rates up to 1.096 GSPS
- Proprietary, low spurious and distortion design
  - Single carrier LTE 20 MHz bandwidth (BW), ACLR = 77 dBc at 180 MHz IF
  - Six carrier GSM IMD = 78 dBc, 600 kHz carrier spacing at 180 MHz IF
  - SFDR = 72 dBc at 180 MHz IF, −6 dBFS single tone
- Flexible 8-lane JESD204B interface
- Multiple chip synchronization
  - Fixed latency
  - Data generator latency compensation
- Input signal power detection
- High performance, low noise phase-locked loop (PLL) clock multiplier
- Digital inverse sinc filter
- Digital quadrature modulation using a numerically controlled oscillator (NCO)
- Nyquist band selection—mix mode
- Selectable 1×, 2×, 4×, and 8× interpolation filters
- Low power: 2.11 W at 1.6 GSPS, full operating conditions
- 88-lead, exposed pad LFCSP

APPLICATIONS

- Wireless communications
  - Multicarrier LTE and GSM base stations
  - Wideband repeaters
  - Software defined radios
- Wideband communications
  - Point to point microwave radio
- Transmit diversity, multiple input/multiple output (MIMO)
- Instrumentation
- Automated test equipment

FUNCTIONAL BLOCK DIAGRAM

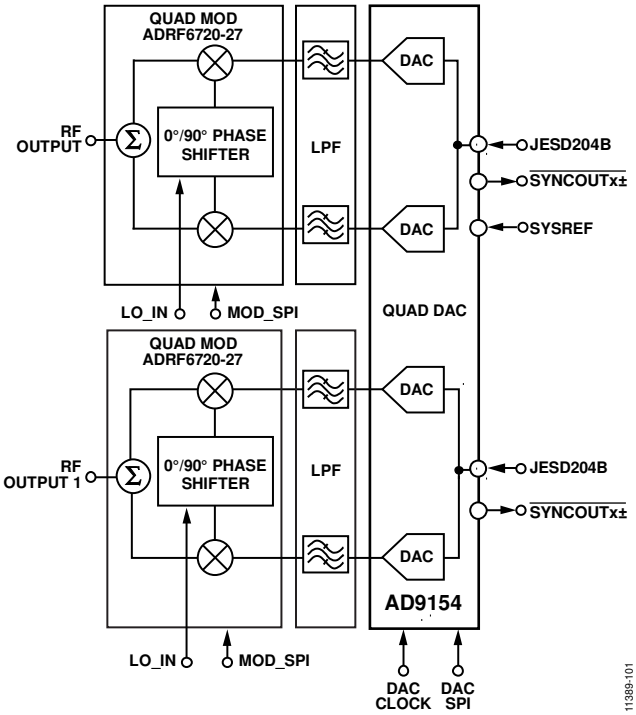

Figure 1.

GENERAL DESCRIPTION

The AD9154 is a quad, 16-bit, high dynamic range digital-to-analog converter (DAC) that provides a maximum sample rate of 2.4 GSPS, permitting multicarrier generation up to the Nyquist frequency in baseband mode. The AD9154 includes features optimized for direct conversion transmit applications, including complex digital modulation, input signal power detection, and gain, phase, and offset compensation. The DAC outputs are optimized to interface seamlessly with the ADRF6720-27 radio frequency quadrature modulator (AQM) from Analog Devices, Inc. In mix mode, the AD9154 DAC can reconstruct carriers in the second and third Nyquist zones. A serial port interface (SPI) provides the programming/readback of internal parameters.

The full-scale output current can be programmed over a range of 4 mA to 20 mA. The AD9154 is available in two different 88-lead LFCSP packages.

PRODUCT HIGHLIGHTS

1. Ultrawide signal bandwidth enables emerging wideband and multiband wireless applications.
2. Advanced low spurious and distortion design techniques provide high quality synthesis of wideband signals from baseband to high intermediate frequencies.
3. JESD204B Subclass 1 support simplifies multichip synchronization.
4. Small package size with a 12 mm × 12 mm footprint.

Rev. C Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD9154* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- Evaluation board for evaluating AD9154 Quad, 16-Bit, 2.4 GSPS, TxDAC+®Digital-to-Analog Product

DOCUMENTATION

Data Sheet

- AD9154: Quad, 16-Bit, 2.4 GSPS, TxDAC+® Digital-to-Analog Converter

TOOLS AND SIMULATIONS

- AD9144/AD9152/AD9154/AD9135/AD9136 AMI Model Download
- AD9154 IBIS Model

REFERENCE MATERIALS

Press

- Industry's Highest Dynamic-Range Quad, 16-bit D/A Converter Supports All Wireless and Mobile Device Frequency Standards

Technical Articles

- Digital Signal Process in IF RF Data Converters

DESIGN RESOURCES

- AD9154 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9154 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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3/2015—Rev. 0 to Rev. A

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2/2015—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

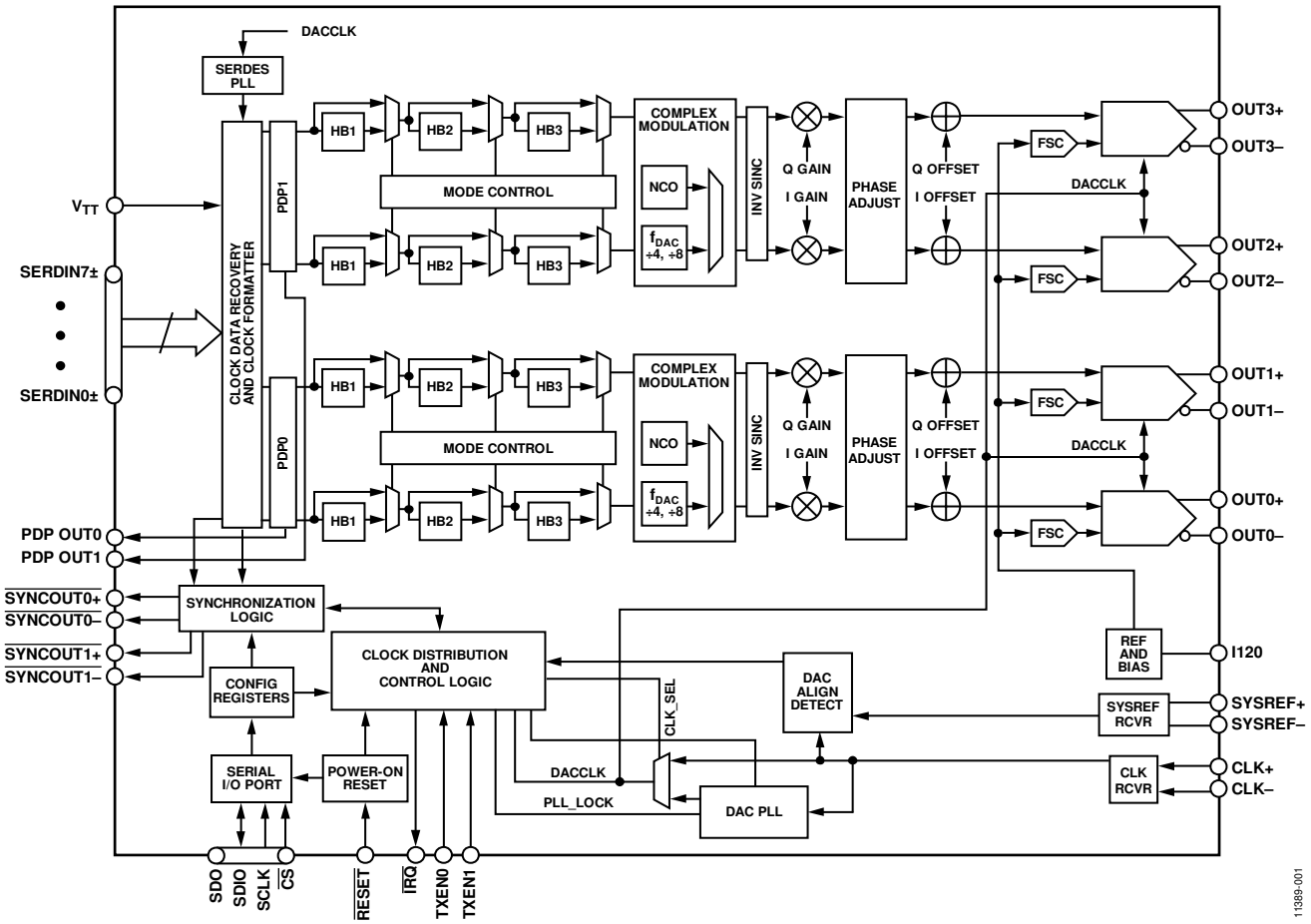


Figure 2. Detailed Functional Block Diagram

SPECIFICATIONS

DC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION			16		Bits
ACCURACY					
Differential Nonlinearity (DNL)			±4.3		LSB
Integral Nonlinearity (INL)			±8.2		LSB
MAIN DAC OUTPUTS					
Gain Error	With internal reference	−8.0	−3.01	+8.0	% FSR
Offset Error[1]			2322		ppm
I/Q Gain Mismatch		−3.0	+0.54	+3.0	% FSR
Full-Scale Output Current	Based on a 4 kΩ external resistor between I120 and ground				
Maximum Setting		19.9	20.85	21.3	mA
Minimum Setting		3.9	4.17	4.4	mA
Output Compliance Range		2.0	2.8	3.37	V
Output Resistance			15		MΩ
Output Capacitance			3.0		pF
Full-Scale Current DAC Monotonicity			Guaranteed		
MAIN DAC TEMPERATURE DRIFT					
Gain[2]			−114		ppm/°C
REFERENCE					
Internal Reference Voltage			1.2		V
ANALOG SUPPLY VOLTAGES					
AVDD33	5%	3.13	3.3	3.47	V
PVDD12	5%	1.14	1.2	1.26	V
	2%	1.274	1.3	1.326	V
CVDD12	5%	1.14	1.2	1.26	V
	2%	1.274	1.3	1.326	V
DIGITAL SUPPLY VOLTAGES					
SIOVDD33	5%	3.13	3.3	3.47	V
V_{TT}		1.1	1.2	1.37	V
DVDD12	5%	1.14	1.2	1.26	V
	2%	1.274	1.3	1.326	V
SVDD12	5%	1.14	1.2	1.26	V
	2%	1.274	1.3	1.326	V
IOVDD	5%	1.71	1.8	3.47	V
POWER CONSUMPTION					
2× Interpolation Mode, JESD204B Mode 4, Dual Link, 8 SERDES Lanes	f_{DAC} = 1.6 GSPS, NCO on, IF_{OUT} = 40 MHz, PLL on, DAC full-scale current = 20 mA		2.11	2.63	W
AVDD33			159	185	mA
PVDD12			152	174	mA
CVDD12			355	397	mA
SVDD12	Includes V_{TT}		541.9	682	mA
DVDD12			264.5	442	mA
SIOVDD33 + IOVDD			10.6	11.4	mA

[1] Offset error is a measure of how far from full-scale range (FSR) the DAC output current is at 25°C (in ppm).
[2] Gain drift is a measure of the slope of the DAC output current across its full temperature range (in ppm/°C).

DIGITAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL						
Input Voltage (V_{IN}) Logic						
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.7 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.3 × IOVDD	V
CMOS OUTPUT LOGIC LEVEL						
Output Voltage (V_{OUT}) Logic						
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.7 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.3 × IOVDD	V
MAXIMUM DAC UPDATE RATE[1]		1× interpolation[2] (see Table 4)	1096			MSPS
		2× interpolation[3]	2192			MSPS
		4× interpolation	2400			MSPS
		8× interpolation	2400			MSPS
ADJUSTED DAC UPDATE RATE		1× interpolation	1096			MSPS
		2× interpolation	1096			MSPS
		4× interpolation	600			MSPS
		8× interpolation	300			MSPS
INTERFACE[4]						
Number of JESD204B Lanes				8		Lanes
JESD204B Serial Interface Speed						
Minimum		Per lane			1.44	Gbps
Maximum		Per lane, SVDD12 = 1.3 V ± 2%	10.96			Gbps
DAC CLOCK INPUT (CLK±)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage		Self biased input, ac-coupled		600		mV
Maximum Clock Rate, DAC Clock Sourced Directly from CLK±			2400			MHz
PLL Multiplier Mode Clock Input Frequency[5]		6.0 GHz ≤ f_{VCO} ≤ 12.0 GHz	35		1000	MHz
SYSREF INPUT (SYSREF±)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage			0		2000	mV
SYSREF± Frequency[6]					$f_{DATA}/(K \times (F/S))$	Hz
SYSREF± TO DAC CLOCK[7]		SYSREF± differential swing = 0.4 V, slew rate = 1.3 V/ns, (ac-coupled, and 0 V, 0.6 V, 1.25 V, 2.0 V dc-coupled common-mode voltages)				
Setup Time	t_{SSD}		111			ps
Hold Time	t_{HSD}		145			ps
SPI		See timing diagrams shown in Figure 39 and Figure 40				
Maximum Clock Rate	SCLK	IOVDD = 1.8 V	10			MHz
Minimum SCLK Pulse Width						
High	t_{PWH}				8	ns
Low	t_{PWL}				12	ns
SDIO to SCLK						
Setup Time	t_{DS}		5			ns
Hold Time	t_{DH}		2			ns
SDO to SCLK						
Data Valid Window	t_{DV}		25			ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
$\overline{CS}$ to SCLK						
Setup Time	$t_{S\overline{CS}}$		5			ns
Hold Time	$t_{HCS\overline{CS}}$		2			ns

[1] See Table 3 for detailed specifications for DAC update rate conditions.
[2] Maximum speed for 1× interpolation is limited by the JESD204B interface. See Table 4 for details.
[3] Maximum speed for 2× interpolation is limited by the JESD204B interface. See Table 4 for details.
[4] See Table 4 for detailed specifications for JESD204B speed conditions.
[5] CLK+/CLK– serve as a reference oscillator input for the on-chip PLL clock multiplier when in use.
[6] K, F, and S are JESD204B transport layer parameters. See Table 42 for the full definitions.
[7] See Table 5 for detailed specifications for SYSREF to DAC clock timing conditions.

MAXIMUM DAC UPDATE RATE SPEED SPECIFICATIONS BY SUPPLY

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DAC UPDATE RATE	DVDD12, CVDD12, PVDD12 = 1.2 V ± 5%	1.93			GSPS
	DVDD12, CVDD12, PVDD12 = 1.2 V ± 2%	2.07			GSPS
	DVDD12, CVDD12, PVDD12 = 1.3 V ± 2%	2.4			GSPS

JESD204B SERIAL INTERFACE SPEED SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK AND DATA RECOVERY (CDR) HALF RATE MODE	SVDD12 = 1.2 V ± 5%	5.74		9.04	Gbps
	SVDD12 = 1.2 V ±2%	5.74		9.65	Gbps
	SVDD12 = 1.3 V ± 2%	5.74		10.96	Gbps
CDR FULL RATE MODE	SVDD12 = 1.2 V ± 5%	2.87		4.79	Gbps
	SVDD12 = 1.2 V ±2%	2.87		4.93	Gbps
	SVDD12 = 1.3 V ± 2%	2.87		5.73	Gbps
CDR OVERSAMPLING MODE	SVDD12 = 1.2 V ± 5%	1.44		2.39	Gbps
	SVDD12 = 1.2 V ±2%	1.44		2.50	Gbps
	SVDD12 = 1.3 V ± 2%	1.44		2.93	Gbps

SYSREF TO DAC CLOCK TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, SYSREF± common-mode voltages = 0.0 V, 0.6 V, 1.25 V, and 2.0 V, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSREF	Differential swing = 0.4 V, slew rate = 1.3 V/ns				
Setup Time	AC-coupled	89			ps
	DC-coupled	111			ps
Hold Time	AC-coupled	105			ps
	DC-coupled	145			ps
	Differential swing = 0.7 V, slew rate = 2.28 V/ns				
Setup Time	AC-coupled	71			ps
	DC-coupled	81			ps
Hold Time	AC-coupled	97			ps
	DC-coupled	118			ps
	Differential swing = 1.0 V, slew rate = 3.26 V/ns				
Setup Time	AC-coupled	58			ps
	DC-coupled	64			ps
Hold Time	AC-coupled	92			ps
	DC-coupled	108			ps

DIGITAL INPUT DATA TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LATENCY					
Interface, Excluding Transport Layer Delay Buffer			17		PClock[1] cycles
Interpolation	With or without modulation				
1×			94		DAC clock cycles
2×			130		DAC clock cycles
4×			250		DAC clock cycles
8×			474		DAC clock cycles
Inverse Sinc			17		DAC clock cycles
Fine Modulation			20		DAC clock cycles
Coarse Modulation					
$f_S/8$			8		DAC clock cycles
$f_S/4$			4		DAC clock cycles
Digital Phase Adjust			12		DAC clock cycles
Digital Gain Adjust			12		DAC clock cycles
Power-Up Time					
Dual A Only	Register 0x011 from 0x60 to 0x00		30		µs
Dual B Only	Register 0x011 from 0x18 to 0x00		30		µs
All DACs	Register 0x011 from 0x78 to 0x00		30		µs

[1] PClock is the AD9154 internal processing clock running at the JESD204B lane rate ÷ 40.

LATENCY VARIATION SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 7.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC LATENCY VARIATION					
Subclass 1					
PLL Off			0	1	DACCLK cycles
PLL On		−1		+1	DACCLK cycles

JESD204B INTERFACE ELECTRICAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 8.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B DATA INPUTS						
Input Leakage Current		T_A = 25°C				
Logic High		Input level = 1.2 V ± 0.25 V, V_{TT} = 1.2 V		10		µA
Logic Low		Input level = 0 V		−4		µA
Unit Interval	UI		94		714	ps
Common-Mode Voltage	V_{RCM}	AC-coupled V_{TT} = SVDD12[1]	−0.05		+1.85	V
Differential Voltage	R_V_{DIFF}		110		1050	mV
V_{TT} Source Impedance	Z_{TT}	At dc			30	Ω
Differential Impedance	Z_{RDIFF}	At dc	80	100	120	Ω
Differential Return Loss	RL_{RDIF}			8		dB
Common-Mode Return Loss	RL_{RCM}			6		dB
DIFFERENTIAL OUTPUTS ($\overline{SYNCOUT}$±)[2]						
Output Offset Voltage	V_{OS}		1.19		1.27	V
DETERMINISTIC LATENCY						
Fixed					17	PClock[3] cycles
Variable					2	PClock[3] cycles
SYSREF± TO LOCAL MULTIFRAME CLOCK (LMFC) DELAY				4		DAC clock cycles

[1] As measured on the input side of the ac coupling capacitor.
[2] IEEE Standard 1596.3 LVDS compatible.
[3] PClock is the AD9154 internal processing clock; its frequency is equal to the JESD204B lane rate ÷ 40.

AC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 9.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	−6 dBFS single tone				
f_{DAC} = 1966.08 MSPS	f_{OUT} = 20 MHz		76		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		73		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 180 MHz		72		dBc
TWO-TONE THIRD INTERMODULATION DISTORTION (IMD)	−6 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 30 MHz		87		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		77		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 30 MHz		86		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 180 MHz		78		dBc
NOISE SPECTRAL DENSITY (NSD), SINGLE TONE	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		−164		dBm/Hz
f_{DAC} = 1966.08 MSPS	f_{OUT} = 180 MHz		−163		dBm/Hz
5 MHz BW LTE FIRST ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER	0 dBFS, PLL off				
f_{DAC} = 1966.08 MSPS	f_{OUT} = 50 MHz		79		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		77		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 180 MHz		77		dBc
5 MHz BW LTE SECOND ACLR, SINGLE CARRIER	0 dBFS, PLL off				
f_{DAC} = 1966.08 MSPS	f_{OUT} = 50 MHz		82		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		81		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 180 MHz		81		dBc

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
I120 to Ground	−0.3 V to AVDD33 + 0.3 V
SERDINx±, V_{TT}, $\overline{SYNCOUTx}$±, and TXENx	−0.3 V to SIOVDD33 + 0.3 V
OUTx±	−0.3 V to AVDD33 + 0.3 V
SYSREF±	GND − 0.5 V
CLK± to Ground	−0.3 V to PVDD12 + 0.3 V
$\overline{RESET}$, $\overline{IRQ}$, $\overline{CS}$, SCLK, SDIO, SDO, and PDP OUTx to Ground	−0.3 V to IOVDD + 0.3 V
LDO_BYP1	−0.3 V to SVDD12 + 0.3 V
LDO_BYP2	−0.3 V to PVDD12 + 0.3 V
Ambient Operating Temperature (T_A)	−40°C to +85°C
Junction Temperature	125°C
Storage Temperature	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The exposed pad (EPAD) must be soldered to the ground plane for the 88-lead LFCSP. The EPAD provides an electrical, thermal, and mechanical connection to the board.

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer, JESD51-7 high effective thermal conductivity test board for leaded surface-mount packages. θ_{JA} is obtained in still air conditions (JESD51-2). Airflow increases heat dissipation, effectively reducing θ_{JA}. θ_{JB} is obtained following double-ring cold plate test conditions (JESD51-8). θ_{JC} is obtained with the test case temperature monitored at the bottom of the exposed pad.

Ψ_{JT} and Ψ_{JB} are thermal characteristic parameters obtained with θ_{JA} in still air test conditions.

Junction temperature (T_J) can be estimated using the following equations:

$$T_J = T_T + (\Psi_{JT} \times P),$$

or

$$T_J = T_B + (\Psi_{JB} \times P)$$

where:
T_T is the temperature measured at the top of the package.
P is the total device power dissipation.
T_B is the temperature measured at the board.

Table 11. Thermal Resistance

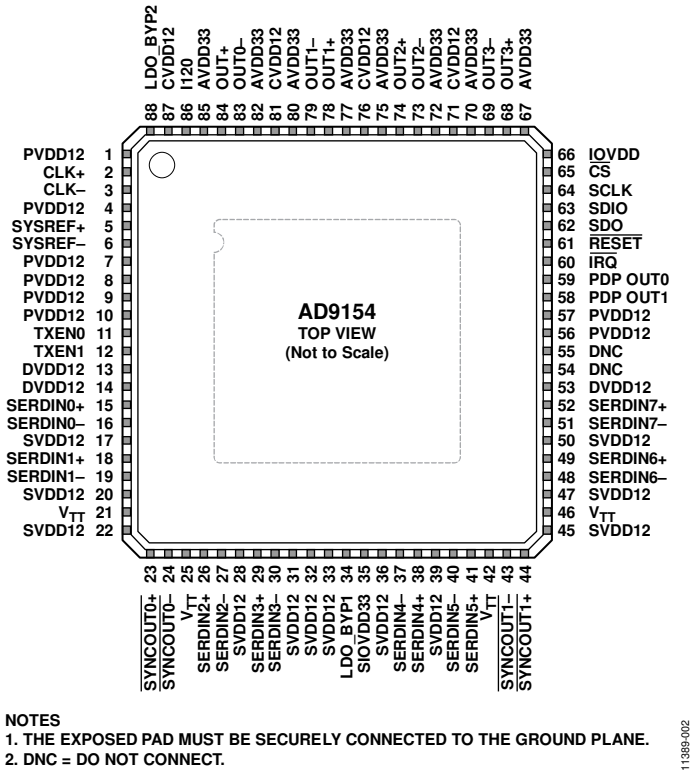
Package	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
88-Lead LFCSP[1]	22.6	5.59	1.17	0.1	5.22	°C/W

[1] The exposed pad must be securely connected to the ground plane.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE SECURELY CONNECTED TO THE GROUND PLANE.
2. DNC = DO NOT CONNECT.

11389-002

Figure 3. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 7, 8, 9, 10, 56, 57	PVDD12	1.2 V Clock Supplies.
2	CLK+	PLL Reference/Clock Input, Positive. When the PLL is used, this pin is the positive reference clock input. When the PLL is not used, this pin is the positive device clock input. This pin is self biased and must be ac-coupled.
3	CLK–	PLL Reference/Clock Input, Negative. When the PLL is used, this pin is the negative reference clock input. When the PLL is not used, this pin is the negative device clock input. This pin is self biased and must be ac-coupled.
5	SYSREF+	Timing Reference Input, Positive. This pin is used in JESD204B Subclass 1 systems and is self biased, ac-coupled, or dc-coupled.
6	SYSREF–	Timing Reference Input, Negative. This pin is used in JESD204B Subclass 1 systems and is self biased, ac-coupled, or dc-coupled.
11	TXEN0	Transmit enable for DAC0 and DAC1. CMOS levels are determined with respect to IOVDD.
12	TXEN1	Transmit Enable for DAC2 and DAC3. CMOS levels are determined with respect to IOVDD.
13, 14, 53	DVDD12	1.2 V Digital Supplies.
15	SERDIN0+	Serial Channel Input 0, Positive. CML compliant. SERDIN0+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
16	SERDIN0–	Serial Channel Input 0, Negative. CML compliant. SERDIN0– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
17, 20, 22, 28, 31, 32, 33, 36, 39, 45, 47, 50	SVDD12	1.2 V JESD204B Receiver Supplies.
18	SERDIN1+	Serial Channel Input 1, Positive. CML compliant. SERDIN1+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
19	SERDIN1–	Serial Channel Input 1, Negative. CML compliant. SERDIN1– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
21, 25, 42, 46	V_{TT}	1.2 V Termination Voltage Pins.

Pin No.	Mnemonic	Description
23	$\overline{\text{SYNCOUT0+}}$	Positive LVDS Synchronization Output Signal for Channel Link 0.
24	$\overline{\text{SYNCOUT0–}}$	Negative LVDS Synchronization Output Signal for Channel Link 0.
26	SERDIN2+	Serial Channel Input 2, Positive. CML compliant. SERDIN2+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
27	SERDIN2–	Serial Channel Input 2, Negative. CML compliant. SERDIN2– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
29	SERDIN3+	Serial Channel Input 3, Positive. CML compliant. SERDIN3+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
30	SERDIN3–	Serial Channel Input 3, Negative. CML compliant. SERDIN3– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
34	LDO_BYP1	LDO SERDES Bypass. This pin requires a 1 Ω resistor in series with a 1 µF capacitor to ground.
35	SIOVDD33	SERDES Ports Input/Output Supply.
37	SERDIN4–	Serial Channel Input 4, Negative. CML compliant. SERDIN4– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
38	SERDIN4+	Serial Channel Input 4, Positive. CML compliant. SERDIN4+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
40	SERDIN5–	Serial Channel Input 5, Negative. CML compliant. SERDIN5– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
41	SERDIN5+	Serial Channel Input 5, Positive. CML compliant. SERDIN5+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
43	$\overline{\text{SYNCOUT1–}}$	Negative LVDS Synchronization Output Signal for Channel Link 1.
44	$\overline{\text{SYNCOUT1+}}$	Positive LVDS Synchronization Output Signal for Channel Link 1.
48	SERDIN6–	Serial Channel Input 6, Negative. CML compliant. SERDIN6– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
49	SERDIN6+	Serial Channel Input 6, Positive. CML compliant. SERDIN6+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
51	SERDIN7–	Serial Channel Input 7, Negative. CML compliant. SERDIN7– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
52	SERDIN7+	Serial Channel Input 7, Positive. CML compliant. SERDIN7+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
54, 55	DNC	Do Not Connect. Do not connect to this pin.
58	PDP OUT1	Power Detection and Protection (PDP) Indicator for DAC2 and DAC3.
59	PDP OUT0	PDP Indicator for DAC0 and DAC1.
60	$\overline{\text{IRQ}}$	Interrupt Request (Active Low, Open Drain).
61	$\overline{\text{RESET}}$	Reset (Active Low). CMOS levels with are determined with respect to IOVDD.
62	SDO	Serial Port Data Output. CMOS levels with are determined with respect to IOVDD.
63	SDIO	Serial Port Data Input/Output. CMOS levels with are determined with respect to IOVDD.
64	SCLK	Serial Port Clock Input. CMOS levels with are determined with respect to IOVDD.
65	$\overline{\text{CS}}$	Serial Port Chip Select (Active Low). CMOS levels with are determined with respect to IOVDD.
66	IOVDD	CMOS Input/Output and SPI Pin Supply.
67, 70, 72, 75, 77, 80, 82, 85	AVDD33	3.3 V Analog Supplies for the DAC Cores.
68	OUT3+	DAC3 Positive Current Output.
69	OUT3–	DAC3 Negative Current Output.
71, 76, 81, 87	CVDD12	1.2 V Clock Supplies.
73	OUT2–	DAC2 Negative Current Output.
74	OUT2+	DAC2 Positive Current Output.
78	OUT1+	DAC1 Positive Current Output.
79	OUT1–	DAC1 Negative Current Output.
83	OUT0–	DAC0 Negative Current Output.
84	OUT0+	DAC0 Positive Current Output.
86	I120	Output Current Generation Pin for DAC Full-Scale Current. Tie a 4 kΩ resistor from this pin to ground.
88	LDO_BYP2	LDO Clock Bypass for the DAC PLL. Tie a 1 Ω resistor in series with a 1 µF capacitor from this pin to ground.
	EPAD	Exposed Pad. The exposed pad must be securely connected to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

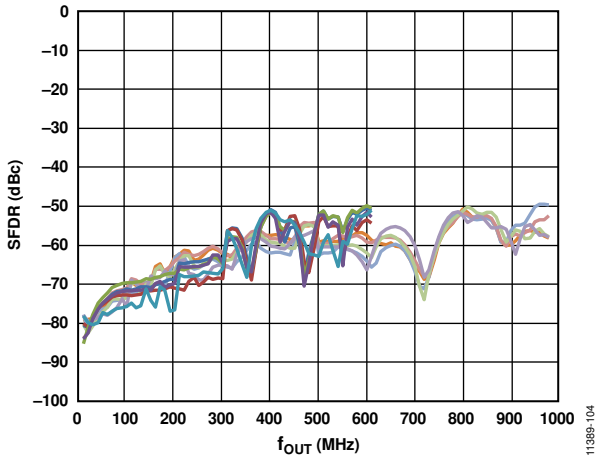


Figure 4. Single Tone (0 dBFS) SFDR vs. f_{OUT} in the First Nyquist Zone over f_{DAC} = 1966.08 MHz and 1228.80 MHz, All Four DAC Outputs

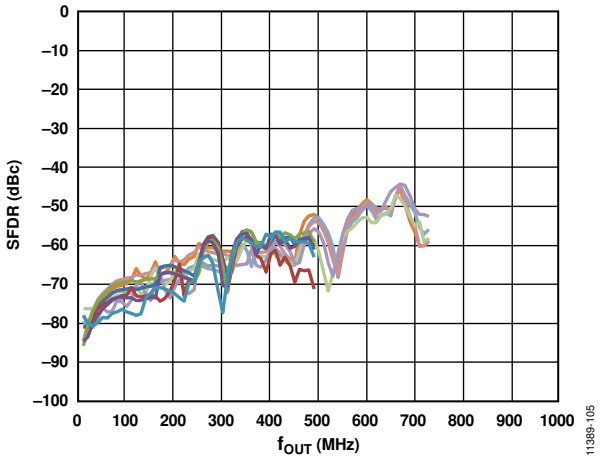


Figure 5. Single Tone (0 dBFS) SFDR vs. f_{OUT} in the First Nyquist Zone over f_{DAC} = 1474.56 MHz and 983.04 MHz, All Four DAC Outputs

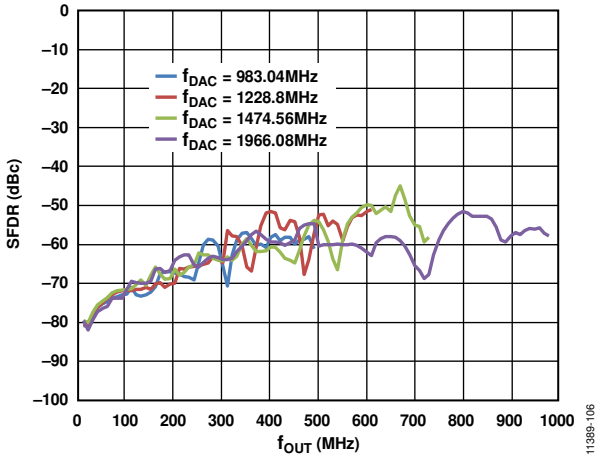


Figure 6. Single Tone (0 dBFS) SFDR vs. f_{OUT} in the First Nyquist Zone over f_{DAC} = 1966.08 MHz, 1474.56 MHz, 1228.8 MHz, and 983.04 MHz

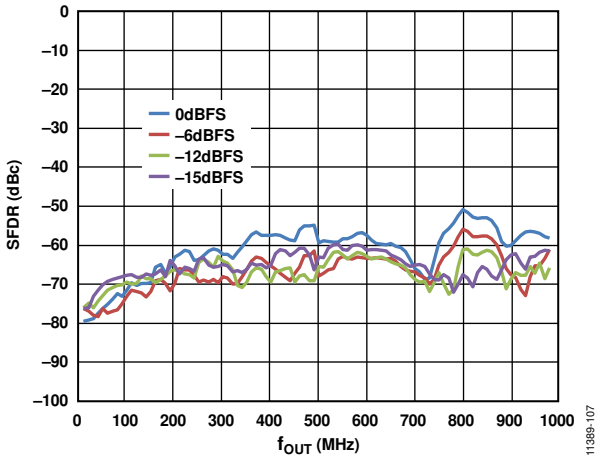


Figure 7. Single Tone SFDR vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 1966.08 MHz

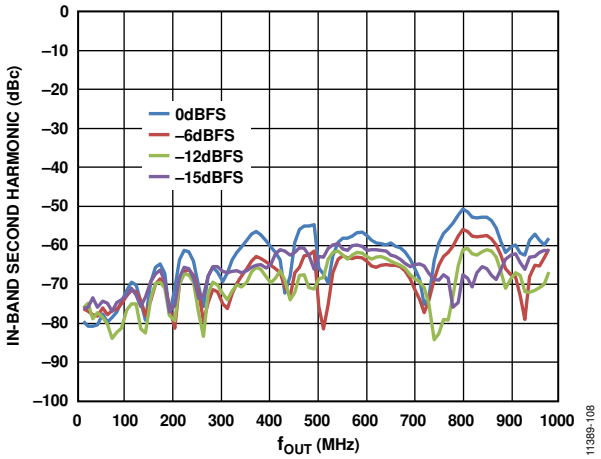


Figure 8. In-Band Second Harmonic vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 1966.08 MHz

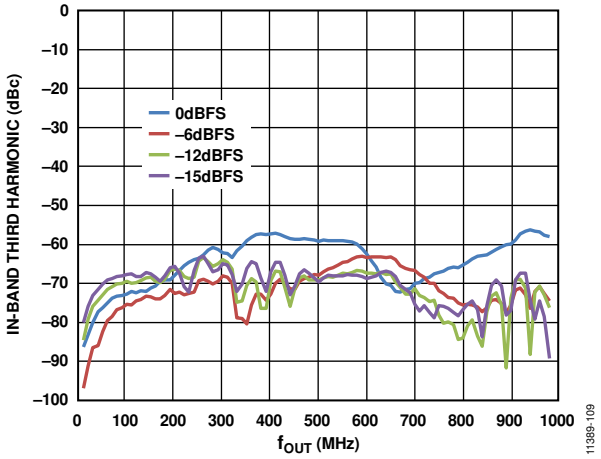


Figure 9. In-Band Third Harmonic vs. f_{OUT} in the First Nyquist Zone, f_{DAC} = 1966.08 MHz

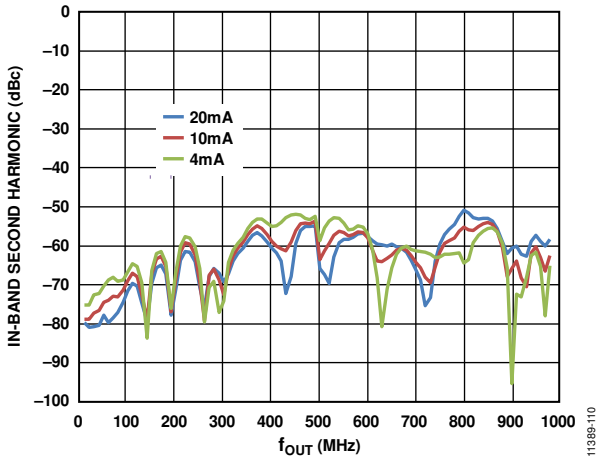


Figure 10. In-Band Second Harmonic vs. f_{OUT} in the First Nyquist Zone over Analog Full-Scale Current, f_{DAC} = 1966.08 MHz

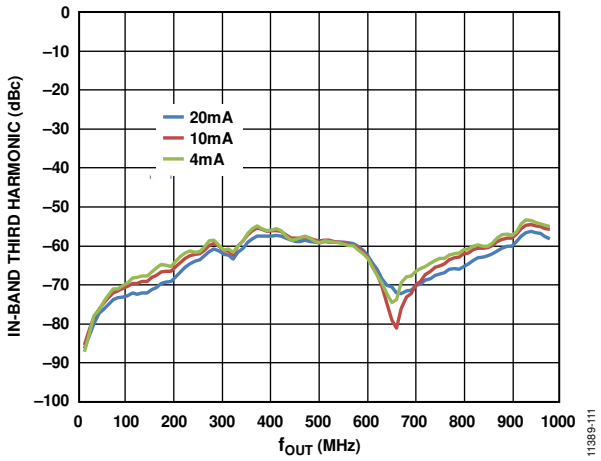


Figure 11. In-Band Third Harmonic vs. f_{OUT} in the First Nyquist Zone over Analog Full-Scale Current, f_{DAC} = 1966.08 MHz

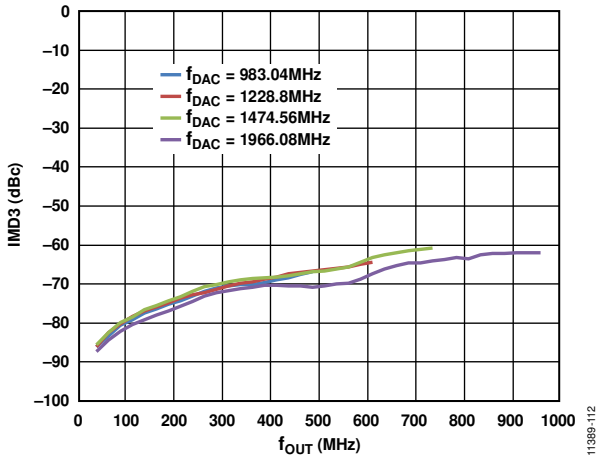


Figure 12. Two-Tone Third Harmonic (IMD3) vs. f_{OUT}, f_{DAC} = 1966.08 MHz, 1474.56 MHz, 1228.8 MHz, and 983.04 MHz

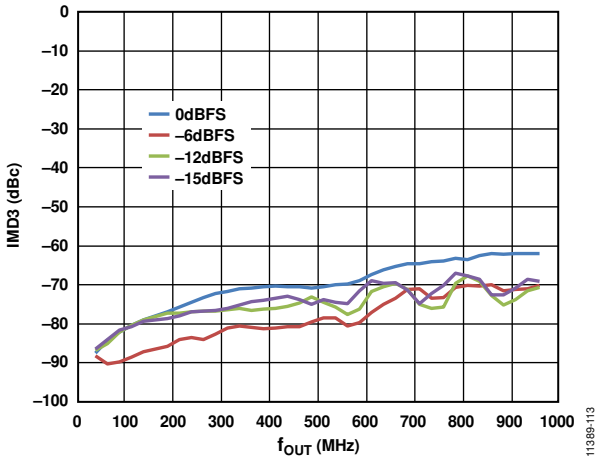


Figure 13. Two-Tone Third Harmonic (IMD3) vs. f_{OUT} over Digital Backoff

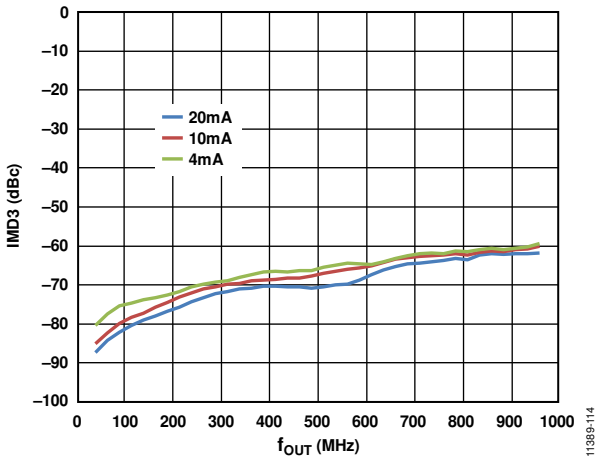


Figure 14. Two-Tone Third Harmonic (IMD3) vs. f_{OUT} over Analog Full-Scale Current, f_{DAC} = 1966.08 MHz

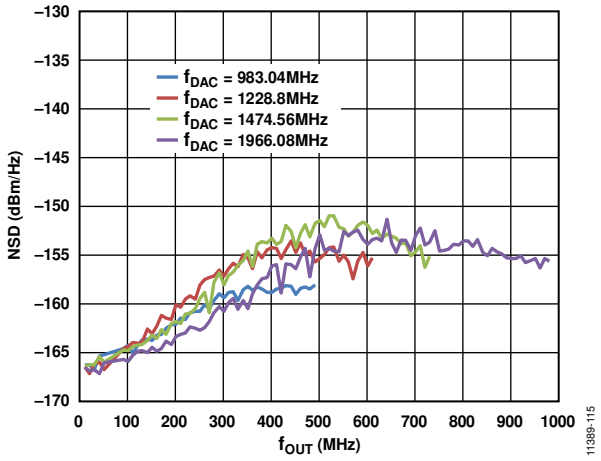


Figure 15. Single Tone (0 dBFS) NSD vs. f_{OUT} over f_{DAC} = 1966.08 MHz, 1474.56 MHz, 1228.8 MHz, and 983.04 MHz at 70 MHz

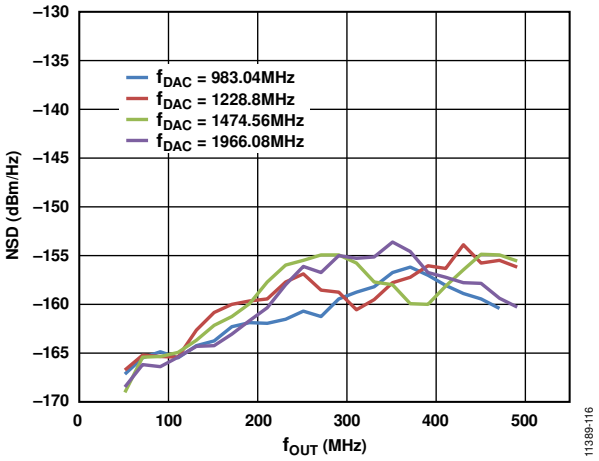


Figure 16. Single Tone (0 dBFS) NSD vs. f_{OUT} over f_{DAC}, 20 MHz Offset from Carrier

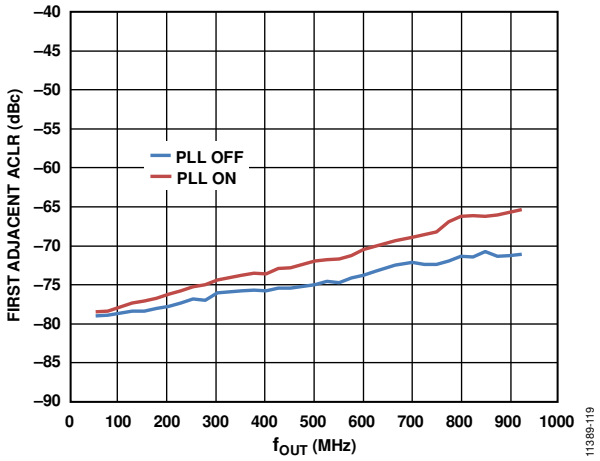


Figure 19. 1-Channel (1C) 5 MHz BW LTE, First Adjacent ACLR vs. f_{OUT}, PLL On and Off

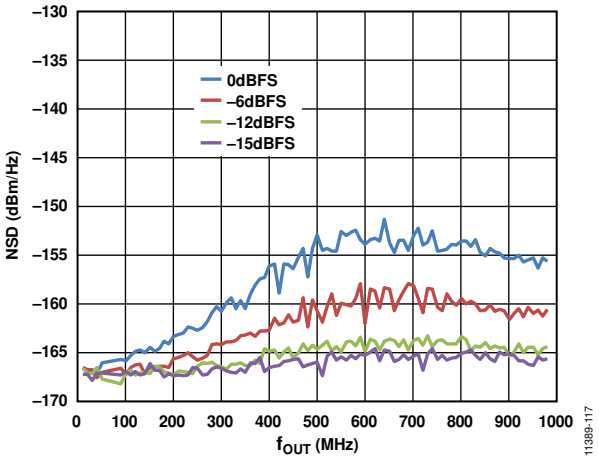


Figure 17. Single Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966.08 MHz, Measured at 70 MHz

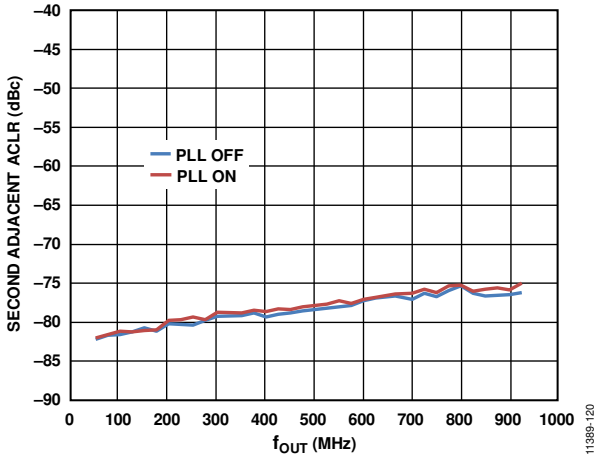


Figure 20. 1C 5 MHz BW LTE, Second Adjacent ACLR vs. f_{OUT}, PLL On and Off

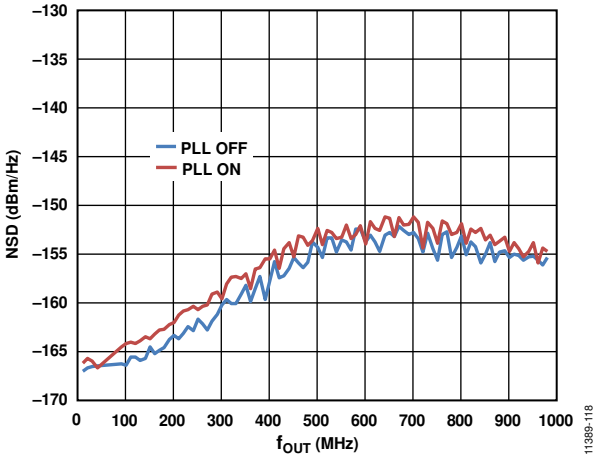


Figure 18. Single Tone NSD vs. f_{OUT}, f_{DAC} = 1966.08 MHz, Measured at 70 MHz, PLL On and Off

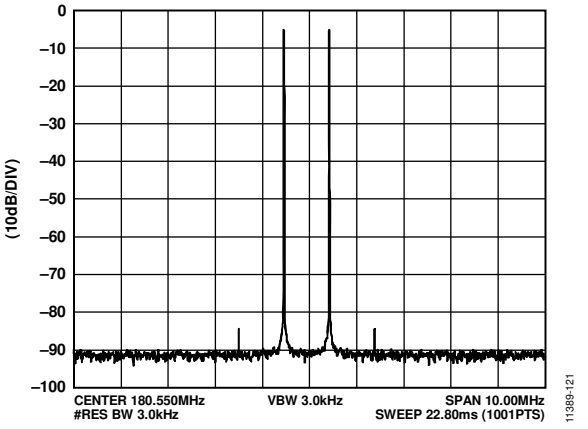


Figure 21. Two-Tone, Third IMD Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

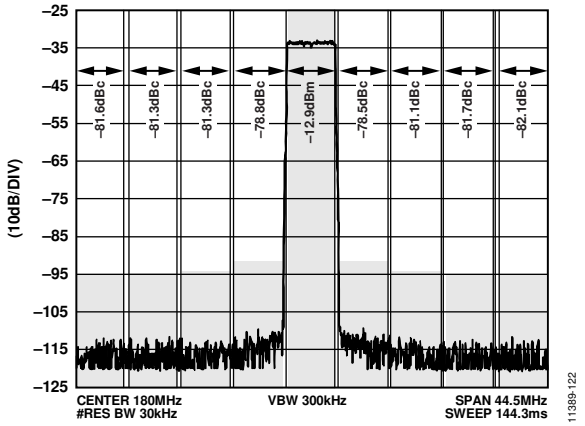


Figure 22. 1C 5 MHz BW LTE ACLR Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

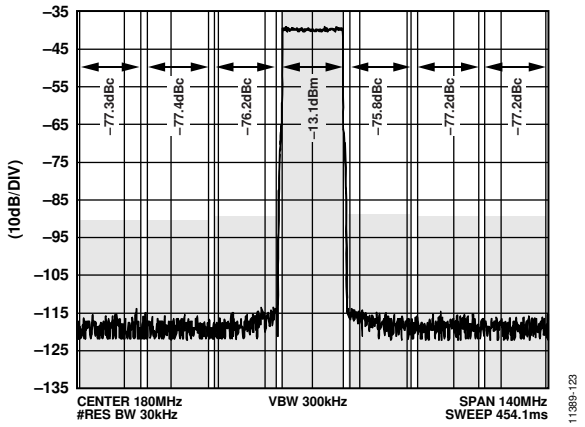


Figure 23. 1C 20 MHz BW LTE ACLR Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

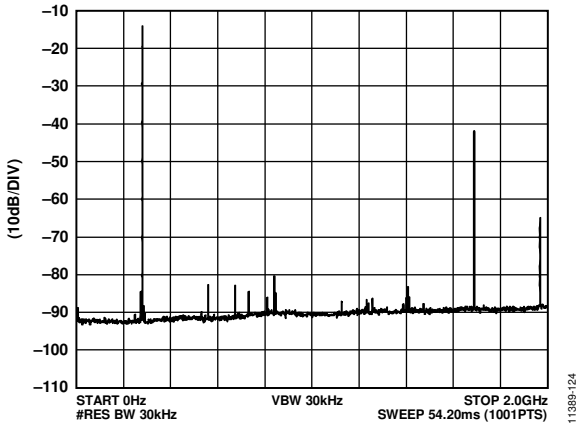


Figure 24. Single Tone f_{DAC} = 1966.08 MHz, f_{OUT} = 280 MHz, −14 dBFS

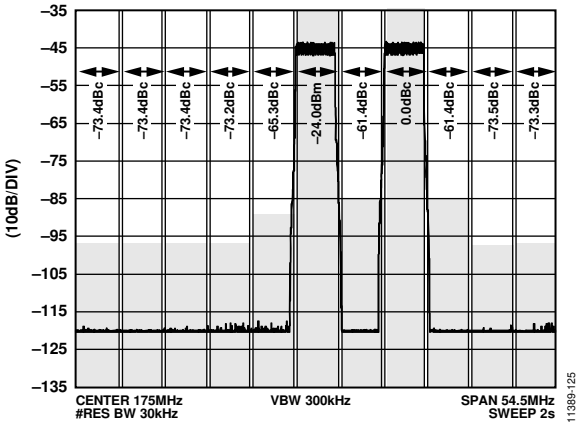


Figure 25. 2-Channel (2C) 5 MHz BW with 5 MHz Gap, LTE ACLR Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz (Total LTE Carrier Power is 20.982 dBm)

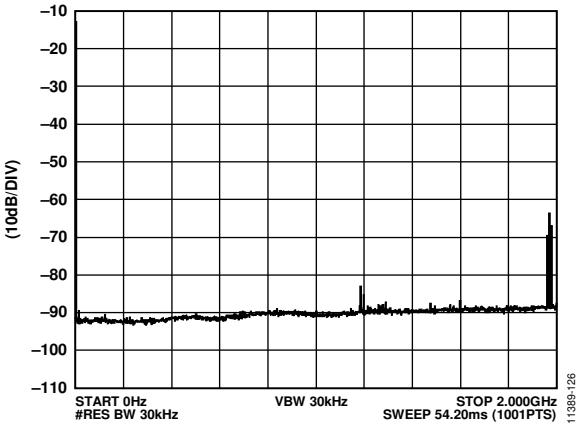


Figure 26. Single Tone SFDR f_{DAC} = 1966.08 MHz, 4× Interpolation, f_{OUT} = 10 MHz, −14 dBFS

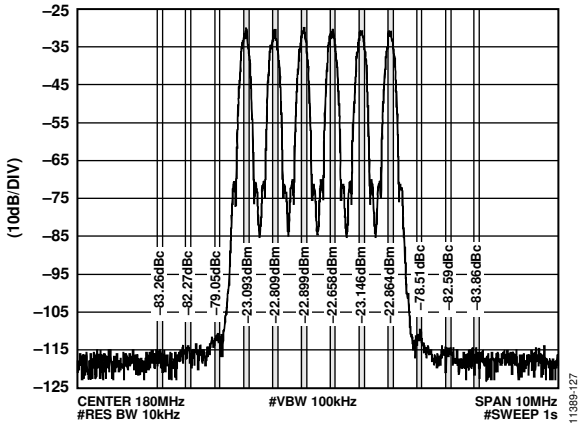


Figure 27. 6-Channel (6C) Spaced by 600 kHz GSM, Enhanced Data Rates for GSM Evolution (EDGE) Adjacent Channel Power (ACP) IMD Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

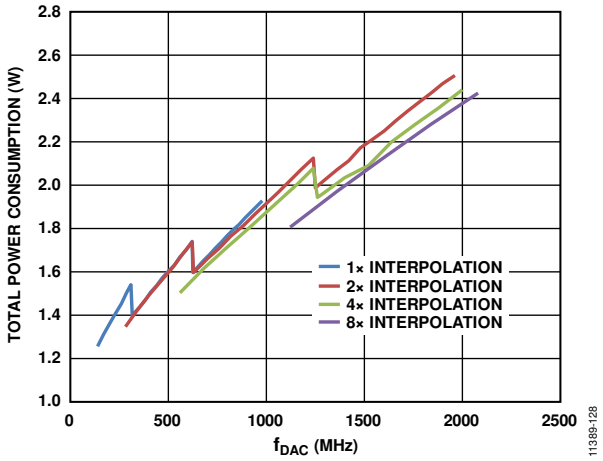


Figure 28. Total Power Consumption vs. f_{DAC} over Interpolation

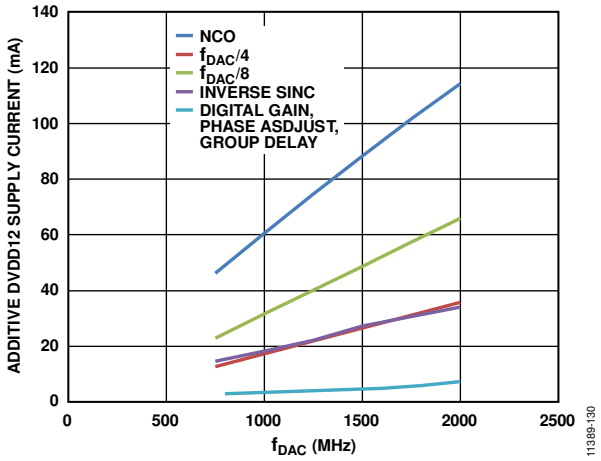


Figure 30. Additive DVDD12 Supply Current vs. f_{DAC} over Digital Functions

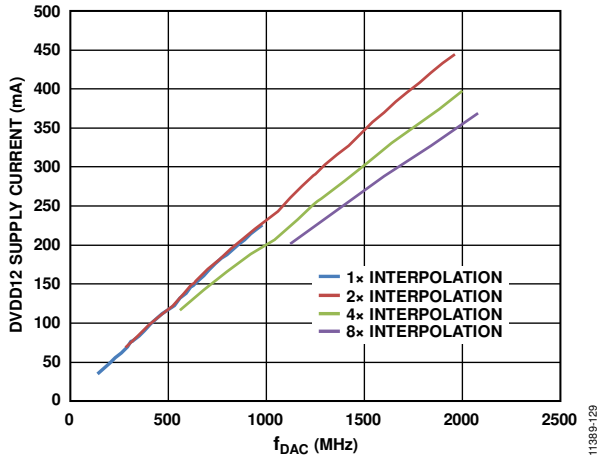


Figure 29. DVDD12 Supply Current vs. f_{DAC} over Interpolation

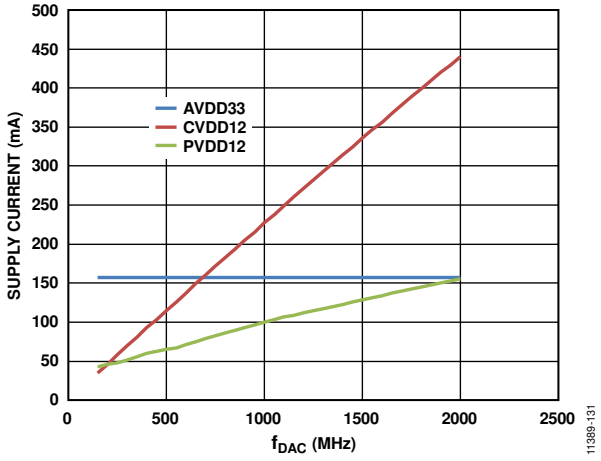


Figure 31. AVDD33, CVDD12, and PVDD12 Supply Current vs. f_{DAC}

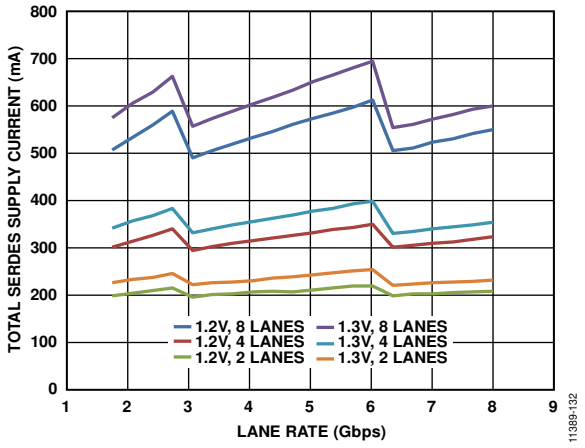


Figure 32. Total SERDES Supply Current (SVDD12) vs. Lane Rate: 2, 4, and 8 Lanes

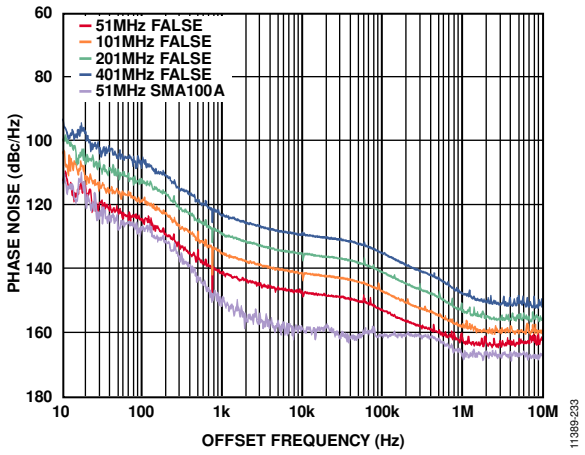


Figure 33. Single Tone Phase Noise vs. Offset Frequency at Four Different f_{OUT} Rates, f_{DAC} = 2.0 GHz, PLL Off

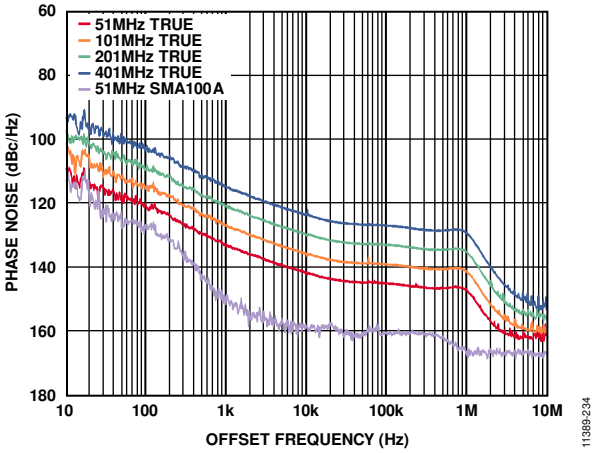


Figure 34. Single Tone Phase Noise vs. Offset Frequency at Four Different f_{OUT} Rates, f_{DAC} = 2.0 GHz, PLL On

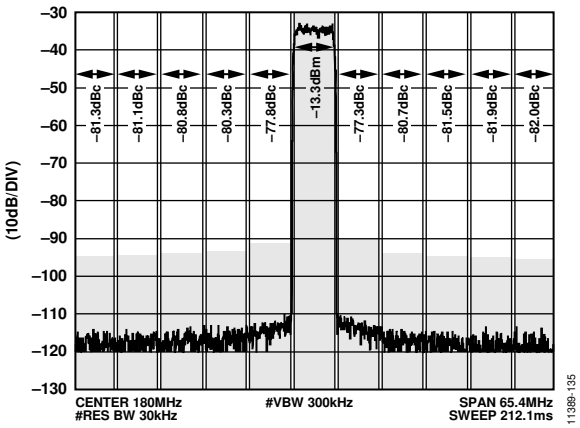


Figure 35. 1C 256 Point Quadrature Amplitude Modulation (QAM) Signal ACLR Performance, IF = 180 MHz, f_{DAC} = 1966.08 MHz

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error
Offset error is a measure of how far from full-scale range (FSR) the DAC output current is at 25°C (in ppm).

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when the input is at its minimum code and the output when the input is at its maximum code.

Output Compliance Range
The output compliance range is the range of allowable voltages at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient value (25°C) to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of FSR per degree Celsius.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a single sideband upconversion, two images are created around the second IF frequency; the desired signal is on one of these images. The other signal is unwanted, and a complex modulator rejects this unwanted image.

Adjusted DAC Update Rate
The adjusted DAC update rate the DAC update rate divided by the selected interpolation factor.

Physical Lane
Physical Lane x refers to SERDINx±.

Logical Lane
Logical Lane x refers to physical lanes after optionally being remapped by the crossbar block (Register 0x308 to Register 0x30B).

Link Lane
Link Lane x refers to logical lanes considered per link. When paging Link 0 (Register 0x300, Bit 2 = 0), Link Lane x = Logical Lane x. When paging Link 1 (Register 0x300, Bit 2 = 1, dual link only), Link Lane x = Logical Lane x + 4.

THEORY OF OPERATION

The AD9154 is a 16-bit, quad DAC with a SERDES interface. Figure 2 shows a detailed functional block diagram of the AD9154. Eight high speed serial lanes carry data into the AD9154.

The clock for the input data is derived from the device clock (as called out in the JESD204B specification). This device clock can be sourced with a phase-locked loop (PLL) reference clock used by the on-chip PLL to generate a DAC clock or a high fidelity direct external DAC sampling clock. The device can be configured to operate in one-, two-, four-, or eight-lane modes, depending on the required input data rate. The quad DAC can be configured as a dual link device with each JESD204B link providing data for a dual DAC pair to add application flexibility.

The signal processing datapath of the AD9154 offers four interpolation modes (1×, 2×, 4×, and 8×) through three half-band filters. An inverse sinc filter compensates for DAC output sinc roll-off. A digital inphase and quadrature modulator upcoverts a pair of DAC input signals to an IF frequency within the first Nyquist zone of the DAC programmed into an NCO. Gain, phase, dc offset, and group delay adjustments can programmably predistort the DAC input signals to improve LO feedthrough and unwanted sideband cancellation performance of an analog quadrature modulator following the AD9154 in a transmitter signal chain.

The AD9154 DAC cores provide a differential current output with a nominal full-scale current of 20 mA. The differential current outputs are optimized for integration with the Analog Devices ADRF6720-27 wideband quadrature modulator. The AD9154 has a mechanism for multichip synchronization, as well as a mechanism for achieving deterministic latency (latency locking). The latency for each DAC remains constant from link establishment to link establishment. The AD9154 makes use of the JESD204B Subclass 1 SYSREF signal to establish multichip synchronization.

The various functional blocks and the data interface must be set up in a specific sequence for proper operation (see the Device Setup Guide section). This data sheet describes the various blocks of the AD9154 in detail, including descriptions of the JESD204B interface, the control parameters, and the various registers that set up and monitor the device. The recommended start-up routine reliably sets up the data link.

SERIAL PORT OPERATION

The serial port interface (SPI) is a flexible, synchronous serial communications port that allows easy interfacing with many industry-standard microcontrollers and microprocessors. The interface facilitates read/write access to all registers that configure the AD9154. MSB first or LSB first transfer formats are supported. The SPI is configurable as a 4-wire interface or a 3-wire interface in which the input and output share a single-pin I/O, SDIO.

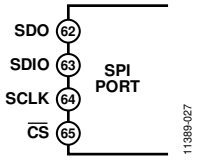


Figure 36. SPI Pins

There are two phases to a communication cycle with the AD9154. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first 16 SCLK rising edges. The instruction word provides the serial port controller with information regarding the data transfer cycle, Phase 2 of the communication cycle. The Phase 1 instruction word defines whether the upcoming data transfer is a read or write, along with the starting register address for the following data transfer.

A logic high on the $\overline{CS}$ pin, followed by a logic low, resets the serial port timing to the initial state of the instruction cycle. From this state, the next 16 rising SCLK edges represent the instruction bits of the current input/output (I/O) operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one or more data bytes. Eight × N SCLK cycles are needed to transfer N bytes during the transfer cycle. Registers change immediately upon writing to the last bit of each transfer byte, except for the frequency tuning word (FTW) and numerically controlled oscillator (NCO) phase offsets, which change only when the frequency tuning word FTW_UPDATE_REQ bit is set.

DATA FORMAT

The instruction byte contains the information shown in Table 13.

Table 13. Serial Port Instruction Word

I15 (MSB)	I[14:0]
R/$\overline{W}$	A[14:0]

R/$\overline{W}$, Bit 15 of the instruction word, determines whether a read or a write data transfer occurs after the instruction word write. Logic 1 indicates a read operation, and Logic 0 indicates a write operation.

A14 to A0, Bit 14 to Bit 0 of the instruction word, determine the register accessed during the data transfer portion of the communication cycle. For multibyte transfers, A[14:0] is the starting address. The device generates the remaining register addresses based on the address increment bits. If the address increment bits are set high (Register 0x000, Bit 5 and Bit 2), multibyte SPI writes start on A[14:0] and increment by 1 every eight bits sent/received. If the address increment bits are set to 0, the address decrements by 1 every eight bits.

SERIAL PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is specified in Table 2. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

An active low input starts and gates a communication cycle. It allows the use of more than one device on the same serial communications lines. The SDIO pin goes to a high impedance state when this input is high. During the communication cycle, chip select must stay low.

Serial Data I/O (SDIO)

This pin is a bidirectional data line. In 4-wire mode, this pin acts as the data input and SDO acts as the data output.

SERIAL PORT OPTIONS

The serial port can support both MSB first and LSB first data formats. The LSB first bits (Register 0x000, Bit 6 and Bit 1) control this functionality. The default is MSB first (the LSB first bits = 0).

When the LSB first bits = 0 (MSB first), the instruction and data bits must be written from MSB to LSB. R/$\overline{W}$ is followed by A[14:0] as the instruction word, and D[7:0] is the data-word. When the LSB first bits = 1 (LSB first), the opposite is true. A[0:14] is followed by R/$\overline{W}$, which is subsequently followed by D[0:7].

The serial port supports a 3-wire or 4-wire interface. When the SDO active bits = 1 (Register 0x000, Bit 4 and Bit 3), a 4-wire interface with a separate input pin (SDIO) and output pin (SDO) is used. When the SDO active bits = 0, the SDO pin is unused and the SDIO pin is used for both input and output.

Multibyte data transfers can be performed as well. Hold the $\overline{CS}$ pin low for multiple data transfer cycles (eight SCLKs) after the first data transfer word following the instruction cycle. The first eight SCLKs following the instruction cycle read from or write to the register provided in the instruction cycle. For each additional eight SCLK cycles, the address is either incremented or decremented and the read/write occurs on the new register. Set the direction of the address using the address increment bits (Register 0x000, Bit 5 and Bit 2).

When the address increment bits = 1, the multicycle addresses are incremented. When the address increment bits = 0, the addresses are decremented. A new write cycle can always be initiated by bringing $\overline{CS}$ high and then low again.

During writes to Register 0x0000 only, the chip tests the first nibble following the address phase, ignoring the second nibble. This is completed independently from the LSB first bit and ensures that there are extra clock cycles following the soft reset bits (Register 0x000, Bit 0 and Bit 7).

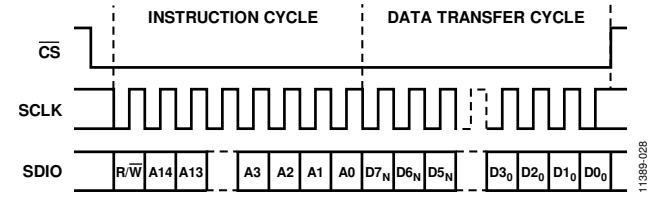


Figure 37. Serial Register Interface Timing, MSB First, Address Increment Bits = 0

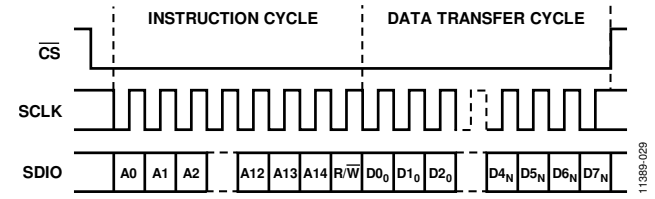


Figure 38. Serial Register Interface Timing, LSB First, Address Increment Bits = 1

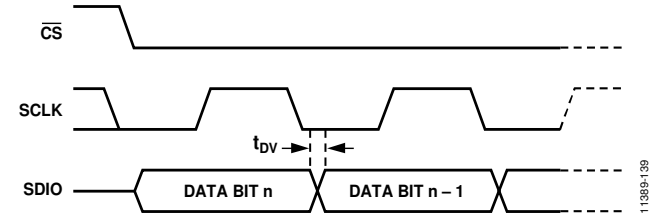


Figure 39. Timing Diagram for Serial Port Register Read

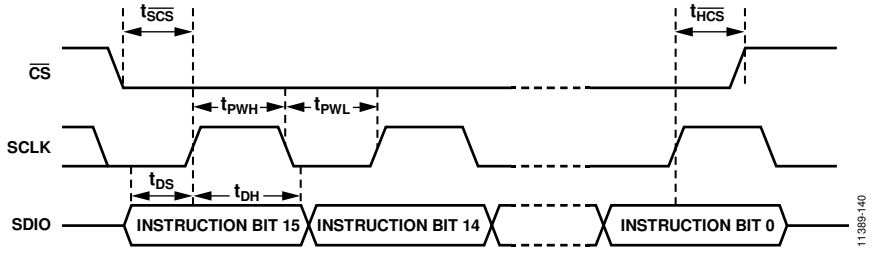


Figure 40. Timing Diagram for Serial Port Register Write

CHIP INFORMATION

Register 0x003 to Register 0x006 contain chip information, as shown in Table 14.

Table 14. Chip Information

Information	Description
Chip Type	The product is a high speed DAC represented by a code of 0x04 in Register 0x003.
Product ID	8 MSBs in Register 0x005 and 8 LSBs in Register 0x004. The product ID is 0x9154.
Product Grade	Register 0x006, Bits[7:4]. The product grade is 0x9.
Device Revision	Register 0x006, Bits[3:0]. The device revision is 0x9.