Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

16-Bit, 12 GSPS, RF DAC and Direct Digital Synthesizer

Data Sheet **AD9164**

FEATURES

- **DAC update rate up to 12 GSPS (minimum)**
- **Direct RF synthesis at 6 GSPS (minimum)**
  - **DC to 2.5 GHz in baseband mode**
  - **DC to 6 GHz in 2× nonreturn-to-zero (NRZ) mode**
  - **1.5 GHz to 7.5 GHz in Mix-Mode**
- **Bypassable interpolation**
  - **2×, 3×, 4×, 6×, 8×, 12×, 16×, 24×**
- **Excellent dynamic performance**

APPLICATIONS

- **Broadband communications systems**
  - **DOCSIS 3.1 cable modem termination system (CMTS)/ video on demand (VOD)/edge quadrature amplitude modulation (EQAM)**
- **Wireless communications infrastructure**
  - **W-CDMA, LTE, LTE-A, point to point**

GENERAL DESCRIPTION

The AD9164[1] is a high performance, 16-bit digital-to-analog converter (DAC) and direct digital synthesizer (DDS) that supports update rates to 6 GSPS. The DAC core is based on a quad-switch architecture coupled with a 2× interpolator filter that enables an effective DAC update rate of up to 12 GSPS in some modes. The high dynamic range and bandwidth makes these DACs ideally suited for the most demanding high speed radio frequency (RF) DAC applications.

The DDS consists of a bank of 32, 32-bit numerically controlled oscillators (NCOs), each with its own phase accumulator.

When combined with a 100 MHz serial peripheral interface (SPI) and fast hop modes, phase coherent fast frequency hopping (FFH) is enabled, with several modes to support multiple applications.

In baseband mode, wide analog bandwidth capability combines with high dynamic range to support DOCSIS 3.1 cable infrastructure compliance from the minimum of one carrier up to the full maximum spectrum of 1.791 GHz of signal bandwidth. A 2× interpolator filter (FIR85) enables the AD9164 to be configured for lower data rates and converter clocking to reduce the overall system power and ease the filtering requirements. In Mix-Mode™ operation, the AD9164 can reconstruct RF carriers in the second and third Nyquist zones up to 7.5 GHz while still maintaining exceptional dynamic range. The output current can be programmed from 8 mA to 38.76 mA. The AD9164 data interface consists of up to eight JESD204B serializer/deserializer (SERDES) lanes that are programmable in terms of lane speed and number of lanes to enable application flexibility.

An SPI interface configures the AD9164 and monitors the status of all registers. The AD9164 is offered in an 165-ball, 8 mm × 8 mm, 0.5 mm pitch CSP_BGA package, and an 169-ball, 11 mm × 11 mm, 0.8 mm pitch, CSP_BGA package, including a leaded ball option.

PRODUCT HIGHLIGHTS

1. High dynamic range and signal reconstruction bandwidth supports RF signal synthesis of up to 7.5 GHz.
2. Up to eight lanes JESD204B SERDES interface flexible in terms of number of lanes and lane speed.
3. Bandwidth and dynamic range to meet DOCSIS 3.1 compliance and multiband wireless communications standards with margin.

FUNCTIONAL BLOCK DIAGRAM

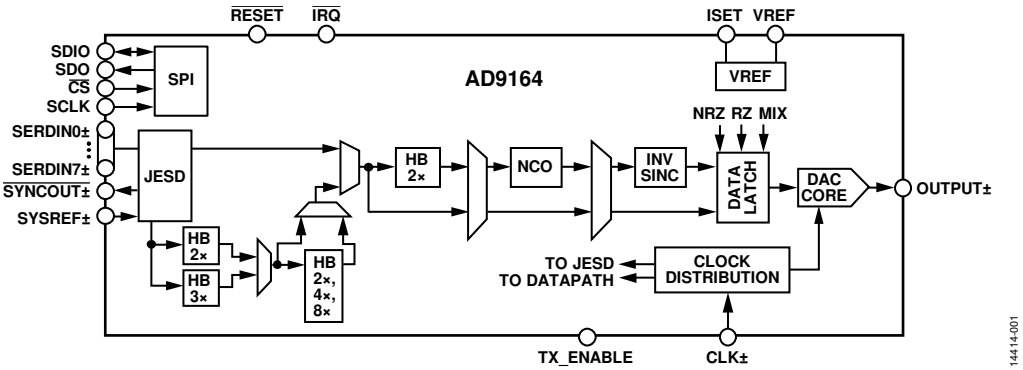

Figure 1.

[1] Protected by U.S. Patents 6,842,132 and 7,796,971.

Rev. A **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

AD9164* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9161/AD9162/AD9163/AD9164 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9164 16-Bit, 12 GSPS, RF DAC and Direct Digital Synthesizer Data Sheet

TOOLS AND SIMULATIONS

- AD916X Remote Evaluation Tool
- AD9164bbcaz IBIS Model
- AD9164bbcz IBIS Model

REFERENCE MATERIALS

Press

- D/A Converter Offers More Accuracy in a Smaller Footprint for Diverse Applications Ranging from Radar to Smartphone Testing

DESIGN RESOURCES

- AD9164 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9164 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

1/2017—Rev. 0 to Rev. A

Deleted DLL_VDD_1P2 Parameter, Table 1 4
Added Temperature Sensor Parameter, Table 1 4
Change to Endnote 1, Table 1 4
Change to OUTPUT± to VNEG_N1P2 Parameter, Table 10 11
Changes to Link Delay Setup Example, With Known Delays Section 43
Changes to Link Delay Setup Example, Without Known Delay Section 45
Changes to Table 24 46
Added Datapath PRBS Section 59
Added Datapath PRBS IRQ Section 60
Moved Figure 135 67
Added Temperature Sensor Section 68
Changes to Equivalent DAC Output and Transfer Function Section 68
Changes to Output Stage Configuration Section and Figure 142 Caption 69
Added Register 0x132 Row to Register 0x135 Row, Table 45 74
Added Register 0x132 Row to Register 0x135 Row, Table 46 91
Change to Register 0x230 93

7/2016—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

VDD25_DAC = 2.5 V, VDD12A = VDD12_CLK = 1.2 V, VNEG_N1P2 = −1.2 V, DVDD = 1.2 V, IOVDD = 2.5 V, VDD_1P2 = DVDD_1P2 = PLL_LDO_VDD12 = 1.2 V, SYNC_VDD_3P3 = 3.3 V, DAC output full-scale current (I_{OUTFS}) = 40 mA, and T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bit
DAC Update Rate					
Minimum				1.5	GSPS
Maximum	VDDx[1] = 1.3 V ± 2%[2]	6	6.4		GSPS
	VDDx[1] = 1.3 V ± 2%[2], FIR85[3] 2× interpolator enabled	12	12.8		GSPS
Adjusted[4]	VDDx[1] = 1.3 V ± 2%[2]	6	6.4		GSPS
ACCURACY					
Integral Nonlinearity (INL)			±2.7		LSB
Differential Nonlinearity (DNL)			±1.7		LSB
ANALOG OUTPUTS					
Gain Error (with Internal Reference)			−1.7		%
Full-Scale Output Current					
Minimum	R_{SET} = 9.76 kΩ	7.37	8	8.57	mA
Maximum	R_{SET} = 9.76 kΩ	35.8	38.76	41.3	mA
DAC CLOCK INPUT (CLK+, CLK−)					
Differential Input Power	R_{LOAD} = 90 Ω differential on-chip	−20	0	+10	dBm
Common-Mode Voltage	AC-coupled		0.6		V
Input Impedance[1]	3 GSPS input clock		90		Ω
TEMPERATURE DRIFT					
Gain			105		ppm/°C
Reference Voltage			75		ppm/°C
TEMPERATURE SENSOR					
Accuracy	After single point calibration (See the Temperature Sensor section)		±5		%
REFERENCE					
Internal Reference Voltage			1.19		V
ANALOG SUPPLY VOLTAGES					
VDD25_DAC		2.375	2.5	2.625	V
VDD12A[2]		1.14	1.2	1.326	V
VDD12_CLK[2]		1.14	1.2	1.326	V
VNEG_N1P2		−1.26	−1.2	−1.14	V
DIGITAL SUPPLY VOLTAGES					
DVDD	Includes VDD12_DCD/DLL	1.14	1.2	1.326	V
IOVDD[3]		1.71	2.5	3.465	V
SERDES SUPPLY VOLTAGES					
VDD_1P2		1.14	1.2	1.326	V
VTT_1P2	Can connect to VDD_1P2	1.14	1.2	1.326	V
DVDD_1P2		1.14	1.2	1.326	V
PLL_LDO_VDD12		1.14	1.2	1.326	V
PLL_CLK_VDD12	Can connect to PLL_LDO_VDD12	1.14	1.2	1.326	V
SYNC_VDD_3P3		3.135	3.3	3.465	V
BIAS_VDD_1P2	Can connect to VDD_1P2	1.14	1.2	1.326	V

[1] See the Clock Input section for more details.
[2] For the lowest noise performance, use a separate power supply filter network for the VDD12_CLK and the VDD12A pins.
[3] IOVDD can range from 1.8 V to 3.3 V, with ±5% tolerance.
[4] The adjusted DAC update rate is calculated as f_{DAC} divided by the minimum required interpolation factor. For the AD9164, the minimum interpolation factor is 1. Therefore, with f_{DAC} = 6 GSPS, f_{DAC} adjusted = 6 GSPS. When FIR85 is enabled, which puts the device into 2× NRZ mode, f_{DAC} = 2 × (DAC clock input frequency), and the minimum interpolation increases to 2× (interpolation value). Thus, for the AD9164, with FIR85 enabled and DAC clock = 6 GSPS, f_{DAC} = 12 GSPS, minimum interpolation = 2×, and the adjusted DAC update rate = 6 GSPS.

DAC INPUT CLOCK OVERCLOCKING SPECIFICATIONS

VDD25_DAC = 2.5 V, VDD12A = VDD12_CLK = 1.2 V, VNEG_N1P2 = −1.2 V, DVDD = 1.2 V, IOVDD = 2.5 V, VDD_1P2 = DVDD_1P2 = PLL_LDO_VDD12 = 1.2 V, SYNC_VDD_3P3 = 3.3 V, I_{OUTFS} = 40 mA, T_A = −40°C to +85°C, unless otherwise noted.

Maximum guaranteed speed using the temperature and voltage conditions as shown in Table 2, where VDDx is VDD12_CLK, DVDD, VDD_1P2, DVDD_1P2, and PLL_LDO_VDD12. Any DAC clock speed over 5.1 GSPS requires a maximum junction temperature that does not exceed 105°C to avoid damage to the device. See Table 10 for details on maximum junction temperature permitted for certain clock speeds.

Table 2.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DAC UPDATE RATE					
VDDx = 1.2 V ± 5%	T_{JMAX} = 25°C	6.0			GSPS
	T_{JMAX} = 85°C	5.6			GSPS
	T_{JMAX} = 105°C	5.4			GSPS
VDDx = 1.2 V ± 2%	T_{JMAX} = 25°C	6.1			GSPS
	T_{JMAX} = 85°C	5.8			GSPS
	T_{JMAX} = 105°C	5.6			GSPS
VDDx = 1.3 V ± 2%	T_{JMAX} = 25°C	6.4			GSPS
	T_{JMAX} = 85°C	6.2			GSPS
	T_{JMAX} = 105°C	6.0			GSPS

[1] T_{JMAX} is the maximum junction temperature.

POWER SUPPLY DC SPECIFICATIONS

I_{OUTFS} = 40 mA, T_A = −40°C to +85°C, unless otherwise noted. FIR85 is the finite impulse response with 85 dB digital attenuation.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
8 LANES, 2× INTERPOLATION (80%), 3 GSPS	NCO on, FIR85 on				
Analog Supply Currents					
VDD25_DAC = 2.5 V			93.8	100	mA
VDD12A = 1.2 V			3.7	150	µA
VDD12_CLK = 1.2 V			229	279	mA
VNEG_N1P2 = −1.2 V		−119	−112		mA
Digital Supply Currents					
DVDD = 1.2 V	Includes VDD12_DCD/DLL		621.3	971	mA
IOVDD[1] = 2.5 V			2.5	2.7	mA
SERDES Supply Currents					
VDD_1P2 = 1.2 V	Includes VTT_1P2, BIAS_VDD_1P2		425.5	550	mA
DVDD_1P2 = 1.2 V			62	86	mA
PLL_LDO_VDD12 = 1.2 V	Connected to PLL_CLK_VDD12		84.4	106	mA
SYNC_VDD_3P3 = 3.3 V			9.3	11	mA
8 LANES, 6× INTERPOLATION (80%), 3 GSPS	NCO on, FIR85 on				
Analog Supply Currents					
VDD25_DAC = 2.5 V			93.8		mA
VDD12A = 1.2 V			3.7		µA
VDD12_CLK = 1.2 V			228.7		mA
VNEG_N1P2 = −1.2 V			−120.7		mA
Digital Supply Currents					
DVDD = 1.2 V	Includes VDD12_DCD/DLL		598.4		mA
IOVDD[1] = 2.5 V			2.5		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SERDES Supply Currents					
VDD_1P2 = 1.2 V	Includes VTT_1P2, BIAS_VDD_1P2		443.4		mA
DVDD_1P2 = 1.2 V			72.3		mA
PLL_LDO_VDD12 = 1.2 V	Connected to PLL_CLK_VDD12		81.8		mA
SYNC_VDD_3P3 = 3.3 V			9.4		mA
NCO ONLY MODE, 5 GSPS					
Analog Supply Currents					
VDD25_DAC = 2.5 V			93.7	100	mA
VDD12A = 1.2 V			10	150	µA
VDD12_CLK = 1.2 V			340.6	432	mA
VNEG_N1P2 = −1.2 V		−119	−112		mA
Digital Supply Currents					
DVDD = 1.2 V	Includes VDD12_DCD/DLL		425.5	753	mA
IOVDD[1] = 2.5 V			2.5	2.7	mA
SERDES Supply Currents					
VDD_1P2 = 1.2 V	Includes VTT_1P2, BIAS_VDD_1P2		1.4	34	mA
DVDD_1P2 = 1.2 V			1.0	14.1	mA
PLL_LDO_VDD12 = 1.2 V	Connected to PLL_CLK_VDD12		0.13	1.5	mA
SYNC_VDD_3P3 = 3.3 V			0.32	0.43	mA
8 LANES, 4× INTERPOLATION (80%), 5 GSPS	NCO on, FIR85 off (unless otherwise noted)				
Analog Supply Currents					
VDD25_DAC = 2.5 V			102	108	mA
VDD12A = 1.2 V			80	150	µA
VDD12_CLK = 1.2 V			340.5	432.4	mA
	At 6 GSPS		408		mA
VNEG_N1P2 = −1.2 V		−127.4	−120.2		mA
Digital Supply Currents					
DVDD = 1.2 V (Includes VDD12_DCD/DLL)	NCO on, FIR85 off		665.4	1033	mA
DVDD = 1.2 V	NCO off, FIR85 on		706.5		mA
	NCO on, FIR85 on		894.6		mA
	NCO on, FIR85 on, at 6 GSPS		1090		mA
IOVDD[1] = 2.5 V			2.5	2.7	mA
SERDES Supply Currents					
VDD_1P2 = 1.2 V	Includes VTT_1P2, BIAS_VDD_1P2		411.2	550	mA
DVDD_1P2 = 1.2 V			52.1	73	mA
PLL_LDO_VDD12 = 1.2 V	Connected to PLL_CLK_VDD12		85.8	105	mA
SYNC_VDD_3P3 = 3.3 V			9.3	11	mA
8 LANES, 3× INTERPOLATION (80%), 4.5 GSPS	NCO on, FIR85 on				
Analog Supply Currents					
VDD25_DAC = 2.5 V			94		mA
VDD12A = 1.2 V			85	175	µA
VDD12_CLK = 1.2 V			314.3		mA
VNEG_N1P2 = −1.2 V			−112.1		mA
Digital Supply Currents					
DVDD = 1.2 V	Includes VDD12_DCD/DLL		948.5		mA
IOVDD[1] = 2.5 V	IOVDD = 2.5 V		2.5		mA
SERDES Supply Currents					
VDD_1P2 = 1.2 V	Includes VTT_1P2, BIAS_VDD_1P2		432.3		mA
DVDD_1P2 = 1.2 V			62.3		mA
PLL_LDO_VDD12 = 1.2 V	Connected to PLL_CLK_VDD12		84.7		mA
SYNC_VDD_3P3 = 3.3 V			9.2		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER DISSIPATION					
3 GSPS					
2× NRZ Mode, 6×, FIR85 Enabled, NCO On	Using 80%, 3× filter, eight-lane JESD204B		2.1		W
NRZ Mode, 24×, FIR85 Disabled, NCO On	Using 80%, 2× filter, one-lane JESD204B		1.3		W
5 GSPS					
NRZ Mode, 8×, FIR85 Disabled, NCO On	Using 80%, 2× filter, eight-lane JESD204B		2.18		W
NRZ Mode, 16×, FIR85 Disabled, NCO On	Using 80%, 2× filter, eight-lane JESD204B		2.09		W
2× NRZ Mode, 6×, FIR85 Enabled, NCO On	Using 80%, 3× filter, eight-lane JESD204B		2.65		W

[1] IOVDD can range from 1.8 V to 3.3 V, with ±5% tolerance.

SERIAL PORT AND CMOS PIN SPECIFICATIONS

VDD25_DAC = 2.5 V, VDD12A = VDD12_CLK = 1.2 V, VNEG_N1P2 = −1.2 V, DVDD = 1.2 V, IOVDD = 2.5 V, VDD_1P2 = DVDD_1P2 = PLL_LDO_VDD12 = 1.2 V, SYNC_VDD_3P3 = 3.3 V, I_{OUTFS} = 40 mA, T_A = −40°C to +85°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Comments/Conditions	Min	Typ	Max	Unit
WRITE OPERATION		See Figure 90				
Maximum SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$		100			MHz
SCLK Clock High	t_{PWH}	SCLK = 20 MHz	3.5			ns
SCLK Clock Low	t_{PWL}	SCLK = 20 MHz	4			ns
SDIO to SCLK Setup Time	t_{DS}		4	2		ns
SCLK to SDIO Hold Time	t_{DH}		1	0.5		ns
$\overline{CS}$ to SCLK Setup Time	t_S		9	1		ns
SCLK to $\overline{CS}$ Hold Time	t_H		9	0.5		ns
READ OPERATION		See Figure 89				
SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$				20	MHz
SCLK Clock High	t_{PWH}		20			ns
SCLK Clock Low	t_{PWL}		20			ns
SDIO to SCLK Setup Time	t_{DS}		10			ns
SCLK to SDIO Hold Time	t_{DH}		5			ns
$\overline{CS}$ to SCLK Setup Time	t_S		10			ns
SCLK to SDIO (or SDO) Data Valid Time	t_{DV}				17	ns
$\overline{CS}$ to SDIO (or SDO) Output Valid to High-Z		Not shown in Figure 89 or Figure 90			45	ns
INPUTS (SDIO, SCLK, $\overline{CS}$, $\overline{RESET}$, TX_ENABLE)						
Voltage Input						
High	V_{IH}	1.8 V ≤ IOVDD ≤ 2.5 V	0.7 × IOVDD			V
Low	V_{IL}	1.8 V ≤ IOVDD ≤ 2.5 V			0.3 × IOVDD	V
Current Input						
High	I_{IH}				75	µA
Low	I_{IL}		−150			µA
OUTPUTS (SDIO, SDO)						
Voltage Output						
High	V_{OH}	1.8 V ≤ IOVDD ≤ 3.3 V	0.8 × IOVDD			V
Low	V_{OL}	1.8 V ≤ IOVDD ≤ 3.3 V			0.2 × IOVDD	V
Current Output						
High	I_{OH}			4		mA
Low	I_{OL}			4		mA

JESD204B SERIAL INTERFACE SPEED SPECIFICATIONS

VDD25_DAC = 2.5 V, VDD12A = VDD12_CLK = 1.2 V, VNEG_N1P2 = −1.2 V, DVDD = 1.2 V, IOVDD = 2.5 V, VDD_1P2 = DVDD_1P2 = PLL_LDO_VDD12 = 1.2 V, SYNC_VDD_3P3 = 3.3 V, I_{OUTFS} = 40 mA, T_A = −40°C to +85°C, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL INTERFACE SPEED	Guaranteed operating range				
Half Rate		6		12.5	Gbps
Full Rate		3		6.25	Gbps
Oversampling		1.5		3.125	Gbps
2× Oversampling		0.750		1.5625	Gbps

SYSREF± TO DAC CLOCK TIMING SPECIFICATIONS

VDD25_DAC = 2.5 V, VDD12A = VDD12_CLK = 1.2 V, VNEG_N1P2 = −1.2 V, DVDD = 1.2 V, IOVDD = 2.5 V, VDD_1P2 = DVDD_1P2 = PLL_LDO_VDD12 = 1.2 V, SYNC_VDD_3P3 = 3.3 V, I_{OUTFS} = 40 mA, T_A = −40°C to +85°C, unless otherwise noted.

Table 6.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
SYSREF± (AD9164BBCZ ONLY)	DC-coupled, common-mode voltage = 1.2 V				
SYSREF± Differential Swing = 0.4 V					
Minimum Setup Time, t_{SYSS}			163	424	ps
Minimum Hold Time, t_{SYSH}			160	318	ps
SYSREF± Differential Swing = 0.8 V					
Minimum Setup Time, t_{SYSS}			162	412	ps
Minimum Hold Time, t_{SYSH}			169	350	ps
SYSREF± Differential Swing = 1.0 V					
Minimum Setup Time, t_{SYSS}			163	376	ps
Minimum Hold Time, t_{SYSH}			176	354	ps
SYSREF± (AD9164BBCAZ ONLY)					
SYSREF± Differential Swing = 1.0 V					
Minimum Setup Time, t_{SYSS}	AC-coupled		65	117	ps
	DC-coupled, common-mode voltage = 0 V		45	77	ps
	DC-coupled, common-mode voltage = 1.25 V		68	129	ps
Minimum Hold Time, t_{SYSH}	AC-coupled		19	63	ps
	DC-coupled, common-mode voltage = 0 V		5	37	ps
	DC-coupled, common-mode voltage = 1.25 V		51	114	ps

[1] The SYSREF± pulse must be at least four DAC clock edges wide plus the setup and hold times in Table 6. For more information, see the Sync Processing Modes Overview section.

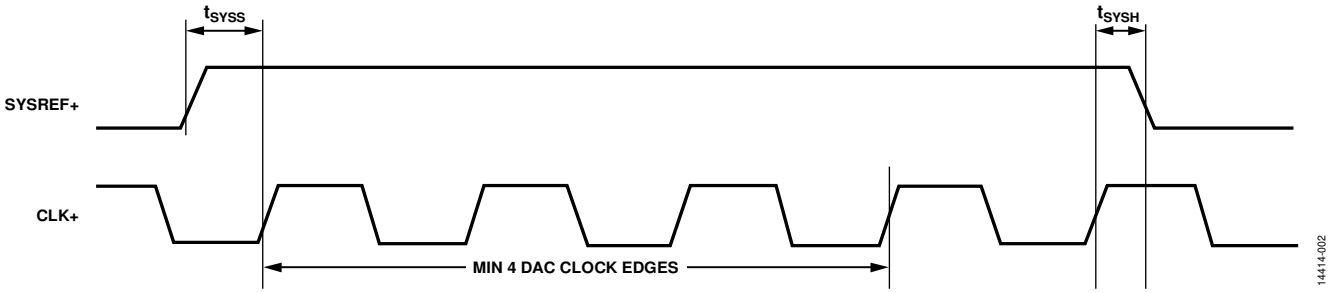

Figure 2. SYSREF± to DAC Clock Timing Diagram (Only SYSREF+ and CLK+ Shown)

DIGITAL INPUT DATA TIMING SPECIFICATIONS

VDD25_DAC = 2.5 V, VDD12A = VDD12_CLK = 1.2 V, VNEG_N1P2 = −1.2 V, DVDD = 1.2 V, IOVDD = 2.5 V, VDD_1P2 = DVDD_1P2 = PLL_LDO_VDD12 = 1.2 V, SYNC_VDD_3P3 = 3.3 V, I_{OUTFS} = 40 mA, T_A = −40°C to +85°C, unless otherwise noted.

Table 7.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LATENCY[1]					
Interface			1		PCLK[2] cycle
Interpolation			See Table 33		
Power-Up Time	From DAC output off to enabled		10		ns
DETERMINISTIC LATENCY					
Fixed				12	PCLK[2] cycles
Variable				2	PCLK[2] cycles
SYSREF± TO LOCAL MULTIFRAME CLOCKS (LMFC) DELAY			4		DAC clock cycles

[1] Total latency (or pipeline delay) through the device is calculated as follows:
Total Latency = Interface Latency + Fixed Latency + Variable Latency + Pipeline Delay
See Table 33 for examples of the pipeline delay per block.
[2] PCLK is the internal processing clock for the AD9164 and equals the lane rate ÷ 40.

JESD204B INTERFACE ELECTRICAL SPECIFICATIONS

VDD25_DAC = 2.5 V, VDD12A = VDD12_CLK = 1.2 V, VNEG_N1P2 = −1.2 V, DVDD = 1.2 V, IOVDD = 2.5 V, VDD_1P2 = DVDD_1P2 = PLL_LDO_VDD12 = 1.2 V, SYNC_VDD_3P3 = 3.3 V, I_{OUTFS} = 40 mA, T_A = −40°C to +85°C, unless otherwise noted. V_{TT} is the termination voltage.

Table 8.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B DATA INPUTS						
Input Leakage Current		T_A = 25°C				
Logic High		Input level = 1.2 V ± 0.25 V, V_{TT} = 1.2 V		10		µA
Logic Low		Input level = 0 V		−4		µA
Unit Interval	UI		80		1333	ps
Common-Mode Voltage	V_{RCM}	AC-coupled, V_{TT} = VDD_1P2[1]	−0.05		+1.85	V
Differential Voltage	R_V_{DIFF}		110		1050	mV
V_{TT} Source Impedance	Z_{TT}	At dc			30	Ω
Differential Impedance	Z_{RDIFF}	At dc	80	100	120	Ω
Differential Return Loss	RL_{RDIF}			8		dB
Common-Mode Return Loss	RL_{RCM}			6		dB
SYSREF± INPUT						
Differential Impedance		165-ball CSP_BGA		110		Ω
		169-ball CSP_BGA		121		Ω
DIFFERENTIAL OUTPUTS ($\overline{\text{SYNCOUT}}$±)[2]		Driving 100 Ω differential load				
Output Differential Voltage	V_{OD}		350	420	450	mV
Output Offset Voltage	V_{OS}		1.15	1.2	1.27	V

[1] As measured on the input side of the ac coupling capacitor.
[2] IEEE Standard 1596.3 LVDS compatible.

AC SPECIFICATIONS

VDD25_DAC = 2.5 V, VDD12A = VDD12_CLK = 1.2 V, VNEG_N1P2 = −1.2 V, DVDD = 1.2 V, IOVDD = 2.5 V, VDD_1P2 = DVDD_1P2 = PLL_LDO_VDD12 = 1.2 V, SYNC_VDD_3P3 = 3.3 V, I_{OUTFS} = 40 mA, T_A = +25°C.

Table 9.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)[1]					
Single Tone, f_{DAC} = 5000 MSPS					
f_{OUT} = 70 MHz			−82		dBc
f_{OUT} = 500 MHz			−75		dBc
f_{OUT} = 1000 MHz			−65		dBc
f_{OUT} = 2000 MHz			−70		dBc
f_{OUT} = 4000 MHz	FIR85 enabled		−60		dBc
Single Tone, f_{DAC} = 5000 MSPS	−6 dBFS, shuffle enabled				
f_{OUT} = 70 MHz			−75		dBc
f_{OUT} = 500 MHz			−75		dBc
f_{OUT} = 1000 MHz			−70		dBc
f_{OUT} = 2000 MHz			−75		dBc
f_{OUT} = 4000 MHz	FIR85 enabled		−65		dBc
DOCSIS	f_{DAC} = 3076 MSPS				
f_{OUT} = 70 MHz	Single carrier		−70		dBc
f_{OUT} = 70 MHz	Four carriers		−70		dBc
f_{OUT} = 70 MHz	Eight carriers		−67		dBc
f_{OUT} = 950 MHz	Single carrier		−70		dBc
f_{OUT} = 950 MHz	Four carriers		−68		dBc
f_{OUT} = 950 MHz	Eight carriers		−64		dBc
Wireless Infrastructure	f_{DAC} = 5000 MSPS				
f_{OUT} = 960 MHz	Two-carrier GSM signal at −9 dBFS; across 925 MHz to 960 MHz band		−85		dBc
f_{OUT} = 1990 MHz	Two-carrier GSM signal at −9 dBFS; across 1930 MHz to 1990 MHz band		−81		dBc
ADJACENT CHANNEL POWER	f_{DAC} = 5000 MSPS				
f_{OUT} = 877 MHz	One carrier, first adjacent channel		−79		dBc
f_{OUT} = 877 MHz	Two carriers, first adjacent channel		−76		dBc
f_{OUT} = 1887 MHz	One carrier, first adjacent channel		−74		dBc
f_{OUT} = 1980 MHz	Four carriers, first adjacent channel		−70		dBc
INTERMODULATION DISTORTION	f_{DAC} = 5000 MSPS, two-tone test				
f_{OUT} = 900 MHz	0 dBFS		−80		dBc
f_{OUT} = 900 MHz	−6 dBFS, shuffle enabled		−80		dBc
f_{OUT} = 1800 MHz	0 dBFS		−68		dBc
f_{OUT} = 1800 MHz	−6 dBFS, shuffle enabled		−78		dBc
NOISE SPECTRAL DENSITY (NSD)					
Single Tone, f_{DAC} = 5000 MSPS					
f_{OUT} = 550 MHz			−168		dBm/Hz
f_{OUT} = 960 MHz			−167		dBm/Hz
f_{OUT} = 1990 MHz			−164		dBm/Hz
SINGLE SIDEBAND (SSB) PHASE NOISE AT OFFSET	f_{OUT} = 3800 MHz, f_{DAC} = 4000 MSPS				
1 kHz			−119		dBc/Hz
10 kHz			−125		dBc/Hz
100 kHz			−135		dBc/Hz
1 MHz			−144		dBc/Hz
10 MHz			−156		dBc/Hz

[1] See the Clock Input section for more details on optimizing SFDR and reducing the image of the fundamental with clock input tuning.

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
ISET, VREF to VBG_NEG	−0.3 V to VDD25_DAC + 0.3 V
SERDINx±, VTT_1P2, SYNCOUT±	−0.3 V to SYNC_VDD_3P3 + 0.3 V
OUTPUT± to VNEG_N1P2	−0.3 V to VDD25_DAC + 0.2 V
SYSREF±	GND − 0.5 V to +2.5 V
CLK± to Ground	−0.3 V to VDD12_CLK + 0.3 V
RESET, IRQ, CS, SCLK, SDIO, SDO to Ground	−0.3 V to IOVDD + 0.3 V
Junction Temperature[1]	
f_{DAC} = 6 GSPS	105°C
f_{DAC} ≤ 5.1 GSPS	110°C
Ambient Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] Some operating modes of the device may cause the device to approach or exceed the maximum junction temperature during operation at supported ambient temperatures. Removal of heat from the device may require additional measures such as active airflow, heat sinks, or other measures.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The AD9164 reflow profile is in accordance with the JEDEC JESD204B criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL MANAGEMENT

The AD9164 is a high power device that can dissipate nearly 3 W depending on the user application and configuration. Because of the power dissipation, the AD9164 uses an exposed die package to give the customer the most effective method of controlling the die temperature. The exposed die allows cooling of the die directly.

Figure 3 shows the profile view of the device mounted to a user printed circuit board (PCB) and a heat sink (typically the aluminum case) to keep the junction (exposed die) below the maximum junction temperature in Table 10.

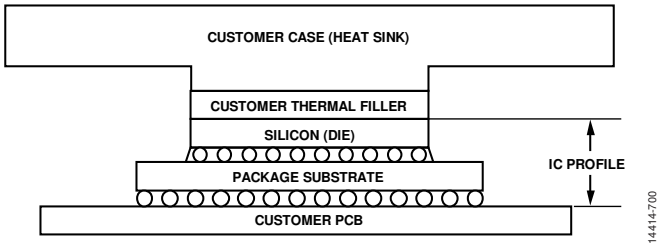

Figure 3. Typical Thermal Management Solution

THERMAL RESISTANCE

Typical θ_{JA} and θ_{JC} values are specified for a 4-layer JEDEC 2S2P high effective thermal conductivity test board for balled surface-mount packages. θ_{JA} is obtained in still air conditions (JESD51-2). Airflow increases heat dissipation, effectively reducing θ_{JA}. θ_{JC} is obtained with the test case temperature monitored at the bottom of the package.

Ψ_{JT} is thermal characteristic parameters obtained with θ_{JA} in still air test conditions but are not applicable to the CSP_BGA package.

Estimate the junction temperature (T_J) using the following equations:

$$T_J = T_T + (\Psi_{JT} \times P_{DISS})$$

where:
T_T is the temperature measured at the top of the package.
P_{DISS} is the total device power dissipation.

Table 11. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
165-Ball CSP_BGA	15.4	0.04	°C/W
169-Ball CSP_BGA	14.6	0.02	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

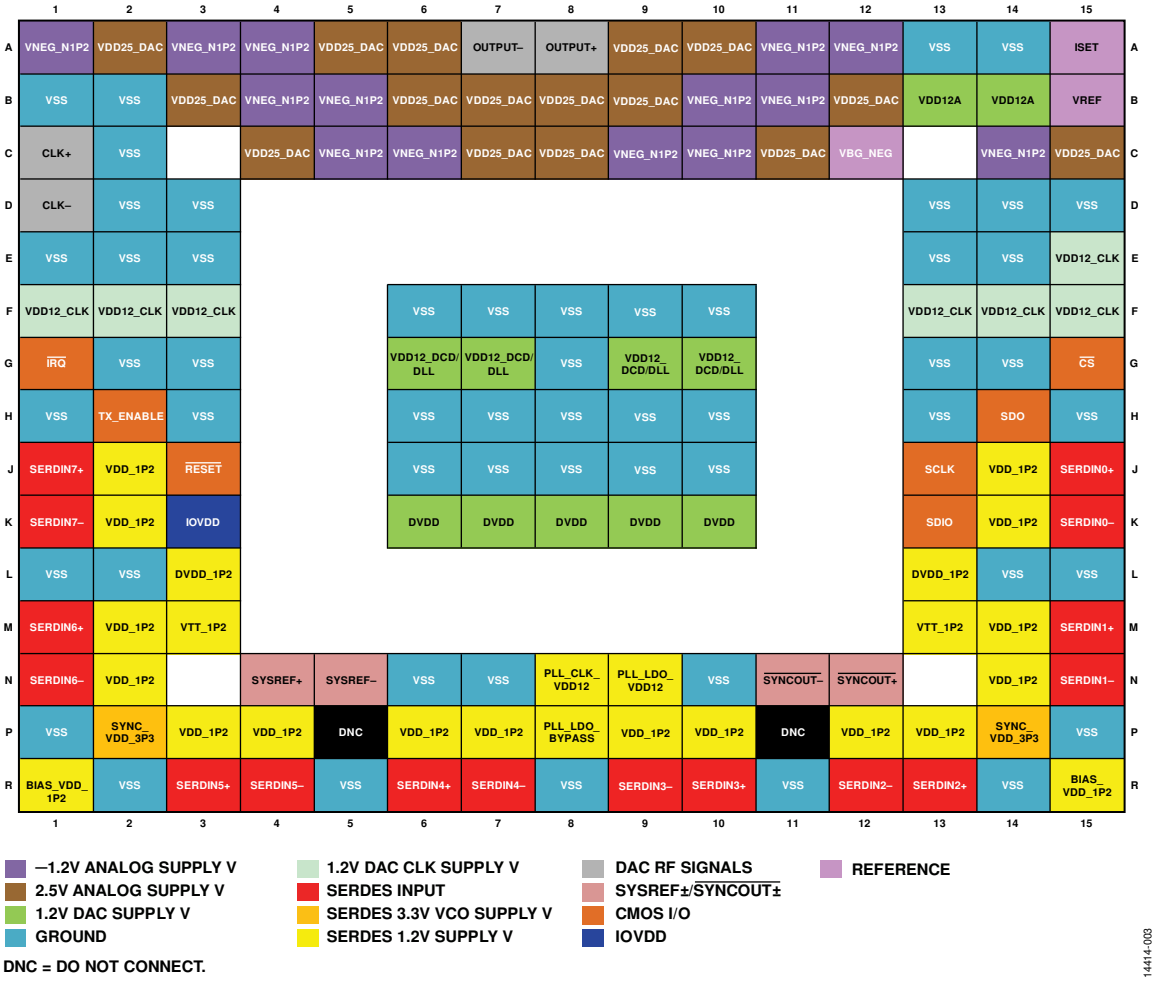

Figure 4. 165-Ball CSP_BGA Pin Configuration

Table 12. 165-Ball CSP_BGA Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, A3, A4, A11, A12, B4, B5, B10, B11, C5, C6, C9, C10, C14	VNEG_N1P2	−1.2 V Analog Supply Voltage.
A2, A5, A6, A9, A10, B3, B6, B7, B8, B9, B12, C4, C7, C8, C11, C15	VDD25_DAC	2.5 V Analog Supply Voltage.
A7	OUTPUT–	DAC Negative Current Output.
A8	OUTPUT+	DAC Positive Current Output.
A13, A14, B1, B2, C2, D2, D3, D13, D14, D15, E1, E2, E3, E13, E14, F6, F7, F8, F9, F10, G2, G3, G8, G13, G14, H1, H3, H6, H7, H8, H9, H10, H13, H15, J6, J7, J8, J9, J10, L1, L2, L14, L15, N6, N7, N10, P1, P15, R2, R5, R8, R11, R14	VSS	Supply Return. Connect these pins to ground.
A15	ISET	Reference Current. Connect this pin to VNEG_N1P2 with a 9.6 kΩ resistor.
B13, B14	VDD12A	1.2 V Analog Supply Voltage.
B15	VREF	1.2 V Reference Input/Output. Connect this pin to VSS with a 1 µF capacitor.
C1, D1	CLK+, CLK–	Positive and Negative DAC Clock Inputs.
C12	VBG_NEG	−1.2 V Reference. Connect this pin to VNEG_N1P2 with a 0.1 µF capacitor.
E15, F1, F2, F3, F13, F14, F15	VDD12_CLK	1.2 V Clock Supply Voltage.
G1	$\overline{\text{IRQ}}$	Interrupt Request Output (Active Low, Open Drain).
G6, G7, G9, G10	VDD12_DCD/DLL	1.2 V Digital Supply Voltage.

Pin No.	Mnemonic	Description
G15	$\overline{CS}$	Serial Port Chip Select Bar (Active Low) Input. CMOS levels on this pin are determined with respect to IOVDD.
H14	SDO	Serial Port Data Output. CMOS levels on this pin are determined with respect to IOVDD.
J13	SCLK	Serial Port Data Clock. CMOS levels on this pin are determined with respect to IOVDD.
K13	SDIO	Serial Port Data Input/Output. CMOS levels on this pin are determined with respect to IOVDD.
J3	$\overline{RESET}$	Reset Bar (Active Low) Input. CMOS levels on this pin are determined with respect to IOVDD.
H2	TX_ENABLE	Transmit Enable Input. This pin can be used instead of the DAC output bias power-down bits in Register 0x040, Bits[1:0] to enable the DAC output. CMOS levels are determined with respect to IOVDD.
P5, P11	DNC	Do Not Connect. Do not connect to these pins.
J2, J14, K2, K14, M2, M14, N2, N14, P3, P4, P6, P7, P9, P10, P12, P13	VDD_1P2	1.2 V SERDES Digital Supply.
K3	IOVDD	Supply Voltage for CMOS Input/Output and SPI. Operational for 1.8 V to 3.3 V plus tolerance (see Table 1 for details).
K6, K7, K8, K9, K10	DVDD	1.2 V Digital Supply Voltage.
L3, L13	DVDD_1P2	1.2 V SERDES Digital Supply Voltage.
M3, M13	VTT_1P2	1.2 V SERDES V_{TT} Digital Supply Voltage.
J1, K1	SERDIN7+, SERDIN7−	SERDES Lane 7 Positive and Negative Inputs.
M1, N1	SERDIN6+, SERDIN6−	SERDES Lane 6 Positive and Negative Inputs.
R3, R4	SERDIN5+, SERDIN5−	SERDES Lane 5 Positive and Negative Inputs.
R6, R7	SERDIN4+, SERDIN4-	SERDES Lane 4 Positive and Negative Inputs.
R9, R10	SERDIN3−, SERDIN3+	SERDES Lane 3 Negative and Positive Inputs.
R12, R13	SERDIN2−, SERDIN2+	SERDES Lane 2 Negative and Positive Inputs.
M15, N15	SERDIN1+, SERDIN1−	SERDES Lane 1 Positive and Negative Inputs.
J15, K15	SERDIN0+, SERDIN0−	SERDES Lane 0 Positive and Negative Inputs.
N4, N5	SYSREF+, SYSREF−	System Reference Positive and Negative Inputs. These pins are self biased for ac coupling. They can be ac-coupled or dc-coupled.
N8	PLL_CLK_VDD12	1.2 V SERDES Phase-Locked Loop (PLL) Clock Supply Voltage.
N9	PLL_LDO_VDD12	1.2 V SERDES PLL Supply.
N11, N12	$\overline{SYNCOUT-}$, $\overline{SYNCOUT+}$	Negative and Positive LVDS Sync (Active Low) Output Signals.
P2, P14	SYNC_VDD_3P3	3.3 V SERDES Sync Supply Voltage.
P8	PLL_LDO_BYPASS	1.2 V SERDES PLL Supply Voltage Bypass.
R1, R15	BIAS_VDD_1P2	1.2 V SERDES Supply Voltage.

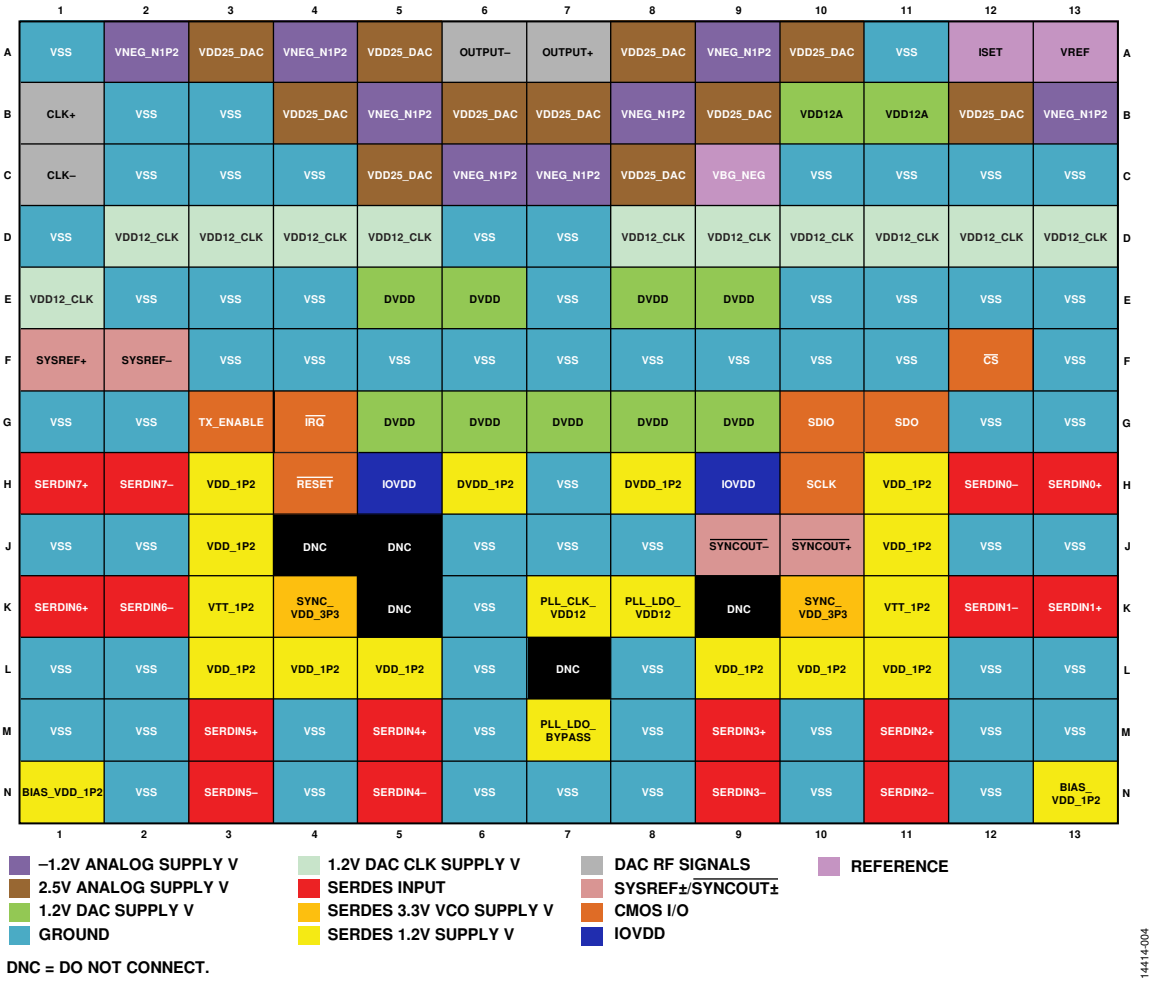

Figure 5. 169-Ball CSP_BGA Pin Configuration

Table 13. 169-Ball CSP_BGA Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, A11, B2, B3, C2, C3, C4, C10, C11, C12, C13, D1, D6, D7, E2, E3, E4, E7, E10, E11, E12, E13, F3, F4, F5, F6, F7, F8, F9, F10, F11, F13, G1, G2, G12, G13, H7, J1, J2, J6, J7, J8, J12, J13, K6, L1, L2, L6, L8, L12, L13, M1, M2, M4, M6, M8, M10, M12, M13, N2, N4, N6, N7, N8, N10, N12	VSS	Supply Return. Connect these pins to ground.
A2, A4, A9, B5, B8, B13, C6, C7	VNEG_N1P2	−1.2 V Analog Supply Voltage.
A3, A5, A8, A10, B4, B6, B7, B9, B12, C5, C8	VDD25_DAC	2.5 V Analog Supply Voltage.
A6	OUTPUT−	DAC Negative Current Output.
A7	OUTPUT+	DAC Positive Current Output.
A12	ISET	Reference Current. Connect this pin to VNEG_N1P2 with a 9.6 kΩ resistor.
A13	VREF	1.2 V Reference Input/Output. Connect this pin to VSS with a 1 µF capacitor.
B1, C1	CLK+, CLK−	Positive and Negative DAC Clock Inputs.
B10, B11	VDD12A	1.2 V Analog Supply Voltage.
C9	VBG_NEG	−1.2 V Reference. Connect this pin to VNEG_N1P2 with a 0.1 µF capacitor.
D2, D3, D4, D5, D8, D9, D10, D11, D12, D13, E1	VDD12_CLK	1.2 V Clock Supply Voltage.
E5, E6, E8, E9, G5, G6, G7, G8, G9	DVDD	1.2 V Digital Supply Voltage.

Pin No.	Mnemonic	Description
F1, F2	SYSREF+, SYSREF−	System Reference Positive and Negative Inputs. These pins are self biased for ac coupling. They can be ac-coupled or dc-coupled.
F12	$\overline{CS}$	Serial Port Chip Select Bar (Active Low) Input. CMOS levels on this pin are determined with respect to IOVDD.
G3	TX_ENABLE	Transmit Enable Input. This pin can be used instead of the DAC output bias power-down bits in Register 0x040, Bits[1:0] to enable the DAC output. CMOS levels are determined with respect to IOVDD.
G4	$\overline{IRQ}$	Interrupt Request Output (Active Low, Open Drain).
G10	SDIO	Serial Port Data Input/Output. CMOS levels on this pin are determined with respect to IOVDD.
G11	SDO	Serial Port Data Output. CMOS levels on this pin are determined with respect to IOVDD.
H10	SCLK	Serial Port Data Clock. CMOS levels on this pin are determined with respect to IOVDD.
H3, H11, J3, J11, L3, L4, L5, L9, L10, L11	VDD_1P2	1.2 V SERDES Digital Supply.
H4	$\overline{RESET}$	Reset Bar (Active Low) Input. CMOS levels on this pin are determined with respect to IOVDD.
H5, H9	IOVDD	Supply Voltage for CMOS Input/Output and SPI. Operational for 1.8 V to 3.3 V (see Table 1 for details).
H6, H8	DVDD_1P2	1.2 V SERDES Digital Supply Voltage.
H1, H2	SERDIN7+, SERDIN7−	SERDES Lane 7 Positive and Negative Inputs.
K1, K2	SERDIN6+, SERDIN6−	SERDES Lane 6 Positive and Negative Inputs.
M3, N3	SERDIN5+, SERDIN5−	SERDES Lane 5 Positive and Negative Inputs.
M5, N5	SERDIN4+, SERDIN4−	SERDES Lane 4 Positive and Negative Inputs.
M9, N9	SERDIN3+, SERDIN3−	SERDES Lane 3 Positive and Negative Inputs.
M11, N11	SERDIN2+, SERDIN2−	SERDES Lane 2 Positive and Negative Inputs.
K12, K13	SERDIN1−, SERDIN1+	SERDES Lane 1 Negative and Positive Inputs.
H12, H13	SERDIN0−, SERDIN0+	SERDES Lane 0 Negative and Positive Inputs.
J4, J5, K5, K9, L7	DNC	Do Not Connect. Do not connect to these pins.
J9, J10	$\overline{SYNCOUT-}$, $\overline{SYNCOUT+}$	Negative and Positive LVDS Sync (Active Low) Output Signals.
K3, K11	VTT_1P2	1.2 V SERDES V_{TT} Digital Supply Voltage.
K4, K10	SYNC_VDD_3P3	3.3 V SERDES Sync Supply Voltage.
K7	PLL_CLK_VDD12	1.2 V SERDES PLL Clock Supply Voltage.
K8	PLL_LDO_VDD12	1.2 V SERDES PLL Supply.
M7	PLL_LDO_BYPASS	1.2 V SERDES PLL Supply Voltage Bypass.
N1, N13	BIAS_VDD_1P2	1.2 V SERDES Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

STATIC LINEARITY

I_{OUTFS} = 40 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

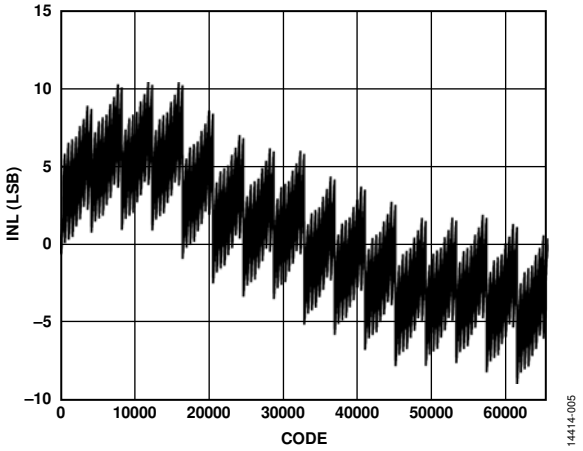

Figure 6. INL, I_{OUTFS} = 20 mA

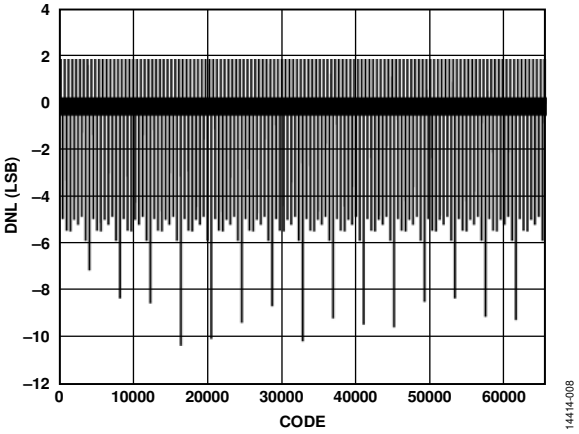

Figure 9. DNL, I_{OUTFS} = 20 mA

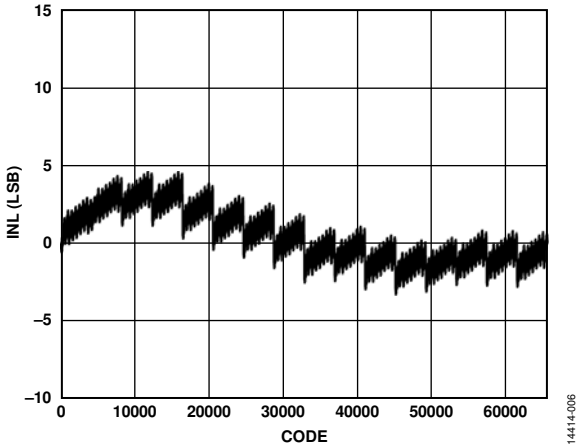

Figure 7. INL, I_{OUTFS} = 30 mA

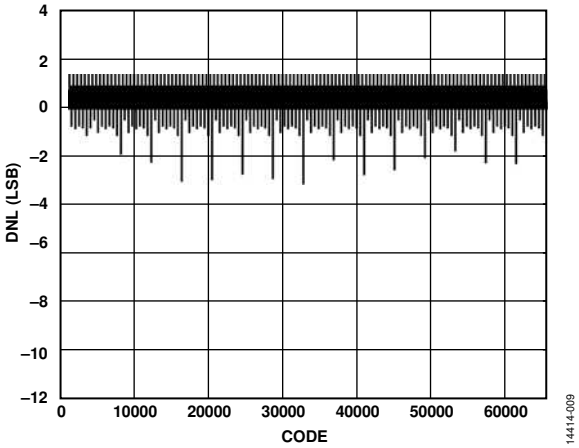

Figure 10. DNL, I_{OUTFS} = 30 mA

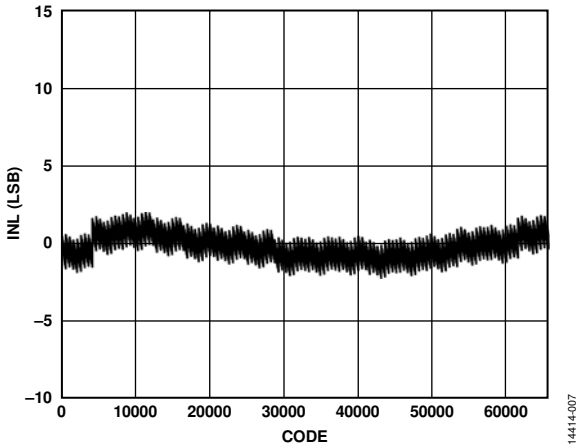

Figure 8. INL, I_{OUTFS} = 40 mA

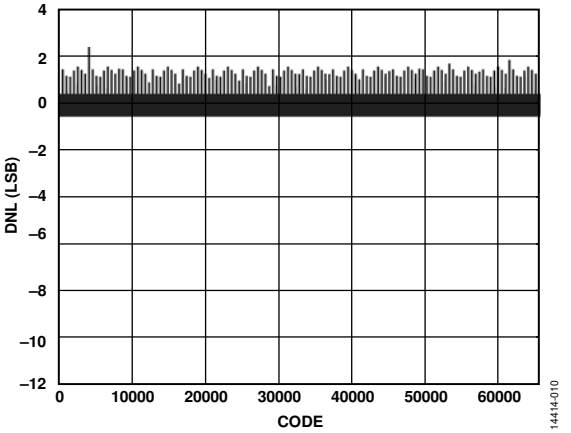

Figure 11. DNL, I_{OUTFS} = 40 mA

AC PERFORMANCE (NRZ MODE)

I_{OUTFS} = 40 mA, f_{DAC} = 5.0 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

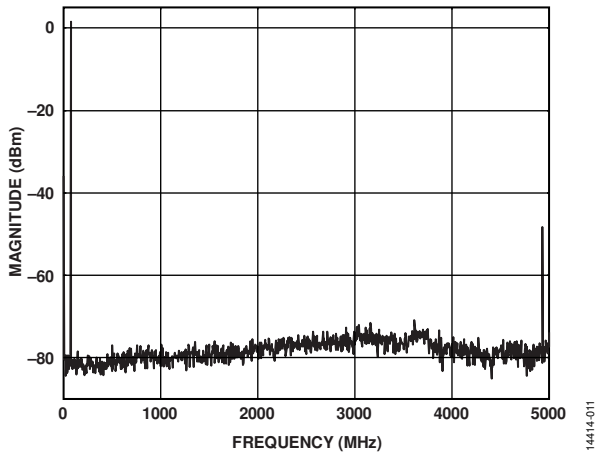

Figure 12. Single-Tone Spectrum at f_{OUT} = 70 MHz

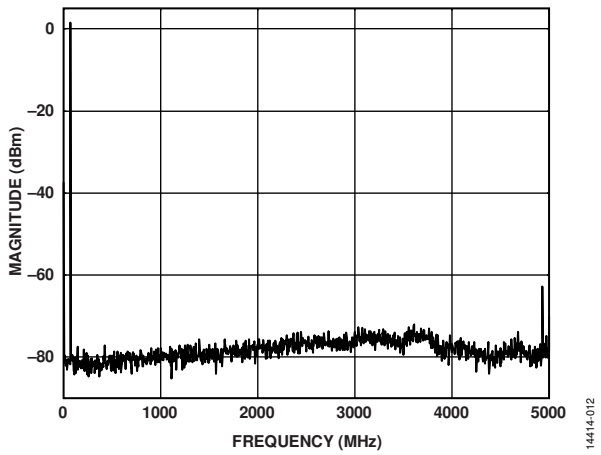

Figure 13. Single-Tone Spectrum at f_{OUT} = 70 MHz (FIR85 Enabled)

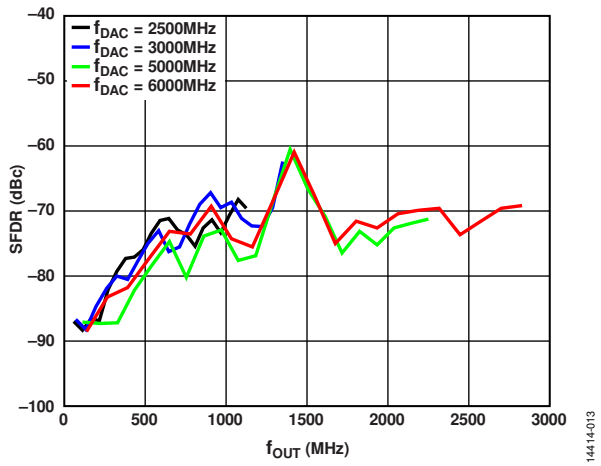

Figure 14. SFDR vs. f_{OUT} over f_{DAC}

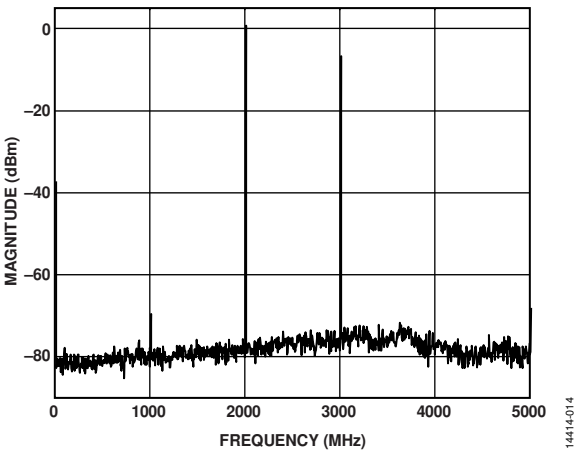

Figure 15. Single-Tone Spectrum at f_{OUT} = 2000 MHz

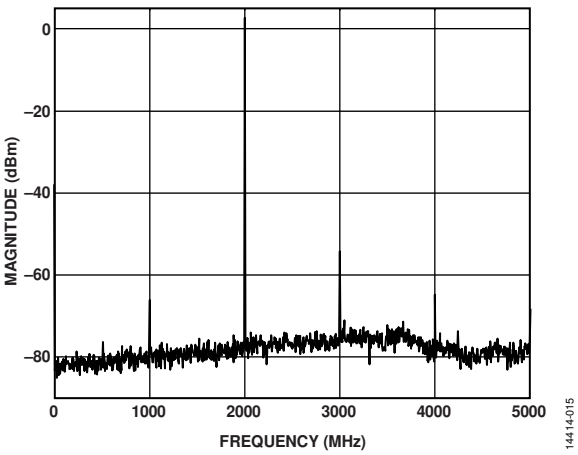

Figure 16. Single-Tone Spectrum at f_{OUT} = 2000 MHz (FIR85 Enabled)

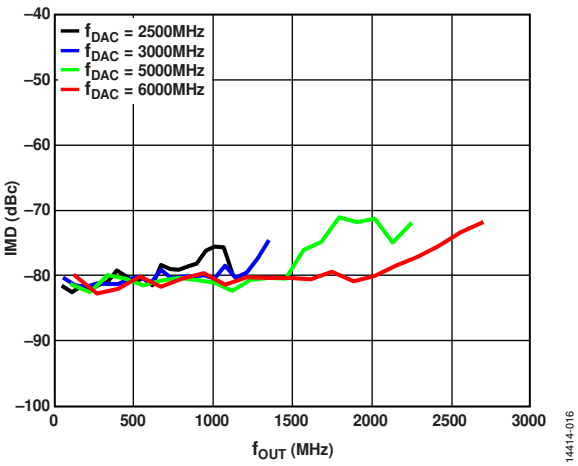

Figure 17. IMD vs. f_{OUT} over f_{DAC}

I_{OUTFS} = 40 mA, f_{DAC} = 5.0 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

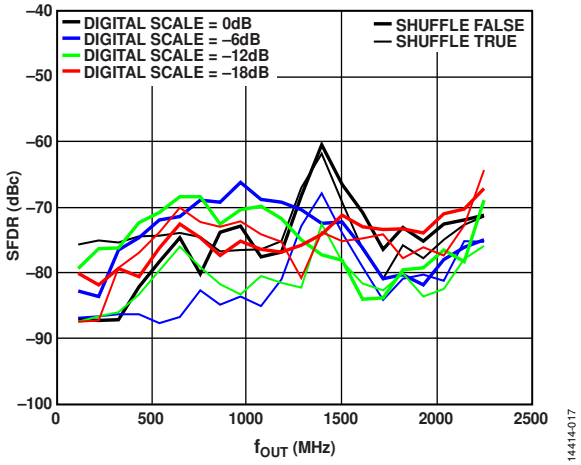

Figure 18. SFDR vs. f_{OUT} over Digital Scale

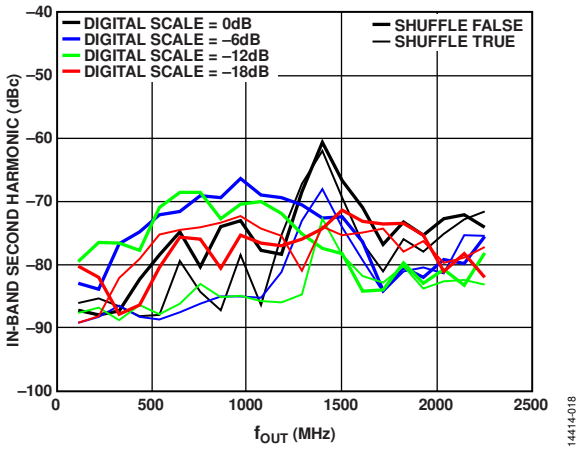

Figure 19. SFDR for In-Band Second Harmonic vs. f_{OUT} over Digital Scale

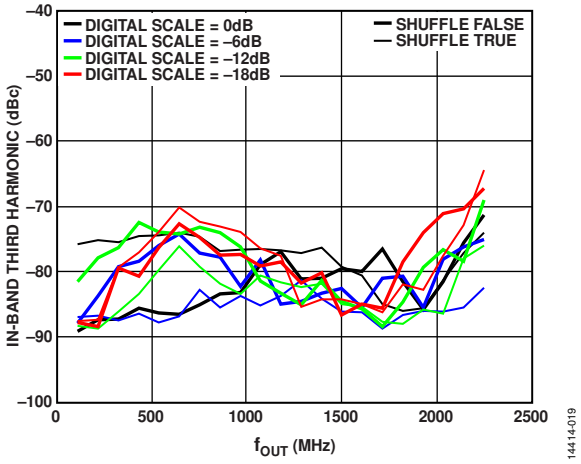

Figure 20. SFDR for In-Band Third Harmonic vs. f_{OUT} over Digital Scale

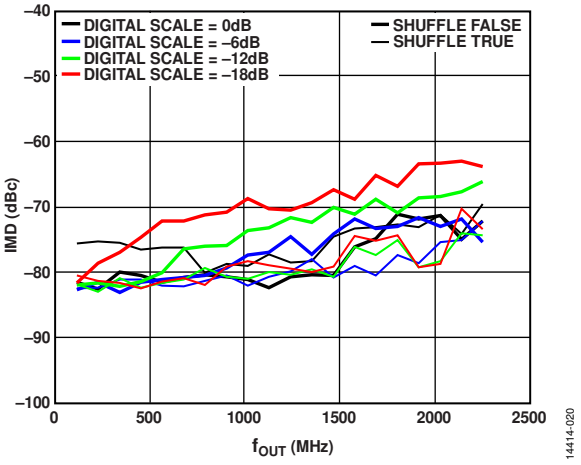

Figure 21. IMD vs. f_{OUT} over Digital Scale

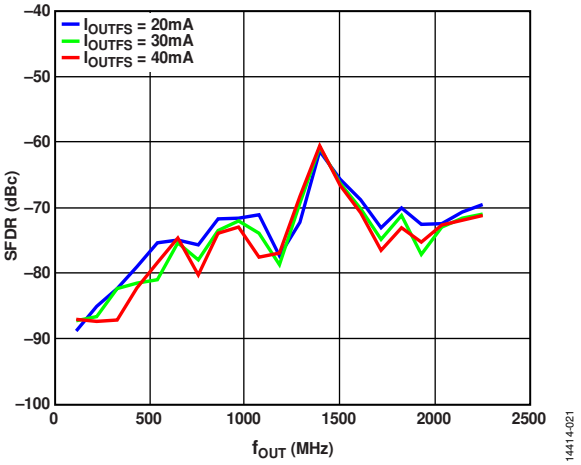

Figure 22. SFDR vs. f_{OUT} over DAC I_{OUTFS}

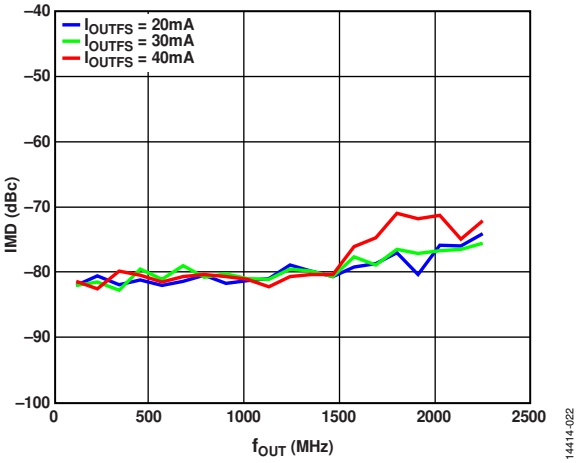

Figure 23. IMD vs. f_{OUT} over DAC I_{OUTFS}

I_{OUTFS} = 40 mA, f_{DAC} = 5.0 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

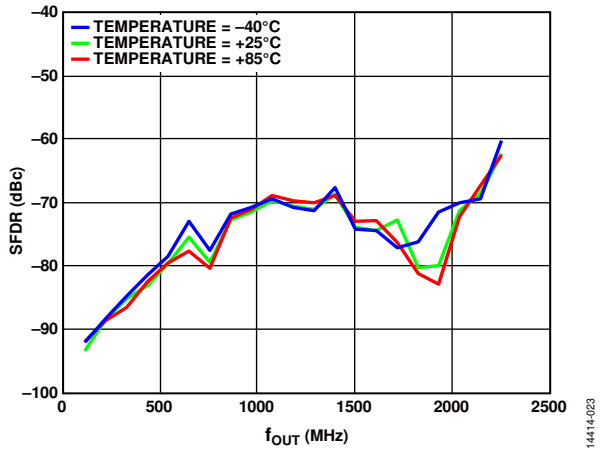

Figure 24. SFDR vs. f_{OUT} over Temperature

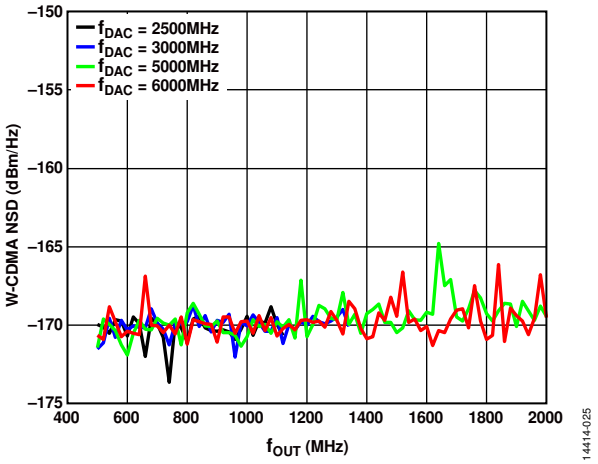

Figure 27. W-CDMA NSD Measured at 70 MHz vs. f_{OUT} over f_{DAC}

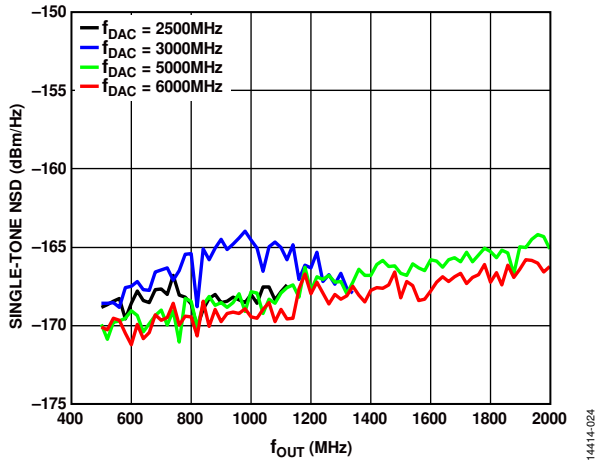

Figure 25. Single-Tone NSD Measured at 70 MHz vs. f_{OUT} over f_{DAC}

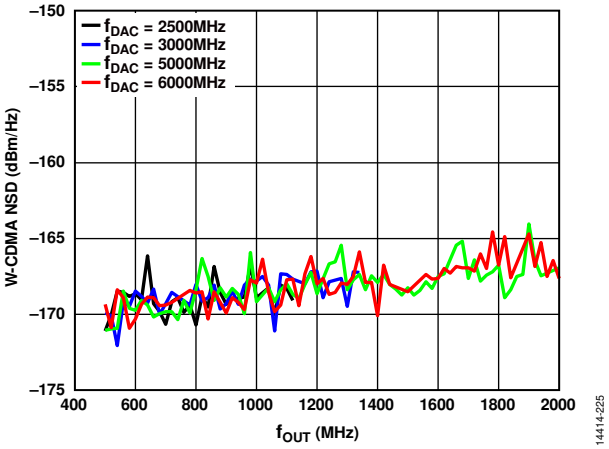

Figure 28. W-CDMA NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT} over f_{DAC}

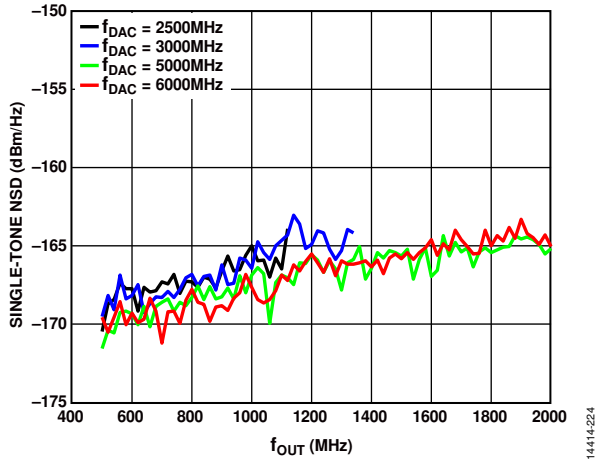

Figure 26. Single-Tone NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT} over f_{DAC}

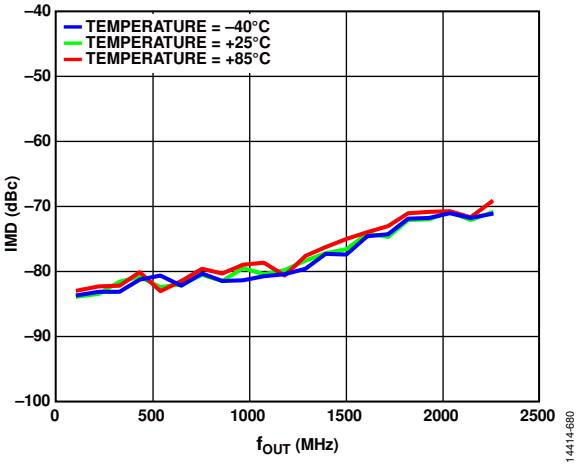

Figure 29. IMD vs. f_{OUT} over Temperature

I_{OUTFS} = 40 mA, f_{DAC} = 5.0 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

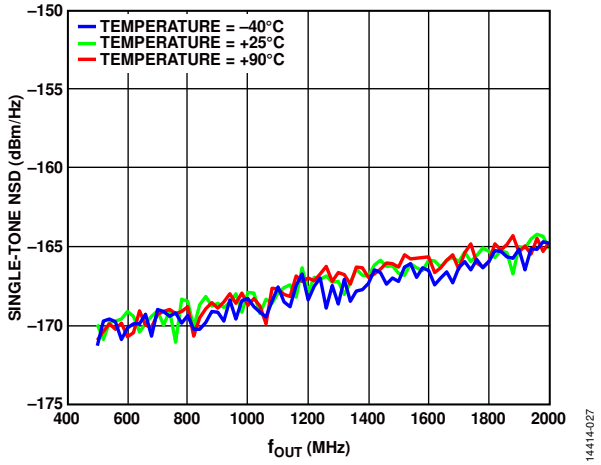

Figure 30. Single-Tone NSD Measured at 70 MHz vs. f_{OUT} over Temperature

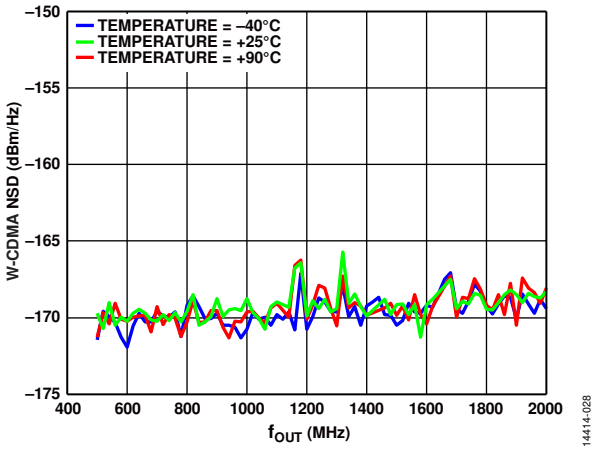

Figure 33. W-CDMA NSD Measured at 70 MHz vs. f_{OUT} over Temperature

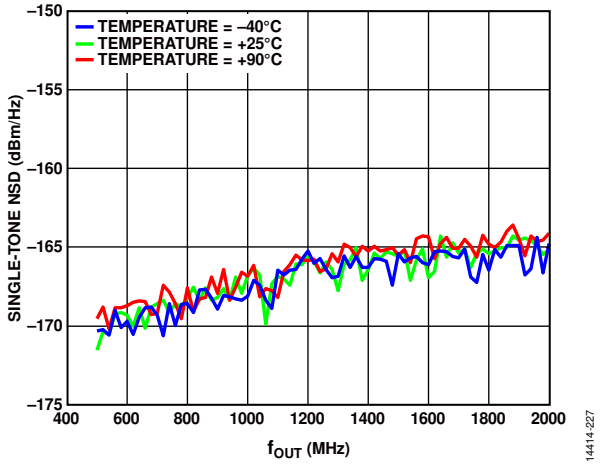

Figure 31. Single-Tone NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT} over Temperature

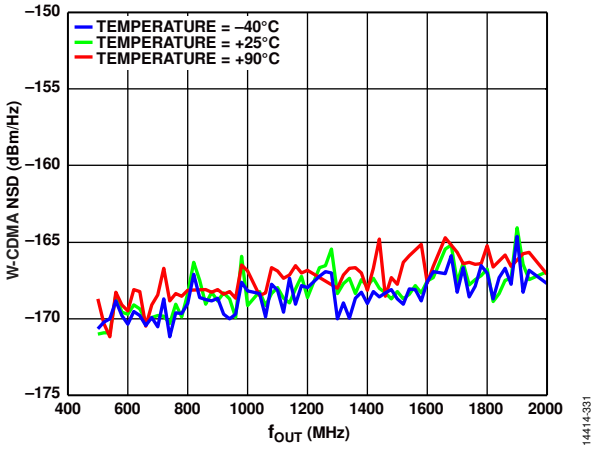

Figure 34. W-CDMA NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT} over Temperature

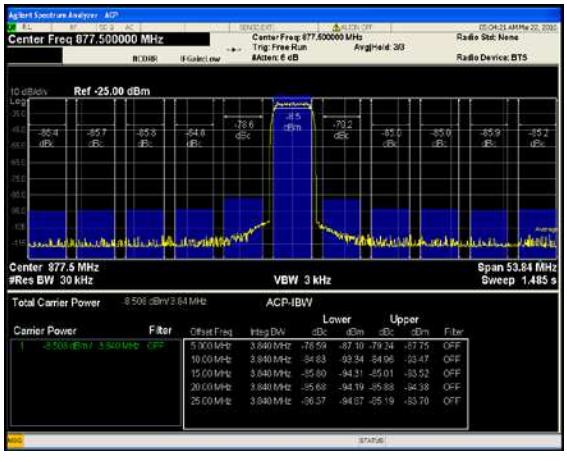

Figure 32. Single-Carrier W-CDMA at 877.5 MHz

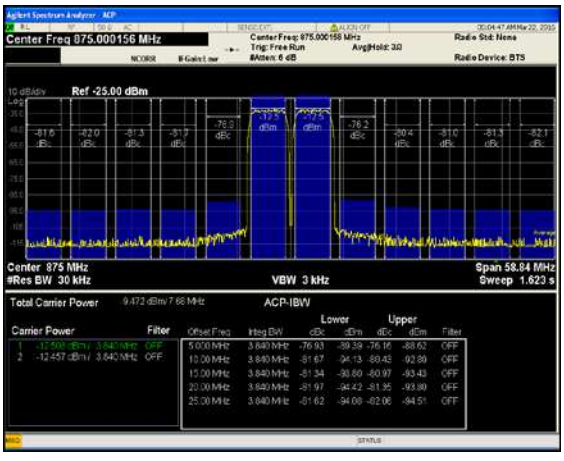

Figure 35. Two-Carrier W-CDMA at 875 MHz

I_{OUTFS} = 40 mA, f_{DAC} = 5.0 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

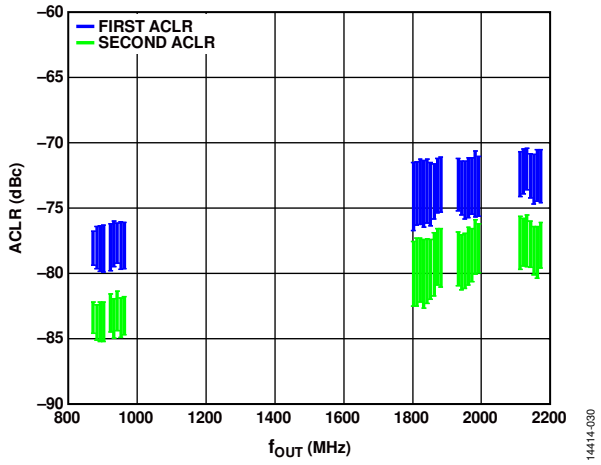

Figure 36. Single-Carrier, W-CDMA Adjacent Channel Leakage Ratio (ACLR) vs. f_{OUT} (First ACLR, Second ACLR)

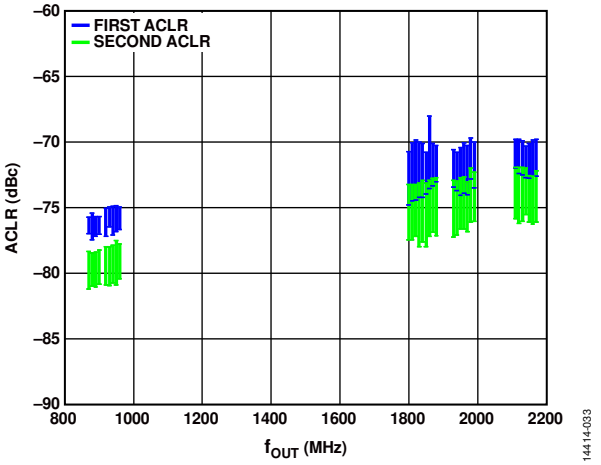

Figure 39. Two-Carrier, W-CDMA ACLR vs. f_{OUT} (First ACLR, Second ACLR)

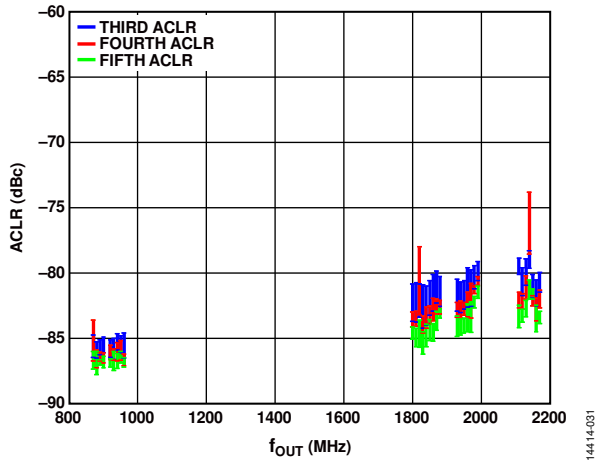

Figure 37. Single-Carrier, W-CDMA ACLR vs. f_{OUT} (Third ACLR, Fourth ACLR, Fifth ACLR)

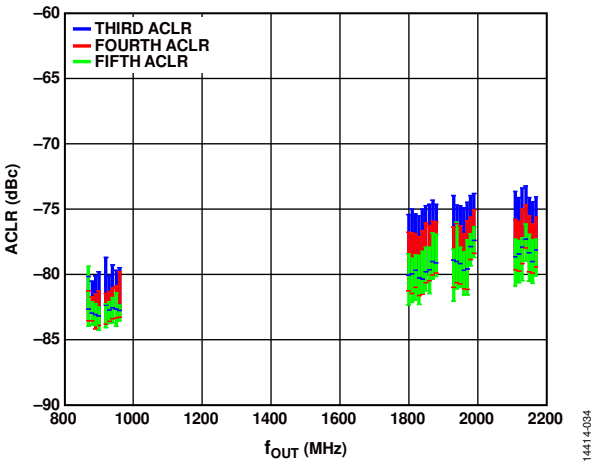

Figure 40. Two-Carrier, W-CDMA ACLR vs. f_{OUT} (Third ACLR, Fourth ACLR, Fifth ACLR)

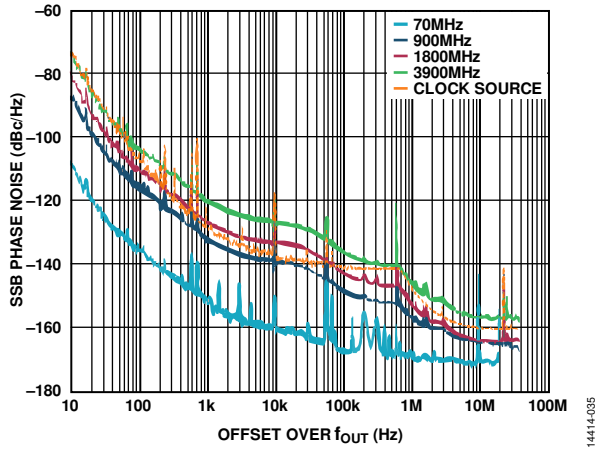

Figure 38. SSB Phase Noise vs. Offset over f_{OUT}, f_{DAC} = 4000 MSPS (Two Different DAC Clock Sources Used for Best Composite Curve)

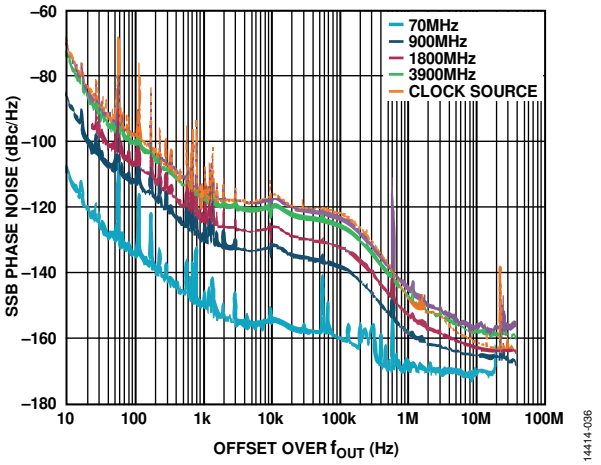

Figure 41. SSB Phase Noise vs. Offset over f_{OUT}, f_{DAC} = 6000 MSPS

AC (MIX-MODE)

I_{OUTFS} = 40 mA, f_{DAC} = 5.0 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

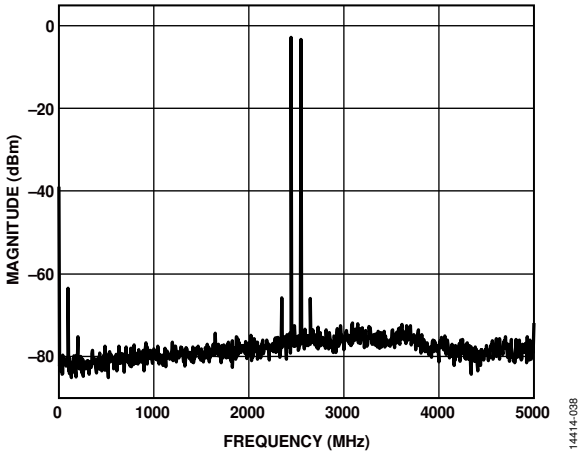

Figure 42. Single-Tone Spectrum at f_{OUT} = 2350 MHz

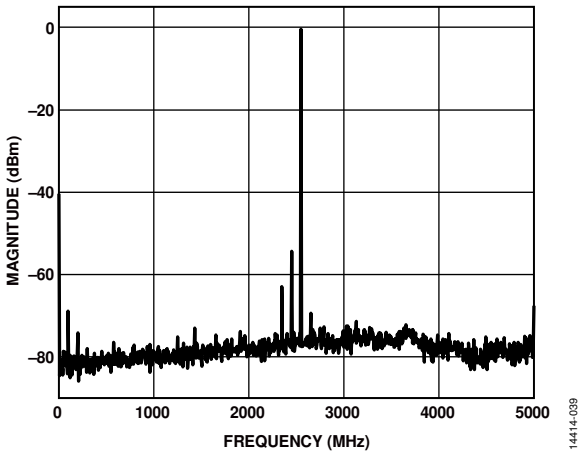

Figure 43. Single-Tone Spectrum at f_{OUT} = 2350 MHz (FIR85 Enabled)

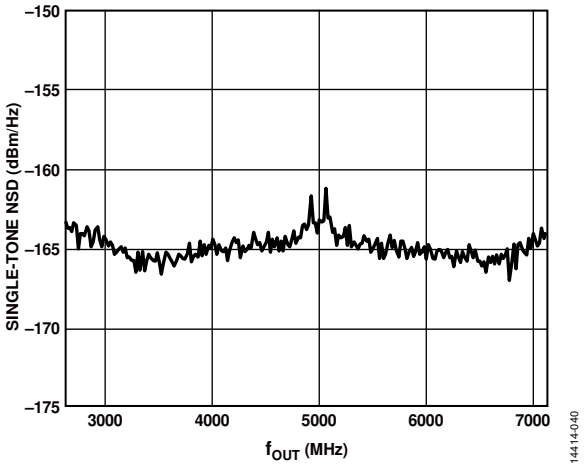

Figure 44. Single-Tone NSD vs. f_{OUT}

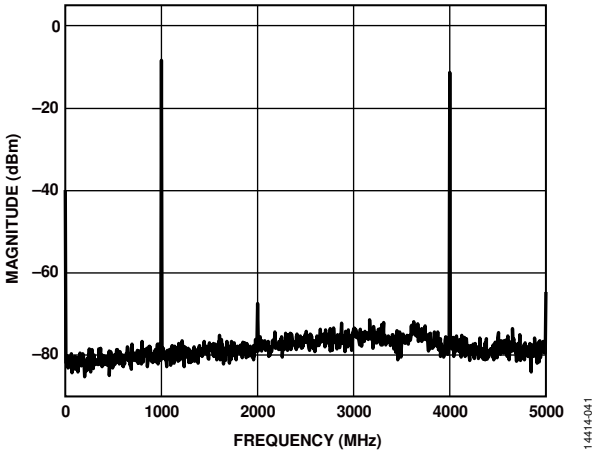

Figure 45. Single-Tone Spectrum at f_{OUT} = 4000 MHz

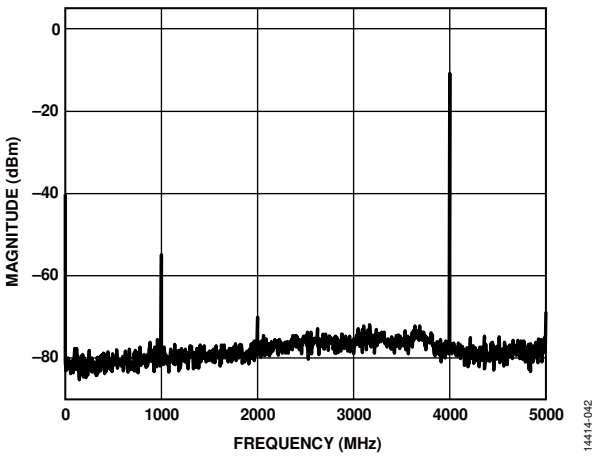

Figure 46. Single-Tone Spectrum at f_{OUT} = 4000 MHz (FIR85 Enabled)

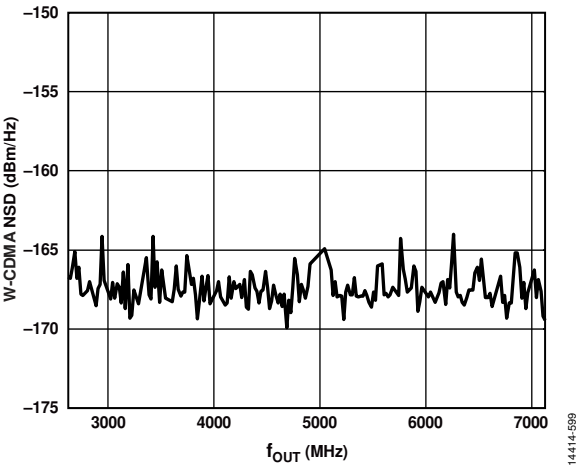

Figure 47. W-CDMA NSD vs. f_{OUT}

I_{OUTFS} = 40 mA, f_{DAC} = 5.0 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

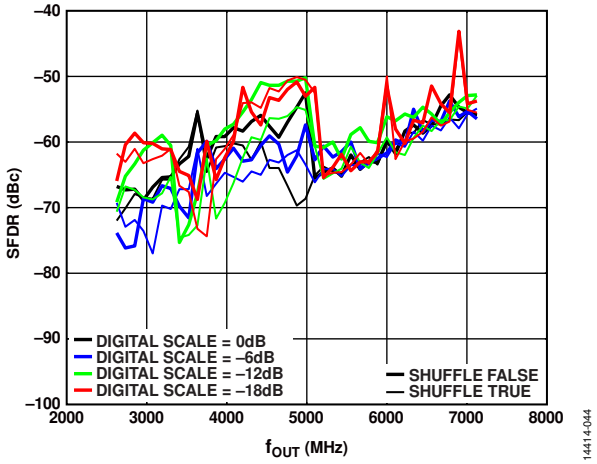

Figure 48. SFDR vs. f_{OUT} over Digital Scale

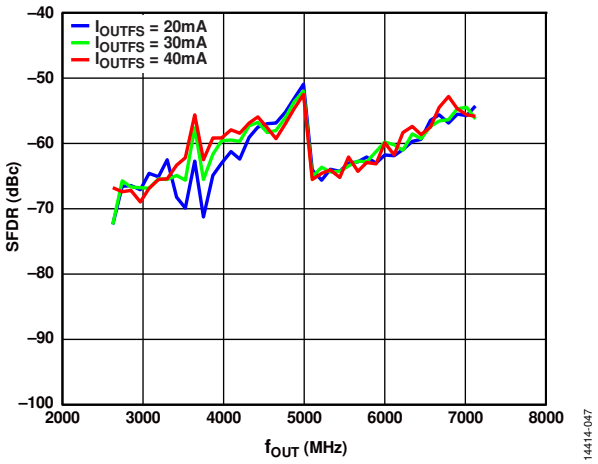

Figure 51. SFDR vs. f_{OUT} over DAC I_{OUTFS}

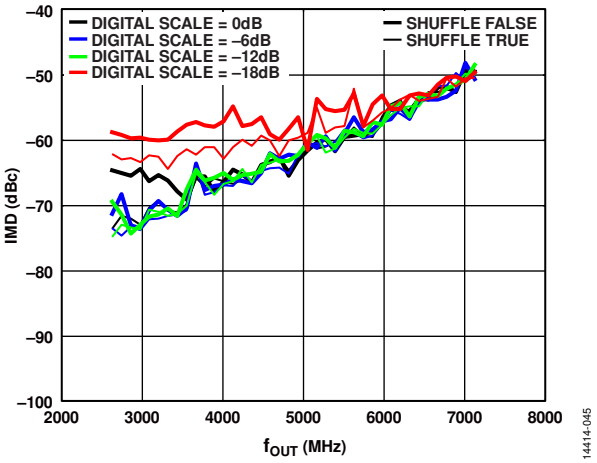

Figure 49. IMD vs. f_{OUT} over Digital Scale

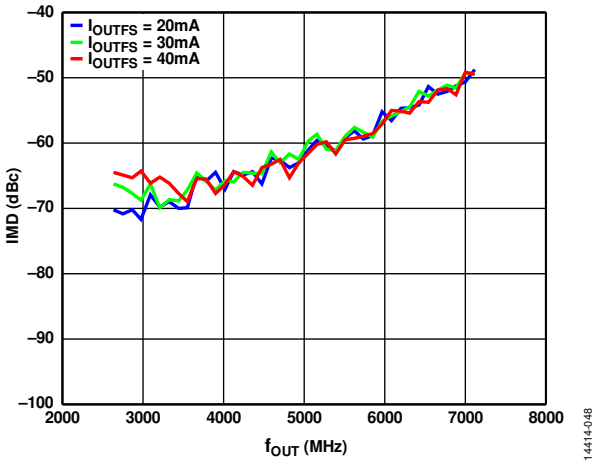

Figure 52. IMD vs. f_{OUT} over DAC I_{OUTFS}

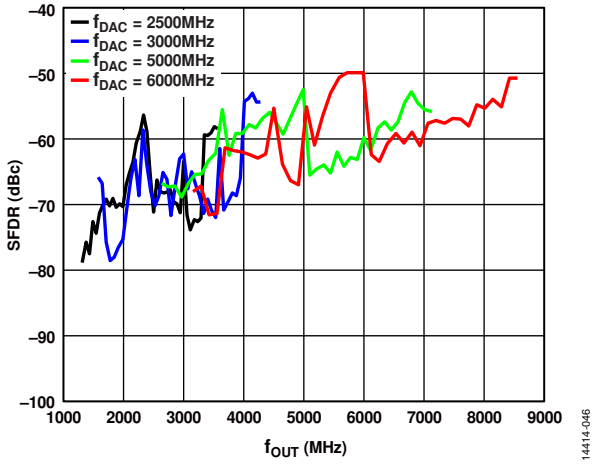

Figure 50. SFDR vs. f_{OUT} over f_{DAC}

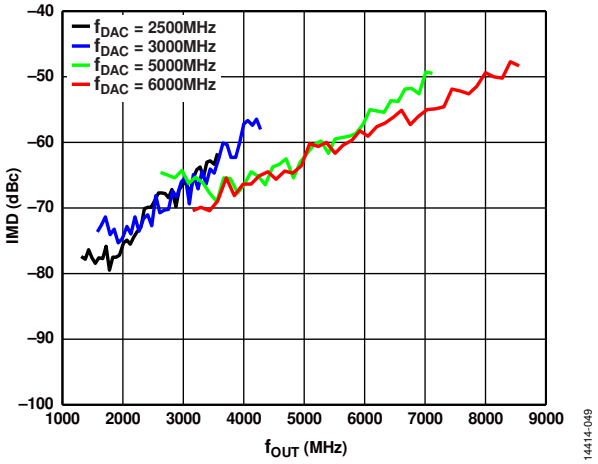

Figure 53. IMD vs. f_{OUT} over f_{DAC}

I_{OUTFS} = 40 mA, f_{DAC} = 5.0 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

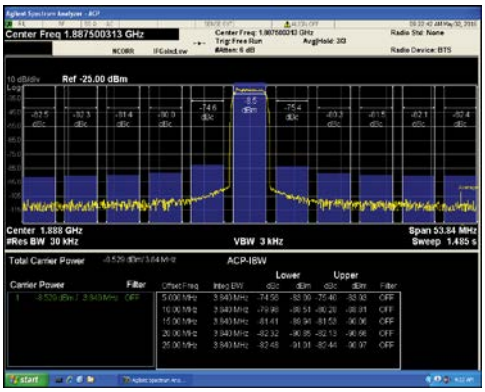

Figure 54. Single-Carrier W-CDMA at 1887.5 MHz

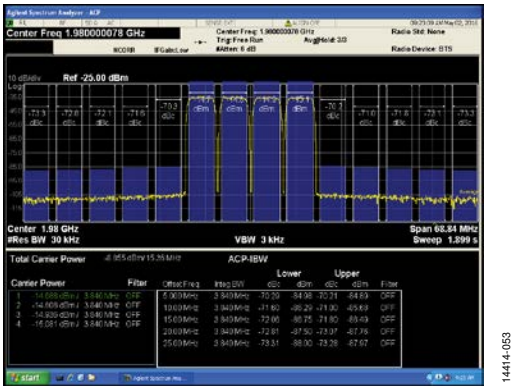

Figure 57. Four-Carrier W-CDMA at 1980 MHz

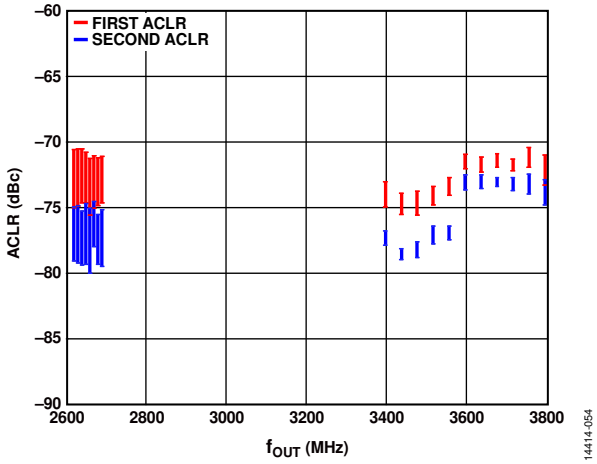

Figure 55. Single-Carrier, W-CDMA ACLR vs. f_{OUT} (First ACLR, Second ACLR)

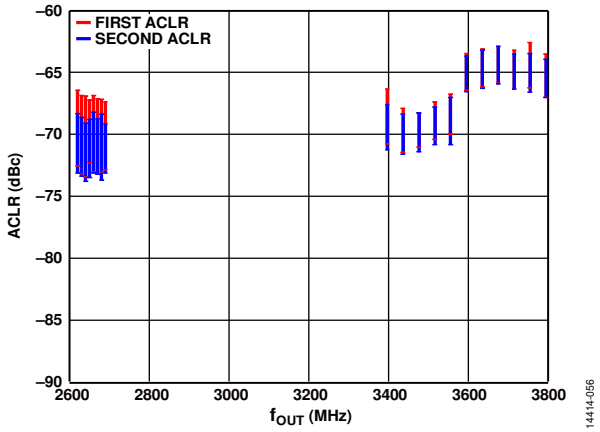

Figure 58. Four-Carrier, W-CDMA ACLR vs. f_{OUT} (First ACLR, Second ACLR)

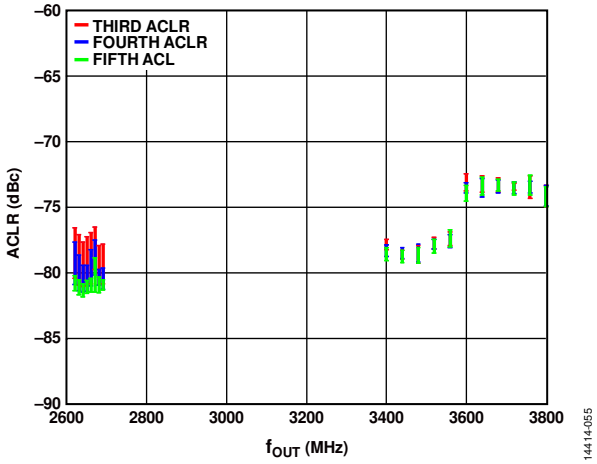

Figure 56. Single-Carrier, W-CDMA ACLR vs. f_{OUT} (Third ACLR, Fourth ACLR, Fifth ACLR)

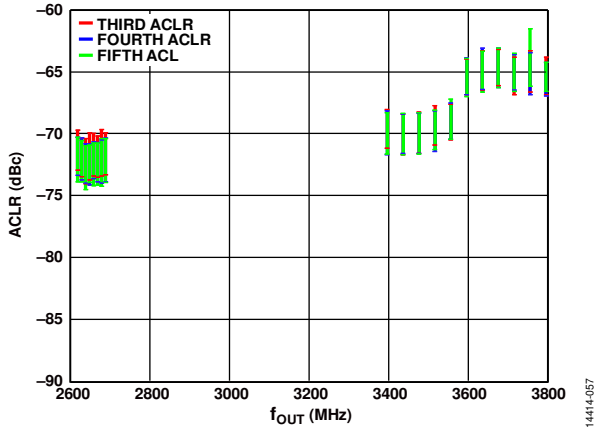

Figure 59. Four-Carrier, W-CDMA ACLR vs. f_{OUT} (Third ACLR, Fourth ACLR, Fifth ACLR)