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Dual, 16-Bit, 6.2 GSPS RF DAC with Single Channelizer

Data Sheet **AD9171**

FEATURES

- Supports single-band wireless applications
  - 1 complex data input channel per RF DAC
  - 516 MSPS maximum complex input data rate per input channel
  - 1 independent NCO per input channel
- Proprietary, low spurious and distortion design
  - 2-tone IMD = −83 dBc at 1.8 GHz, −7 dBFS/tone RF output
  - SFDR < −80 dBc at 1.8 GHz, −7 dBFS RF output
- Flexible 8-lane, 15.4 Gbps JESD204B interface
  - Supports single-band use cases
  - Supports 12-bit high density mode for increased data throughput
- Multiple chip synchronization
  - Supports JESD204B Subclass 1
- Selectable interpolation filter for a complete set of input data rates
  - 2×, 3×, 4×, and 6× configurable data channel interpolation
  - 6× and 8× configurable final interpolation
- Final 48-bit NCO that operates at the DAC rate to support frequency synthesis up to 3.1 GHz
- Transmit enable function allows extra power saving and downstream circuitry protection
- High performance, low noise PLL clock multiplier
  - Supports 6.2 GSPS DAC update rate
  - Observation ADC clock driver with selectable divide ratios
- Low power
  - 1.45 W at 6 GSPS, single-channel mode
- 10 mm × 10 mm, 144-ball BGA_ED with metal enhanced thermal lid, 0.80 mm pitch

APPLICATIONS

- Wireless communications infrastructure
  - Single-band base station radios
- Instrumentation, automatic test equipment (ATE)

GENERAL DESCRIPTION

The AD9171 is a high performance, dual, 16-bit digital-to-analog converter (DAC) that supports DAC sample rates to 6.2 GSPS. The device features an 8-lane, 15.4 Gbps JESD204B data input port, a high performance, on-chip DAC clock multiplier, and digital signal processing capabilities targeted at single-band direct to radio frequency (RF) wireless applications.

The AD9171 features one complex data input channels per RF DAC. Each data input channel includes a configurable gain stage, an interpolation filter, and a channel numerically controlled oscillator (NCO) for flexible, frequency planning. The device supports up to a 516 MSPS complex data rate per input channel.

The AD9171 is available in a 144-ball BGA_ED package.

PRODUCT HIGHLIGHTS

1. Supports one complex data input channel per RF DAC at a maximum complex input data rate of 513 MSPS with 12-bit resolution and 516 MSPS with 16-bit resolution options. There is one independent NCO per input channel.
2. Low power dual converter decreases the amount of power consumption needed in high bandwidth and multichannel applications.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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REVISION HISTORY

1/2018—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

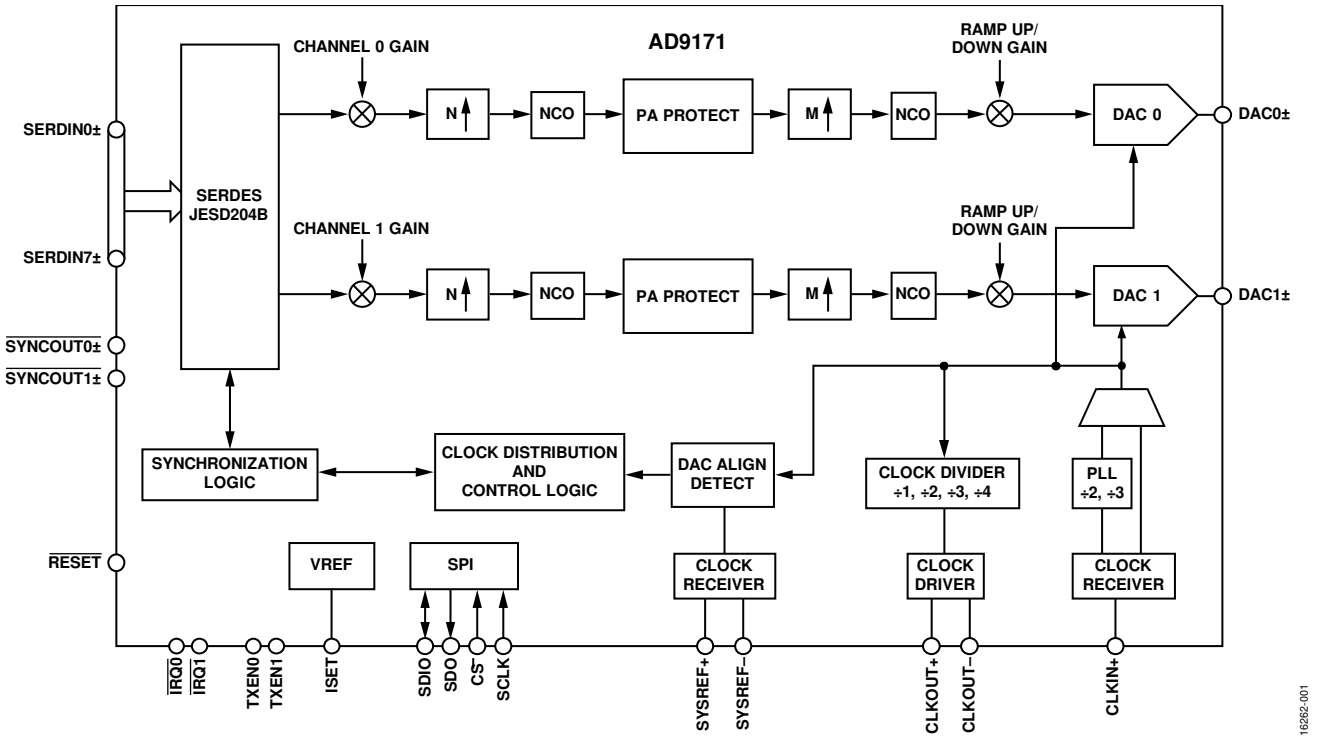

Figure 1. Functional Block Diagram

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bit
ACCURACY					
Integral Nonlinearity (INL)			±7		LSB
Differential Nonlinearity (DNL)			±7		LSB
ANALOG OUTPUTS (DAC0+, DAC0−, DAC1+, DAC1−)					
Gain Error (with Internal ISET Reference)			±15		%
Full-Scale Output Current					
Minimum	R_{SET} = 5 kΩ	14.2	16	17.8	mA
Maximum	R_{SET} = 5 kΩ	23.6	26	28.8	mA
Common-Mode Voltage			0		V
Differential Impedance			100		Ω
DAC DEVICE CLOCK INPUT (CLKIN+, CLKIN−)					
Differential Input Power	R_{LOAD} = 100 Ω differential on-chip				
Minimum			0		dBm
Maximum			6		dBm
Differential Input Impedance[1]			100		Ω
Common-Mode Voltage	AC-coupled		0.5		V
CLOCK OUTPUT DRIVER (CLKOUT+, CLKOUT−)					
Differential Output Power					
Minimum			−9		dBm
Maximum			0		dBm
Differential Output Impedance			100		Ω
Common-Mode Voltage	AC-coupled		0.5		V
Output Frequency		727.5		3000	MHz
TEMPERATURE DRIFT					
Gain			10		ppm/°C
REFERENCE					
Internal Reference Voltage			0.495		V
ANALOG SUPPLY VOLTAGES					
AVDD1.0		0.95	1.0	1.05	V
AVDD1.8		1.71	1.8	1.89	V
DIGITAL SUPPLY VOLTAGES					
DVDD1.0		0.95	1.0	1.05	V
DAVDD1.0		0.95	1.0	1.05	V
DVDD1.8		1.71	1.8	1.89	V
SERDES SUPPLY VOLTAGES					
SVDD1.0		0.95	1.0	1.05	V

[1] See the DAC Input Clock Configurations section for more details.

DIGITAL SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = +25°C, which corresponds to T_J = 51°C.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC UPDATE RATE					
Minimum				2.91	GSPS
Maximum[1]		6.2			GSPS
Adjusted[2]		516			MSPS
DAC PHASE-LOCKED LOOP (PLL) VOLTAGE CONTROLLED OSCILLATOR (VCO) FREQUENCY RANGES					
VCO Output Divide by 2		4.37		6.2	GSPS
VCO Output Divide by 3		2.91		4.14	GSPS
PHASE FREQUENCY DETECT INPUT FREQUENCY RANGES					
9.96 GHz ≤ VCO Frequency ≤ 10.87 GHz		25		225	MHz
VCO Frequency < 9.96 GHz orVCO Frequency > 10.87 GHz		25		770	MHz
DAC DEVICE CLOCK INPUT (CLKIN+, CLKIN−) FREQUENCY RANGES					
PLL Off		2.91		6.2	GHz
PLL On	M divider set to divide by 1	25		770	MHz
	M divider set to divide by 2	50		1540	MHz
	M divider set to divide by 3	75		2310	MHz
	M divider set to divide by 4	100		3080	MHz

[1] The maximum DAC update rate varies depending on the selected JESD204B mode and the lane rate for the given configuration used. The maximum DAC rate according to lane rate and voltage supply levels is listed in Table 3.
[2] The adjusted DAC update rate is calculated as f_{DAC}, divided by the minimum required interpolation factor for a given mode or the maximum channel data rate for a given mode. Different modes have different maximum DAC update rates, minimum interpolation factors, and maximum channel data rates, as shown in Table 13.

POWER SUPPLY DC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DUAL-LINK MODE, Mode 0 (L = 1, M = 2, NP = 16, N = 16)	5.89824 GSPS DAC rate, 184.32 MHz PLL reference clock, 16× total interpolation (2×, 8×), 40 MHz tone at −3 dBFS, channel NCO disabled, main NCO = 1.8425 GHz, SYNCOUTx± in LVDS mode				
AVDD1.0	All supply levels set to nominal values		400	670	mA
	All supplies at 5% tolerance		425	745	mA
AVDD1.8			110	130	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply				
	All supply levels set to nominal values		625	960	mA
	All supplies at 5% tolerance		670	1070	mA
DVDD1.8			35	50	mA
SVDD1.0			175	340	mA
Total Power Dissipation			1.45	2.15	W

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DUAL-LINK, MODE 3 (NCO ONLY, SINGLE-CHANNEL MODE, NO SERDES)	6 GSPS DAC rate, 300 MHz PLL reference clock, 8× total interpolation (1×, 8×), no input tone (dc internal level = 0x50FF), channel NCO = 40 MHz, main NCO = 1.8425 GHz				
AVDD1.0					
	All supply levels set to nominal values		410	660	mA
	All supplies at 5% tolerance		435	750	mA
AVDD1.8			110	130	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply				
	All supply levels set to nominal values		500	780	mA
	All supplies at 5% tolerance		515	950	mA
DVDD1.8			0.3	1	mA
SVDD1.0	All supply levels set to nominal values		5	100	mA
	All supplies at 5% tolerance		3	120	mA
Total Power Dissipation			1.1	1.671	W

SERIAL PORT AND CMOS PIN SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 4.

Parameter	Symbol	Test Comments/Conditions	Min	Typ	Max	Unit
WRITE OPERATION		See Figure 48				
Maximum SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$		80			MHz
SCLK Clock High	t_{PWH}	SCLK = 20 MHz	5.03			ns
SCLK Clock Low	t_{PWL}	SCLK = 20 MHz	1.6			ns
SDIO to SCLK Setup Time	t_{DS}		1.154			ns
SCLK to SDIO Hold Time	t_{DH}		0.577			ns
$\overline{CS}$ to SCLK Setup Time	t_S		1.036			ns
SCLK to $\overline{CS}$ Hold Time	t_H		−5.3			ps
READ OPERATION		See Figure 47				
SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$				48.58	MHz
SCLK Clock High	t_{PWH}		5.03			ns
SCLK Clock Low	t_{PWL}		1.6			ns
SDIO to SCLK Setup Time	t_{DS}		1.158			ns
SCLK to SDIO Hold Time	t_{DH}		0.537			ns
$\overline{CS}$ to SCLK Setup Time	t_S		1.036			ns
SCLK to SDIO Data Valid Time	t_{DV}		9.6			ns
SCLK to SDO Data Valid Time	t_{DV}		13.7			ns
$\overline{CS}$ to SDIO Output Valid to High-Z		Not shown in Figure 47 or Figure 48	5.4			ns
$\overline{CS}$ to SDO Output Valid to High-Z		Not shown in Figure 47 or Figure 48	9.59			ns
INPUTS (SDIO, SCLK, $\overline{CS}$, $\overline{RESET}$, TXEN0, and TXEN1)						
Voltage Input						
High	V_{IH}		1.48			V
Low	V_{IL}				0.425	V
Current Input						
High	I_{IH}				±100	nA
Low	I_{IL}		±100			nA

Parameter	Symbol	Test Comments/Conditions	Min	Typ	Max	Unit
OUTPUTS (SDIO, SDO)						
Voltage Output						
High	V_{OH}					
0 mA load			1.69			V
4 mA load			1.52			V
Low	V_{OL}					
0 mA load					0.045	V
4 mA load					0.175	V
Current Output						
High	I_{OH}			4		mA
Low	I_{OL}			4		mA
INTERRUPT OUTPUTS ($\overline{IRQ0}$, $\overline{IRQ1}$)						
Voltage Output						
High	V_{OH}		1.71			V
Low	V_{OL}				0.075	V

DIGITAL INPUT DATA TIMING SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LATENCY[1]					
Channel Interpolation Factor, Main Datapath Interpolation Factor	LMFC_VAR_x = 12, LMFC_DELAY_x = 12, unless otherwise noted				
2×, 6×	JESD204B Mode 3		1970		DAC clock cycle
	JESD204B Mode 5		1770		DAC clock cycle
2×, 8×	JESD204B Mode 0		2020		DAC clock cycle
	JESD204B Mode 3		2500		DAC clock cycle
3×, 6×	JESD204B Mode 3		2880		DAC clock cycle
	JESD204B Mode 5		2630		DAC clock cycle
3×, 8×	JESD204B Mode 3		3310		DAC clock cycle
	JESD204B Mode 5		2980		DAC clock cycle
4×, 6×	JESD204B Mode 0		2410		DAC clock cycle
4×, 8×	JESD204B Mode 0		3090		DAC clock cycle
6×, 6×	JESD204B Mode 0		3190		DAC clock cycle
6×, 8×	JESD204B Mode 0		4130		DAC clock cycle
DETERMINISTIC LATENCY					
Fixed				13	PCLK[2]
Variable				2	PCLK cycles
SYSREF± TO LOCAL MULTIFRAME CLOCK (LMFC) DELAY	Indicates the relationship between the SYSREF± signal and the LMFC Clock Phase 0		0		DAC clock cycles

[1] Total latency (or pipeline delay) through the device is calculated as follows: total latency = interface latency + fixed latency + variable latency + pipeline delay.
[2] PCLK is the internal processing clock for the AD9171 and equals the lane rate ÷ 40.

JESD204B INTERFACE ELECTRICAL AND SPEED SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B SERIAL INTERFACE RATE (SERIAL LANE RATE)			3		15.4	Gbps
JESD204B DATA INPUTS						
Input Leakage Current		T_A = 25°C				
Logic High		Input level = 1.0 V ± 0.25 V		10		µA
Logic Low		Input level = 0 V		−4		µA
Unit Interval	UI		333		66.7	ps
Common-Mode Voltage	V_{RCM}	AC-coupled	−0.05		+1.1	V
Differential Voltage	R_V_{DIFF}		110		1050	mV
Differential Impedance	Z_{RDIFF}	At dc	80	100	120	Ω
SYSREF± INPUT						
Differential Impedance				100		Ω
DIFFERENTIAL OUTPUTS ($\overline{\text{SYNCOUT0}}$±, $\overline{\text{SYNCOUT1}}$±)[1]		Driving 100 Ω differential load				
Output Differential Voltage	V_{OD}		320	390	460	mV
Output Offset Voltage	V_{OS}		1.08	1.12	1.15	V
SINGLE-ENDED OUTPUTS ($\overline{\text{SYNCOUT0}}$±, $\overline{\text{SYNCOUT1}}$±)		Driving 100 Ω differential load				
Output Voltage						
High	V_{OH}		1.69			V
Low	V_{OL}				0.045	V
Current Output						
High	I_{OH}			0		mA
Low	I_{OL}			0		mA

[1] IEEE Standard 1596.3 LVDS compatible.

INPUT DATA RATES AND SIGNAL BANDWIDTH SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 7.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT DATA RATE PER INPUT CHANNEL	1 complex channel enabled			516	MSPS
COMPLEX SIGNAL BANDWIDTH PER INPUT CHANNEL	1 complex channel enabled (0.8 × f_{DATA})			413.34	MHz
MAXIMUM NCO CLOCK RATE					
Channel NCO		−258		+258	MHz
Main NCO				6.2	GHz
MAXIMUM NCO SHIFT FREQUENCY RANGE					
Channel NCO		−258.34		+258.34	MHz
Main NCO		−3.1		+3.1	GHz
MAXIMUM FREQUENCY SPACING ACROSS INPUT CHANNELS	Maximum NCO output frequency × 0.8			412.8	MHz

[1] Values listed for these parameters are the maximum possible when considering all JESD204B modes of operation. Some modes are more limiting, based on other parameters.

AC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. For the minimum and maximum, T_J = −40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 8.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
Single Tone, f_{DAC} = 6000 MSPS, Mode 0 (L = 1, M = 2)	−7 dBFS, shuffle enabled				
f_{OUT} = 100 MHz			−85		dBc
f_{OUT} = 500 MHz			−85		dBc
f_{OUT} = 950 MHz			−78		dBc
f_{OUT} = 1840 MHz			−75		dBc
f_{OUT} = 2650 MHz			−69		dBc
Single-Band Application—Band 3 (1805 MHz to 1880 MHz)	Mode 0, 2× to 8×, f_{DAC} = 6000 MSPS, 368.64 MHz reference clock				
SFDR Harmonics	−7 dBFS, shuffle enabled				
In-Band			−82		dBc
Digital Predistortion (DPD) Band	DPD bandwidth = data rate × 0.8		−80		dBc
Second Harmonic			−82		dBc
Third Harmonic			−80		dBc
Fourth and Fifth Harmonic			−95		dBc
SFDR Nonharmonics	−7 dBFS, shuffle enabled				
In-Band			−74		dBc
DPD Band			−74		dBc
ADJACENT CHANNEL LEAKAGE RATIO					
4C-WCDMA	−1 dBFS digital backoff				
f_{DAC} = 6000 MSPS, Mode 0 (L = 1, M = 2)	f_{OUT} = 1840 MHz		−71		dBc
	f_{OUT} = 2650 MHz		−66		dBc
THIRD-ORDER INTERMODULATION DISTORTION (IMD)	Two-tone test, −7 dBFS/tone, 1 MHz spacing				
f_{DAC} = 6000 MSPS, Mode 0 (L = 1, M = 2)	f_{OUT} = 1840 MHz		−74		dBc
	f_{OUT} = 2650 MHz		−72		dBc
NOISE SPECTRAL DENSITY (NSD)	0 dBFS, NSD measurement taken at 10% away from f_{OUT}, shuffle off				
Single Tone, f_{DAC} = 6000 MSPS, Mode 3 (L = 2, M = 2)					
f_{OUT} = 100 MHz			−169		dBm/Hz
f_{OUT} = 500 MHz			−167		dBm/Hz
f_{OUT} = 950 MHz			−166		dBm/Hz
f_{OUT} = 1840 MHz			−163		dBm/Hz
f_{OUT} = 2150 MHz			−162		dBm/Hz
SINGLE-SIDEBAND PHASE NOISE OFFSET	Loop filter component values according to Figure 89 are as follows: C1 = 22 nF, R1 = 232 Ω, C2 = 2.4 nF, C3 = 33 nF; PFD frequency = 500 MHz, f_{OUT} = 1.8 GHz, f_{DAC} = 6 GHz				
1 kHz			−97		dBc/Hz
10 kHz			−105		dBc/Hz
100 kHz			−114		dBc/Hz
600 kHz			−126		dBc/Hz
1.2 MHz			−133		dBc/Hz
1.8 MHz			−137		dBc/Hz
6 MHz			−148		dBc/Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC TO DAC OUTPUT ISOLATION	Taken using the AD9171-FMC-EBZ evaluation board				
Single-Band—f_{DAC} = 6000 MSPS, Mode 0 (L = 1, M = 2)					
	f_{OUT} = 1840 MHz		−81		dBc
	f_{OUT} = 2100 MHz		−78		dBc
	f_{OUT} = 2650 MHz		−73		dBc

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
ISET, FILT_COARSE, FILT_BYP, FILT_VCM	−0.3 V to AVDD1.8 + 0.3 V
SERDINx±	−0.2 V to SVDD1.0 + 0.2 V
$\overline{\text{SYNCOUT0}}$±, $\overline{\text{SYNCOUT1}}$±, $\overline{\text{RESET}}$, TXEN0, TXEN1, $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{CS}}$, SCLK, SDIO, SDO	−0.3 V to DVDD1.8 + 0.3 V
DAC0±, DAC1±, CLKIN±, CLKOUT±, FILT_FINE	−0.2 V to AVDD1.0 + 0.2 V
SYSREF±	−0.2 V to DVDD1.0 + 0.2 V
AVDD1.0, DVDD1.0, SVDD1.0 to GND	−0.2 V to +1.2 V
AVDD1.8, DVDD1.8 to GND	−0.3 V to 2.2 V
Maximum Junction Temperature (T_J)[1]	118°C
Storage Temperature Range	−65°C to +150°C
Reflow	260°C

[1] Some operating modes of the device may cause the device to approach or exceed the maximum junction temperature during operation at supported ambient temperatures. Removal of heat from the device may require additional measures such as active airflow, heat sinks, or other measures.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The AD9171 reflow profile is in accordance with the JEDEC JESD20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Thermal resistances and thermal characterization parameters are specified vs. the number of PCB layers in different airflow velocities (in m/sec). The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 10.

Use the values in Table 11 in compliance with JEDEC 51-12.

Table 10. Simulated Thermal Resistance vs. PCB Layers[1]

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	25.3	2.4[3]	3.0[4]	°C/W
	1.0	22.6	N/A	N/A	°C/W
	2.5	21.0	N/A	N/A	°C/W
12-Layer PCB[2]	0.0	15.4	2.4	2.6	°C/W
	1.0	13.1	N/A	N/A	°C/W
	2.5	11.6	N/A	N/A	°C/W

[1] N/A means not applicable.
[2] Non JEDEC thermal resistance.
[3] 1SOP PCB with no vias in PCB.
[4] 1SOP PCB with 7 × 7 standard JEDEC vias.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

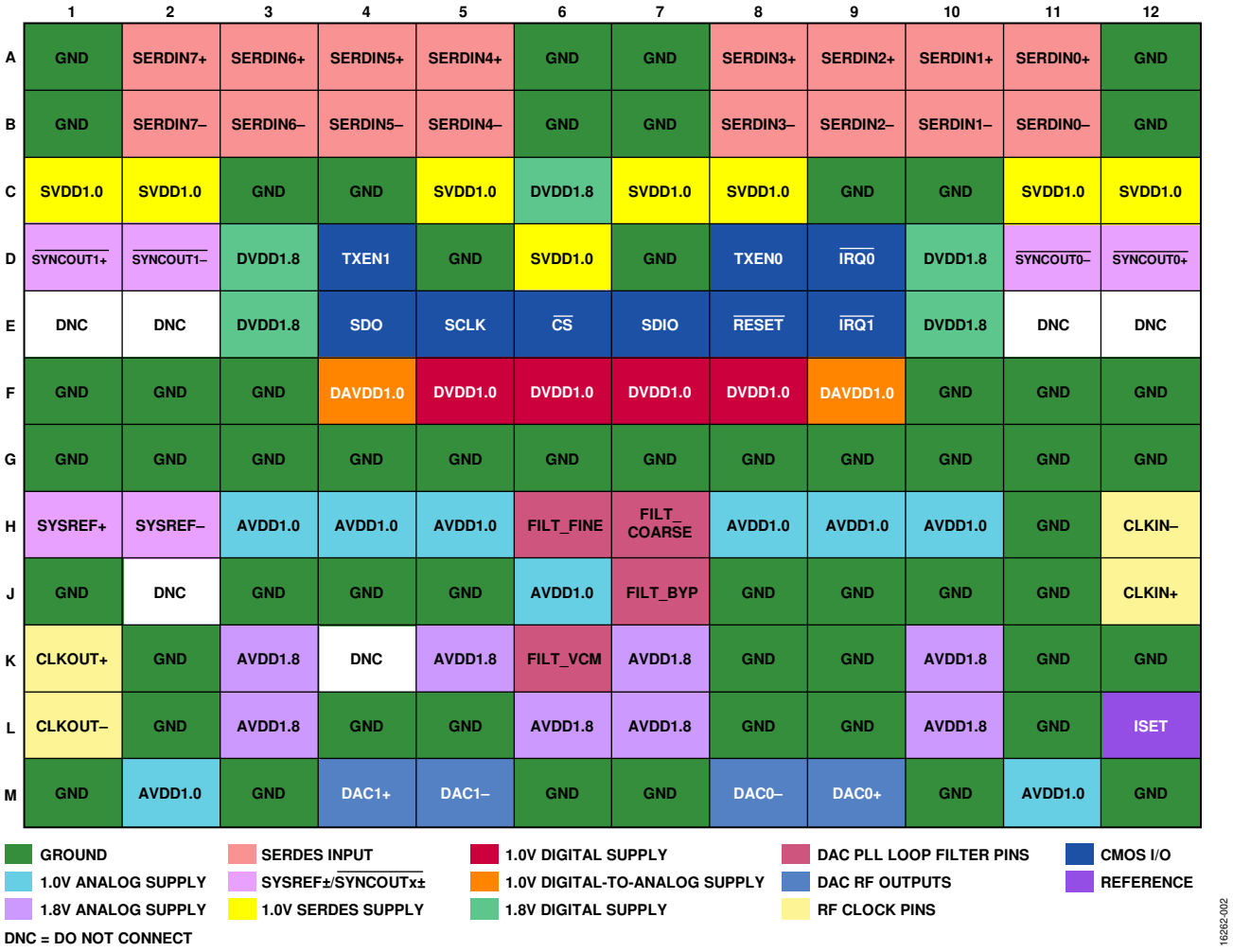

Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1.0 V Supply		
H3 to H5, H8 to H10, J6, M2, M11	AVDD1.0	1.0 V Clock and Analog Supplies. These pins supply the clock receivers, clock distribution, the on-chip DAC clock multiplier, and the DAC analog core. Clean power supply rail sources are required on these pins.
F5 to F8	DVDD1.0	1.0 V Digital Supplies. These pins supply power to the DAC digital circuitry. Clean power supply rail sources are required on these pins.
F4, F9	DAVDD1.0	1.0 V Digital to Analog Supplies. These pins can share a supply rail with the DVDD1.0 supply (electrically connected) but must have separate supply plane and decoupling capacitors for the PCB layout to improve isolation for these two pins. Clean power supply rail sources are required on these pins.
C1, C2, C5, C7, C8, C11, C12, D6	SVDD1.0	1.0 V SERDES Supplies to the JESD204B Data Interface. Clean power supply rail sources are required on these pins.
1.8 V Supply		
K3, K5, K7, K10, L3, L6, L7, L10	AVDD1.8	1.8 V Analog Supplies to the On-Chip DAC Clock Multiplier and the DAC Analog Core. Clean power supply rail sources are required on these pins.
C6, D3, D10, E3, E10	DVDD1.8	1.8 V Digital Supplies to the JESD204B Data Interface and the Other Input/Output Circuitry, Such as the Serial Port Interface (SPI). Clean power supply rail sources are required on these pins.

Pin No.	Mnemonic	Description
Ground		
A1, A6, A7, A12, B1, B6, B7, B12, C3, C4, C9, C10, D5, D7, F1 to F3, F10 to F12, G1 to G12, H11, J1, J3 to J5, J8 to J11, K2, K8, K9, K11, K12, L2, L4, L5, L8, L9, L11, M1, M3, M6, M7, M10, M12	GND	Device Common Ground.
RF Clock		
J12	CLKIN+	Positive Device Clock Input. This pin is the clock input for the on-chip DAC clock multiplier, REFCLK, when the DAC PLL is on. This pin is also the clock input for the DAC sample clock or device clock (DACCLK) when the DAC PLL is off. AC couple this input. There is an internal 100 Ω resistor between this pin and CLKIN−.
H12	CLKIN−	Negative Device Clock Input.
K1	CLKOUT+	Positive Device Clock Output. This pin is the clock output of a divided down DACCLK and is available with the DAC PLL on and off. The divide down ratios are by 1, 2, or 4.
L1	CLKOUT−	Negative Device Clock Output.
System Reference		
H1	SYSREF+	Positive System Reference Input. It is recommended to ac couple this pin, but dc coupling is also acceptable. See Table 7 for the dc common-mode voltage.
H2	SYSREF−	Negative System Reference Input. It is recommended to ac couple this pin, but dc coupling is also acceptable. See Table 7 for the dc common-mode voltage.
On-Chip DAC PLL Loop Filter		
H6	FILT_FINE	On-Chip DAC Clock Multiplier and PLL Fine Loop Filter Input.
H7	FILT_COARSE	On-Chip DAC Clock Multiplier and PLL Coarse Loop Filter Input.
J7	FILT_BYP	On-Chip DAC Clock Multiplier and LDO Bypass.
K6	FILT_VCM	On-Chip DAC Clock Multiplier and VCO Common-Mode Input.
SERDES Data Bits		
A2	SERDIN7+	SERDES Data Bit 7, Positive.
B2	SERDIN7−	SERDES Data Bit 7, Negative.
A3	SERDIN6+	SERDES Data Bit 6, Positive.
B3	SERDIN6−	SERDES Data Bit 6, Negative.
A4	SERDIN5+	SERDES Data Bit 5, Positive.
B4	SERDIN5−	SERDES Data Bit 5, Negative.
A5	SERDIN4+	SERDES Data Bit 4, Positive.
B5	SERDIN4−	SERDES Data Bit 4, Negative.
A8	SERDIN3+	SERDES Data Bit 3, Positive.
B8	SERDIN3−	SERDES Data Bit 3, Negative.
A9	SERDIN2+	SERDES Data Bit 2, Positive.
B9	SERDIN2−	SERDES Data Bit 2, Negative.
A10	SERDIN1+	SERDES Data Bit 1, Positive.
B10	SERDIN1−	SERDES Data Bit 1, Negative.
A11	SERDIN0+	SERDES Data Bit 0, Positive.
B11	SERDIN0−	SERDES Data Bit 0, Negative.
Sync Output		
D12	$\overline{\text{SYNCOUT0+}}$	Positive Sync (Active Low) Output Signal, Channel Link 0. This pin is LVDS or CMOS selectable.
D11	$\overline{\text{SYNCOUT0−}}$	Negative Sync (Active Low) Output Signal, Channel Link 0. This pin is LVDS or CMOS selectable.
D1	$\overline{\text{SYNCOUT1+}}$	Positive Sync (Active Low) Output Signal, Channel Link 1. This pin is LVDS or CMOS selectable.
D2	$\overline{\text{SYNCOUT1−}}$	Negative Sync (Active Low) Output Signal, Channel Link 1. This pin is LVDS or CMOS selectable.

Pin No.	Mnemonic	Description
Serial Port Interface		
E4	SDO	Serial Port Data Output (CMOS Levels with Respect to DVDD1.8).
E7	SDIO	Serial Port Data Input/Output (CMOS Levels with Respect to DVDD1.8).
E5	SCLK	Serial Port Clock Input (CMOS Levels with Respect to DVDD1.8).
E6	$\overline{CS}$	Serial Port Chip Select, Active Low (CMOS Levels with Respect to DVDD1.8).
E8	$\overline{RESET}$	Reset, Active Low (CMOS Levels with Respect to DVDD1.8).
Interrupt Request		
D9	$\overline{IRQ0}$	Interrupt Request 0. This pin is an open-drain, active low output (CMOS levels with respect to DVDD1.8). Connect a pull-up resistor to DVDD1.8 to prevent this pin from floating when inactive.
E9	$\overline{IRQ1}$	Interrupt Request 1. This pin is an open-drain, active low output (CMOS levels with respect to DVDD1.8). Connect a pull-up resistor to DVDD1.8 to prevent this pin from floating when inactive.
CMOS Input/Outputs		
D8	TXEN0	Transmit Enable for DAC0. The CMOS levels are determined with respect to DVDD1.8.
D4	TXEN1	Transmit Enable for DAC1. The CMOS levels are determined with respect to DVDD1.8.
DAC Analog Outputs		
M9	DAC0+	DAC0 Positive Current Output.
M8	DAC0−	DAC0 Negative Current Output.
M4	DAC1+	DAC1 Positive Current Output.
M5	DAC1−	DAC1 Negative Current Output.
Reference		
L12	ISET	Device Bias Current Setting Pin. Connect a 5 kΩ resistor, preferably with 0.1% tolerance and ±25 ppm/°C to this pin.
Do Not Connect		
E1, E2, E11, E12, J2, K4	DNC	Do Not Connect. Do not connect to these pins.

TYPICAL PERFORMANCE CHARACTERISTICS

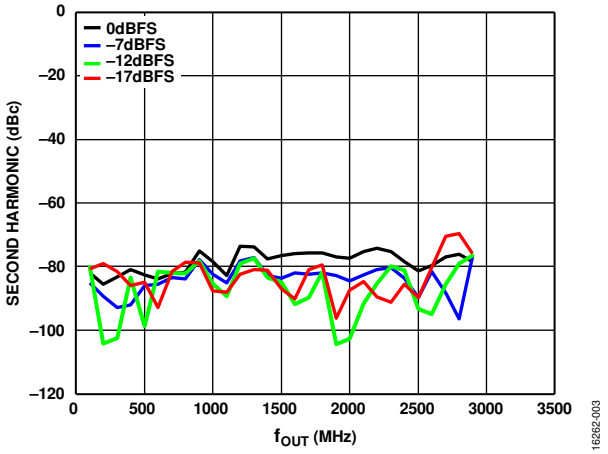

Figure 3. Second Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×

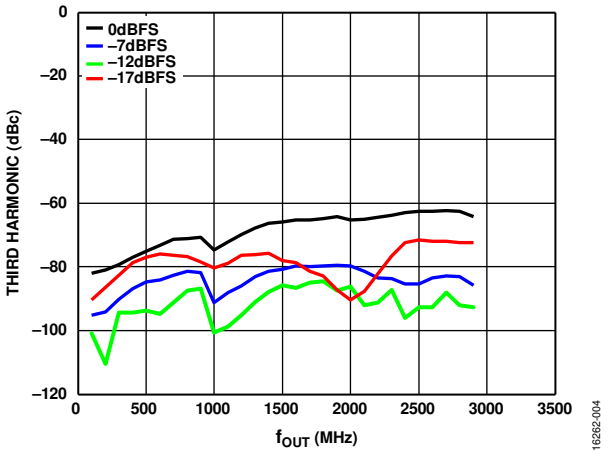

Figure 4. Third Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×

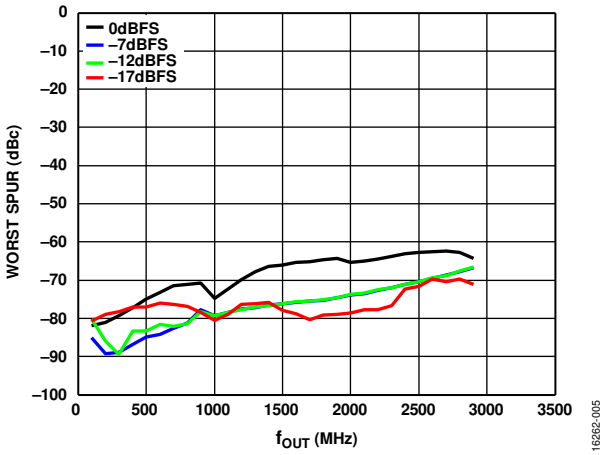

Figure 5. Worst Spur (dBc) vs. f_{OUT} over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×

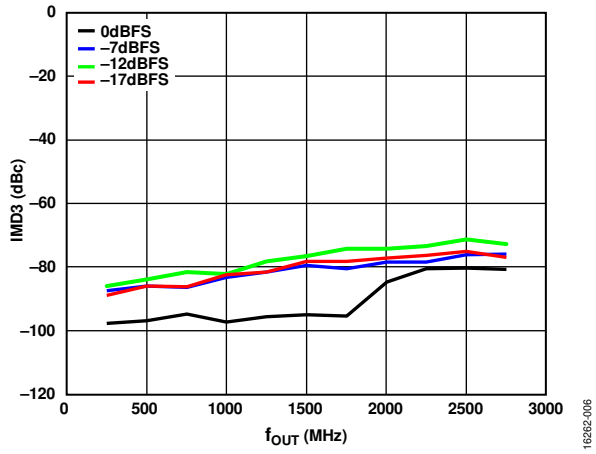

Figure 6. IMD3 vs. f_{OUT} over Digital Scale (Mode 0) 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×, 1 MHz Tone Spacing

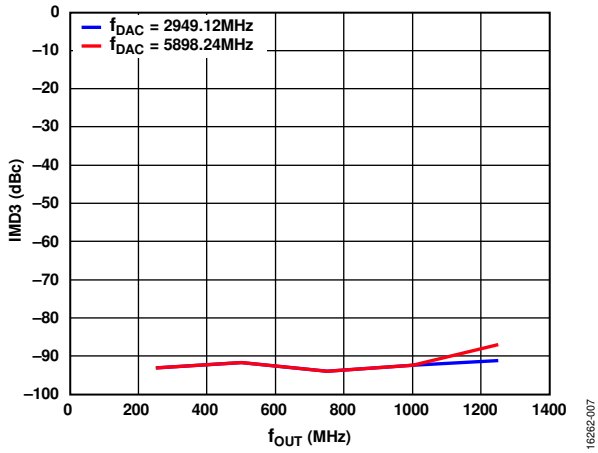

Figure 7. IMD3 vs. f_{OUT} over f_{DAC} (Mode 0), Channel Interpolation 2×, Main Interpolation 8×, 1 MHz Tone Spacing

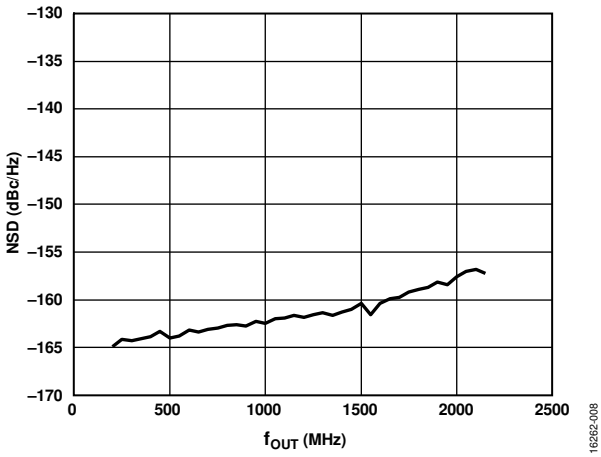

Figure 8. Single-Tone NSD Measured at 70 MHz vs. f_{OUT}, f_{DAC} = 5.89824 GHz, 16-Bit Resolution, Shuffle On

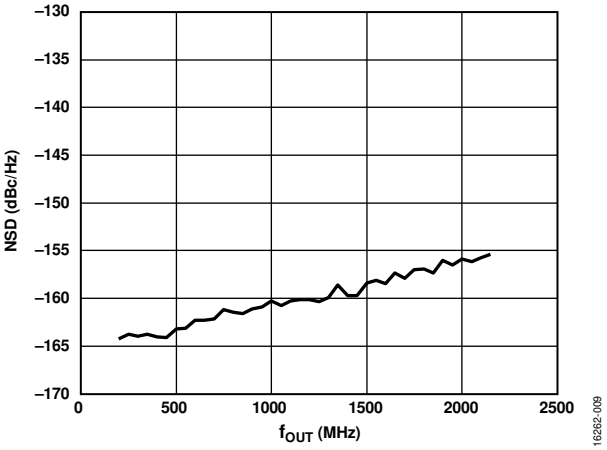

Figure 9. Single-Tone NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT}, f_{DAC} = 5.89824 GHz, 16-Bit Resolution, Shuffle On

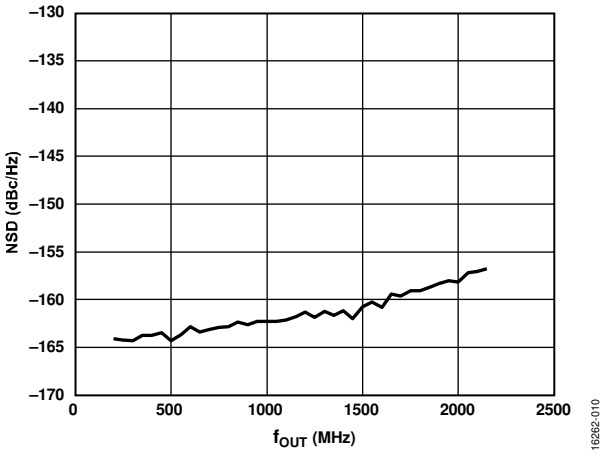

Figure 10. Single-Tone NSD Measured at 70 MHz vs. f_{OUT}, f_{DAC} = 5.89824 GHz,12-Bit Resolution, Shuffle On

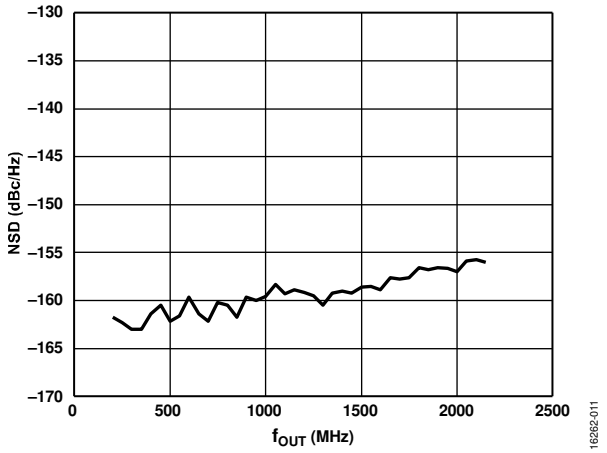

Figure 11. Single-Tone NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT}, f_{DAC} = 5.89824 GHz, 12-Bit Resolution, Shuffle On

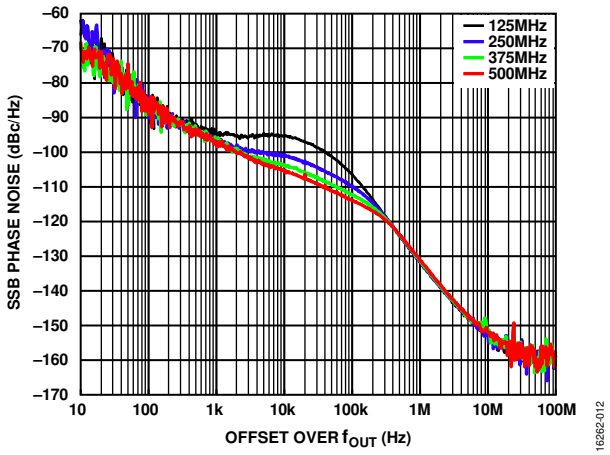

Figure 12. Single-Sideband (SSB) Phase Noise vs. Offset over f_{OUT}, over PFD Frequency, f_{DAC} = 6 GHz, f_{OUT} = 1.8 GHz, PLL On, PLL Reference Clock = PFD Frequency

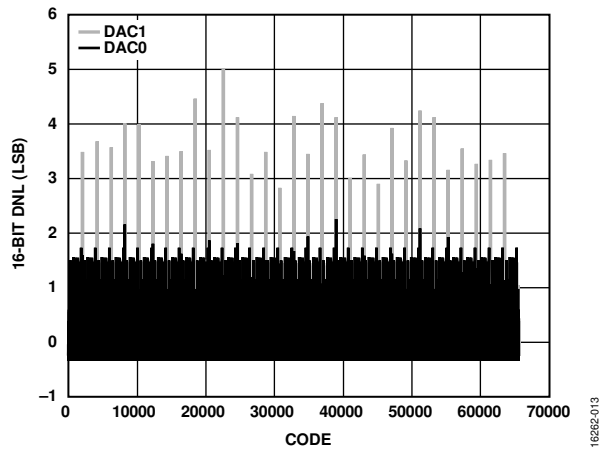

Figure 13. DNL, I_{OUTFS} = 26 mA, 16-Bit Resolution

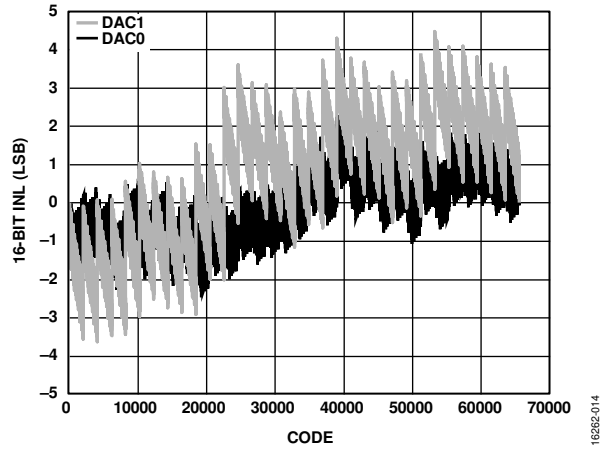

Figure 14. INL, I_{OUTFS} = 26 mA, 16-Bit Resolution

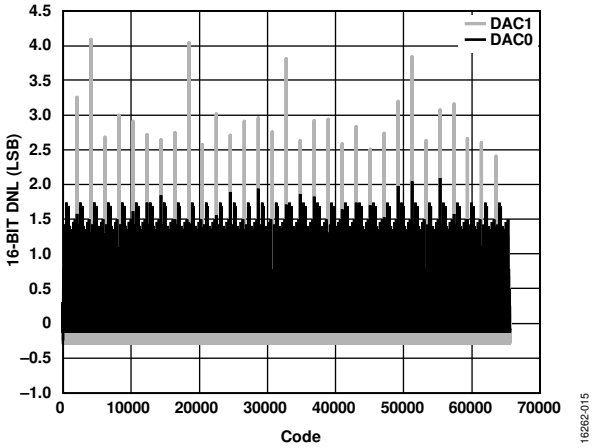

Figure 15. DNL, I_{OUTFS} = 20 mA, 16-Bit Resolution

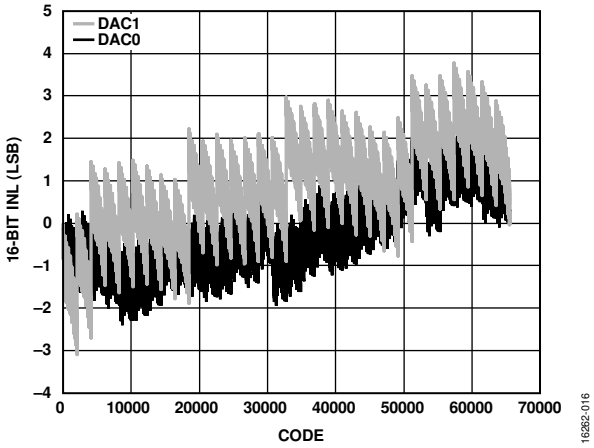

Figure 16. INL, I_{OUTFS} = 20 mA, 16-Bit Resolution

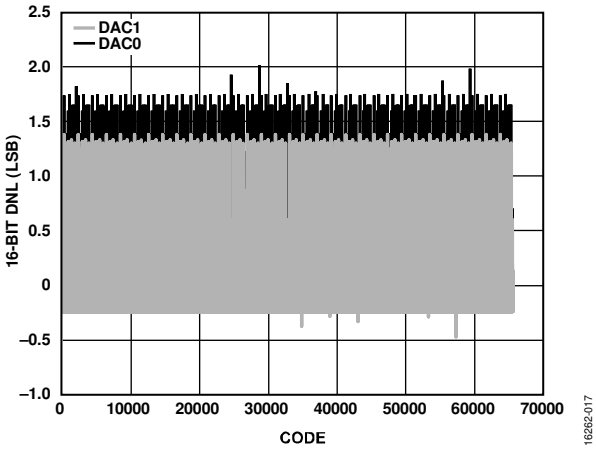

Figure 17. DNL, I_{OUTFS} = 15.6 mA, 16-Bit Resolution

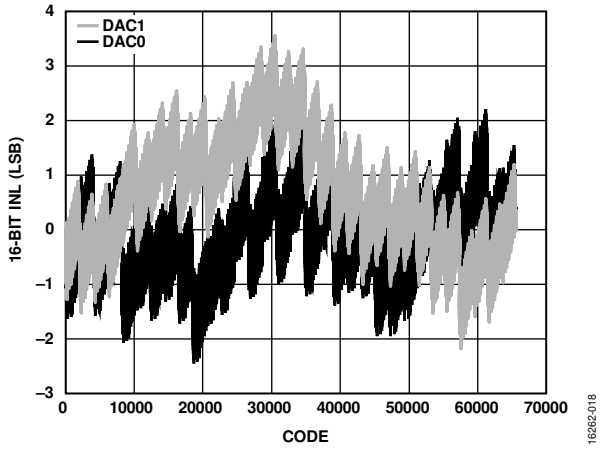

Figure 18. INL, I_{OUTFS} = 15.6 mA, 16-Bit Resolution

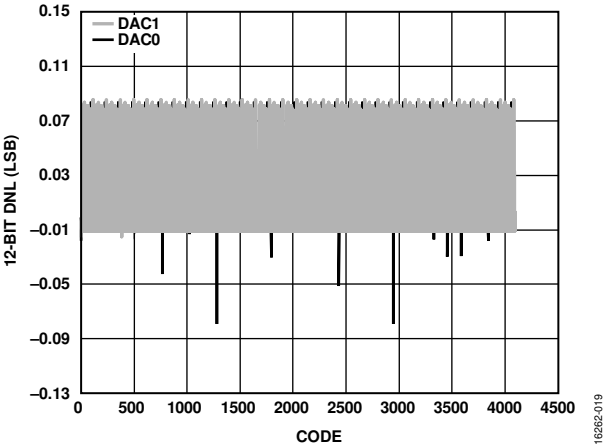

Figure 19. DNL, I_{OUTFS} = 20 mA, 12-Bit Resolution

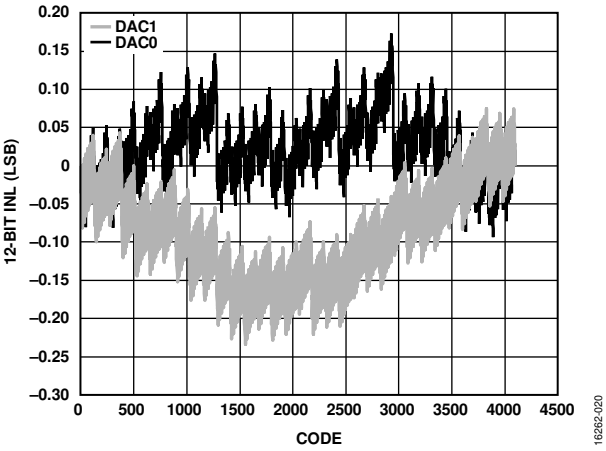

Figure 20. INL, I_{OUTFS} = 20 mA, 12-Bit Resolution

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error
Offset error is the deviation of the output current from the ideal value of 0 mA. For DACx+, a 0 mA output is expected when all inputs are set to 0. For DACx−, a 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when the input is at its minimum code and the output when the input is at its maximum code.

Output Compliance Range
The output compliance range is the range of allowable voltages at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in parts per million of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in parts per million per degrees Celsius.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of the interpolation rate (f_{DATA}), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around the output data rate (f_{DAC}) can be greatly suppressed.

Channel Datapath
The channel datapaths, sometimes referred to as channelizers, are the complex data channel datapaths, before the summing node in the chip, that can be used or bypassed depending on the mode of operation chosen. When these channelizers are in use, complex data input is required. The channel datapaths include independently controlled optional gain stages and channel NCOs per channel. There is also a selectable channel interpolation block that is configurable (same setting for all channel interpolation blocks) depending on the mode of operation chosen.

Main Datapath
The main datapath refers to the portion of the digital datapath after the summing node in the chip, up to each of the main DAC analog cores. Each of these main datapaths includes an optional PA protection block with a feed forward to the ramp up/down gain stage block for muting the DAC outputs before damaging a power amplifier in the transmit path. There is a selectable main interpolation block that is configurable (same setting for both main interpolation blocks) depending on the mode of operation chosen. Each main datapath also contains an individually programmable main NCO per main DAC datapath that can be optionally used depending on the mode of operation.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Adjusted DAC Update Rate
The adjusted DAC update rate is the DAC update rate divided by the smallest interpolating factor. For clarity on DACs with multiple interpolating factors, the adjusted DAC update rate for each interpolating factor may be given.

Physical (PHY) Lane
Physical Lane x refers to SERDINx±.

Logical Lane
Logical Lane x refers to physical lanes after optionally being remapped by the crossbar block (Register 0x308 to Register 0x30B).

Link Lane
Link Lane x refers to logical lanes considered per link. When paging Link 0 (Register 0x300, Bit 2 = 0), Link Lane x = Logical Lane x. When paging Link 1 (Register 0x300, Bit 2 = 1, dual link only), Link Lane x = Logical Lane x + 4.

THEORY OF OPERATION

The AD9171 is a 16-bit, dual RF DAC with a high speed JESD204B SERDES interface, compliant with Subclass 0 and Subclass 1 operation. Figure 1 shows a functional block diagram of the AD9171. Each DAC core has one channelizer that supports up to 516 MSPS of complex data rate input per channel. Eight high speed serial lanes carry data at a maximum of 15.4 Gbps to the channel datapaths. The JESD204B interface supports both single-link and dual-link modes of operation, depending on the selected mode configuration. Compared to either LVDS or CMOS interfaces, the SERDES interface simplifies pin count, board layout, and input clock requirements to the device.

The clock for the input data is derived from the DAC clock, or device clock (required by the JESD204B specification). This device clock can be sourced with a PLL reference clock used by the on-chip PLL to generate a DAC clock, or a high fidelity, direct external DAC sampling clock. The device can be configured to operate in one- or two-lane per link modes, depending on the required input data rate.

The digital datapath of the AD9171 offers selectable 2×, 3×, 4×, and 6× interpolation options for the channel datapaths, and 6× and 8× interpolation options for the main datapaths. See Table 13 for a summary of the various JESD204B modes available, as well as the respective interpolation options.

For each of the channel digital datapaths, there are individually programmable gain stages and NCO blocks available. The NCO blocks have a 48-bit modulus NCO option to enable digital frequency shifts of signals with near infinite precision.

The NCO can operate alone in NCO only mode using a programmable dc value input via the SPI or with digital data from the SERDES interface and digital datapath. At the end of the channelizer datapaths, the data then passes along to each of the main DAC datapaths for further digital feature options.

Each of the main DAC datapaths contain an optional power amplifier (PA) protection block, a main datapath interpolation block, a main NCO with an optional modulus feature, and a ramp-up/ramp-down gain block that is fed by the PA protection block. Additionally, there is an optional calibration tone feature, as well as four modulator switch modes that are part of the main NCO block.

The AD9171 is capable of multichip synchronization that can both synchronize multiple DACs and establish a constant and deterministic latency (latency locking) path for the DACs. The latency for each of the DACs remains constant to within several DAC clock cycles from link establishment to link establishment. An external alignment signal (SYSREF±) makes the AD9171 JESD204B Subclass 1 compliant. Several modes of SYSREF± signal handling are available for use in the system.

An SPI configures the various functional blocks and monitors their statuses. The various functional blocks and the data interface must be set up in a specific sequence for proper operation (see the Start-Up Sequence section). Simple SPI initialization routines set up the JESD204B link and are included in the evaluation board software support.

This data sheet describes the various blocks of the AD9171 in detail. Descriptions of the JESD204B interface, control parameters, and various registers to set up and monitor the device are provided. The recommended start-up routine reliably sets up the data link.

Table 12. JESD204B Supported Operating Modes and Interpolation Combinations

	JESD204B Operation Modes			Channel Datapath			Main DAC Datapath	
Application	Link Modes	JESD204B Modes	Lanes per Link	Channels per DAC	Maximum Channel Data Rate (MSPS)[1]	Channel Interpolations	Main Datapath Interpolations	Maximum DAC Rate (GSPS)
Single Channel, 375 MHz (N = 16 Bits)	Single, dual	0	1	1	385	2×	8×	6.2
						4×, 6×	6×, 8×	6.2
Single Channel, 500 MHz (N = 12 Bits, NP = 12 Bits)	Single, dual	5	1	1	513	2×	6×	6.2
						3×	6×, 8×	6.2
Single Channel, 500 MHz (N = 16 Bits)	Single, dual	3	2	1	516	2×, 3×	6×, 8×	6.2

[1] The maximum data rate is calculated based on either the maximum lane rate as listed in Table 7 or the maximum DAC rate. The data rate is calculated either using the formula lane rate = (10/8) × NP × data rate × (M/L), where the NP, M, and L values depend on the selected mode or the DAC rate is data rate × minimum channel interpolation × minimum main datapath interpolation, whichever value for the data rate is smallest.

SERIAL PORT OPERATION

The serial port is a flexible, synchronous serial communications port that allows easy interfacing with many industry-standard microcontrollers and microprocessors. The serial input/output is compatible with most synchronous transfer formats, including both the Motorola, Inc., SPI and Intel® SSR protocols. The interface allows read and write access to all registers that configure the AD9171. MSB first or LSB first transfer formats are supported. The serial port interface can be configured as a 4-wire interface or a 3-wire interface in which the input and output share a single pin input/output (SDIO).

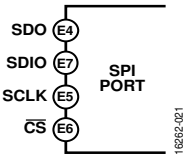

Figure 21. Serial Port Interface Pins (144-Ball BGA_ED)

There are two phases to a communication cycle with the AD9171. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first 16 SCLK rising edges. The instruction word provides the serial port controller with information regarding the data transfer cycle, Phase 2 of the communication cycle. The Phase 1 instruction word defines whether the upcoming data transfer is a read or write, along with the starting register address for the following data transfer.

A logic high on the $\overline{CS}$ pin followed by a logic low resets the serial port timing to the initial state of the instruction cycle. From this state, the next 16 rising SCLK edges represent the instruction bits of the current input/output operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one or more data bytes. Eight × N SCLK cycles are required to transfer N bytes during the transfer cycle. Registers change immediately upon writing to the last bit of each transfer byte, except for the frequency tuning word (FTW) and NCO phase offsets, which change only when the frequency tuning word load request bit (DDSM_FTW_LOAD_REQ or DDSC_FTW_LOAD_REQ) is set.

DATA FORMAT

The instruction byte contains the information shown in Table 14.

Table 13. Serial Port Instruction Word

I15 (MSB)	I[14:0]
R/$\overline{W}$	A[14:0]

R/$\overline{W}$, Bit 15 of the instruction word, determines whether a read or a write data transfer occurs after the instruction word write. Logic 1 indicates a read operation, and Logic 0 indicates a write operation.

A14 to A0, Bit I14 to Bit I0 of the instruction word, determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, A[14:0] is the starting address. The remaining register addresses are generated by the device based on the address increment bit. If the address increment bits are set high (Register 0x000, Bit 5 and Bit 2), multibyte SPI writes start on A[14:0] and increment by 1 every for eight bits sent/received. If the address increment bits are set to 0, the address decrements by 1 every eight bits.

SERIAL PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is 80 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

An active low input starts and gates a communication cycle. $\overline{CS}$ allows more than one device to be used on the same serial communication lines. The SDIO pin goes to a high impedance state when this input is high. During the communication cycle, the chip select must stay low.

Serial Data Input/Output (SDIO)

This pin is a bidirectional data line. In 4-wire mode, this pin acts as the data input and SDO acts as the data output.

SERIAL PORT OPTIONS

The serial port can support both MSB first and LSB first data formats. This functionality is controlled by the LSB first bit (Register 0x000, Bit 6 and Bit 1). The default is MSB first (LSBFIRST bit = 0).

When the LSB first bits = 0 (MSB first), the instruction and data bits must be written from MSB to LSB. R/$\overline{W}$ is followed by A[14:0] as the instruction word, and D[7:0] is the data-word. When the LSB first bits = 1 (LSB first), the opposite is true. A[0:14] is followed by R/$\overline{W}$, which is subsequently followed by D[0:7].

The serial port supports a 3-wire or 4-wire interface. When the SDO active bits = 1 (Register 0x000, Bit 4 and Bit 3), a 4-wire interface with a separate input pin (SDIO) and output pin (SDO) is used. When the SDO active bits = 0, the SDO pin is unused and the SDIO pin is used for both the input and the output.

Multibyte data transfers can be performed as well by holding the $\overline{CS}$ pin low for multiple data transfer cycles (eight SCLKs) after the first data transfer word following the instruction cycle. The first eight SCLKs following the instruction cycle read from or write to the register provided in the instruction cycle. For each additional eight SCLK cycles, the address is either incremented or decremented and the read/write occurs on the new register. The direction of the address can be set using ADDRINC or ADDRINC_M (Register 0x000, Bit 5 and Bit 2). When ADDRINC or ADDRINC_M is 1, the multicycle addresses are incremented. When ADDRINC or ADDRINC_M is 0, the addresses are decremented. A new write cycle can always be initiated by bringing $\overline{CS}$ high and then low again.

To prevent confusion and to ensure consistency between devices, the chip tests the first nibble following the address phase, ignoring the second nibble. This test is completed independently from the LSB first bits and ensures that there are extra clock cycles following the soft reset bits (Register 0x000, Bit 0 and Bit 7). This test of the first nibble only applies when writing to Register 0x000.

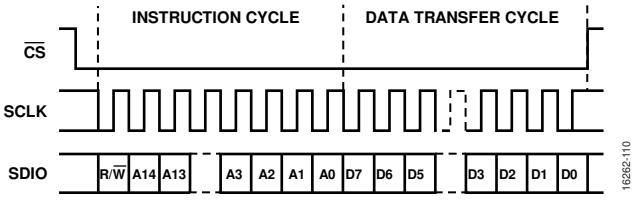

Figure 22. Serial Register Interface Timing, MSB First, Register 0x000, Bit 6 and Bit 1 = 0

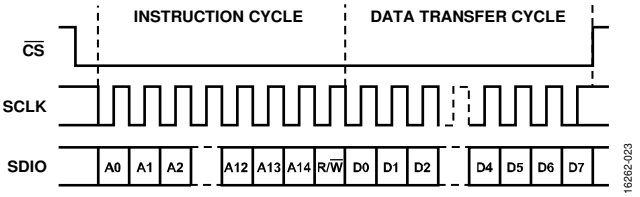

Figure 23. Serial Register Interface Timing, LSB First, Register 0x000, Bit 6 and Bit 1 = 1

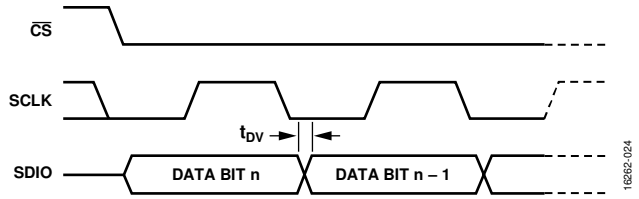

Figure 24. Timing Diagram for Serial Port Register Read

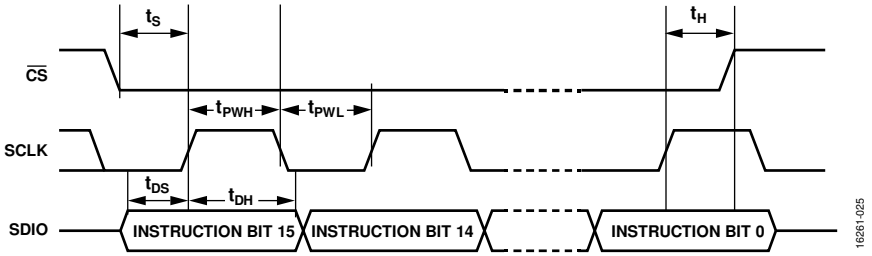

Figure 25. Timing Diagram for Serial Port Register Write

JESD204B SERIAL DATA INTERFACE

JESD204B OVERVIEW

The AD9171 has eight JESD204B data ports that receive data. The eight JESD204B ports can be configured as part of a single or dual JESD204B link that uses a single system reference (SYSREF±) and device clock (CLKIN±).

The JESD204B serial interface hardware consists of three layers: the physical layer, the data link layer, and the transport layer. These sections of the hardware are described in subsequent sections, including information for configuring every aspect of the interface. Figure 49 shows the communication layers implemented in the AD9171 serial data interface to recover the clock and deserialize, descramble, and deframe the data before it is sent to each of the digital signal processing channelizers of the device.

The physical layer establishes a reliable channel between the transmitter (Tx) and the receiver (Rx), and the data link layer is responsible for unpacking the data into octets and descrambling the data. The transport layer receives the descrambled JESD204B frames and converts them to DAC samples.

A number of JESD204B parameters (L, F, K, M, N, NP, S, HD) define how the data is packed and tell the device how to turn the serial data into samples. These parameters are defined in detail in the Transport Layer section. The AD9171 also has a descrambling option (see the Descrambler section for more information). The AD9171 has the ability to use 12-bit packing mode (NP = 12, N = 12) to increase the maximum data rate achievable by this device for applications that do not require 16-bit resolution capabilities.

The AD9171 has multiple single-link and dual-link mode options available for various application purposes. These modes and their respective JESD204B link parameters are described in Table 15 and Table 16.

There are different interpolation combinations available for the channel and main datapaths, as well as whether single-link and dual-link options are available depending on which JESD204B mode is chosen. Table 13 lists the possible link and interpolation combinations available.

The AD9171 has two DAC outputs; however, for the purposes of complex signal processing on chip, the converter count, represented by the M JESD204B parameter, reflects the number of complex subchannels of data required per link when using a total interpolation greater than 1×. The number of complex subchannels of data per link required to be sent to the device also depends on the number of channelizers being used, based on the mode of operation chosen. If the channelizer datapaths are bypassed (channel interpolation is set to 1×) and the main datapath interpolation is set to 1×, the converter count (M) reflects the number of real converters per link being used in the mode of operation; in this case, complex data is not required.

For a particular JESD204B mode of operation, the following relationships exist:

$$Total\ Interpolation = Channel\ Interpolation \times Main\ Interpolation$$

$$Data\ Rate = DAC\ Rate / Total\ Interpolation$$

$$Lane\ Rate = (M/L) \times NP \times (10/8) \times Data\ Rate$$

where:
Lane Rate must be between 3 Gbps and 15 Gbps.
M, *L*, and *NP* are JESD204B link parameters for the chosen JESD204B operating mode.

Achieving and recovering synchronization of the lanes is important. To simplify the interface to the transmitter, the AD9171 designates a master synchronization signal for each JESD204B link. The SYNCOUT0± and SYNCOUT1± pins are used as the master signal for all lanes on each link. If any lane in a link loses synchronization, a resynchronization request is sent to the transmitter via the synchronization signal of the link. The transmitter stops sending data and instead sends synchronization characters to all lanes in that link until resynchronization is achieved.

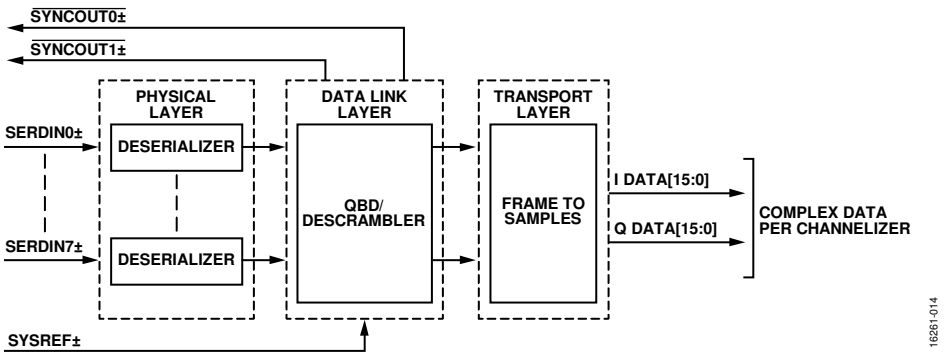

Figure 26. Functional Block Diagram of Serial Link Receiver

Table 14. Single-Link or Dual-Link JESD204B Operating Modes

	Single-Link or Dual-Link JESD204B Modes		
Parameter	**0**	**3**	**5**
Lane Count (L)	1	2	1
Converter Count (M)	2	2	2
Octets per Frame per Lane (F)	4	2	3
Samples per Converter per Frame (S)	1	1	1
Total Number of Bits per Sample (NP)	16	16	12
Converter Resolution (N)	16	16	12
Frames per Multiframe (K)	32	32	32
High Density User Data Format (HD)	1	1	1

Table 15. Data Structure per Lane for F = 2 JESD204B Operating Modes[1]

JESD204B Mode and Parameters	Link Logical Lane	Frame 0		Frame 1	
		Octet 0	**Octet 1**	**Octet 0**	**Octet 2**
Mode 3 (L = 2, M = 2, S = 1, NP = 16, N = 16)	Lane 0	M0S0[15:8]	M0S0[7:0]	M0S1[15:8]	M0S1[7:0]
	Lane 1	M1S0[15:8]	M1S0[7:0]	M1S1[15:8]	M1S1[7:0]

[1] Mx is the converter number and Sy is the sample number. For example, M0S0 means Converter 0, Sample 0.

Table 16. Data Structure per Lane for F = 3 JESD204B Operating Modes[1]

JESD204B Mode and Parameters	Link Logical Lane	Frame 0					
		Octet 0		**Octet 1**		**Octet 2**	
		Nibble 0	**Nibble1**	**Nibble 0**	**Nibble1**	**Nibble 0**	**Nibble1**
Mode 5 (L = 1, M = 2, S = 1, NP = 12, N = 12)	Lane 0	M0S0[11:8]	M0S0[7:4]	M0S0[3:0]	M1S0[11:8]	M1S0[7:4]	M1S0[3:0]

[1] Mx is the converter number and Sy is the sample number. For example, M0S0 means Converter 0, Sample 0.

Table 17. Data Structure per Lane for F = 4 JESD204B Operating Modes[1]

JESD204B Mode and Parameters	Link Logical Lane	Frame 0				Frame 1			
		Octet 0	**Octet 1**	**Octet 2**	**Octet 3**	**Octet 0**	**Octet 1**	**Octet 2**	**Octet 3**
Mode 0 (L = 1, M = 2, S = 1, NP = 16, N = 16)	Lane 0	M0S0[15:8]	M0S0[7:0]	M1S0[15:8]	M1S0[7:0]	M0S1[15:8]	M0S1[7:0]	M1S1[15:8]	M1S1[7:0]

[1] Mx is the converter number and Sy is the sample number. For example, M0S0 means Converter 0, Sample 0.

PHYSICAL LAYER

The physical layer of the JESD204B interface, hereafter referred to as the deserializer, has eight identical channels. Each channel consists of the termination, an equalizer, a clock and data recovery (CDR) circuit, and the 1:40 demux function (see Figure 50).

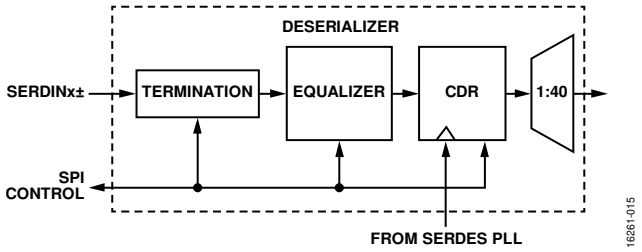

Figure 27. Deserializer Block Diagram

JESD204B data is input to the AD9171 via the SERDINx± differential input pins, per the JESD204B specification.

Interface Power-Up and Input Termination

Before using the JESD204B interface, it must be powered up by setting Register 0x200, Bit 0 = 0. In addition, each physical lane (PHY) that is not being used (SERDINx±) must be powered down. To do so, set the corresponding Bit x for Physical Lane x in Register 0x201 to 0 if the physical lane is being used, and to 1 if it is not being used.

The AD9171 autocalibrates the input termination to 50 Ω. This calibration routine is performed automatically when the JESD204B interface blocks are configured and does not require any additional SPI register writes.

Receiver Eye Mask

The AD9171 is compatible with the JESD204B specification regarding the receiver eye mask and is capable of capturing data that complies with the mask in Figure 51. Figure 51 shows the receiver eye normalized to the data rate interval. The AD9171 also supports an increased insertion loss limit, as defined in the Equalization section.

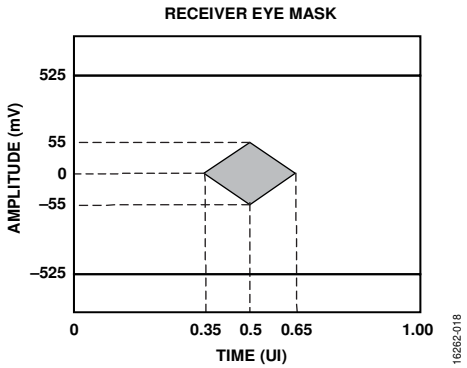

Figure 28. Receiver Eye Mask

Clock Relationships

The following clocks rates are used throughout the rest of the JESD204B section. The relationship between any of the clocks can be derived from the following equations:

$$Data\ Rate = DAC\ Rate / Total\ Interpolation$$

$$Lane\ Rate = (M/L) \times NP \times (10/8) \times Data\ Rate$$

$$Byte\ Rate = Lane\ Rate/10$$

This relationship comes from 8-bit/10-bit encoding, where each byte is represented by 10 bits.

$$PCLK\ Rate = Byte\ Rate/4$$

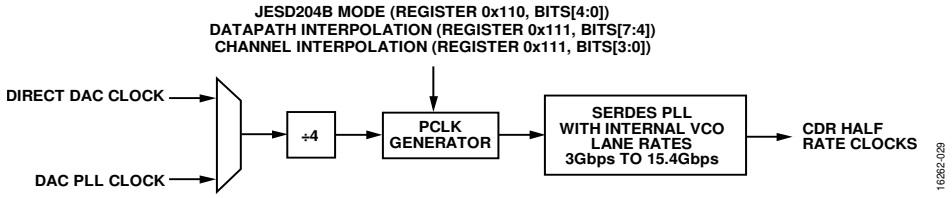

Figure 29. SERDES PLL Synthesizer Block Diagram Including VCO Divider Block

The processing clock is used for a quad-byte decoder.

Frame Rate = Byte Rate/F

where *F* is defined as octets per frame per lane.

PCLK Factor = Frame Rate/PCLK Rate = 4/F

where:
M is the JESD204B parameter for converters per link.
L is the JESD204B parameter for lanes per link.
F is the JESD204B parameter for octets per frame per lane.
NP is the JESD204B parameter for the total number of bits per sample.

SERDES PLL

Functional Overview of the SERDES PLL

The independent SERDES PLL uses integer N techniques to achieve clock synthesis. The entire SERDES PLL is integrated on chip, including the VCO and the loop filter. The SERDES PLL is capable of providing quadrature clocks to allow a wide range of data rates (3 Gbps to 15 Gbps) with no gaps.

These clocks are the input to the CDR block that is described in the Clock and Data Recovery section.

The reference clock to the SERDES PLL is always running at a frequency, f_{REF}, that is equal to 1/40 of the lane rate (PCLK rate). For more information about the SERDES circuitry setup and relevant register writes, see the Start-Up Sequence section. The SERDES PLL block automatically tunes to the appropriate divider range for the lane rate based on the SERDES mode being used. It takes the DAC clock generated by either the DAC PLL, if in use, or from the direct clock being sourced at the CLKIN± pins, divides the DAC clock frequency by 4, and uses the JESD204B parameters corresponding to the mode and interpolation values programmed in Register 0x110 and Register 0x111 to determine the proper dividers for generating the PCLK frequency (lane rate ÷ 40), as shown in Figure 52.

Confirm that the SERDES PLL is working by reading Register 0x281. If Register 0x281, Bit 0 = 1, the SERDES PLL has locked.

Clock and Data Recovery

The deserializer is equipped with a CDR circuit. Instead of recovering the clock from the JESD204B serial lanes, the CDR recovers the clocks from the SERDES PLL.

The CDR circuit synchronizes the phase used to sample the data on each serial lane independently. This independent phase adjustment per serial interface ensures accurate data sampling and eases the implementation of multiple serial interfaces on a PCB.

Power-Down Unused PHYs

Note that any unused physical and enabled lanes consume extra power unnecessarily. Each lane that is not being used (SERDINx±) must be powered off by writing a 1 to the corresponding bit of PHY_PD (Register 0x201).

Equalization

To compensate for signal integrity distortions for each PHY channel due to PCB trace length and impedance, the AD9171 employs an easy to use, low power equalizer on each JESD204B channel. The AD9171 equalizers operating at the maximum lane rate of 15 Gbps can compensate for up to 16 dB of insertion loss. This equalizer performance is shown in Figure 53 for 15 Gbps, near the maximum baud rate for the AD9171. The channel must also meet the insertion loss deviation requirement of the JESD204B specification (less than 1.5 dB from 50 MHz to 0.75 times the baud rate).

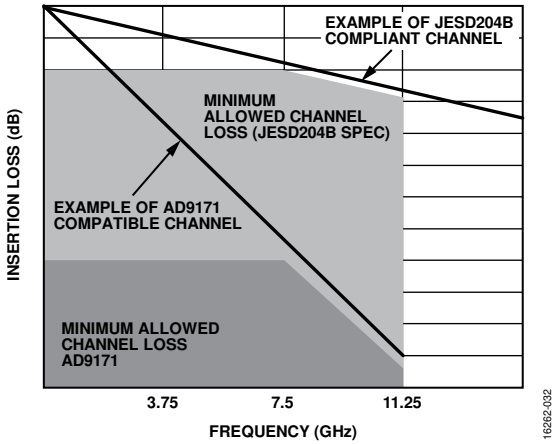

Figure 30. Insertion Loss Allowed