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# Dual, 16-Bit, 12.6 GSPS RF DAC with Channelizers

Data Sheet **AD9172**

## FEATURES

- Supports multiband wireless applications
  - 3 bypassable, complex data input channels per RF DAC
  - 1.54 GSPS maximum complex input data rate per input channel
  - 1 independent NCO per input channel
- Proprietary, low spurious and distortion design
  - 2-tone intermodulation distortion (IMD) = −83 dBc at 1.8 GHz, −7 dBFS/tone RF output
  - Spurious free dynamic range (SFDR) <−80 dBc at 1.8 GHz, −7 dBFS RF output
- Flexible 8-lane, 15.4 Gbps JESD204B interface
  - Supports single-band and multiband use cases
  - Supports 12-bit high density mode for increased data throughput
- Multiple chip synchronization
  - Supports JESD204B Subclass 1
- Selectable interpolation filter for a complete set of input data rates
  - 1×, 2×, 3×, 4×, 6×, and 8× configurable data channel interpolation
  - 1×, 2×, 4×, 6×, 8×, and 12× configurable final interpolation
- Final 48-bit NCO that operates at the DAC rate to support frequency synthesis up to 6 GHz
- Transmit enable function allows extra power saving and downstream circuitry protection
- High performance, low noise PLL clock multiplier
  - Supports 12.6 GSPS DAC update rate
  - Observation ADC clock driver with selectable divide ratios
- Low power
  - 2.55 W at 12 GSPS, dual channel mode
- 10 mm × 10 mm, 144-ball BGA_ED with metal enhanced thermal lid, 0.80 mm pitch

## APPLICATIONS

- Wireless communications infrastructure
  - Multiband base station radios
  - Microwave/E-band backhaul systems
- Instrumentation, automatic test equipment (ATE)
- Radars and jammers

## GENERAL DESCRIPTION

The AD9172 is a high performance, dual, 16-bit digital-to-analog converter (DAC) that supports DAC sample rates to 12.6 GSPS. The device features an 8-lane, 15 Gbps JESD204B data input port, a high performance, on-chip DAC clock multiplier, and digital signal processing capabilities targeted at single-band and multiband direct to radio frequency (RF) wireless applications.

The AD9172 features three complex data input channels per RF DAC that are bypassable. Each data input channel includes a configurable gain stage, an interpolation filter, and a channel numerically controlled oscillator (NCO) for flexible, multiband frequency planning. The device supports up to a 1.5 GSPS complex data rate per input channel and is capable of aggregating multiple complex input data streams up to a maximum complex data rate of 1.5 GSPS. Additionally, the AD9172 supports ultrawide bandwidth modes bypassing the channelizers to provide maximum data rates of up to 3.08 GSPS (with 16-bit resolution) and 4.1 GSPS (with 12-bit resolution).

The AD9172 is available in a 144-ball BGA_ED package.

## PRODUCT HIGHLIGHTS

1. Supports single-band and multiband wireless applications with three bypassable complex data input channels per RF DAC at a maximum complex input data rate of 1.5 GSPS. One independent NCO per input channel.
2. Ultrawide bandwidth channel bypass modes supporting up to 3 GSPS data rates with 16-bit resolution and 4 GSPS with 12-bit resolution.
3. Low power dual converter decreases the amount of power consumption needed in high bandwidth and multichannel applications.

Rev. 0 Document Feedback


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## REVISION HISTORY

**6/2017—Revision 0: Initial Version**

# FUNCTIONAL BLOCK DIAGRAM

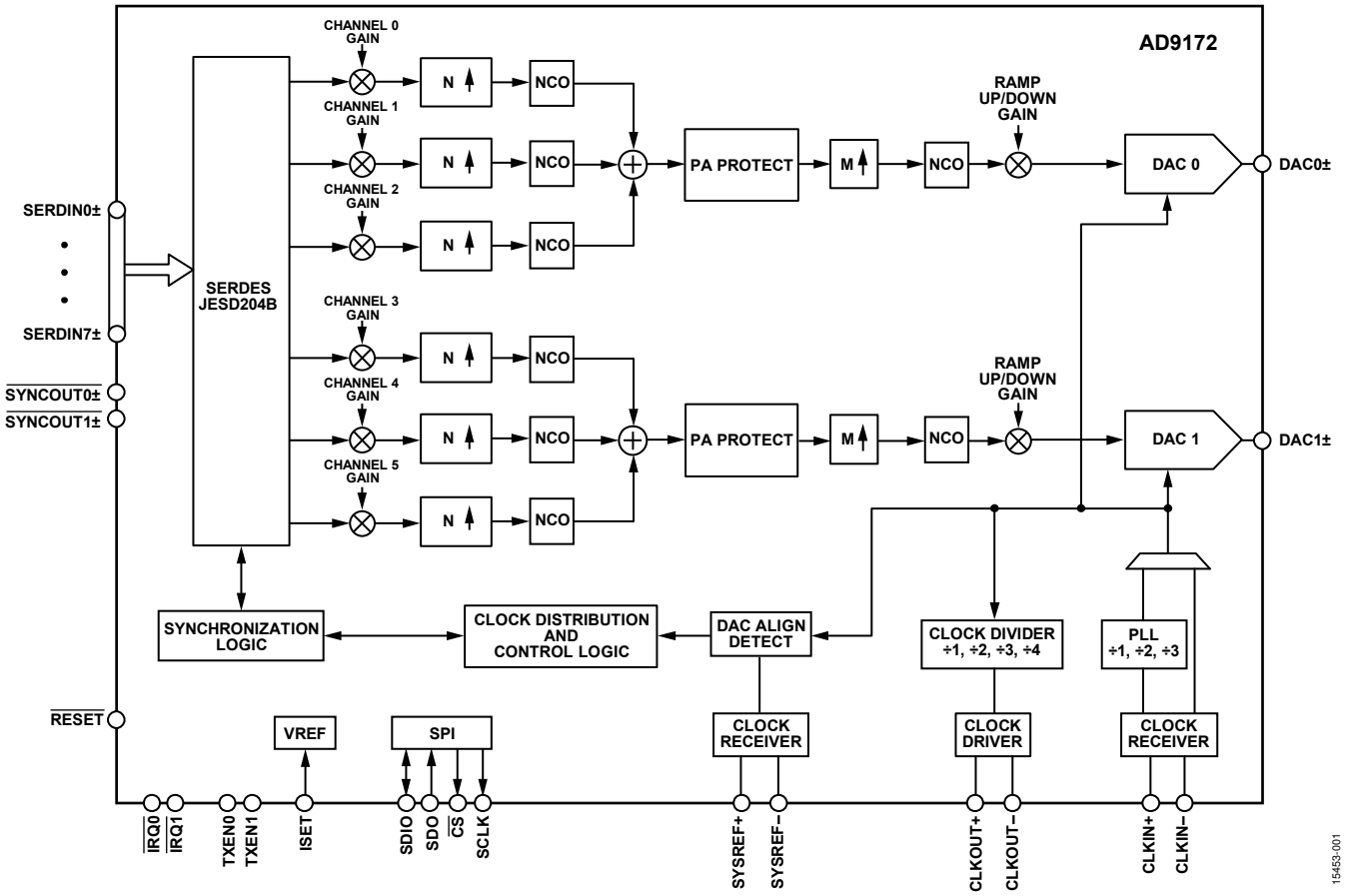


*Figure 1.*

# SPECIFICATIONS

## DC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current ($I_{OUTFS}$) = 20 mA, unless otherwise noted. For the minimum and maximum values, $T_J$ = −40°C to +118°C. For the typical values, $T_A$ = 25°C, which corresponds to $T_J$ = 51°C.

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESOLUTION | | 16 | | | Bit |
| ACCURACY | | | | | |
| Integral Nonlinearity (INL) | | | ±7 | | LSB |
| Differential Nonlinearity (DNL) | | | ±7 | | LSB |
| ANALOG OUTPUTS (DAC0+, DAC0−, DAC1+, DAC1−) | | | | | |
| Gain Error (with Internal ISET Reference) | | | ±15 | | % |
| Full-Scale Output Current | | | | | |
| Minimum | $R_{SET}$ = 5 kΩ | 14.2 | 16 | 17.8 | mA |
| Maximum | $R_{SET}$ = 5 kΩ | 23.6 | 26 | 28.8 | mA |
| Common-Mode Voltage | | | 0 | | V |
| Differential Impedance | | | 100 | | Ω |
| DAC DEVICE CLOCK INPUT (CLKIN+, CLKIN−) | | | | | |
| Differential Input Power | $R_{LOAD}$ = 100 Ω differential on-chip | | | | |
| Minimum | | | 0 | | dBm |
| Maximum | | | 6 | | dBm |
| Differential Input Impedance[1] | | | 100 | | Ω |
| Common-Mode Voltage | AC-coupled | | 0.5 | | V |
| CLOCK OUTPUT DRIVER (CLKOUT+, CLKOUT−) | | | | | |
| Differential Output Power | | | | | |
| Minimum | | | −9 | | dBm |
| Maximum | | | 0 | | dBm |
| Differential Output Impedance | | | 100 | | Ω |
| Common-Mode Voltage | AC-coupled | | 0.5 | | V |
| Output Frequency | | 727.5 | | 3000 | MHz |
| TEMPERATURE DRIFT | | | | | |
| Gain | | | 10 | | ppm/°C |
| REFERENCE | | | | | |
| Internal Reference Voltage | | | 0.495 | | V |
| ANALOG SUPPLY VOLTAGES | | | | | |
| AVDD1.0 | | 0.95 | 1.0 | 1.05 | V |
| AVDD1.8 | | 1.71 | 1.8 | 1.89 | V |
| DIGITAL SUPPLY VOLTAGES | | | | | |
| DVDD1.0 | | 0.95 | 1.0 | 1.05 | V |
| DAVDD1.0 | | 0.95 | 1.0 | 1.05 | V |
| DVDD1.8 | | 1.71 | 1.8 | 1.89 | V |
| SERIALIZER/DESERIALIZER (SERDES) SUPPLY VOLTAGES | | | | | |
| SVDD1.0 | | 0.95 | 1.0 | 1.05 | V |

[1] See the DAC Input Clock Configurations section for more details.

## DIGITAL SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current ($I_{OUTFS}$) = 20 mA, unless otherwise noted. For the minimum and maximum values, $T_J$ = −40°C to +118°C. For the typical values, $T_A$ = +25°C, which corresponds to $T_J$ = 51°C.

**Table 2.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DAC UPDATE RATE | | | | | |
| Minimum | | | | 2.91 | GSPS |
| Maximum[1] | 16-bit resolution, with interpolation | 12.6 | | | GSPS |
| | 16-bit resolution, no interpolation | 6.16 | | | GSPS |
| Adjusted[2] | 16-bit resolution, with interpolation | 1.575 | | | GSPS |
| | 16-bit resolution, no interpolation | 6.16 | | | GSPS |
| DAC PHASE-LOCKED LOOP (PLL) VOLTAGE CONTROLLED OSCILLATOR (VCO) FREQUENCY RANGES | | | | | |
| VCO Output Divide by 1 | | 8.74 | | 12.42 | GSPS |
| VCO Output Divide by 2 | | 4.37 | | 6.21 | GSPS |
| VCO Output Divide by 3 | | 2.91 | | 4.14 | GSPS |
| PHASE FREQUENCY DETECT INPUT FREQUENCY RANGES | | | | | |
| 9.96 GHz ≤ VCO Frequency ≤ 10.87 GHz | | 25 | | 225 | MHz |
| VCO Frequency < 9.96 GHz or VCO Frequency > 10.87 GHz | | 25 | | 770 | MHz |
| DAC DEVICE CLOCK INPUT (CLKIN+, CLKIN–) FREQUENCY RANGES | | | | | |
| PLL Off | | 2.91 | | 12.6 | GHz |
| PLL On | M divider set to divide by 1 | 25 | | 770 | MHz |
| | M divider set to divide by 2 | 50 | | 1540 | MHz |
| | M divider set to divide by 3 | 75 | | 2310 | MHz |
| | M divider set to divide by 4 | 100 | | 3080 | MHz |

[1] The maximum DAC update rate varies depending on the selected JESD204B mode and the lane rate for the given configuration used. The maximum DAC rate according to lane rate and voltage supply levels is listed in Table 3.
[2] The adjusted DAC update rate is calculated as $f_{DAC}$, divided by the minimum required interpolation factor for a given mode or the maximum channel data rate for a given mode. Different modes have different maximum DAC update rates, minimum interpolation factors, and maximum channel data rates, as shown in Table 13.

## MAXIMUM DAC SAMPLING RATE SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current ($I_{OUTFS}$) = 20 mA, unless otherwise noted. For the minimum and maximum values, $T_J$ = −40°C to +118°C. For the typical values, $T_A$ = 25°C, which corresponds to $T_J$ = 51°C.

**Table 3.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| MAXIMUM DAC UPDATE RATE | | | | | |
| SVDD1.0 = 1.0 V ± 5% | | | | | |
| | Lane rate > 11 Gbps | 11.67 | | | GSPS |
| | Lane rate ≤ 11 Gbps | 12.37 | | | GSPS |
| SVDD1.0 = 1.0 V ± 2.5% | | | | | |
| | Lane rate > 11 Gbps | 11.79 | | | GSPS |
| | Lane rate ≤ 11 Gbps[1] | 12.6 | | | GSPS |

[1] If using the on-chip PLL, the maximum DAC speed is limited to the maximum PLL speed of 12.42 GSPS, as listed in Table 2.

## POWER SUPPLY DC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current ($I_{OUTFS}$) = 20 mA, unless otherwise noted. For the minimum and maximum values, $T_J$ = −40°C to +118°C. For the typical values, $T_A$ = 25°C, which corresponds to $T_J$ = 51°C.

**Table 4.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DUAL-LINK MODES | | | | | |
| Mode 1 (L = 2, M = 4, NP = 16, N = 16) | 11.7965 GSPS DAC rate, 184.32 MHz PLL reference clock, 32× total interpolation (4×, 8×), 40 MHz tone at −3 dBFS, channel gain = −6 dB, channel NCOs = ±150 MHz, main NCO = 2 GHz, SYNCOUTx± in LVDS mode | | | | |
| AVDD1.0 | All supply levels set to nominal values | | 725 | 1020 | mA |
| | All supply levels set to 5% tolerance | | 775 | 1120 | mA |
| AVDD1.8 | | | 110 | 130 | mA |
| DVDD1.0 | Combined current consumption with the DAVDD1.0 supply | | | | |
| | All supply levels set to nominal values | | 1270 | 1670 | mA |
| | All supplies at 5% tolerance | | 1350 | 1850 | mA |
| DVDD1.8 | | | 35 | 50 | mA |
| SVDD1.0 | | | | | |
| | All supply levels set to nominal values | | 290 | 510 | mA |
| | All supplies at 5% tolerance | | 305 | 560 | mA |
| Total Power Dissipation | | | 2.55 | 3.38 | W |
| Mode 4 (L = 4, M = 4, NP = 16, N = 16) | 11.7965 GSPS DAC rate, 491.52 MHz PLL reference clock, 24× total interpolation (3×, 8×), 40 MHz tone at −3 dBFS, channel gain = −6 dB, channel NCOs = ±150 MHz, main NCO = 2 GHz, SYNCOUTx± in LVDS mode | | | | |
| AVDD1.0 | | | 725 | | mA |
| AVDD1.8 | | | 110 | | mA |
| DVDD1.0 | Combined current consumption with the DAVDD1.0 supply | | 1340 | | mA |
| DVDD1.8 | | | 35 | | mA |
| SVDD1.0 | | | 425 | | mA |
| Total Power Dissipation | | | 2.75 | | W |
| Mode 0 (L = 1, M = 2, NP = 16, N = 16) | 5.89824 GSPS DAC rate, 184.32 MHz PLL reference clock, 16× total interpolation (2×, 8×), 40 MHz tone at −3 dBFS, channel NCO disabled, main NCO = 1.8425 GHz, SYNCOUTx± in LVDS mode | | | | |
| AVDD1.0 | All supply levels set to nominal values | | 400 | 670 | mA |
| | All supplies at 5% tolerance | | 425 | 745 | mA |
| AVDD1.8 | | | 110 | 130 | mA |
| DVDD1.0 | Combined current consumption with the DAVDD1.0 supply | | | | |
| | All supply levels set to nominal values | | 625 | 960 | mA |
| | All supplies at 5% tolerance | | 670 | 1070 | mA |
| DVDD1.8 | | | 35 | 50 | mA |
| SVDD1.0 | | | 175 | 340 | mA |
| Total Power Dissipation | | | 1.45 | 2.15 | W |
| Mode 3 (L = 2, M = 2, NP = 16, N = 16) | 11.7965 GSPS DAC rate, 184.32 MHz PLL reference clock, 24× total interpolation (3×, 8×), 40 MHz tone at −3 dBFS, channel NCO disabled, main NCO = 2.655 GHz, SYNCOUTx± in LVDS mode | | | | |
| AVDD1.0 | All supply levels set to nominal values | | 725 | | mA |
| | All supplies at 5% tolerance | | 775 | | mA |
| AVDD1.8 | | | 110 | | mA |
| DVDD1.0 | Combined current consumption with the DAVDD1.0 supply | | | | |
| | All supply levels set to nominal values | | 1175 | | mA |
| | All supplies at 5% tolerance | | 1250 | | mA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DVDD1.8 | | | 35 | | mA |
| SVDD1.0 | All supply levels set to nominal values | | 245 | | mA |
| | All supplies at 5% tolerance | | 250 | | mA |
| Total Power Dissipation | | | 2.4 | | W |
| Mode 9 (L = 4, M = 2, NP = 16, N = 16) | 12 GSPS DAC rate, 187.5 MHz PLL reference clock, 8× total interpolation (1×, 8×), 10 MHz tone at −3 dBFS, channel NCO disabled, main NCO = 3.072 GHz, SYNCOUTx± in LVDS mode | | | | |
| AVDD1.0 | All supply levels set to nominal values | | 740 | 1030 | mA |
| | All supplies at 5% tolerance | | 785 | 1135 | mA |
| AVDD1.8 | | | 110 | 130 | mA |
| DVDD1.0 | Combined current consumption with the DAVDD1.0 supply | | | | |
| | All supply levels set to nominal values | | 1170 | 1580 | mA |
| | All supplies at 5% tolerance | | 1250 | 1740 | mA |
| DVDD1.8 | | | 35 | 50 | mA |
| SVDD1.0 | All supply levels set to nominal values | | 530 | 840 | mA |
| | All supplies at 5% tolerance | | 550 | 910 | mA |
| Total Power Dissipation | | | 2.7 | 3.63 | W |
| Mode 2 (L = 3, M = 6, NP = 16, N = 16) | 12 GSPS DAC rate, 375 MHz PLL reference clock, 48× total interpolation (6×, 8×), 30 MHz tone at −3 dBFS, channel gain = −11 dB, channel NCOs = 20 MHz, main NCO = 2.1 GHz | | | | |
| AVDD1.0 | All supply levels set to nominal values | | 735 | 1030 | mA |
| | All supplies at 5% tolerance | | 785 | 1135 | mA |
| AVDD1.8 | | | 110 | 130 | mA |
| DVDD1.0 | Combined current consumption with the DAVDD1.0 supply | | | | mA |
| | All supply levels set to nominal values | | 1370 | 1800 | mA |
| | All supplies at 5% tolerance | | 1460 | 1980 | mA |
| DVDD1.8 | | | 35 | 50 | mA |
| SVDD1.0 | All supply levels set to nominal values | | 410 | 680 | mA |
| | All supplies at 5% tolerance | | 430 | 755 | mA |
| Total Power Dissipation | | | 2.77 | 3.69 | W |
| SINGLE-LINK MODES | | | | | |
| Mode 20 (L = 8, M = 1, NP = 16, N = 16) | 6 GSPS DAC rate, 187.5 MHz PLL reference clock, 1× total interpolation (1×, 1×), 1.8 GHz tone at −3 dBFS, channel and main NCOs disabled | | | | |
| AVDD1.0 | All supply levels set to nominal values | | 400 | 670 | mA |
| | All supplies at 5% tolerance | | 430 | 745 | mA |
| AVDD1.8 | | | 75 | 100 | mA |
| DVDD1.0 | Combined current consumption with the DAVDD1.0 supply | | | | |
| | All supply levels set to nominal values | | 400 | 700 | mA |
| | All supplies at 5% tolerance | | 420 | 810 | mA |
| DVDD1.8 | | | 35 | 50 | mA |
| SVDD1.0 | All supply levels set to nominal values | | 525 | 820 | mA |
| | All supplies at 5% tolerance | | 550 | 880 | mA |
| Total Power Dissipation | | | 1.5 | 2.34 | W |
| Mode 12 (L = 8, M = 2, NP = 12, N = 12) | 4 GSPS DAC rate, 187.5 MHz PLL reference clock, 1× total interpolation (1×, 1×), 1 GHz tone at −3 dBFS, channel and main NCOs disabled | | | | |
| AVDD1.0 | All supply levels set to nominal values | | 300 | 550 | mA |
| | All supplies at 5% tolerance | | 315 | 620 | mA |
| AVDD1.8 | | | 75 | 100 | mA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DVDD1.0 | Combined current consumption with the DAVDD1.0 supply | | | | |
| | All supply levels set to nominal values | | 325 | 630 | mA |
| | All supplies at 5% tolerance | | 340 | 725 | mA |
| DVDD1.8 | | | 35 | 50 | mA |
| SVDD1.0 | All supply levels set to nominal values | | 525 | 820 | mA |
| | All supplies at 5% tolerance | | 550 | 880 | mA |
| Total Power Dissipation | | | 1.32 | 2.15 | W |
| DUAL-LINK, MODE 3 (NCO ONLY, SINGLE-CHANNEL MODE, NO SERDES) | 6 GSPS DAC rate, 300 MHz PLL reference clock, 8× total interpolation (1×, 8×), no input tone (dc internal level = 0x50FF), channel NCO = 40 MHz, main NCO = 1.8425 GHz | | | | |
| Mode 3 | | | | | |
| AVDD1.0 | | | | | |
| | All supply levels set to nominal values | | 410 | 660 | mA |
| | All supplies at 5% tolerance | | 435 | 750 | mA |
| AVDD1.8 | | | 110 | 130 | mA |
| DVDD1.0 | Combined current consumption with the DAVDD1.0 supply | | | | |
| | All supply levels set to nominal values | | 500 | 780 | mA |
| | All supplies at 5% tolerance | | 515 | 950 | mA |
| DVDD1.8 | | | 0.3 | 1 | mA |
| SVDD1.0 | All supply levels set to nominal values | | 5 | 100 | mA |
| | All supplies at 5% tolerance | | 3 | 120 | mA |
| Total Power Dissipation | | | 1.1 | 1.671 | W |
| DUAL-LINK, MODE 4 (NCO ONLY, DUAL-CHANNEL MODE, NO SERDES) | 12 GSPS DAC rate, 500 MHz PLL reference clock, 32× total interpolation (4×, 8×), no input tone (dc internal level = 0x2AFF), channel NCOs = ±150 MHz, main NCO = 2 GHz | | | | |
| Mode 4 | | | | | |
| AVDD1.0 | All supply levels set to nominal values | | 750 | 1030 | mA |
| | All supplies at 5% tolerance | | 790 | 1130 | mA |
| AVDD1.8 | | | 110 | 130 | mA |
| DVDD1.0 | Combined current consumption with the DAVDD1.0 supply | | | | |
| | All supply levels set to nominal values | | 1200 | 1590 | mA |
| | All supplies at 5% tolerance | | 1300 | 1750 | mA |
| DVDD1.8 | | | 0.3 | 1 | mA |
| SVDD1.0 | | | 5 | 100 | mA |
| Total Power Dissipation | | | 2.2 | 2.851 | W |

## SERIAL PORT AND CMOS PIN SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current ($I_{OUTFS}$) = 20 mA, unless otherwise noted. For the minimum and maximum values, $T_J$ = −40°C to +118°C. For the typical values, $T_A$ = 25°C, which corresponds to $T_J$ = 51°C.

**Table 5.**

| Parameter | Symbol | Test Comments/Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| WRITE OPERATION | | See Figure 44 | | | | |
| Maximum SCLK Clock Rate | $f_{SCLK}$, $1/t_{SCLK}$ | | 80 | | | MHz |
| SCLK Clock High | $t_{PWH}$ | SCLK = 20 MHz | 5.03 | | | ns |
| SCLK Clock Low | $t_{PWL}$ | SCLK = 20 MHz | 1.6 | | | ns |
| SDIO to SCLK Setup Time | $t_{DS}$ | | 1.154 | | | ns |
| SCLK to SDIO Hold Time | $t_{DH}$ | | 0.577 | | | ns |
| $\overline{CS}$ to SCLK Setup Time | $t_S$ | | 1.036 | | | ns |
| SCLK to $\overline{CS}$ Hold Time | $t_H$ | | −5.3 | | | ps |
| READ OPERATION | | See Figure 43 | | | | |
| SCLK Clock Rate | $f_{SCLK}$, $1/t_{SCLK}$ | | | | 48.58 | MHz |
| SCLK Clock High | $t_{PWH}$ | | 5.03 | | | ns |
| SCLK Clock Low | $t_{PWL}$ | | 1.6 | | | ns |
| SDIO to SCLK Setup Time | $t_{DS}$ | | 1.158 | | | ns |
| SCLK to SDIO Hold Time | $t_{DH}$ | | 0.537 | | | ns |
| $\overline{CS}$ to SCLK Setup Time | $t_S$ | | 1.036 | | | ns |
| SCLK to SDIO Data Valid Time | $t_{DV}$ | | 9.6 | | | ns |
| SCLK to SDO Data Valid Time | $t_{DV}$ | | 13.7 | | | ns |
| $\overline{CS}$ to SDIO Output Valid to High-Z | | Not shown in Figure 43 or Figure 44 | 5.4 | | | ns |
| $\overline{CS}$ to SDO Output Valid to High-Z | | Not shown in Figure 43 or Figure 44 | 9.59 | | | ns |
| INPUTS (SDIO, SCLK, $\overline{CS}$, $\overline{RESET}$, TXEN0, and TXEN1) | | | | | | |
| Voltage Input | | | | | | |
| High | $V_{IH}$ | | 1.48 | | | V |
| Low | $V_{IL}$ | | | | 0.425 | V |
| Current Input | | | | | | |
| High | $I_{IH}$ | | | | ±100 | nA |
| Low | $I_{IL}$ | | ±100 | | | nA |
| OUTPUTS (SDIO, SDO) | | | | | | |
| Voltage Output | | | | | | |
| High | $V_{OH}$ | | | | | |
| 0 mA load | | | 1.69 | | | V |
| 4 mA load | | | 1.52 | | | V |
| Low | $V_{OL}$ | | | | | |
| 0 mA load | | | | | 0.045 | V |
| 4 mA load | | | | | 0.175 | V |
| Current Output | | | | | | |
| High | $I_{OH}$ | | | 4 | | mA |
| Low | $I_{OL}$ | | | 4 | | mA |
| INTERRUPT OUTPUTS ($\overline{IRQ0}$, $\overline{IRQ1}$) | | | | | | |
| Voltage Output | | | | | | |
| High | $V_{OH}$ | | 1.71 | | | V |
| Low | $V_{OL}$ | | | | 0.075 | V |

## DIGITAL INPUT DATA TIMING SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current ($I_{OUTFS}$) = 20 mA, unless otherwise noted. For the minimum and maximum values, $T_J$ = −40°C to +118°C. For the typical values, $T_A$ = 25°C, which corresponds to $T_J$ = 51°C.

**Table 6.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LATENCY[1] | | | | | |
| Channel Interpolation Factor, Main Datapath Interpolation Factor | LMFC_VAR_x = 12, LMFC_DELAY_x = 12, unless otherwise noted | | | | |
| 1×, 1×[2] | JESD204B Mode 10,[3] Mode 18[3] | | 420 | | DAC clock cycle |
| | JESD204B Mode 11, Mode 19 | | 440 | | DAC clock cycle |
| | JESD204B Mode 12, Mode 19 | | 590 | | DAC clock cycle |
| | JESD204B Mode 20[3] | | 700 | | DAC clock cycle |
| | JESD204B Mode 21 | | 750 | | DAC clock cycle |
| 1×, 2×[2] | JESD204B Mode 8[3] | | 670 | | DAC clock cycle |
| | JESD204B Mode 9 | | 700 | | DAC clock cycle |
| 1×, 4×[2] | JESD204B Mode 8[3] | | 1090 | | DAC clock cycle |
| | JESD204B Mode 9 | | 1140 | | DAC clock cycle |
| 1×, 6×[2] | JESD204B Mode 8[3] | | 1460 | | DAC clock cycle |
| | JESD204B Mode 9 | | 1530 | | DAC clock cycle |
| 1×, 8×[2] | JESD204B Mode 3 | | 1390 | | DAC clock cycle |
| | JESD204B Mode 8[3] | | 1820 | | DAC clock cycle |
| | JESD204B Mode 9 | | 1920 | | DAC clock cycle |
| 1×, 12×[2] | JESD204B Mode 8[3] | | 2700 | | DAC clock cycle |
| | JESD204B Mode 9 | | 2840 | | DAC clock cycle |
| 2×, 6×[2] | JESD204B Mode 3, Mode 4 | | 1970 | | DAC clock cycle |
| | JESD204B Mode 5 | | 1770 | | DAC clock cycle |
| 2×, 8×[2] | JESD204B Mode 0 | | 2020 | | DAC clock cycle |
| | JESD204B Mode 3, Mode 4 | | 2500 | | DAC clock cycle |
| 3×, 6×[2] | JESD204B Mode 3, Mode 4 | | 2880 | | DAC clock cycle |
| | JESD204B Mode 5, Mode 6 | | 2630 | | DAC clock cycle |
| 3×, 8×[2] | JESD204B Mode 3, Mode 4 | | 3310 | | DAC clock cycle |
| | JESD204B Mode 5, Mode 6 | | 2980 | | DAC clock cycle |
| 4×, 6×[2] | JESD204B Mode 0, Mode 1, Mode 2 | | 2410 | | DAC clock cycle |
| 4×, 8×[2] | JESD204B Mode 0, Mode 1, Mode 2 | | 3090 | | DAC clock cycle |
| 6×, 6×[2] | JESD204B Mode 0, Mode 1, Mode 2 | | 3190 | | DAC clock cycle |
| 6×, 8×[2] | JESD204B Mode 0, Mode 1, Mode 2 | | 4130 | | DAC clock cycle |
| 8×, 6×[2] | JESD204B Mode 7 | | 3300 | | DAC clock cycle |
| 8×, 8×[2] | JESD204B Mode 7 | | 4270 | | DAC clock cycle |
| DETERMINISTIC LATENCY | | | | | |
| Fixed | | | | 13 | PCLK[4] |
| Variable | | | | 2 | PCLK cycles |
| SYSREF± TO LMFC DELAY | | | 0 | | DAC clock cycles |

[1] Total latency (or pipeline delay) through the device is calculated as follows: total latency = interface latency + fixed latency + variable latency + pipeline delay.
[2] The first value listed in this specification is the channel interpolation factor, and the second value is the main datapath interpolation factor.
[3] LMFC_VAR_x = 7 and LMFC_DELAY_x = 4
[4] PCLK is the internal processing clock for the AD9172 and equals the lane rate ÷ 40.

## JESD204B INTERFACE ELECTRICAL AND SPEED SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current ($I_{OUTFS}$) = 20 mA, unless otherwise noted. For the minimum and maximum values, $T_J$ = −40°C to +118°C. For the typical values, $T_A$ = 25°C, which corresponds to $T_J$ = 51°C.

**Table 7.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| JESD204B SERIAL INTERFACE RATE (SERIAL LANE RATE) | | | 3 | | 15.4 | Gbps |
| JESD204B DATA INPUTS | | | | | | |
| Input Leakage Current | | $T_A$ = 25°C | | | | |
| Logic High | | Input level = 1.0 V ± 0.25 V | | 10 | | µA |
| Logic Low | | Input level = 0 V | | −4 | | µA |
| Unit Interval | UI | | 333 | | 66.7 | ps |
| Common-Mode Voltage | $V_{RCM}$ | AC-coupled | −0.05 | | +1.1 | V |
| Differential Voltage | $R\_V_{DIFF}$ | | 110 | | 1050 | mV |
| Differential Impedance | $Z_{RDIFF}$ | At dc | 80 | 100 | 120 | Ω |
| SYSREF± INPUT | | | | | | |
| Differential Impedance | | | | 100 | | Ω |
| DIFFERENTIAL OUTPUTS ($\overline{SYNCOUT0}$±, $\overline{SYNCOUT1}$±)[1] | | Driving 100 Ω differential load | | | | |
| Output Differential Voltage | $V_{OD}$ | | 320 | 390 | 460 | mV |
| Output Offset Voltage | $V_{OS}$ | | 1.08 | 1.12 | 1.15 | V |
| SINGLE-ENDED OUTPUTS ($\overline{SYNCOUT0}$±, $\overline{SYNCOUT1}$±) | | Driving 100 Ω differential load | | | | |
| Output Voltage | | | | | | |
| High | $V_{OH}$ | | 1.69 | | | V |
| Low | $V_{OL}$ | | | | 0.045 | V |
| Current Output | | | | | | |
| High | $I_{OH}$ | | | 0 | | mA |
| Low | $I_{OL}$ | | | 0 | | mA |

[1] IEEE Standard 1596.3 LVDS compatible.

## INPUT DATA RATES AND SIGNAL BANDWIDTH SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current ($I_{OUTFS}$) = 20 mA, unless otherwise noted. For the minimum and maximum values, $T_J$ = −40°C to +118°C. For the typical values, $T_A$ = 25°C, which corresponds to $T_J$ = 51°C.

**Table 8.**

| Parameter[1] | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| INPUT DATA RATE PER INPUT CHANNEL | | | | | |
| | Channel datapaths bypassed (1× interpolation), single-DAC mode, 16-bit resolution | | | 6160 | MSPS |
| | Channel datapaths bypassed (1× interpolation), dual DAC mode, 16-bit resolution | | | 3080 | MSPS |
| | Channel datapaths bypassed (1× interpolation), dual DAC mode, 12-bit resolution | | | 4100 | MSPS |
| | 1 complex channel enabled | | | 1540 | MSPS |
| | 2 complex channels enabled | | | 770 | MSPS |
| | 3 complex channels enabled | | | 385 | MSPS |
| COMPLEX SIGNAL BANDWIDTH PER INPUT CHANNEL | | | | | |
| | 1 complex channel enabled (0.8 × $f_{DATA}$) | | | 1232 | MHz |
| | 2 complex channels enabled (0.8 × $f_{DATA}$) | | | 616 | MHz |
| | 3 complex channels enabled (0.8 × $f_{DATA}$) | | | 308 | MHz |
| MAXIMUM NCO CLOCK RATE | | | | | |
| Channel NCO | | | | 1540 | MHz |
| Main NCO | | | | 12.6 | GHz |
| MAXIMUM NCO SHIFT FREQUENCY RANGE | | | | | |
| Channel NCO | Channel summing node = 1.575 GHz, channel interpolation rate > 1× | −770 | | +770 | MHz |
| Main NCO | $f_{DAC}$ = 12.6 GHz, main interpolation rate > 1× | −6.3 | | +6.3 | GHz |
| MAXIMUM FREQUENCY SPACING ACROSS INPUT CHANNELS | Maximum NCO output frequency × 0.8 | | | 1232 | MHz |

[1] Values listed for these parameters are the maximum possible when considering all JESD204B modes of operation. Some modes are more limiting, based on other parameters.

## AC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current ($I_{OUTFS}$) = 20 mA, unless otherwise noted. For the minimum and maximum, $T_J$ = −40°C to +118°C. For the typical values, $T_A$ = 25°C, which corresponds to $T_J$ = 51°C.

**Table 9.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SPURIOUS-FREE DYNAMIC RANGE (SFDR) | | | | | |
| Single Tone, $f_{DAC}$ = 12000 MSPS, Mode 1 (L = 2, M = 4) | −7 dBFS, shuffle enabled | | | | |
| $f_{OUT}$ = 100 MHz | | | −81 | | dBc |
| $f_{OUT}$ = 500 MHz | | | −80 | | dBc |
| $f_{OUT}$ = 950 MHz | | | −75 | | dBc |
| $f_{OUT}$ = 1840 MHz | | | −80 | | dBc |
| $f_{OUT}$ = 2650 MHz | | | −75 | | dBc |
| $f_{OUT}$ = 3700 MHz | | | −67 | | dBc |
| Single Tone, $f_{DAC}$ = 6000 MSPS, Mode 0 (L = 1, M = 2) | −7 dBFS, shuffle enabled | | | | |
| $f_{OUT}$ = 100 MHz | | | −85 | | dBc |
| $f_{OUT}$ = 500 MHz | | | −85 | | dBc |
| $f_{OUT}$ = 950 MHz | | | −78 | | dBc |
| $f_{OUT}$ = 1840 MHz | | | −75 | | dBc |
| $f_{OUT}$ = 2650 MHz | | | −69 | | dBc |
| Single Tone, $f_{DAC}$ = 3000 MSPS, Mode 10 (L = 8, M = 2) | −7 dBFS, shuffle enabled | | | | |
| $f_{OUT}$ = 100 MHz | | | −87 | | dBc |
| $f_{OUT}$ = 500 MHz | | | −84 | | dBc |
| $f_{OUT}$ = 950 MHz | | | −81 | | dBc |
| Single-Band Application—Band 3 (1805 MHz to 1880 MHz) | Mode 0, 2× to 8×, $f_{DAC}$ = 6000 MSPS, 368.64 MHz reference clock | | | | |
| SFDR Harmonics | −7 dBFS, shuffle enabled | | | | |
| In-Band | | | −82 | | dBc |
| Digital Predistortion (DPD) Band | DPD bandwidth = data rate × 0.8 | | −80 | | dBc |
| Second Harmonic | | | −82 | | dBc |
| Third Harmonic | | | −80 | | dBc |
| Fourth and Fifth Harmonic | | | −95 | | dBc |
| SFDR Nonharmonics | −7 dBFS, shuffle enabled | | | | |
| In-Band | | | −74 | | dBc |
| DPD Band | | | −74 | | dBc |
| ADJACENT CHANNEL LEAKAGE RATIO | | | | | |
| 4C-WCDMA | −1 dBFS digital backoff | | | | |
| $f_{DAC}$ = 1200 MSPS, Mode 1 (L = 2, M = 4) | $f_{OUT}$ = 1840 MHz | | −70 | | dBc |
| | $f_{OUT}$ = 2650 MHz | | −68 | | dBc |
| | $f_{OUT}$ = 3500 MHz | | −66 | | dBc |
| $f_{DAC}$ = 6000 MSPS, Mode 0 (L = 1, M = 2) | $f_{OUT}$ = 1840 MHz | | −71 | | dBc |
| | $f_{OUT}$ = 2650 MHz | | −66 | | dBc |
| THIRD-ORDER INTERMODULATION DISTORTION | Two-tone test, −7 dBFS/tone, 1 MHz spacing | | | | |
| $f_{DAC}$ = 12000 MSPS, Mode 1 (L = 2, M = 4) | $f_{OUT}$ = 1840 MHz | | −83 | | dBc |
| | $f_{OUT}$ = 2650 MHz | | −85 | | dBc |
| | $f_{OUT}$ = 3700 MHz | | −77 | | dBc |
| $f_{DAC}$ = 6000 MSPS, Mode 0 (L = 1, M = 2) | $f_{OUT}$ = 1840 MHz | | −74 | | dBc |
| | $f_{OUT}$ = 2650 MHz | | −72 | | dBc |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| NOISE SPECTRAL DENSITY (NSD) | 0 dBFS, NSD measurement taken at 10% away from $f_{OUT}$, shuffle off | | | | |
| Single Tone, $f_{DAC}$ = 12000 MSPS, Mode 1 (L = 2, M = 4) | | | | | |
| $f_{OUT}$ = 100 MHz | | | −169 | | dBm/Hz |
| $f_{OUT}$ = 500 MHz | | | −168 | | dBm/Hz |
| $f_{OUT}$ = 950 MHz | | | −166 | | dBm/Hz |
| $f_{OUT}$ = 1840 MHz | | | −165 | | dBm/Hz |
| $f_{OUT}$ = 2150 MHz | | | −164 | | dBm/Hz |
| Single Tone, $f_{DAC}$ = 6000 MSPS, Mode 3 (L = 2, M = 2) | | | | | |
| $f_{OUT}$ = 100 MHz | | | −169 | | dBm/Hz |
| $f_{OUT}$ = 500 MHz | | | −167 | | dBm/Hz |
| $f_{OUT}$ = 950 MHz | | | −166 | | dBm/Hz |
| $f_{OUT}$ = 1840 MHz | | | −163 | | dBm/Hz |
| $f_{OUT}$ = 2150 MHz | | | −162 | | dBm/Hz |
| Single Tone, $f_{DAC}$ = 3000 MSPS, Mode 10 (L = 8, M = 2) | | | | | |
| $f_{OUT}$ = 100 MHz | | | −166 | | dBm/Hz |
| $f_{OUT}$ = 500 MHz | | | −163 | | dBm/Hz |
| $f_{OUT}$ = 950 MHz | | | −160 | | dBm/Hz |
| SINGLE-SIDEBAND PHASE NOISE OFFSET | Loop filter component values according to Figure 85 are as follows: C1 = 22 nF, R1 = 232 Ω, C2 = 2.4 nF, C3 = 33 nF; PFD frequency = 500 MHz, $f_{OUT}$ = 1.8 GHz, $f_{DAC}$ = 12 GHz | | | | |
| 1 kHz | | | −97 | | dBc/Hz |
| 10 kHz | | | −105 | | dBc/Hz |
| 100 kHz | | | −114 | | dBc/Hz |
| 600 kHz | | | −126 | | dBc/Hz |
| 1.2 MHz | | | −133 | | dBc/Hz |
| 1.8 MHz | | | −137 | | dBc/Hz |
| 6 MHz | | | −148 | | dBc/Hz |
| DAC TO DAC OUTPUT ISOLATION | Taken using the AD9172-FMC-EBZ evaluation board | | | | |
| Dual Band—$f_{DAC}$ = 12000 MSPS, Mode 1 (L = 2, M = 4) | | | | | |
| | $f_{OUT}$ = 1840 MHz | | −77 | | dB |
| | $f_{OUT}$ = 2650 MHz | | −70 | | dB |
| | $f_{OUT}$ = 3700 MHz | | −68 | | dB |

# ABSOLUTE MAXIMUM RATINGS

**Table 10.**

| Parameter | Rating |
|---|---|
| ISET, FILT_COARSE, FILT_BYP, FILT_VCM | −0.3 V to AVDD1.8 + 0.3 V |
| SERDINx± | −0.2 V to SVDD1.0 + 0.2 V |
| SYNCOUT0±, SYNCOUT1±, RESET, TXEN0, TXEN1, IRQ0, IRQ1, CS, SCLK, SDIO, SDO | −0.3 V to DVDD1.8 + 0.3 V |
| DAC0±, DAC1±, CLKIN±, CLKOUT±, FILT_FINE | −0.2 V to AVDD1.0 + 0.2 V |
| SYSREF± | −0.2 V to DVDD1.0 + 0.2 V |
| AVDD1.0, DVDD1.0, SVDD1.0 to GND | −0.2 V to +1.2 V |
| AVDD1.8, DVDD1.8 to GND | −0.3 V to 2.2 V |
| Maximum Junction Temperature ($T_J$)[1] | 118°C |
| Storage Temperature Range | −65°C to +150°C |
| Reflow | 260°C |

[1] Some operating modes of the device may cause the device to approach or exceed the maximum junction temperature during operation at supported ambient temperatures. Removal of heat from the device may require additional measures such as active airflow, heat sinks, or other measures.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## REFLOW PROFILE

The AD9172 reflow profile is in accordance with the JEDEC JESD20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

## THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$ is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. $\theta_{JC}$ is the junction to case thermal resistance.

Thermal resistances and thermal characterization parameters are specified vs. the number of PCB layers in different airflow velocities (in m/sec). The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 10.

Use the values in Table 11 in compliance with JEDEC 51-12.

**Table 11. Simulated Thermal Resistance vs. PCB Layers[1]**

| PCB Type | Airflow Velocity (m/sec) | $\theta_{JA}$ | $\theta_{JC\_TOP}$ | $\theta_{JC\_BOT}$ | Unit |
|---|---|---|---|---|---|
| JEDEC 2s2p Board | 0.0 | 25.3 | 2.4[3] | 3.0[4] | °C/W |
| | 1.0 | 22.6 | N/A | N/A | °C/W |
| | 2.5 | 21.0 | N/A | N/A | °C/W |
| 12-Layer PCB[2] | 0.0 | 15.4 | 2.4 | 2.6 | °C/W |
| | 1.0 | 13.1 | N/A | N/A | °C/W |
| | 2.5 | 11.6 | N/A | N/A | °C/W |

[1] N/A means not applicable.
[2] Non JEDEC thermal resistance.
[3] 1SOP PCB with no vias in PCB.
[4] 1SOP PCB with 7 × 7 standard JEDEC vias.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS


*Figure 2. Pin Configuration*

**Table 12. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1.0 V Supply | | |
| H3, H4, H5, H8 to H10, J6, M2, M11 | AVDD1.0 | 1.0 V Clock and Analog Supplies. These pins supply the clock receivers, clock distribution, the on-chip DAC clock multiplier, and the DAC analog core. Clean power supply rail sources are required on these pins. |
| F5 to F8 | DVDD1.0 | 1.0 V Digital Supplies. These pins supply power to the DAC digital circuitry. Clean power supply rail sources are required on these pins. |
| F4, F9 | DAVDD1.0 | 1.0 V Digital to Analog Supplies. These pins can share a supply rail with the DVDD1.0 supply (electrically connected) but must have separate supply plane and decoupling capacitors for the PCB layout to improve isolation for these two pins. Clean power supply rail sources are required on these pins. |
| C1, C2, C5, C7, C8, C11, C12, D6 | SVDD1.0 | 1.0 V SERDES Supplies to the JESD204B Data Interface. Clean power supply rail sources are required on these pins. |
| 1.8 V Supply | | |
| K3, K5, K7, K10, L3, L6, L7, L10 | AVDD1.8 | 1.8 V Analog Supplies to the On-Chip DAC Clock Multiplier and the DAC Analog Core. Clean power supply rail sources are required on these pins. |
| C6, D3, D10, E3, E10 | DVDD1.8 | 1.8 V Digital Supplies to the JESD204B Data Interface and the Other Input/Output Circuitry, Such as the Serial Port Interface (SPI). Clean power supply rail sources are required on these pins. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| Ground | | |
| A1, A6, A7, A12, B1, B6, B7, B12, C3, C4, C9, C10, D5, D7, F1 to F3, F10 to F12, G1 to G12, H11, J1, J3 to J5, J8 to J11, K2, K8, K9, K11, K12, L2, L4, L5, L8, L9, L11, M1, M3, M6, M7, M10, M12 | GND | Device Common Ground. |
| RF Clock | | |
| J12 | CLKIN+ | Positive Device Clock Input. This pin is the clock input for the on-chip DAC clock multiplier, REFCLK, when the DAC PLL is on. This pin is also the clock input for the DAC sample clock or device clock (DACCLK) when the DAC PLL is off. AC couple this input. There is an internal 100 Ω resistor between this pin and CLKIN−. |
| H12 | CLKIN− | Negative Device Clock Input. |
| K1 | CLKOUT+ | Positive Device Clock Output. This pin is the clock output of a divided down DACCLK and is available with the DAC PLL on and off. The divide down ratios are by 1, 2, or 4. |
| L1 | CLKOUT− | Negative Device Clock Output. |
| System Reference | | |
| H1 | SYSREF+ | Positive System Reference Input. It is recommended to ac couple this pin, but dc coupling is also acceptable. See the SYSREF± specifications for the dc common-mode voltage. |
| H2 | SYSREF− | Negative System Reference Input. It is recommended to ac couple this pin, but dc coupling is also acceptable. See the SYSREF± specifications for the dc common-mode voltage. |
| On-Chip DAC PLL Loop Filter | | |
| H6 | FILT_FINE | On-Chip DAC Clock Multiplier and PLL Fine Loop Filter Input. |
| H7 | FILT_COARSE | On-Chip DAC Clock Multiplier and PLL Coarse Loop Filter Input. |
| J7 | FILT_BYP | On-Chip DAC Clock Multiplier and LDO Bypass. |
| K6 | FILT_VCM | On-Chip DAC Clock Multiplier and VCO Common-Mode Input. |
| SERDES Data Bits | | |
| A2 | SERDIN7+ | SERDES Data Bit 7, Positive. |
| B2 | SERDIN7− | SERDES Data Bit 7, Negative. |
| A3 | SERDIN6+ | SERDES Data Bit 6, Positive. |
| B3 | SERDIN6− | SERDES Data Bit 6, Negative. |
| A4 | SERDIN5+ | SERDES Data Bit 5, Positive. |
| B4 | SERDIN5− | SERDES Data Bit 5, Negative. |
| A5 | SERDIN4+ | SERDES Data Bit 4, Positive. |
| B5 | SERDIN4− | SERDES Data Bit 4, Negative. |
| A8 | SERDIN3+ | SERDES Data Bit 3, Positive. |
| B8 | SERDIN3− | SERDES Data Bit 3, Negative. |
| A9 | SERDIN2+ | SERDES Data Bit 2, Positive. |
| B9 | SERDIN2− | SERDES Data Bit 2, Negative. |
| A10 | SERDIN1+ | SERDES Data Bit 1, Positive. |
| B10 | SERDIN1− | SERDES Data Bit 1, Negative. |
| A11 | SERDIN0+ | SERDES Data Bit 0, Positive. |
| B11 | SERDIN0− | SERDES Data Bit 0, Negative. |
| Sync Output | | |
| D12 | $\overline{\text{SYNCOUT0+}}$ | Positive Sync (Active Low) Output Signal, Channel Link 0. This pin is LVDS or CMOS selectable. |
| D11 | $\overline{\text{SYNCOUT0−}}$ | Negative Sync (Active Low) Output Signal, Channel Link 0. This pin is LVDS or CMOS selectable. |
| D1 | $\overline{\text{SYNCOUT1+}}$ | Positive Sync (Active Low) Output Signal, Channel Link 1. This pin is LVDS or CMOS selectable. |
| D2 | $\overline{\text{SYNCOUT1−}}$ | Negative Sync (Active Low) Output Signal, Channel Link 1. This pin is LVDS or CMOS selectable. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| Serial Port Interface | | |
| E4 | SDO | Serial Port Data Output (CMOS Levels with Respect to DVDD1.8). |
| E7 | SDIO | Serial Port Data Input/Output (CMOS Levels with Respect to DVDD1.8). |
| E5 | SCLK | Serial Port Clock Input (CMOS Levels with Respect to DVDD1.8). |
| E6 | $\overline{CS}$ | Serial Port Chip Select, Active Low (CMOS Levels with Respect to DVDD1.8). |
| E8 | $\overline{RESET}$ | Reset, Active Low (CMOS Levels with Respect to DVDD1.8). |
| Interrupt Request | | |
| D9 | $\overline{IRQ0}$ | Interrupt Request 0. This pin is an open-drain, active low output (CMOS levels with respect to DVDD1.8). Connect a pull-up resistor to DVDD1.8 to prevent this pin from floating when inactive. |
| E9 | $\overline{IRQ1}$ | Interrupt Request 1. This pin is an open-drain, active low output (CMOS levels with respect to DVDD1.8). Connect a pull-up resistor to DVDD1.8 to prevent this pin from floating when inactive. |
| CMOS Input/Outputs | | |
| D8 | TXEN0 | Transmit Enable for DAC0. The CMOS levels are determined with respect to DVDD1.8. |
| D4 | TXEN1 | Transmit Enable for DAC1. The CMOS levels are determined with respect to DVDD1.8. |
| DAC Analog Outputs | | |
| M9 | DAC0+ | DAC0 Positive Current Output. |
| M8 | DAC0− | DAC0 Negative Current Output. |
| M4 | DAC1+ | DAC1 Positive Current Output. |
| M5 | DAC1− | DAC1 Negative Current Output. |
| Reference | | |
| L12 | ISET | Device Bias Current Setting Pin. Connect a 5 kΩ resistor, preferably with 0.1% tolerance and ±25 ppm/°C. |
| Do Not Connect | | |
| E1, E2, E11, E12, J2, K4 | DNC | Do Not Connect. Do not connect to these pins. |

# TYPICAL PERFORMANCE CHARACTERISTICS

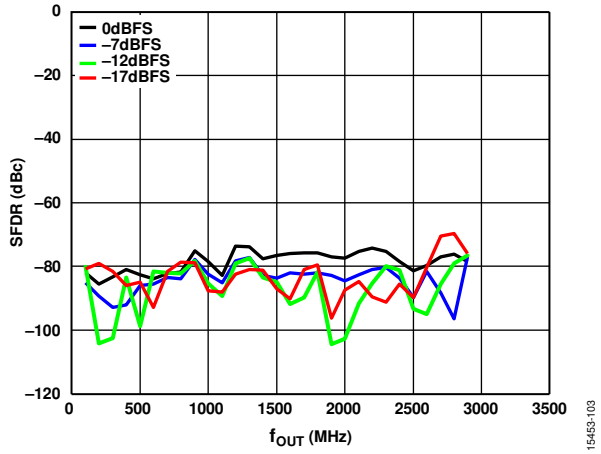


Figure 3. Second Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×

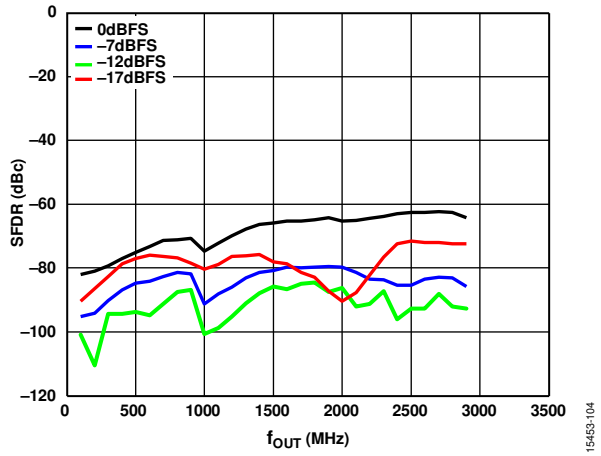


Figure 4. Third Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×

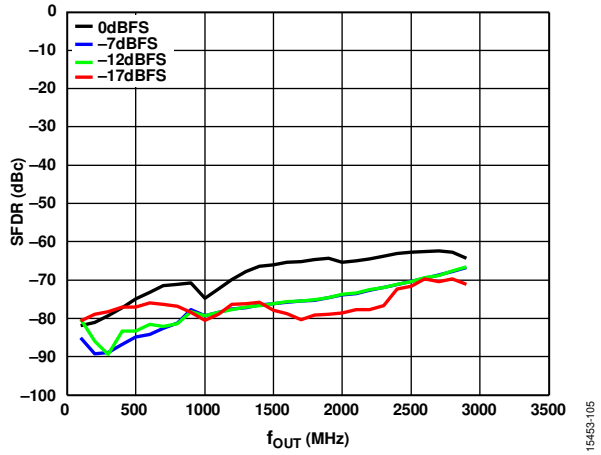


Figure 5. Worst Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×

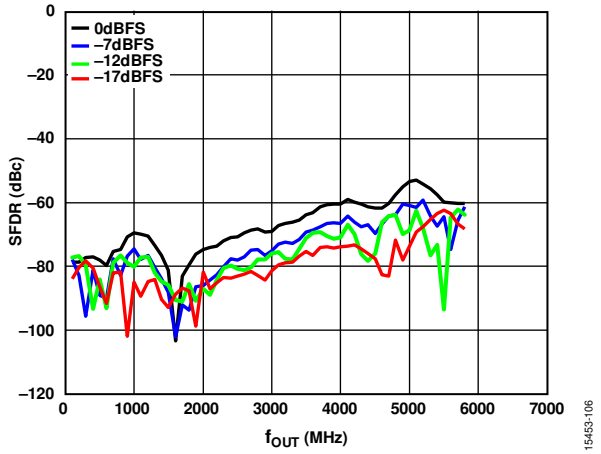


Figure 6. Second Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 1), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

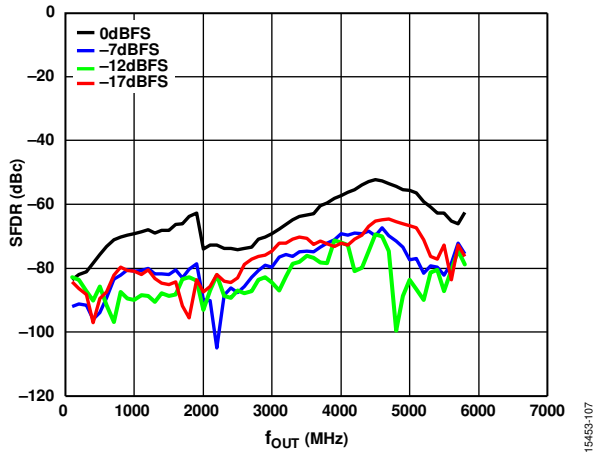


Figure 7. Third Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 1), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

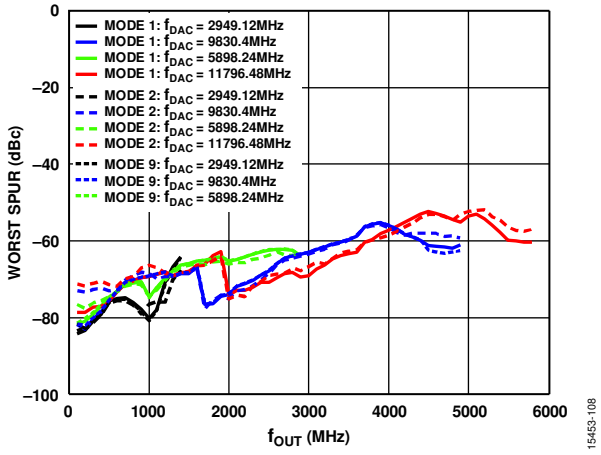


Figure 8. Worst Spur vs. $f_{OUT}$ over $f_{DAC}$ (All Modes), 0 dB Digital Scale

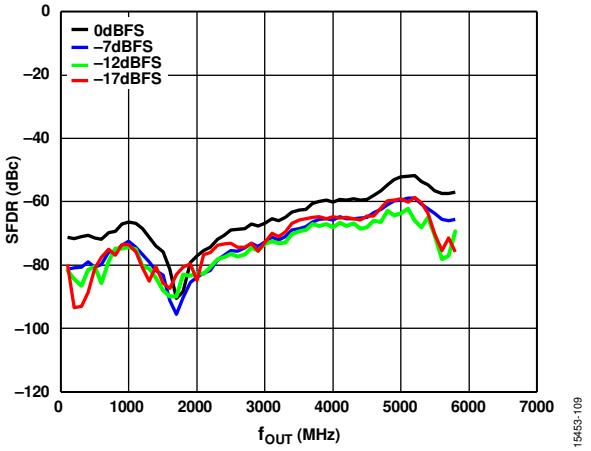


Figure 9. Second Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

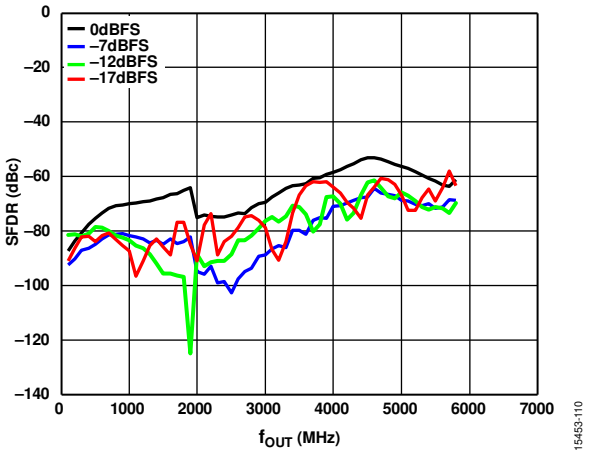


Figure 10. Third Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

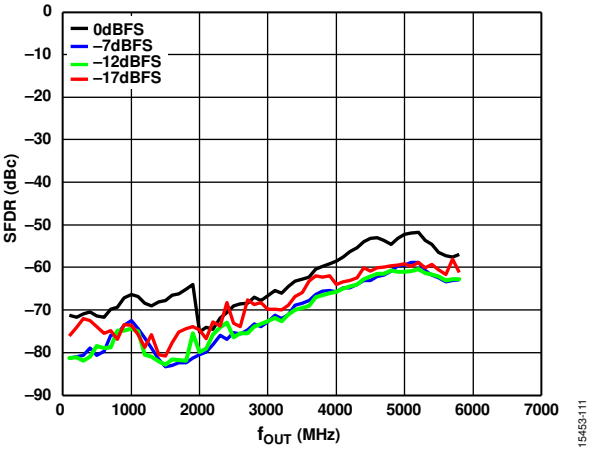


Figure 11. Worst Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×

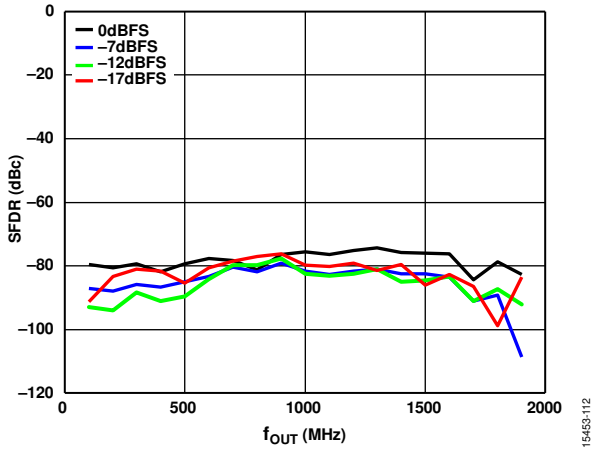


Figure 12. Second Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 12), 4 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 1×, 12-Bit Resolution

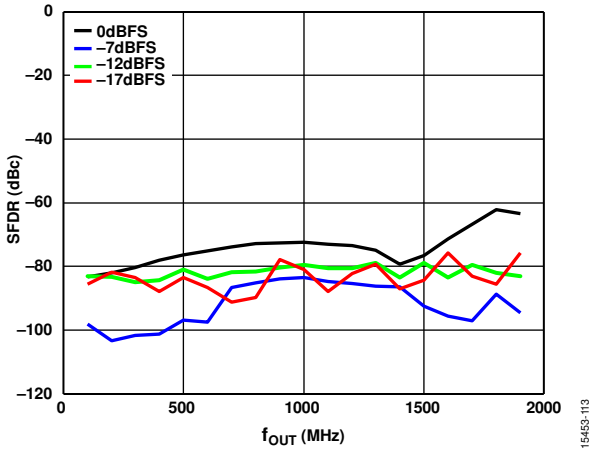


Figure 13. Third Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 12), 4 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 1×, 12-Bit Resolution

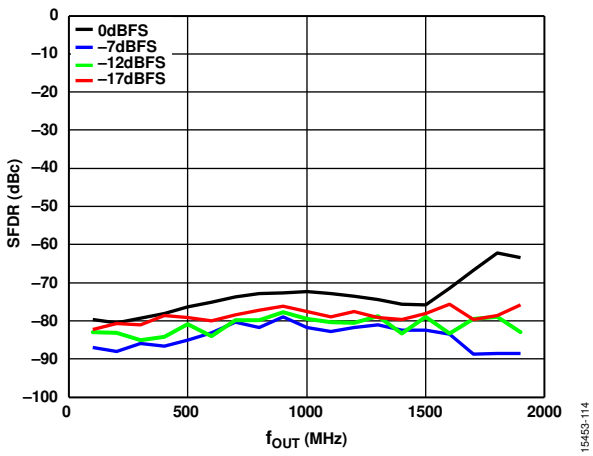


Figure 14. Worst Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 12), 4 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 1×, 12-Bit Resolution

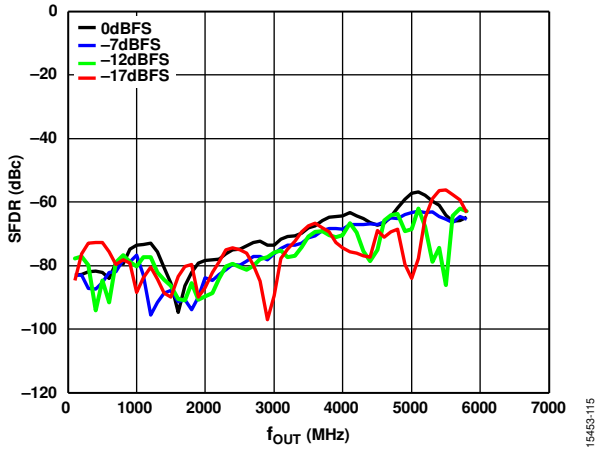


Figure 15. Second Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 9), 12 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×

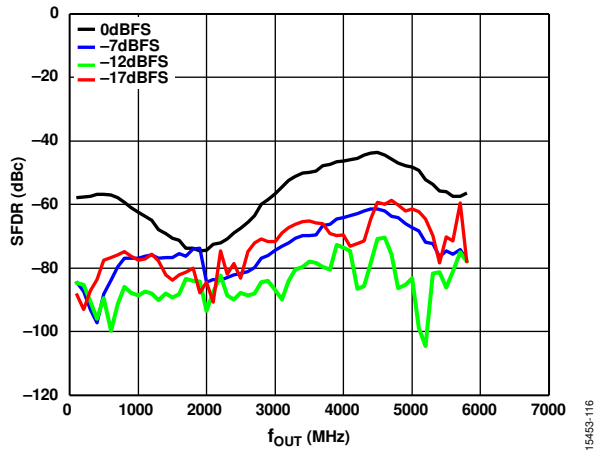


Figure 16. Third Harmonic (SFDR) vs. $f_{OUT}$ over Digital Scale (Mode 9), 12 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×

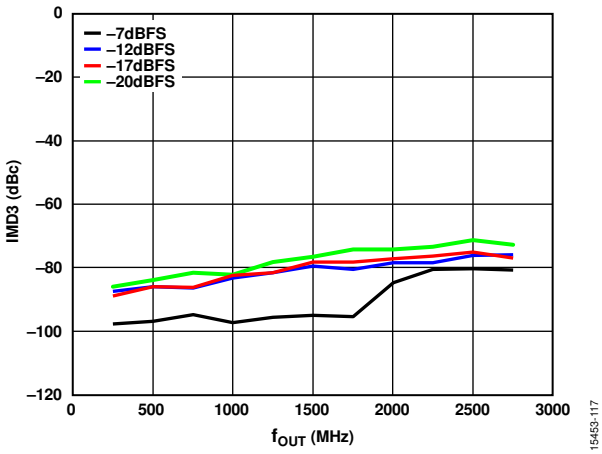


Figure 17. IMD3 vs. $f_{OUT}$ over Digital Scale (Mode 0) 6 GHz DAC Sample Rate, Channel Interpolation 2×, Main Interpolation 8×, 1 MHz Tone Spacing

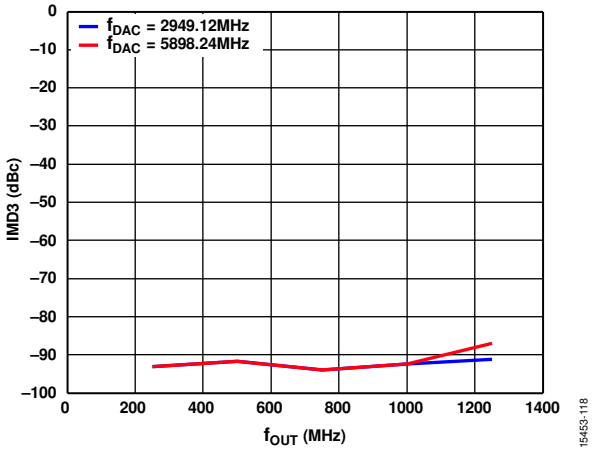


Figure 18. IMD3 vs. $f_{OUT}$ over $f_{DAC}$ (Mode 0), Channel Interpolation 2×, Main Interpolation 8×, 1 MHz Tone Spacing

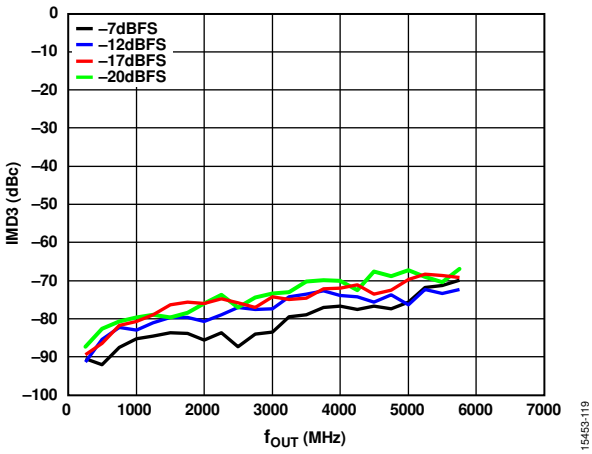


Figure 19. IMD3 vs. $f_{OUT}$ over Digital Scale (Mode 1), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×, 1 MHz Tone Spacing

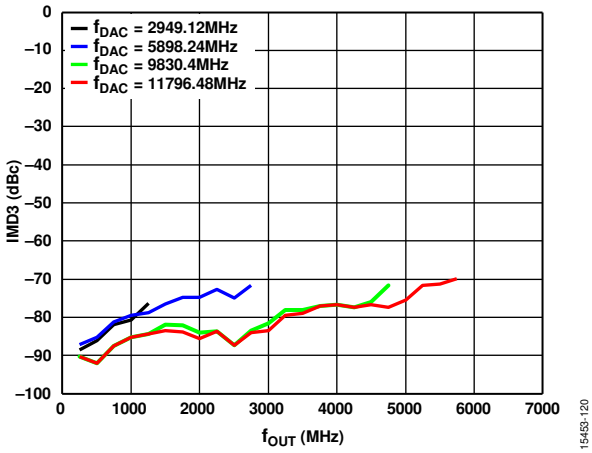


Figure 20. IMD3 vs. $f_{OUT}$ over $f_{DAC}$ (Mode 1), Channel Interpolation 4×, Main Interpolation 8×, 1 MHz Tone Spacing, –7 dB Digital Scale

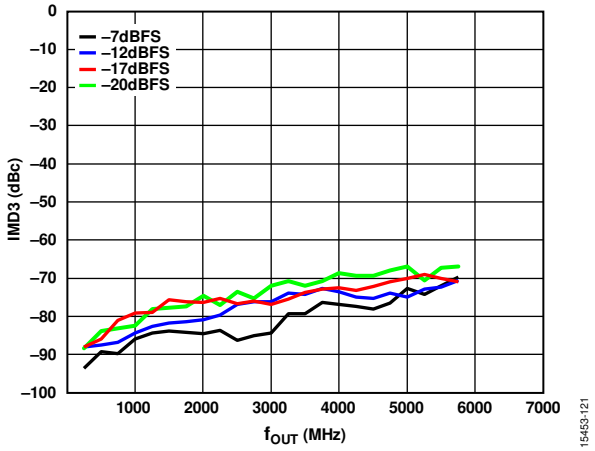


Figure 21. IMD3 vs. $f_{OUT}$ over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×, 1 MHz Tone Spacing

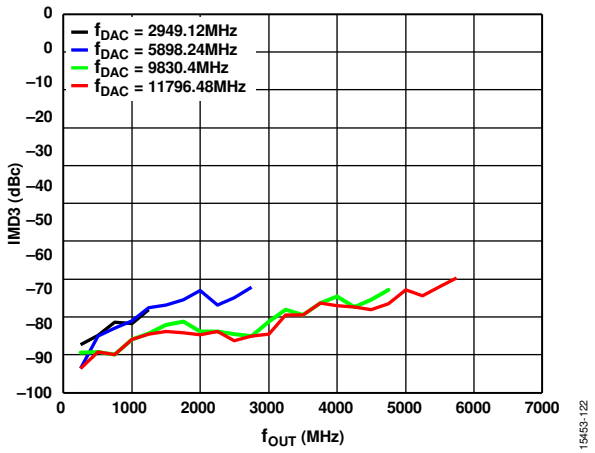


Figure 22. IMD3 vs. $f_{OUT}$ over $f_{DAC}$ (Mode 2), Channel Interpolation 4×, Main Interpolation 8×, 1 MHz Tone Spacing

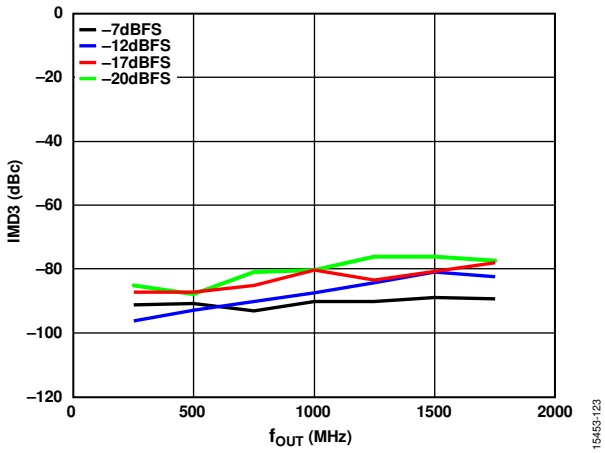


Figure 23. IMD3 vs. $f_{OUT}$ over Digital Scale (Mode 12), 4 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 1×, 1 MHz Tone Spacing, 12-Bit Resolution

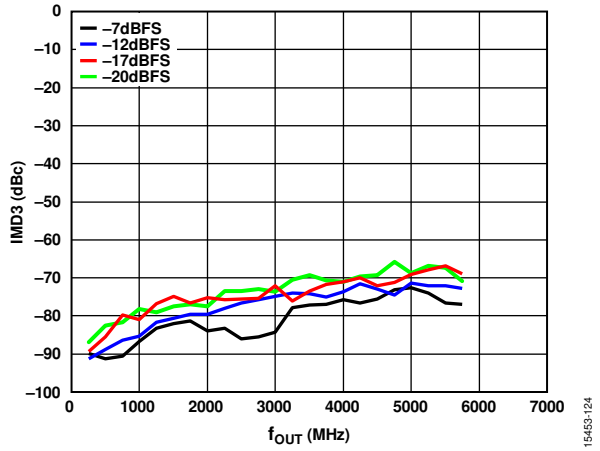


Figure 24. IMD3 vs. $f_{OUT}$ over Digital Scale (Mode 9), 12 GHz DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×, 1 MHz Tone Spacing

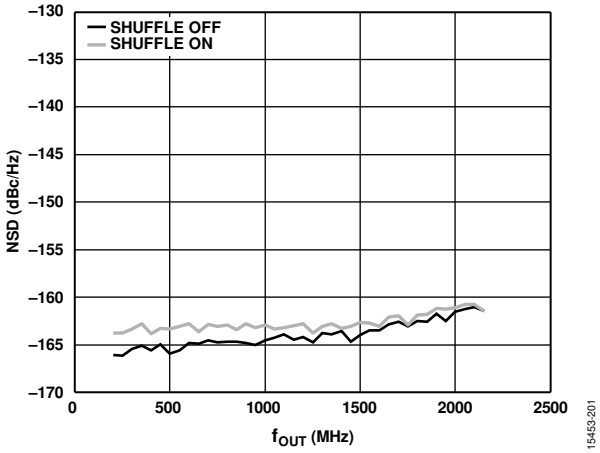


Figure 25. Single-Tone NSD Measured at 70 MHz vs. $f_{OUT}$, 11796.48 MHz $f_{DAC}$, 16-Bit Resolution, Shuffle Off vs. Shuffle On

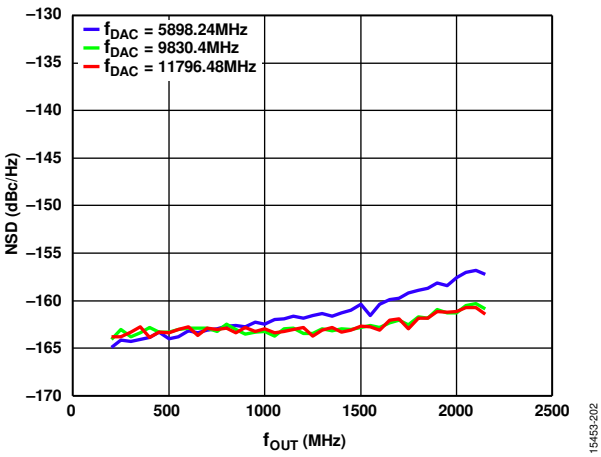


Figure 26. Single-Tone NSD Measured at 70 MHz vs. $f_{OUT}$ over $f_{DAC}$, 16-Bit Resolution, Shuffle On

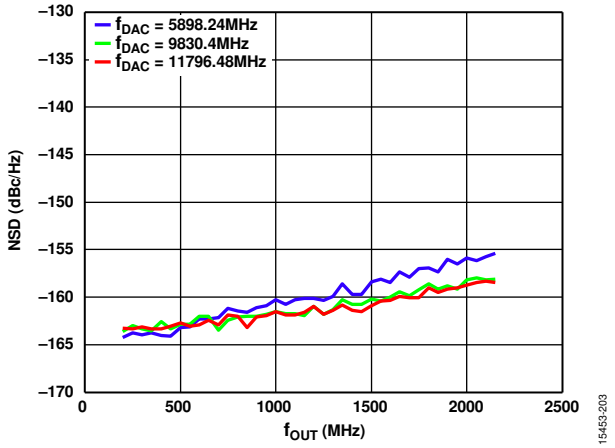


Figure 27. Single-Tone NSD Measured at 10% Offset from $f_{OUT}$ vs. $f_{OUT}$ over $f_{DAC}$, 16-Bit Resolution, Shuffle On

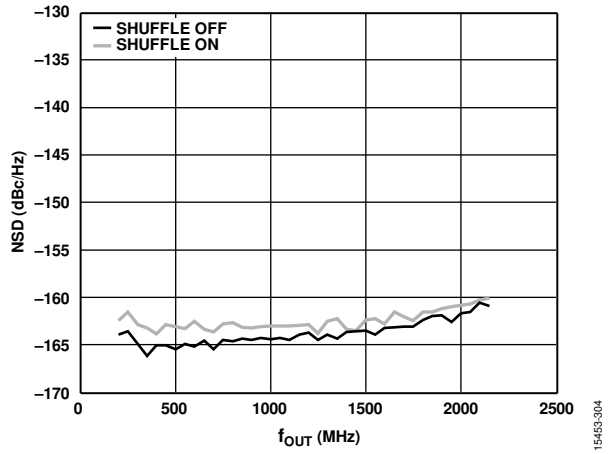


Figure 28. Single-Tone NSD Measured at 70 MHz vs $f_{OUT}$, 11796.48 MHz $f_{DAC}$, 12-Bit Resolution, Shuffle Off vs. Shuffle On

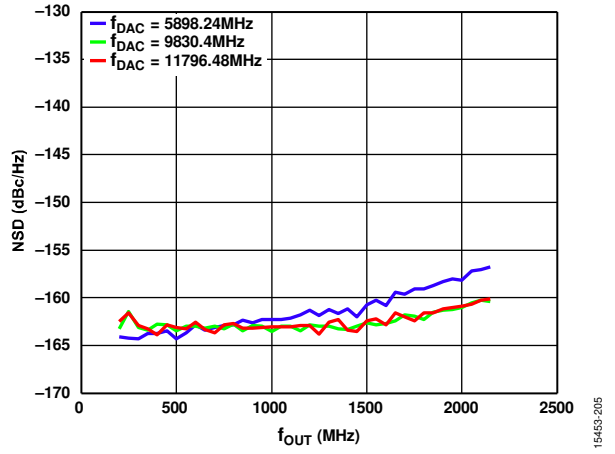


Figure 29. Single-Tone NSD Measured at 70 MHz vs. $f_{OUT}$ over $f_{DAC}$, 12-Bit Resolution, Shuffle On

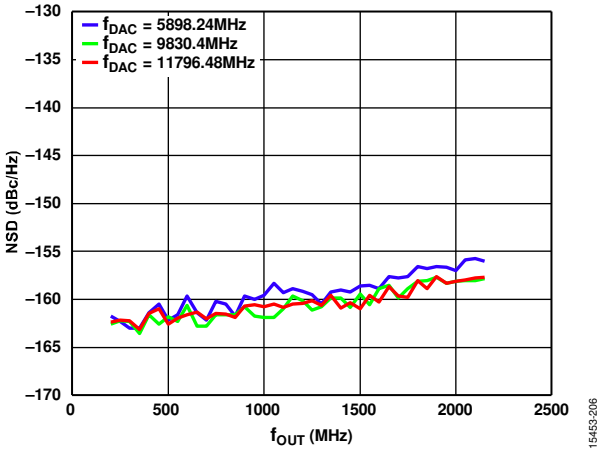


Figure 30. Single-Tone NSD Measured at 10% Offset from $f_{OUT}$ vs. $f_{OUT}$ over $f_{DAC}$, 12-Bit Resolution, Shuffle On

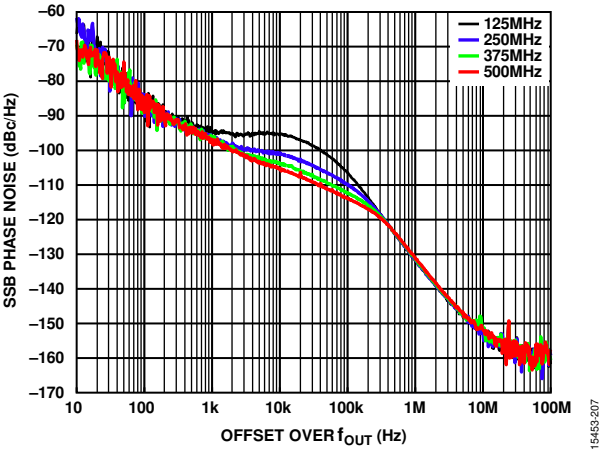


Figure 31. SSB Phase Noise vs. Offset over $f_{OUT}$, over PFD Frequency, $f_{DAC}$ = 12 GHz, $f_{OUT}$ = 1.8 GHz, PLL On, PLL Reference Clock = 500 MHz

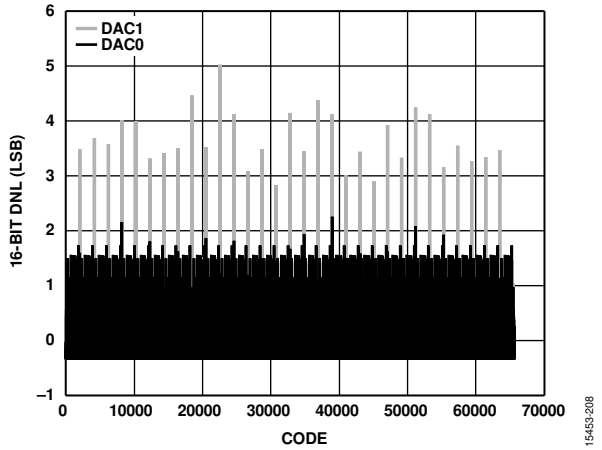


Figure 32. DNL, $I_{OUTFS}$ = 26 mA, 16-Bit Resolution

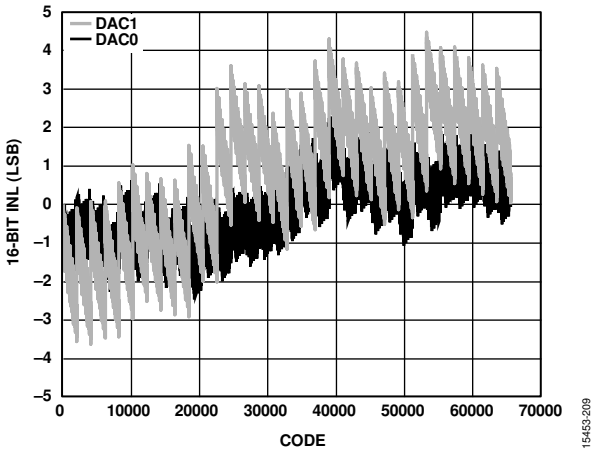


Figure 33. INL, $I_{OUTFS}$ = 26 mA, 16-Bit Resolution

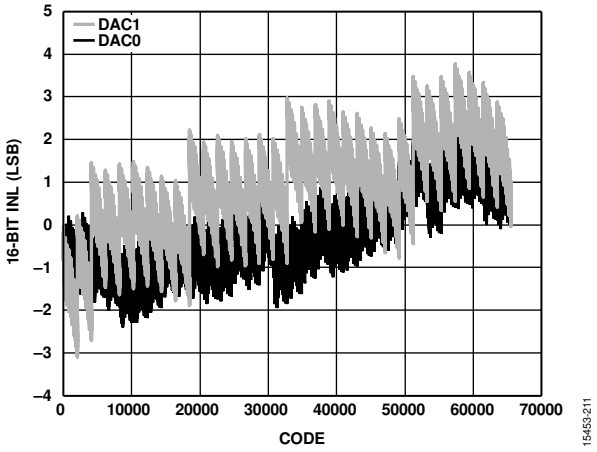


Figure 35. INL, $I_{OUTFS}$ = 20 mA, 16-Bit Resolution

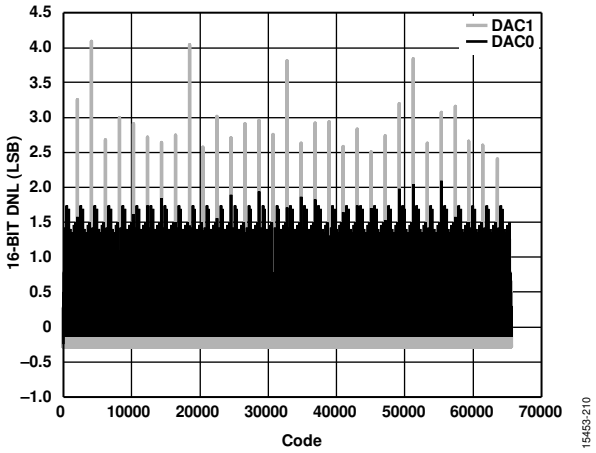


Figure 34. DNL, $I_{OUTFS}$ = 20 mA, 16-Bit Resolution

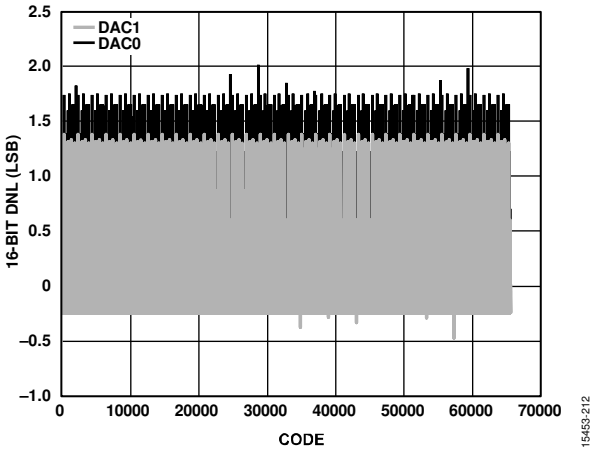


Figure 36. DNL, $I_{OUTFS}$ = 15.6 mA, 16-Bit Resolution

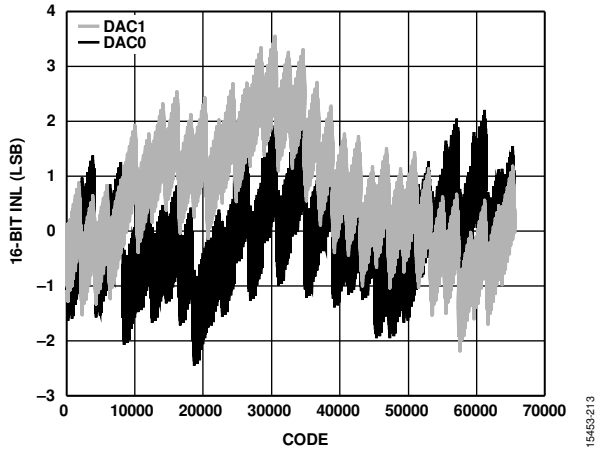


Figure 37. INL, $I_{OUTFS}$ = 15.6 mA, 16-Bit Resolution

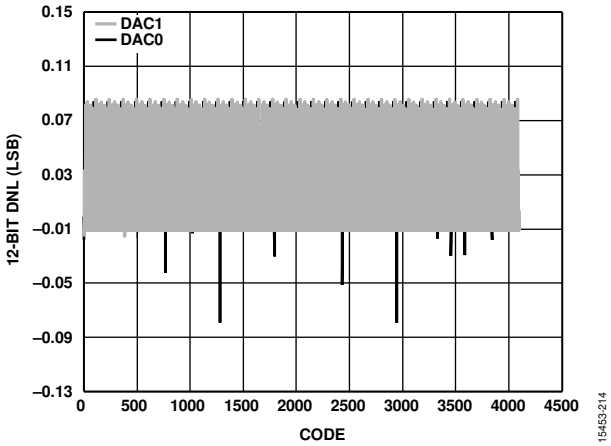


Figure 38. DNL, $I_{OUTFS}$ = 20 mA, 12-Bit Resolution

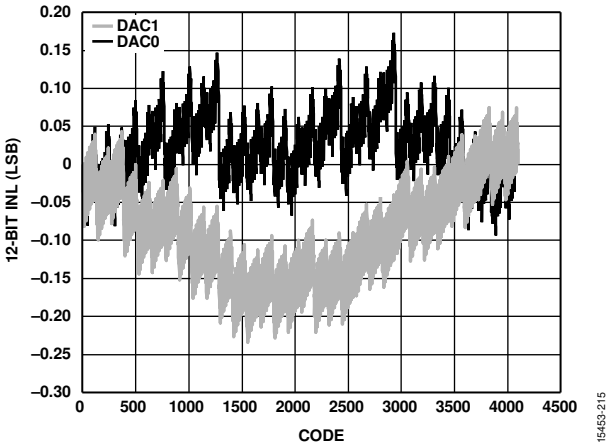


Figure 39. INL, $I_{OUTFS}$ = 20 mA, 12-Bit Resolution