



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



FEATURES**Supports multiband wireless applications**

- 3 bypassable, complex data input channels per RF DAC**
- 1.54 GSPS maximum complex input data rate per input channel**
- 1 independent NCO per input channel**

Proprietary, low spurious and distortion design

- 2-tone IMD = -83 dBc at 1.8 GHz, -7 dBFS/tone RF output**
- SFDR < -80 dBc at 1.8 GHz, -7 dBFS RF output**

Flexible 8-lane, 15.4 Gbps JESD204B interface

- Supports single-band and multiband use cases**
- Supports 12-bit high density mode for increased data throughput**

Multiple chip synchronization

- Supports JESD204B Subclass 1**

Selectable interpolation filter for a complete set of input data rates

- 1x, 2x, 3x, 4x, 6x, and 8x configurable data channel interpolation**
- 1x, 2x, 4x, 6x, 8x, and 12x configurable final interpolation**

Final 48-bit NCO that operates at the DAC rate to support frequency synthesis up to 6 GHz**Transmit enable function allows extra power saving and downstream circuitry protection****High performance, low noise PLL clock multiplier**

- Supports 12.6 GSPS DAC update rate**
- Observation ADC clock driver with selectable divide ratios**

Low power

- 2.55 W at 12 GSPS, dual channel mode**
- 10 mm × 10 mm, 144-ball BGA_ED with metal enhanced thermal lid, 0.80 mm pitch**

APPLICATIONS**Wireless communications infrastructure**

- Multiband base station radios**
- Microwave/E-band backhaul systems**

Instrumentation, automatic test equipment (ATE)**GENERAL DESCRIPTION**

The AD9173 is a high performance, dual, 16-bit digital-to-analog converter (DAC) that supports DAC sample rates to 12.6 GSPS. The device features an 8-lane, 15.4 Gbps JESD204B data input port, a high performance, on-chip DAC clock multiplier, and digital signal processing capabilities targeted at single-band and multiband direct to radio frequency (RF) wireless applications.

The AD9173 features three complex data input channels per RF DAC that are bypassable. Each data input channel includes a configurable gain stage, an interpolation filter, and a channel numerically controlled oscillator (NCO) for flexible, multiband frequency planning. The device supports up to a 1.54 GSPS complex data rate per input channel and is capable of aggregating multiple complex input data streams up to a maximum complex data rate of 1.54 GSPS. Additionally, the AD9173 supports ultrawide bandwidth modes bypassing the channelizers to provide maximum data rates of up to 3.08 GSPS (with 11-bit resolution using 16-bit serializer/deserializer (SERDES) packing) and 3.4 GSPS (with 11-bit resolution using 12-bit SERDES packing).

The AD9173 is available in a 144-ball BGA_ED package.

PRODUCT HIGHLIGHTS

- Supports single-band and multiband wireless applications with three bypassable complex data input channels per RF DAC at a maximum complex input data rate of 1.54 GSPS with 11-bit resolution and 1.23 GSPS with 16-bit resolution. One independent NCO per input channel.
- Ultrawide bandwidth channel bypass modes supporting up to 3.08 GSPS data rates with 11-bit resolution, 16-bit SERDES packing and 3.4 GSPS with 11-bit resolution, 12-bit SERDES packing.
- Low power dual converter decreases the amount of power consumption needed in high bandwidth and multichannel applications.

TABLE OF CONTENTS

Features	1	Serial Port Options.....	27
Applications.....	1	JESD204B Serial Data Interface.....	29
General Description	1	JESD204B Overview	29
Product Highlights	1	Physical Layer	32
Revision History	2	Data Link Layer	34
Functional Block Diagram	3	Syncing LMFC Signals.....	37
Specifications.....	4	Transport Layer	42
DC Specifications	4	JESD204B Test Modes	43
Digital Specifications	5	JESD204B Error Monitoring.....	45
Maximum DAC Sampling Rate Specifications.....	5	Digital Datapath	48
Power Supply DC Specifications	6	Total Datapath Interpolation	48
Serial Port and CMOS Pin Specifications	8	Channel Digital Datapath	50
Digital Input Data Timing Specifications	9	Main Digital Datapath.....	53
JESD204B Interface Electrical and Speed Specifications	10	Interrupt Request Operation	59
Input Data Rates and Signal Bandwidth Specifications	10	Interrupt Service Routine.....	59
AC Specifications.....	11	Applications Information	60
Absolute Maximum Ratings.....	13	Hardware Considerations	60
Reflow Profile.....	13	Analog Interface Considerations.....	63
Thermal Characteristics	13	DAC Input Clock Configurations.....	63
ESD Caution.....	13	Clock Output Driver	65
Pin Configuration and Function Descriptions.....	14	Analog Outputs	65
Typical Performance Characteristics	17	Start-Up Sequence	66
Terminology	24	Register Summary	73
Theory of Operation	25	Register Details	81
Serial Port Operation	27	Outline Dimensions	142
Data Format	27	Ordering Guide	142
Serial Port Pin Descriptions.....	27		

REVISION HISTORY

11/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

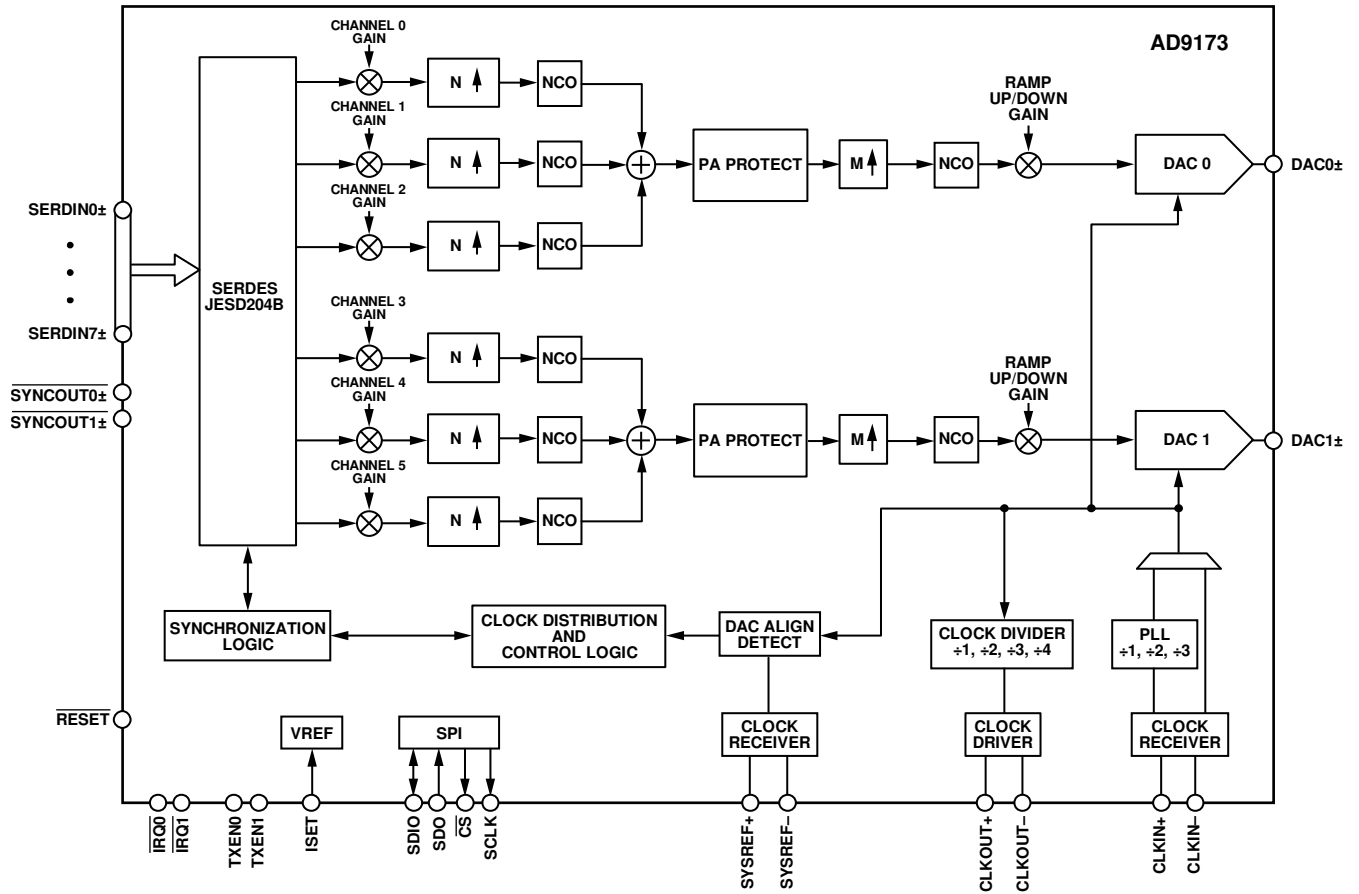


Figure 1.

16261-001

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, $T_j = -40^{\circ}\text{C}$ to $+118^{\circ}\text{C}$. For the typical values, $T_A = 25^{\circ}\text{C}$, which corresponds to $T_j = 51^{\circ}\text{C}$.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bit
ACCURACY					
Integral Nonlinearity (INL)			±7		LSB
Differential Nonlinearity (DNL)			±7		LSB
ANALOG OUTPUTS (DAC0+, DAC0-, DAC1+, DAC1-)					
Gain Error (with Internal ISET Reference)			±15		%
Full-Scale Output Current					
Minimum	$R_{SET} = 5\text{ k}\Omega$	14.2	16	17.8	mA
Maximum	$R_{SET} = 5\text{ k}\Omega$	23.6	26	28.8	mA
Common-Mode Voltage			0		V
Differential Impedance			100		Ω
DAC DEVICE CLOCK INPUT (CLKIN+, CLKIN-)					
Differential Input Power	$R_{LOAD} = 100\text{ }\Omega$ differential on-chip				
Minimum			0		dBm
Maximum			6		dBm
Differential Input Impedance ¹			100		Ω
Common-Mode Voltage	AC-coupled		0.5		V
CLOCK OUTPUT DRIVER (CLKOUT+, CLKOUT-)					
Differential Output Power					
Minimum			-9		dBm
Maximum			0		dBm
Differential Output Impedance			100		Ω
Common-Mode Voltage	AC-coupled		0.5		V
Output Frequency		727.5		3000	MHz
TEMPERATURE DRIFT					
Gain			10		ppm/ $^{\circ}\text{C}$
REFERENCE					
Internal Reference Voltage			0.495		V
ANALOG SUPPLY VOLTAGES					
AVDD1.0		0.95	1.0	1.05	V
AVDD1.8		1.71	1.8	1.89	V
DIGITAL SUPPLY VOLTAGES					
DVDD1.0		0.95	1.0	1.05	V
DAVDD1.0		0.95	1.0	1.05	V
DVDD1.8		1.71	1.8	1.89	V
SERDES SUPPLY VOLTAGES					
SVDD1.0		0.95	1.0	1.05	V

¹ See the DAC Input Clock Configurations section for more details.

DIGITAL SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = -40°C to +118°C. For the typical values, T_A = +25°C, which corresponds to T_J = 51°C.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC UPDATE RATE					
Minimum				2.91	GSPS
Maximum ¹	16-bit resolution, with interpolation	12.6			GSPS
	11-bit resolution, with interpolation	12.6			GSPS
	11-bit resolution, no interpolation	3.4			GSPS
Adjusted ²	16-bit resolution, with interpolation ³	1.23			GSPS
	11-bit resolution, with interpolation	1.54			GSPS
	11-bit resolution, no interpolation ⁴	3.4			GSPS
DAC PHASE-LOCKED LOOP (PLL) VOLTAGE CONTROLLED OSCILLATOR (VCO) FREQUENCY RANGES					
VCO Output Divide by 1		8.74		12.42	GSPS
VCO Output Divide by 2		4.37		6.21	GSPS
VCO Output Divide by 3		2.91		4.14	GSPS
PHASE FREQUENCY DETECT INPUT FREQUENCY RANGES					
9.96 GHz ≤ VCO Frequency ≤ 10.87 GHz		25		225	MHz
VCO Frequency < 9.96 GHz or VCO Frequency > 10.87 GHz		25		770	MHz
DAC DEVICE CLOCK INPUT (CLKIN+, CLKIN-) FREQUENCY RANGES					
PLL Off		2.91		12.6	GHz
PLL On	M divider set to divide by 1	25		770	MHz
	M divider set to divide by 2	50		1540	MHz
	M divider set to divide by 3	75		2310	MHz
	M divider set to divide by 4	100		3080	MHz

¹ The maximum DAC update rate varies depending on the selected JESD204B mode and the lane rate for the given configuration used. The maximum DAC rate according to lane rate and voltage supply levels is listed in Table 3.

² The adjusted DAC update rate is calculated as f_{DAC}, divided by the minimum required interpolation factor for a given mode or the maximum channel data rate for a given mode. Different modes have different maximum DAC update rates, minimum interpolation factors, and maximum channel data rates, as shown in Table 13.

³ The adjusted DAC update rate of 1.23 GSPS is the maximum for any 16-bit resolution mode of operation. See Table 13 for more details.

⁴ The adjusted DAC update rate of 3.4 GSPS is the maximum for any 11-bit resolution mode of operation. See Table 13 for more details.

MAXIMUM DAC SAMPLING RATE SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = -40°C to +118°C. For the typical values, T_A = 25°C, which corresponds to T_J = 51°C.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DAC UPDATE RATE					
SVDD1.0 = 1.0 V ± 5%	Lane rate > 11 Gbps	11.67			GSPS
	Lane rate ≤ 11 Gbps	12.37			GSPS
SVDD1.0 = 1.0 V ± 2.5%	Lane rate > 11 Gbps	11.79			GSPS
	Lane rate ≤ 11 Gbps ¹	12.6			GSPS

¹ If using the on-chip PLL, the maximum DAC speed is limited to the maximum PLL speed of 12.42 GSPS, as listed in Table 2.

POWER SUPPLY DC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. For the minimum and maximum values, T_J = -40°C to $+118^{\circ}\text{C}$. For the typical values, T_A = 25°C , which corresponds to T_J = 51°C .

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DUAL-LINK MODES					
Mode 1 (L = 2, M = 4, NP = 16, N = 16)	11.7965 GSPS DAC rate, 184.32 MHz PLL reference clock, 32x total interpolation (4x, 8x), 40 MHz tone at -3 dBFS, channel gain = -6 dB, channel NCOs = ± 150 MHz, main NCO = 2 GHz, SYNCOUTx \pm in LVDS mode				
AVDD1.0	All supply levels set to nominal values		725	1020	mA
	All supply levels set to 5% tolerance		775	1120	mA
AVDD1.8			110	130	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply				
	All supply levels set to nominal values		1270	1670	mA
	All supplies at 5% tolerance		1350	1850	mA
DVDD1.8			35	50	mA
SVDD1.0					
	All supply levels set to nominal values		290	510	mA
	All supplies at 5% tolerance		305	560	mA
Total Power Dissipation			2.55	3.38	W
Mode 4 (L = 4, M = 4, NP = 16, N = 16)	11.7965 GSPS DAC rate, 491.52 MHz PLL reference clock, 24x total interpolation (3x, 8x), 40 MHz tone at -3 dBFS, channel gain = -6 dB, channel NCOs = ± 150 MHz, main NCO = 2 GHz, SYNCOUTx \pm in LVDS mode				
AVDD1.0			725		mA
AVDD1.8			110		mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply		1340		mA
DVDD1.8			35		mA
SVDD1.0			425		mA
Total Power Dissipation			2.75		W
Mode 0 (L = 1, M = 2, NP = 16, N = 16)	5.89824 GSPS DAC rate, 184.32 MHz PLL reference clock, 16x total interpolation (2x, 8x), 40 MHz tone at -3 dBFS, channel NCO disabled, main NCO = 1.8425 GHz, SYNCOUTx \pm in LVDS mode				
AVDD1.0	All supply levels set to nominal values		400	670	mA
	All supplies at 5% tolerance		425	745	mA
AVDD1.8			110	130	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply				
	All supply levels set to nominal values		625	960	mA
	All supplies at 5% tolerance		670	1070	mA
DVDD1.8			35	50	mA
SVDD1.0			175	340	mA
Total Power Dissipation			1.45	2.15	W
Mode 3 (L = 2, M = 2, NP = 16, N = 16)	11.7965 GSPS DAC rate, 184.32 MHz PLL reference clock, 24x total interpolation (3x, 8x), 40 MHz tone at -3 dBFS, channel NCO disabled, main NCO = 2.655 GHz, SYNCOUTx \pm in LVDS mode				
AVDD1.0	All supply levels set to nominal values		725		mA
	All supplies at 5% tolerance		775		mA
AVDD1.8			110		mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply				
	All supply levels set to nominal values		1175		mA
	All supplies at 5% tolerance		1250		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DVDD1.8			35		mA
SVDD1.0	All supply levels set to nominal values		245		mA
	All supplies at 5% tolerance		250		mA
Total Power Dissipation			2.4		W
Mode 2 (L = 3, M = 6, NP = 16, N = 16)	12 GSPS DAC rate, 375 MHz PLL reference clock, 48× total interpolation (6×, 8×), 30 MHz tone at –3 dBFS, channel gain = –11 dB, channel NCOs = 20 MHz, main NCO = 2.1 GHz				
AVDD1.0	All supply levels set to nominal values		735	1030	mA
	All supplies at 5% tolerance		785	1135	mA
AVDD1.8			110	130	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply				mA
	All supply levels set to nominal values		1370	1800	mA
	All supplies at 5% tolerance		1460	1980	mA
DVDD1.8			35	50	mA
SVDD1.0	All supply levels set to nominal values		410	680	mA
	All supplies at 5% tolerance		430	755	mA
Total Power Dissipation			2.77	3.69	W
SINGLE-LINK MODES					
Mode 17 (L = 8, M = 2, NP = 12, N = 11)	3.4 GSPS DAC rate, 187.5 MHz PLL reference clock, 1× total interpolation (1×, 1×), 1.2 GHz tone at –3 dBFS, channel and main NCOs disabled				
AVDD1.0	All supply levels set to nominal values		260	510	mA
	All supplies at 5% tolerance		275	580	mA
AVDD1.8			85	100	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply				mA
	All supply levels set to nominal values		300	610	mA
	All supplies at 5% tolerance		310	710	mA
DVDD1.8			25	50	mA
SVDD1.0	All supply levels set to nominal values		500	780	mA
	All supplies at 5% tolerance		505	860	mA
Total Power Dissipation			1.2	2.05	W
DUAL-LINK, MODE 3 (NCO ONLY, SINGLE-CHANNEL MODE, NO SERDES)					
Mode 3	6 GSPS DAC rate, 300 MHz PLL reference clock, 8× total interpolation (1×, 8×), no input tone (dc internal level = 0x50FF), channel NCO = 40 MHz, main NCO = 1.8425 GHz				
AVDD1.0	All supply levels set to nominal values		410	660	mA
	All supplies at 5% tolerance		435	750	mA
AVDD1.8			110	130	mA
DVDD1.0	Combined current consumption with the DAVDD1.0 supply				mA
	All supply levels set to nominal values		500	780	mA
	All supplies at 5% tolerance		515	950	mA
DVDD1.8			0.3	1	mA
SVDD1.0	All supply levels set to nominal values		5	100	mA
	All supplies at 5% tolerance		3	120	mA
Total Power Dissipation			1.1	1.671	W

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DUAL-LINK, MODE 4 (NCO ONLY, DUAL-CHANNEL MODE, NO SERDES) Mode 4	12 GSPS DAC rate, 500 MHz PLL reference clock, 32× total interpolation (4×, 8×), no input tone (dc internal level = 0x2AFF), channel NCOs = ±150 MHz, main NCO = 2 GHz				
AVDD1.0	All supply levels set to nominal values All supplies at 5% tolerance		750	1030	mA
AVDD1.8			790	1130	mA
DVDD1.0			110	130	mA
DVDD1.8	Combined current consumption with the DAVDD1.0 supply All supply levels set to nominal values All supplies at 5% tolerance		1200	1590	mA
SVDD1.0			1300	1750	mA
DVDD1.8			0.3	1	mA
SVDD1.0			5	100	mA
Total Power Dissipation			2.2	2.851	W

SERIAL PORT AND CMOS PIN SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC $I_{OUTFS} = 20$ mA, unless otherwise noted. For the minimum and maximum values, $T_J = -40^{\circ}\text{C}$ to $+118^{\circ}\text{C}$. For the typical values, $T_A = 25^{\circ}\text{C}$, which corresponds to $T_J = 51^{\circ}\text{C}$.

Table 5.

Parameter	Symbol	Test Comments/Conditions	Min	Typ	Max	Unit
WRITE OPERATION		See Figure 48				
Maximum SCLK Clock Rate	$f_{SCLK}, 1/t_{SCLK}$		80			MHz
SCLK Clock High	t_{PWH}	SCLK = 20 MHz	5.03			ns
SCLK Clock Low	t_{PWL}	SCLK = 20 MHz	1.6			ns
SDIO to SCLK Setup Time	t_{DS}		1.154			ns
SCLK to SDIO Hold Time	t_{DH}		0.577			ns
\overline{CS} to SCLK Setup Time	t_S		1.036			ns
SCLK to \overline{CS} Hold Time	t_H		-5.3			ps
READ OPERATION		See Figure 47				
SCLK Clock Rate	$f_{SCLK}, 1/t_{SCLK}$				48.58	MHz
SCLK Clock High	t_{PWH}		5.03			ns
SCLK Clock Low	t_{PWL}		1.6			ns
SDIO to SCLK Setup Time	t_{DS}		1.158			ns
SCLK to SDIO Hold Time	t_{DH}		0.537			ns
\overline{CS} to SCLK Setup Time	t_S		1.036			ns
SCLK to SDIO Data Valid Time	t_{DV}		9.6			ns
SCLK to SDO Data Valid Time	t_{DV}		13.7			ns
\overline{CS} to SDIO Output Valid to High-Z		Not shown in Figure 47 or Figure 48	5.4			ns
\overline{CS} to SDO Output Valid to High-Z		Not shown in Figure 47 or Figure 48	9.59			ns
INPUTS (SDIO, SCLK, \overline{CS} , RESET, TXEN0, and TXEN1)						
Voltage Input						
High	V_{IH}		1.48			V
Low	V_{IL}				0.425	V
Current Input						
High	I_{IH}				±100	nA
Low	I_{IL}		±100			nA
OUTPUTS (SDIO, SDO)						
Voltage Output						
High	V_{OH}					
0 mA load			1.69			V
4 mA load			1.52			V

Parameter	Symbol	Test Comments/Conditions	Min	Typ	Max	Unit
Low	V_{OL}					
0 mA load					0.045	V
4 mA load					0.175	V
Current Output						
High	I_{OH}			4		mA
Low	I_{OL}			4		mA
INTERRUPT OUTPUTS (IRQ0, IRQ1)						
Voltage Output						
High	V_{OH}		1.71			V
Low	V_{OL}				0.075	V

DIGITAL INPUT DATA TIMING SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC I_{OUTFS} = 20 mA, unless otherwise noted. For the minimum and maximum values, $T_j = -40^{\circ}\text{C}$ to $+118^{\circ}\text{C}$. For the typical values, $T_A = 25^{\circ}\text{C}$, which corresponds to $T_j = 51^{\circ}\text{C}$.

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LATENCY ¹					
Channel Interpolation Factor, Main Datapath Interpolation Factor	LMFC_VAR_x = 12, LMFC_DELAY_x = 12, unless otherwise noted				
1x, 1x ²	JESD204B Mode 15 ³		420		DAC clock cycle
	JESD204B Mode 16		440		DAC clock cycle
	JESD204B Mode 17		590		DAC clock cycle
1x, 8x ²	JESD204B Mode 3		1390		DAC clock cycle
	JESD204B Mode 8 ³		1820		DAC clock cycle
	JESD204B Mode 9		1920		DAC clock cycle
1x, 12x ²	JESD204B Mode 8 ³		2700		DAC clock cycle
	JESD204B Mode 9		2840		DAC clock cycle
2x, 6x ²	JESD204B Mode 3, Mode 4		1970		DAC clock cycle
	JESD204B Mode 5		1770		DAC clock cycle
2x, 8x ²	JESD204B Mode 0		2020		DAC clock cycle
	JESD204B Mode 3, Mode 4		2500		DAC clock cycle
3x, 6x ²	JESD204B Mode 3, Mode 4		2880		DAC clock cycle
	JESD204B Mode 5, Mode 6		2630		DAC clock cycle
3x, 8x ²	JESD204B Mode 3, Mode 4		3310		DAC clock cycle
	JESD204B Mode 5, Mode 6		2980		DAC clock cycle
4x, 6x ²	JESD204B Mode 0, Mode 1, Mode 2		2410		DAC clock cycle
4x, 8x ²	JESD204B Mode 0, Mode 1, Mode 2		3090		DAC clock cycle
6x, 6x ²	JESD204B Mode 0, Mode 1, Mode 2		3190		DAC clock cycle
6x, 8x ²	JESD204B Mode 0, Mode 1, Mode 2		4130		DAC clock cycle
8x, 6x ²	JESD204B Mode 7		3300		DAC clock cycle
8x, 8x ²	JESD204B Mode 7		4270		DAC clock cycle
DETERMINISTIC LATENCY					
Fixed				13	PCLK ⁴
Variable				2	PCLK cycles
SYSREF \pm TO LOCAL MULTIFRAME CLOCK (LMFC) DELAY			0		DAC clock cycles

¹ Total latency (or pipeline delay) through the device is calculated as follows: total latency = interface latency + fixed latency + variable latency + pipeline delay.

² The first value listed in this specification is the channel interpolation factor, and the second value is the main datapath interpolation factor.

³ LMFC_VAR_x = 7 and LMFC_DELAY_x = 4

⁴ PCLK is the internal processing clock for the AD9173 and equals the lane rate \div 40.

JESD204B INTERFACE ELECTRICAL AND SPEED SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC $I_{OUTFS} = 20$ mA, unless otherwise noted. For the minimum and maximum values, $T_J = -40^\circ\text{C}$ to $+118^\circ\text{C}$. For the typical values, $T_A = 25^\circ\text{C}$, which corresponds to $T_J = 51^\circ\text{C}$.

Table 7.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B SERIAL INTERFACE RATE (SERIAL LANE RATE)			3		15.4	Gbps
JESD204B DATA INPUTS						
Input Leakage Current		$T_A = 25^\circ\text{C}$				
Logic High		Input level = $1.0\text{ V} \pm 0.25\text{ V}$		10		μA
Logic Low		Input level = 0 V		-4		μA
Unit Interval	UI		333		66.7	ps
Common-Mode Voltage	V_{RCM}	AC-coupled	-0.05		+1.1	V
Differential Voltage	$R_{V_{DIFF}}$		110		1050	mV
Differential Impedance	$Z_{R_{DIFF}}$	At dc	80	100	120	Ω
SYSREF \pm INPUT						
Differential Impedance				100		Ω
DIFFERENTIAL OUTPUTS (SYNCOUT0 \pm , SYNCOUT1 \pm) ¹		Driving 100 Ω differential load				
Output Differential Voltage	V_{OD}		320	390	460	mV
Output Offset Voltage	V_{OS}		1.08	1.12	1.15	V
SINGLE-ENDED OUTPUTS (SYNCOUT0 \pm , SYNCOUT1 \pm)		Driving 100 Ω differential load				
Output Voltage						
High	V_{OH}		1.69			V
Low	V_{OL}				0.045	V
Current Output						
High	I_{OH}			0		mA
Low	I_{OL}			0		mA

¹ IEEE Standard 1596.3 LVDS compatible.

INPUT DATA RATES AND SIGNAL BANDWIDTH SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC output full-scale current (I_{OUTFS}) = 20 mA, unless otherwise noted. For the minimum and maximum values, $T_J = -40^\circ\text{C}$ to $+118^\circ\text{C}$. For the typical values, $T_A = 25^\circ\text{C}$, which corresponds to $T_J = 51^\circ\text{C}$.

Table 8.

Parameter ¹	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT DATA RATE PER INPUT CHANNEL	Channel and main datapaths bypassed ($1 \times$ total interpolation), dual DAC mode, 11-bit resolution			3400	MSPS
	1 complex channel enabled, 16-bit resolution			1230	MSPS
	1 complex channel enabled, 11-bit resolution			1540	MSPS
	2 complex channels enabled			770	MSPS
	3 complex channels enabled			385	MSPS
COMPLEX SIGNAL BANDWIDTH PER INPUT CHANNEL	1 complex channel enabled ($0.8 \times f_{DATA}$), 11-bit resolution			984	MHz
	1 complex channel enabled ($0.8 \times f_{DATA}$), 16-bit resolution			1232	MHz
	2 complex channels enabled ($0.8 \times f_{DATA}$)			616	MHz
	3 complex channels enabled ($0.8 \times f_{DATA}$)			308	MHz
MAXIMUM NCO CLOCK RATE					
Channel NCO				1540	MHz
Main NCO				12.6	GHz

Parameter ¹	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM NCO SHIFT FREQUENCY RANGE					
Channel NCO	Channel summing node = 1.5 GHz, channel interpolation rate > 1×	-770		+770	MHz
Main NCO	$f_{DAC} = 12.6$ GHz, main interpolation rate > 1×	-6.3		+6.3	GHz
MAXIMUM FREQUENCY SPACING ACROSS INPUT CHANNELS	Maximum NCO output frequency × 0.8			1232	MHz

¹ Values listed for these parameters are the maximum possible when considering all JESD204B modes of operation. Some modes are more limiting, based on other parameters.

AC SPECIFICATIONS

AVDD1.0 = 1.0 V, AVDD1.8 = 1.8 V, DVDD1.0 = 1.0 V, DVDD1.8 = 1.8 V, SVDD1.0 = 1.0 V, and DAC $I_{OUTFS} = 20$ mA, unless otherwise noted. For the minimum and maximum, $T_J = -40^\circ\text{C}$ to $+118^\circ\text{C}$. For the typical values, $T_A = 25^\circ\text{C}$, which corresponds to $T_J = 51^\circ\text{C}$.

Table 9.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
Single-Tone, $f_{DAC} = 12000$ MSPS, Mode 1 (L = 2, M = 4)	-7 dBFS, shuffle enabled				
$f_{OUT} = 100$ MHz			-81		dBc
$f_{OUT} = 500$ MHz			-80		dBc
$f_{OUT} = 950$ MHz			-75		dBc
$f_{OUT} = 1840$ MHz			-80		dBc
$f_{OUT} = 2650$ MHz			-75		dBc
$f_{OUT} = 3700$ MHz			-67		dBc
Single Tone, $f_{DAC} = 6000$ MSPS, Mode 0 (L = 1, M = 2)	-7 dBFS, shuffle enabled				
$f_{OUT} = 100$ MHz			-85		dBc
$f_{OUT} = 500$ MHz			-85		dBc
$f_{OUT} = 950$ MHz			-78		dBc
$f_{OUT} = 1840$ MHz			-75		dBc
$f_{OUT} = 2650$ MHz			-69		dBc
Single-Tone, $f_{DAC} = 3000$ MSPS, Mode 15 (L = 8, M = 2)	-7 dBFS, shuffle enabled				
$f_{OUT} = 100$ MHz			-87		dBc
$f_{OUT} = 500$ MHz			-84		dBc
$f_{OUT} = 950$ MHz			-81		dBc
Single-Band Application—Band 3 (1805 MHz to 1880 MHz)	Mode 0, 2× to 8×, $f_{DAC} = 6000$ MSPS, 368.64 MHz reference clock				
SFDR Harmonics	-7 dBFS, shuffle enabled				
In-Band			-82		dBc
Digital Predistortion (DPD) Band	DPD bandwidth = data rate × 0.8		-80		dBc
Second Harmonic			-82		dBc
Third Harmonic			-80		dBc
Fourth and Fifth Harmonic			-95		dBc
SFDR Nonharmonics	-7 dBFS, shuffle enabled				
In-Band			-74		dBc
DPD Band			-74		dBc
ADJACENT CHANNEL LEAKAGE RATIO					
4C-WCDMA	-1 dBFS digital backoff				
$f_{DAC} = 1200$ MSPS, Mode 1 (L = 2, M = 4)					
$f_{OUT} = 1840$ MHz			-70		dBc
$f_{OUT} = 2650$ MHz			-68		dBc
$f_{OUT} = 3500$ MHz			-66		dBc
$f_{DAC} = 6000$ MSPS, Mode 0 (L = 1, M = 2)					
$f_{OUT} = 1840$ MHz			-71		dBc
$f_{OUT} = 2650$ MHz			-66		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
THIRD-ORDER INTERMODULATION DISTORTION (IMD) $f_{DAC} = 12000$ MSPS, Mode 1 (L = 2, M = 4)	Two-tone test, -7 dBFS/tone, 1 MHz spacing $f_{OUT} = 1840$ MHz		-83		dBc
	$f_{OUT} = 2650$ MHz		-85		dBc
	$f_{OUT} = 3700$ MHz		-77		dBc
$f_{DAC} = 6000$ MSPS, Mode 0 (L = 1, M = 2)	$f_{OUT} = 1840$ MHz		-74		dBc
	$f_{OUT} = 2650$ MHz		-72		dBc
NOISE SPECTRAL DENSITY (NSD)	0 dBFS, NSD measurement taken at 10% away from f_{OUT} , shuffle off				
Single Tone, $f_{DAC} = 12000$ MSPS, Mode 1 (L = 2, M = 4) $f_{OUT} = 100$ MHz			-169		dBm/Hz
$f_{OUT} = 500$ MHz			-168		dBm/Hz
$f_{OUT} = 950$ MHz			-166		dBm/Hz
$f_{OUT} = 1840$ MHz			-165		dBm/Hz
$f_{OUT} = 2150$ MHz			-164		dBm/Hz
Single Tone, $f_{DAC} = 6000$ MSPS, Mode 3 (L = 2, M = 2) $f_{OUT} = 100$ MHz			-169		dBm/Hz
$f_{OUT} = 500$ MHz			-167		dBm/Hz
$f_{OUT} = 950$ MHz			-166		dBm/Hz
$f_{OUT} = 1840$ MHz			-163		dBm/Hz
$f_{OUT} = 2150$ MHz			-162		dBm/Hz
Single Tone, $f_{DAC} = 3000$ MSPS, Mode 10 (L = 8, M = 2) $f_{OUT} = 100$ MHz			-166		dBm/Hz
$f_{OUT} = 500$ MHz			-163		dBm/Hz
$f_{OUT} = 950$ MHz			-160		dBm/Hz
SINGLE-SIDEBAND PHASE NOISE OFFSET	Loop filter component values according to Figure 89 are as follows: C1 = 22 nF, R1 = 232 Ω , C2 = 2.4 nF, C3 = 33 nF; PFD frequency = 500 MHz, $f_{OUT} = 1.8$ GHz, $f_{DAC} = 12$ GHz				
1 kHz			-97		dBc/Hz
10 kHz			-105		dBc/Hz
100 kHz			-114		dBc/Hz
600 kHz			-126		dBc/Hz
1.2 MHz			-133		dBc/Hz
1.8 MHz			-137		dBc/Hz
6 MHz			-148		dBc/Hz
DAC TO DAC OUTPUT ISOLATION	Taken using the AD9173-FMC-EBZ evaluation board				
Dual-Band— $f_{DAC} = 12000$ MSPS, Mode 1 (L = 2, M = 4) $f_{OUT} = 1840$ MHz			-77		dB
$f_{OUT} = 2650$ MHz			-70		dB
$f_{OUT} = 3700$ MHz			-68		dB

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
ISET, FILT_COARSE, FILT_BYP, FILT_VCM	−0.3 V to AVDD1.8 + 0.3 V
SERDINx±	−0.2 V to SVDD1.0 + 0.2 V
SYNCOUT0±, SYNCOUT1±, RESET, TXEN0, TXEN1, IRQ0, IRQ1, CS, SCLK, SDIO, SDO	−0.3 V to DVDD1.8 + 0.3 V
DAC0±, DAC1±, CLKIN±, CLKOUT±, FILT_FINE	−0.2 V to AVDD1.0 + 0.2 V
SYSREF±	−0.2 V to DVDD1.0 + 0.2 V
AVDD1.0, DVDD1.0, SVDD1.0 to GND	−0.2 V to +1.2 V
AVDD1.8, DVDD1.8 to GND	−0.3 V to 2.2 V
Maximum Junction Temperature (T _J) ¹	118°C
Storage Temperature Range	−65°C to +150°C
Reflow	260°C

¹ Some operating modes of the device may cause the device to approach or exceed the maximum junction temperature during operation at supported ambient temperatures. Removal of heat from the device may require additional measures such as active airflow, heat sinks, or other measures.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The AD9173 reflow profile is in accordance with the JEDEC JESD20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Thermal resistances and thermal characterization parameters are specified vs. the number of PCB layers in different airflow velocities (in m/sec). The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 10.

Use the values in Table 11 in compliance with JEDEC 51-12.

Table 11. Simulated Thermal Resistance vs. PCB Layers¹

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	25.3	2.4 ³	3.0 ⁴	°C/W
	1.0	22.6	N/A	N/A	°C/W
	2.5	21.0	N/A	N/A	°C/W
12-Layer PCB ²	0.0	15.4	2.4	2.6	°C/W
	1.0	13.1	N/A	N/A	°C/W
	2.5	11.6	N/A	N/A	°C/W

¹ N/A means not applicable.

² Non JEDEC thermal resistance.

³ 1SOP PCB with no vias in PCB.

⁴ 1SOP PCB with 7 × 7 standard JEDEC vias.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12
A	GND	SERDIN7+	SERDIN6+	SERDIN5+	SERDIN4+	GND	GND	SERDIN3+	SERDIN2+	SERDIN1+	SERDIN0+	GND
B	GND	SERDIN7-	SERDIN6-	SERDIN5-	SERDIN4-	GND	GND	SERDIN3-	SERDIN2-	SERDIN1-	SERDIN0-	GND
C	SVDD1.0	SVDD1.0	GND	GND	SVDD1.0	DVDD1.8	SVDD1.0	SVDD1.0	GND	GND	SVDD1.0	SVDD1.0
D	SYNCOUT1+	SYNCOUT1-	DVDD1.8	TXEN1	GND	SVDD1.0	GND	TXEN0	IRQ0	DVDD1.8	SYNCOUT0-	SYNCOUT0+
E	DNC	DNC	DVDD1.8	SDO	SCLK	CS	SDIO	RESET	IRQ1	DVDD1.8	DNC	DNC
F	GND	GND	GND	DAVDD1.0	DVDD1.0	DVDD1.0	DVDD1.0	DVDD1.0	DAVDD1.0	GND	GND	GND
G	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
H	SYSREF+	SYSREF-	AVDD1.0	AVDD1.0	AVDD1.0	FILT_FINE	FILT_COARSE	AVDD1.0	AVDD1.0	AVDD1.0	GND	CLKIN-
J	GND	DNC	GND	GND	GND	AVDD1.0	FILT_BYP	GND	GND	GND	GND	CLKIN+
K	CLKOUT+	GND	AVDD1.8	DNC	AVDD1.8	FILT_VCM	AVDD1.8	GND	GND	AVDD1.8	GND	GND
L	CLKOUT-	GND	AVDD1.8	GND	GND	AVDD1.8	AVDD1.8	GND	GND	AVDD1.8	GND	ISET
M	GND	AVDD1.0	GND	DAC1+	DAC1-	GND	GND	DAC0-	DAC0+	GND	AVDD1.0	GND

■ GROUND
 ■ SERDES INPUT
 ■ 1.0V DIGITAL SUPPLY
 ■ DAC PLL LOOP FILTER PINS
 ■ CMOS I/O
■ 1.0V ANALOG SUPPLY
 ■ SYSREF±/SYNCOUTx±
 ■ 1.0V D/A SUPPLY
 ■ DAC RF OUTPUTS
 ■ REFERENCE
■ 1.8V ANALOG SUPPLY
 ■ 1.0V SERDES SUPPLY
 ■ 1.8V DIGITAL SUPPLY
 ■ RF CLOCK PINS

DNC = DO NOT CONNECT

Figure 2. Pin Configuration {change D/A to digital to analog}

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1.0 V Supply H3 to H5, H8 to H10, J6, M2, M11	AVDD1.0	1.0 V Clock and Analog Supplies. These pins supply the clock receivers, clock distribution, the on-chip DAC clock multiplier, and the DAC analog core. Clean power supply rail sources are required on these pins.
F5 to F8	DVDD1.0	1.0 V Digital Supplies. These pins supply power to the DAC digital circuitry. Clean power supply rail sources are required on these pins.
F4, F9	DAVDD1.0	1.0 V Digital to Analog Supplies. These pins can share a supply rail with the DVDD1.0 supply (electrically connected) but must have separate supply plane and decoupling capacitors for the PCB layout to improve isolation for these two pins. Clean power supply rail sources are required on these pins.
C1, C2, C5, C7, C8, C11, C12, D6	SVDD1.0	1.0 V SERDES Supplies to the JESD204B Data Interface. Clean power supply rail sources are required on these pins.
1.8 V Supply K3, K5, K7, K10, L3, L6, L7, L10	AVDD1.8	1.8 V Analog Supplies to the On-Chip DAC Clock Multiplier and the DAC Analog Core. Clean power supply rail sources are required on these pins.
C6, D3, D10, E3, E10	DVDD1.8	1.8 V Digital Supplies to the JESD204B Data Interface and the Other Input/Output Circuitry, Such as the Serial Port Interface (SPI). Clean power supply rail sources are required on these pins.

Pin No.	Mnemonic	Description
Ground A1, A6, A7, A12, B1, B6, B7, B12, C3, C4, C9, C10, D5, D7, F1 to F3, F10 to F12, G1 to G12, H11, J1, J3 to J5, J8 to J11, K2, K8, K9, K11, K12, L2, L4, L5, L8, L9, L11, M1, M3, M6, M7, M10, M12	GND	Device Common Ground.
RF Clock J12	CLKIN+	Positive Device Clock Input. This pin is the clock input for the on-chip DAC clock multiplier, REFCLK, when the DAC PLL is on. This pin is also the clock input for the DAC sample clock or device clock (DACCLK) when the DAC PLL is off. AC couple this input. There is an internal 100 Ω resistor between this pin and CLKIN–.
H12	CLKIN–	Negative Device Clock Input.
K1	CLKOUT+	Positive Device Clock Output. This pin is the clock output of a divided down DACCLK and is available with the DAC PLL on and off. The divide down ratios are by 1, 2, or 4.
L1	CLKOUT–	Negative Device Clock Output.
System Reference H1	SYSREF+	Positive System Reference Input. It is recommended to ac couple this pin, but dc coupling is also acceptable. See Table 7 for the dc common-mode voltage.
H2	SYSREF–	Negative System Reference Input. It is recommended to ac couple this pin, but dc coupling is also acceptable. See Table 7 for the dc common-mode voltage.
On-Chip DAC PLL Loop Filter H6	FILT_FINE	On-Chip DAC Clock Multiplier and PLL Fine Loop Filter Input.
H7	FILT_COARSE	On-Chip DAC Clock Multiplier and PLL Coarse Loop Filter Input.
J7	FILT_BYP	On-Chip DAC Clock Multiplier and LDO Bypass.
K6	FILT_VCM	On-Chip DAC Clock Multiplier and VCO Common-Mode Input.
SERDES Data Bits A2	SERDIN7+	SERDES Data Bit 7, Positive.
B2	SERDIN7–	SERDES Data Bit 7, Negative.
A3	SERDIN6+	SERDES Data Bit 6, Positive.
B3	SERDIN6–	SERDES Data Bit 6, Negative.
A4	SERDIN5+	SERDES Data Bit 5, Positive.
B4	SERDIN5–	SERDES Data Bit 5, Negative.
A5	SERDIN4+	SERDES Data Bit 4, Positive.
B5	SERDIN4–	SERDES Data Bit 4, Negative.
A8	SERDIN3+	SERDES Data Bit 3, Positive.
B8	SERDIN3–	SERDES Data Bit 3, Negative.
A9	SERDIN2+	SERDES Data Bit 2, Positive.
B9	SERDIN2–	SERDES Data Bit 2, Negative.
A10	SERDIN1+	SERDES Data Bit 1, Positive.
B10	SERDIN1–	SERDES Data Bit 1, Negative.
A11	SERDIN0+	SERDES Data Bit 0, Positive.
B11	SERDIN0–	SERDES Data Bit 0, Negative.
Sync Output D12	$\overline{\text{SYNCOUT0+}}$	Positive Sync (Active Low) Output Signal, Channel Link 0. This pin is LVDS or CMOS selectable.
D11	$\overline{\text{SYNCOUT0-}}$	Negative Sync (Active Low) Output Signal, Channel Link 0. This pin is LVDS or CMOS selectable.
D1	$\overline{\text{SYNCOUT1+}}$	Positive Sync (Active Low) Output Signal, Channel Link 1. This pin is LVDS or CMOS selectable.
D2	$\overline{\text{SYNCOUT1-}}$	Negative Sync (Active Low) Output Signal, Channel Link 1. This pin is LVDS or CMOS selectable.

Pin No.	Mnemonic	Description
Serial Port Interface E4 E7 E5 E6 E8	SDO SDIO SCLK $\overline{\text{CS}}$ RESET	Serial Port Data Output (CMOS Levels with Respect to DVDD1.8). Serial Port Data Input/Output (CMOS Levels with Respect to DVDD1.8). Serial Port Clock Input (CMOS Levels with Respect to DVDD1.8). Serial Port Chip Select, Active Low (CMOS Levels with Respect to DVDD1.8). Reset, Active Low (CMOS Levels with Respect to DVDD1.8).
Interrupt Request D9 E9	$\overline{\text{IRQ0}}$ $\overline{\text{IRQ1}}$	Interrupt Request 0. This pin is an open-drain, active low output (CMOS levels with respect to DVDD1.8). Connect a pull-up resistor to DVDD1.8 to prevent this pin from floating when inactive. Interrupt Request 1. This pin is an open-drain, active low output (CMOS levels with respect to DVDD1.8). Connect a pull-up resistor to DVDD1.8 to prevent this pin from floating when inactive.
CMOS Input/Outputs D8 D4	TXEN0 TXEN1	Transmit Enable for DAC0. The CMOS levels are determined with respect to DVDD1.8. Transmit Enable for DAC1. The CMOS levels are determined with respect to DVDD1.8.
DAC Analog Outputs M9 M8 M4 M5	DAC0+ DAC0- DAC1+ DAC1-	DAC0 Positive Current Output. DAC0 Negative Current Output. DAC1 Positive Current Output. DAC1 Negative Current Output.
Reference L12	ISET	Device Bias Current Setting Pin. Connect a 5 k Ω resistor, preferably with 0.1% tolerance and ± 25 ppm/ $^{\circ}\text{C}$ to this pin.
Do Not Connect E1, E2, E11, E12, J2, K4	DNC	Do Not Connect. Do not connect to these pins.

TYPICAL PERFORMANCE CHARACTERISTICS

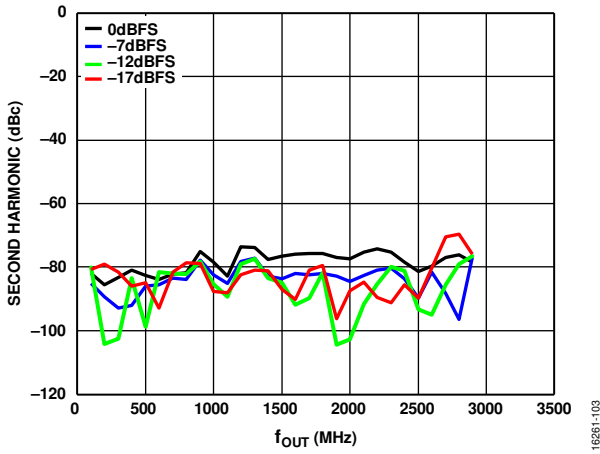


Figure 3. Second Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2x, Main Interpolation 8x

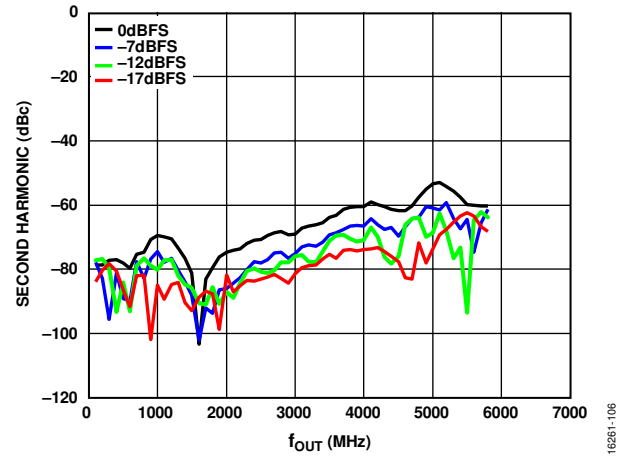


Figure 6. Second Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 1), 12 GHz DAC Sample Rate, Channel Interpolation 4x, Main Interpolation 8x

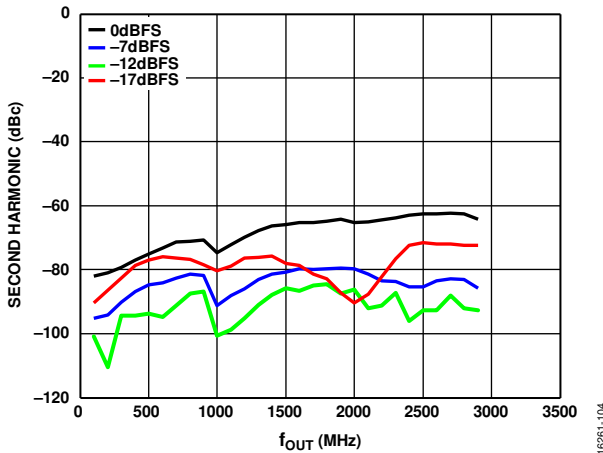


Figure 4. Third Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2x, Main Interpolation 8x

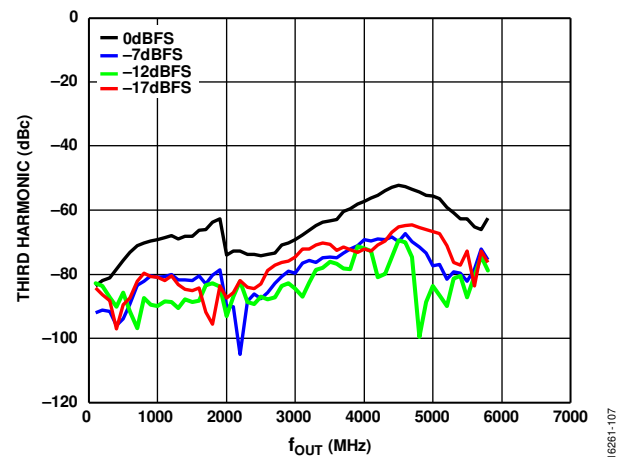


Figure 7. Third Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 1), 12 GHz DAC Sample Rate, Channel Interpolation 4x, Main Interpolation 8x

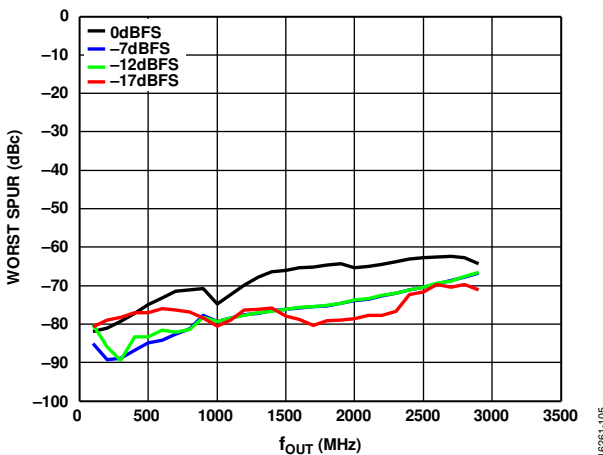


Figure 5. Worst Spur (dBc) vs. f_{OUT} over Digital Scale (Mode 0), 6 GHz DAC Sample Rate, Channel Interpolation 2x, Main Interpolation 8x

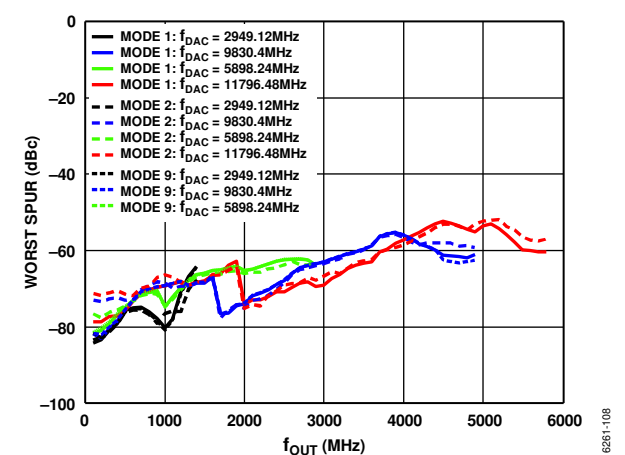


Figure 8. Worst Spur (dBc) vs. f_{OUT} over f_{DAC} (All Modes), 0 dB Digital Scale

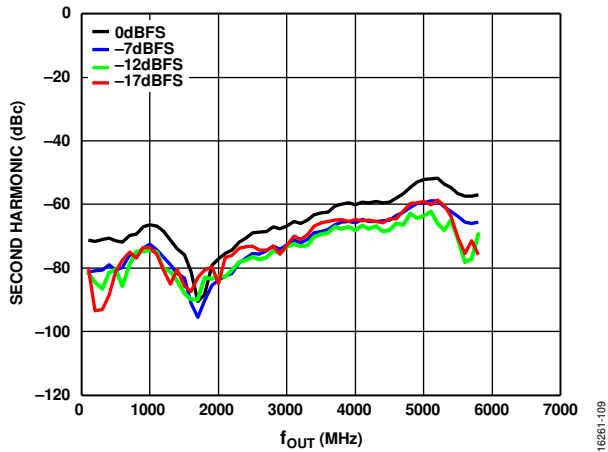


Figure 9. Second Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4x, Main Interpolation 8x

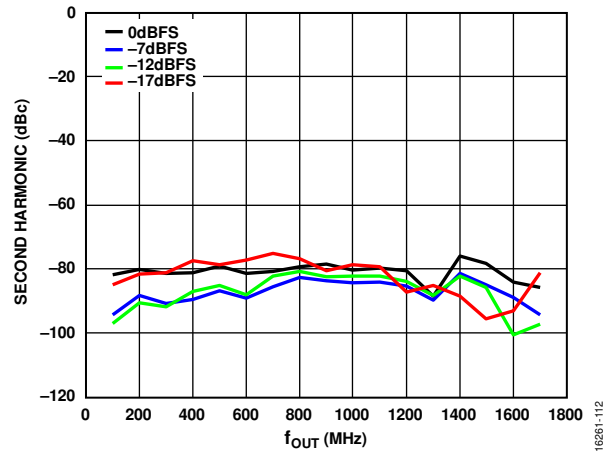


Figure 12. Second Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 17), 3.4 GHz DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 1x, 11-Bit Resolution

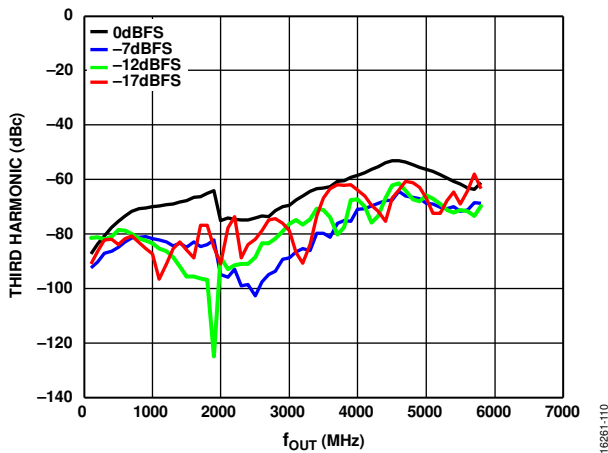


Figure 10. Third Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4x, Main Interpolation 8x

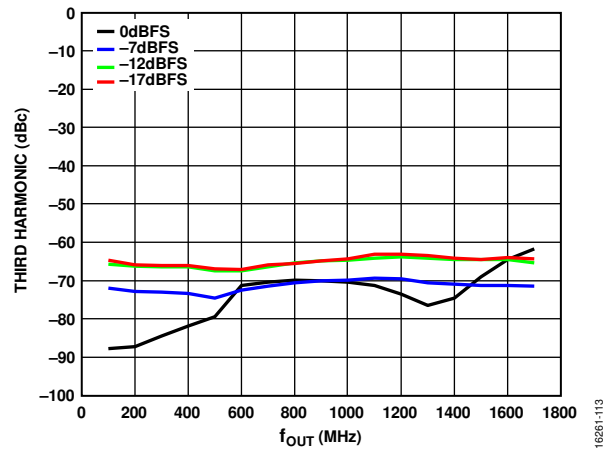


Figure 13. Third Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 17), 3.4 GHz DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 1x, 11-Bit Resolution

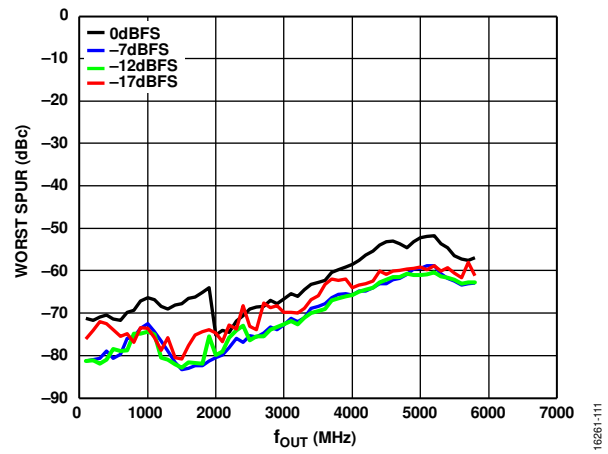


Figure 11. Worst Spur (dBc) vs. f_{OUT} over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4x, Main Interpolation 8x

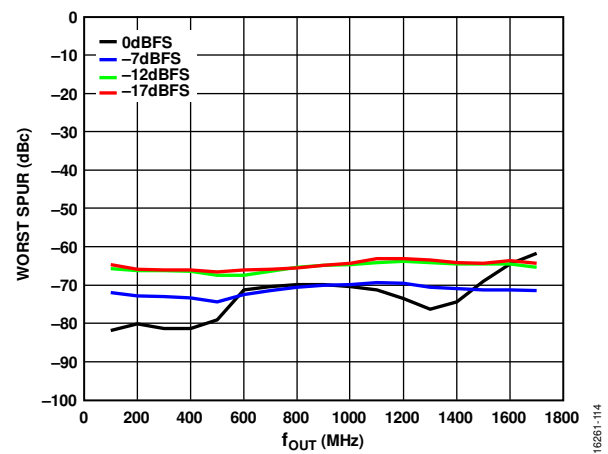


Figure 14. Worst Spur (dBc) vs. f_{OUT} over Digital Scale (Mode 17), 3.4 GHz DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 1x, 11-Bit Resolution

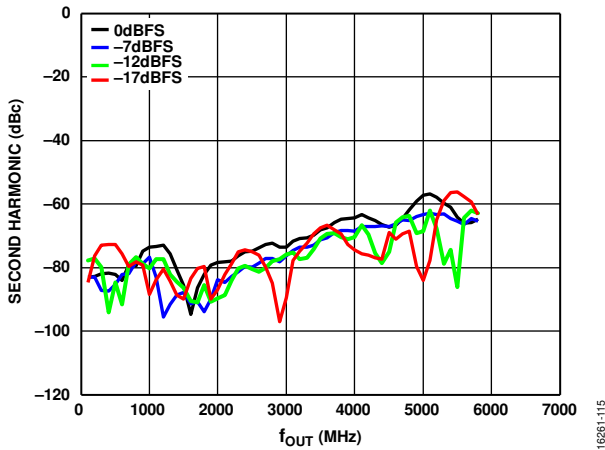


Figure 15. Second Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 9), 12 GHz DAC Sample Rate, Channel Interpolation 1 \times , Main Interpolation 12 \times

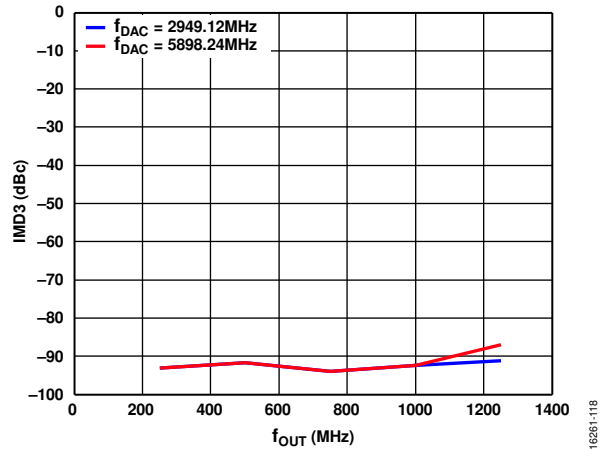


Figure 18. IMD3 vs. f_{OUT} over f_{DAC} (Mode 0), Channel Interpolation 2 \times , Main Interpolation 8 \times , 1 MHz Tone Spacing

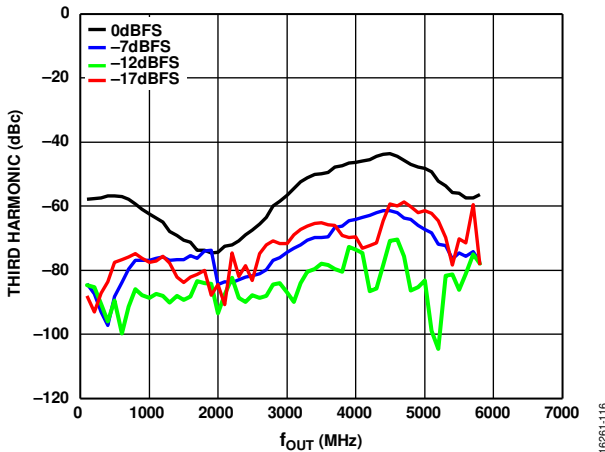


Figure 16. Third Harmonic (dBc) vs. f_{OUT} over Digital Scale (Mode 9), 12 GHz DAC Sample Rate, Channel Interpolation 1 \times , Main Interpolation 12 \times

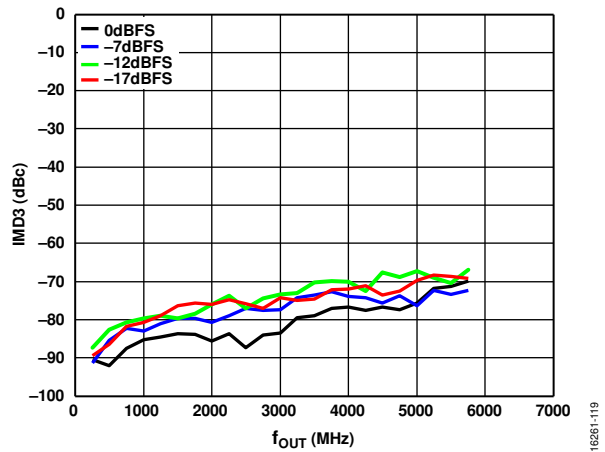


Figure 19. IMD3 vs. f_{OUT} over Digital Scale (Mode 1), 12 GHz DAC Sample Rate, Channel Interpolation 4 \times , Main Interpolation 8 \times , 1 MHz Tone Spacing

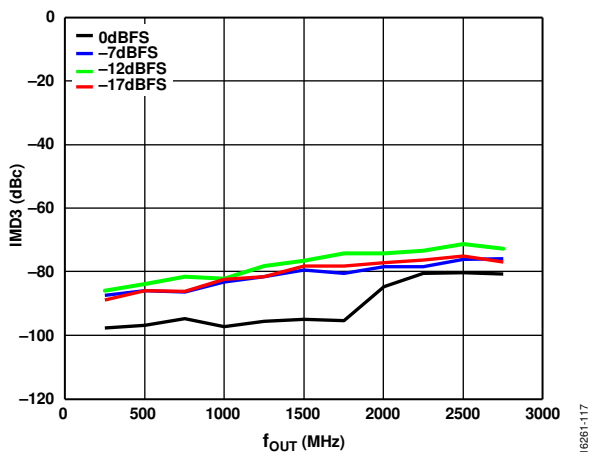


Figure 17. IMD3 vs. f_{OUT} over Digital Scale (Mode 0) 6 GHz DAC Sample Rate, Channel Interpolation 2 \times , Main Interpolation 8 \times , 1 MHz Tone Spacing

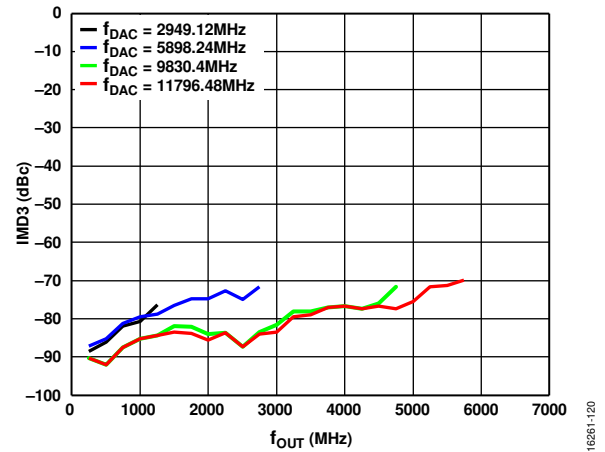


Figure 20. IMD3 vs. f_{OUT} over f_{DAC} (Mode 1), Channel Interpolation 4 \times , Main Interpolation 8 \times , 1 MHz Tone Spacing, -7 dB Digital Scale

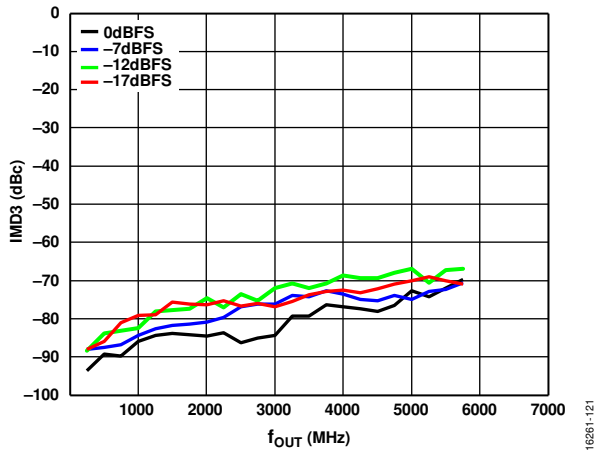


Figure 21. IMD3 vs. f_{OUT} over Digital Scale (Mode 2), 12 GHz DAC Sample Rate, Channel Interpolation 4x, Main Interpolation 8x, 1 MHz Tone Spacing

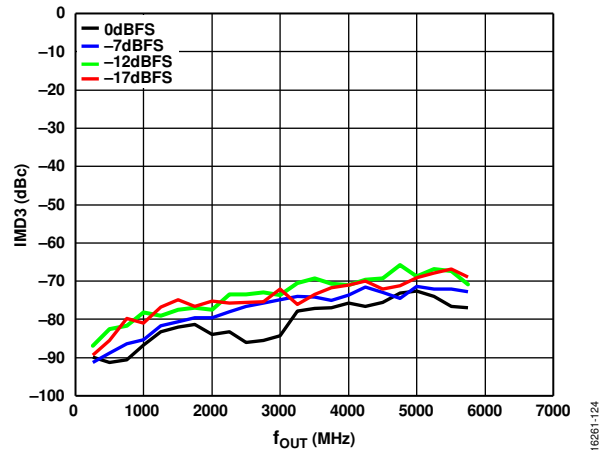


Figure 24. IMD3 vs. f_{OUT} over Digital Scale (Mode 9), 12 GHz DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 12x, 1 MHz Tone Spacing

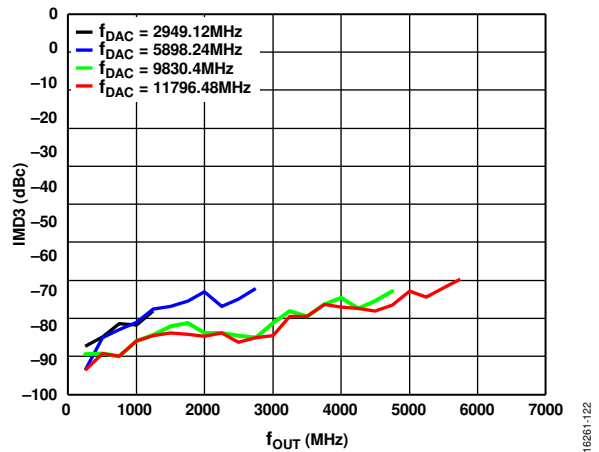


Figure 22. IMD3 vs. f_{OUT} over f_{DAC} (Mode 2), Channel Interpolation 4x, Main Interpolation 8x, 1 MHz Tone Spacing

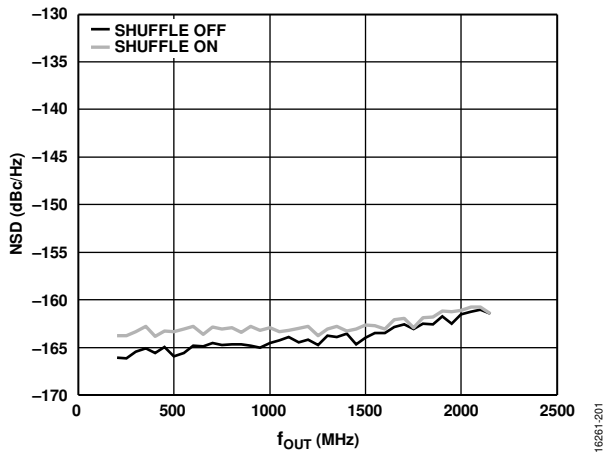


Figure 25. Single-Tone NSD Measured at 70 MHz vs. f_{OUT} , 11796.48 MHz f_{DAC} , 16-Bit Resolution, Shuffle Off vs. Shuffle On

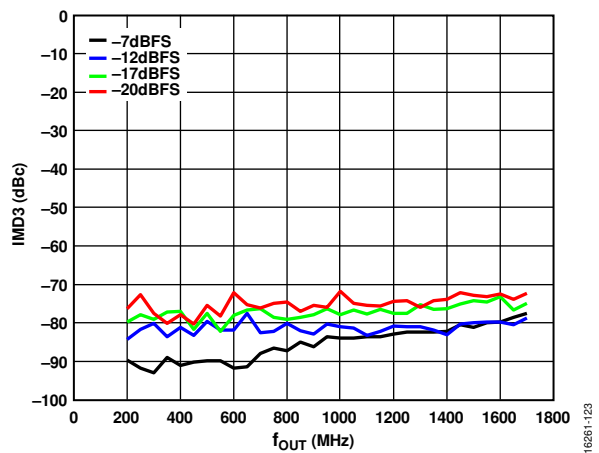


Figure 23. IMD3 vs. f_{OUT} over Digital Scale (Mode 17), 3.4 GHz DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 1x, 1 MHz Tone Spacing, 11-Bit Resolution

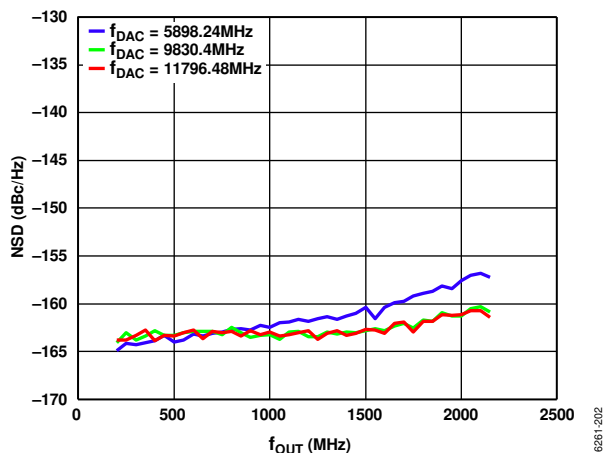


Figure 26. Single-Tone NSD Measured at 70 MHz vs. f_{OUT} over f_{DAC} , 16-Bit Resolution, Shuffle On

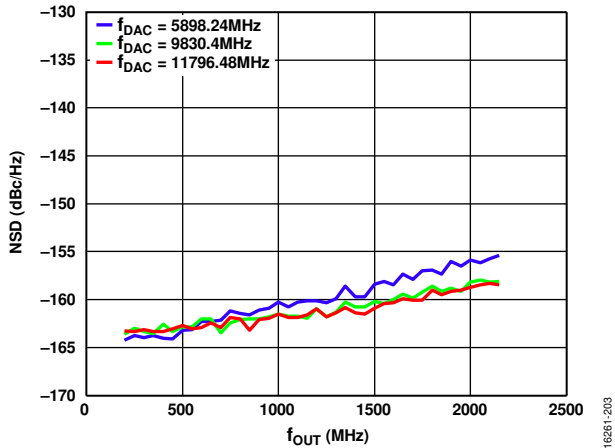


Figure 27. Single-Tone NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT} over f_{DAC} , 16-Bit Resolution, Shuffle On

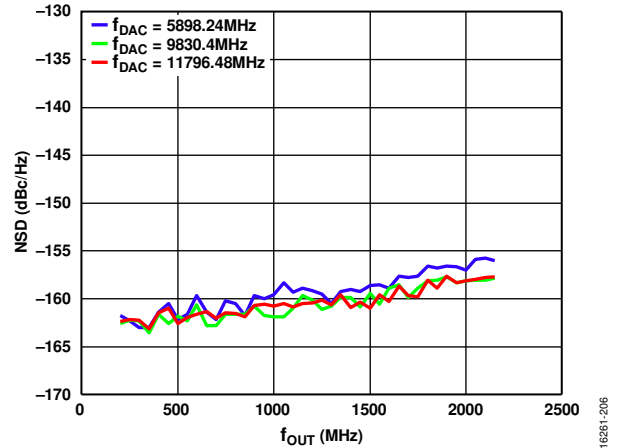


Figure 30. Single-Tone NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT} over f_{DAC} , 12-Bit Resolution, Shuffle On

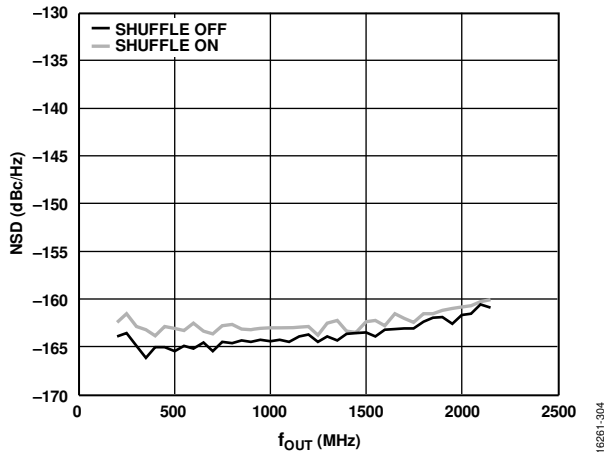


Figure 28. Single-Tone NSD Measured at 70 MHz vs. f_{OUT} , 11796.48 MHz f_{DAC} , 12-Bit Resolution, Shuffle Off vs. Shuffle On

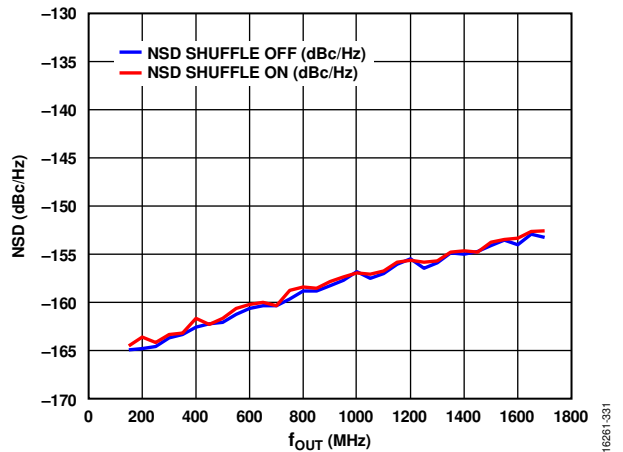


Figure 31. Single-Tone NSD Measured at 70 MHz vs. f_{OUT} , 3.4 GHz f_{DAC} , 11-Bit Resolution, Shuffle Off vs. Shuffle On

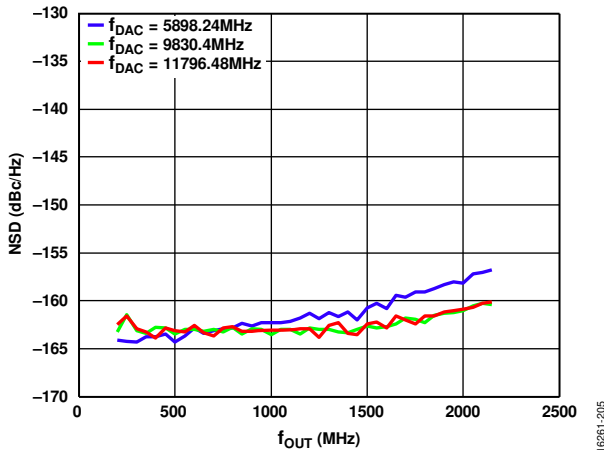


Figure 29. Single-Tone NSD Measured at 70 MHz vs. f_{OUT} over f_{DAC} , 12-Bit Resolution, Shuffle On

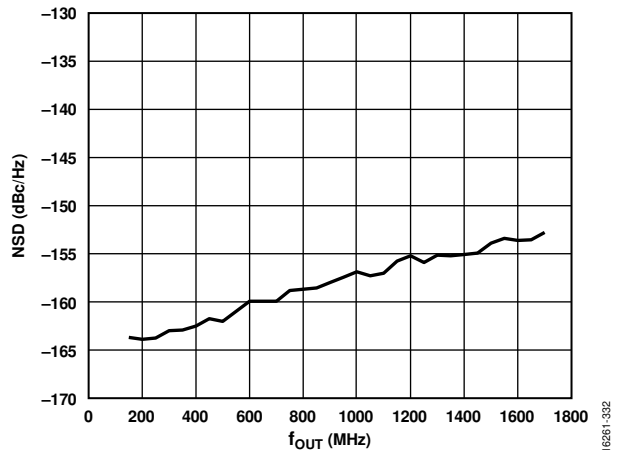


Figure 32. Single-Tone NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT} , 3.4GHz f_{DAC} , 11-Bit Resolution, Shuffle On

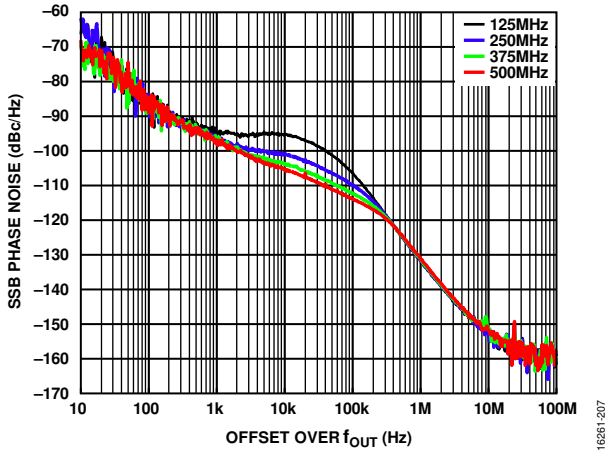


Figure 33. Single-Sideband (SSB) Phase Noise vs. Offset over f_{OUT} , over PFD Frequency, $f_{DAC} = 12\text{ GHz}$, $f_{OUT} = 1.8\text{ GHz}$, PLL On, PLL Reference Clock = 500 MHz

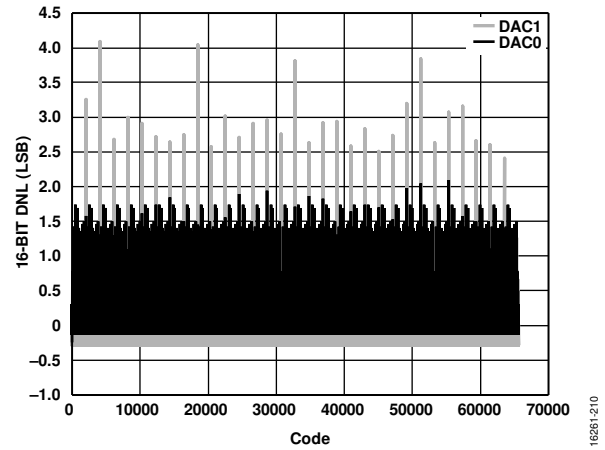


Figure 36. DNL, $I_{OUTFS} = 20\text{ mA}$, 16-Bit Resolution

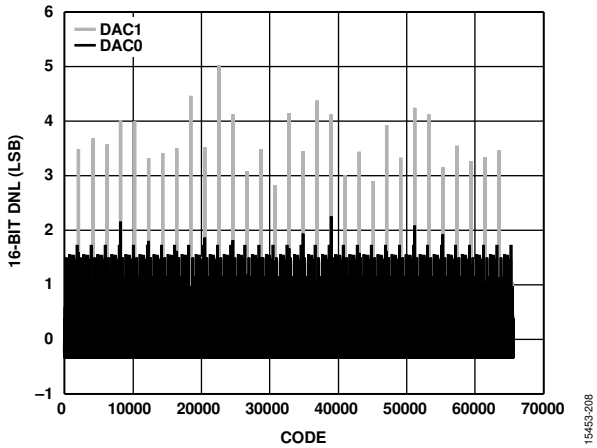


Figure 34. DNL, $I_{OUTFS} = 26\text{ mA}$, 16-Bit Resolution

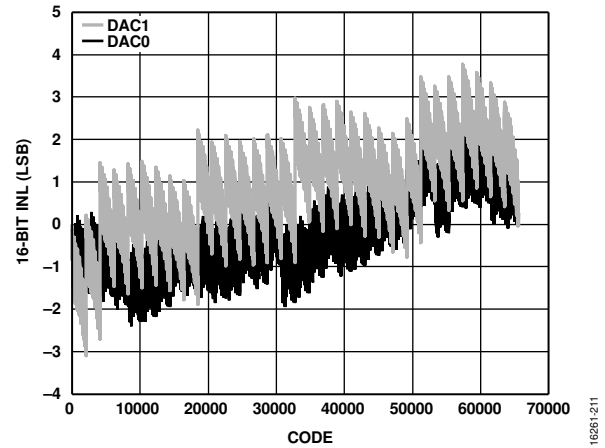


Figure 37. INL, $I_{OUTFS} = 20\text{ mA}$, 16-Bit Resolution

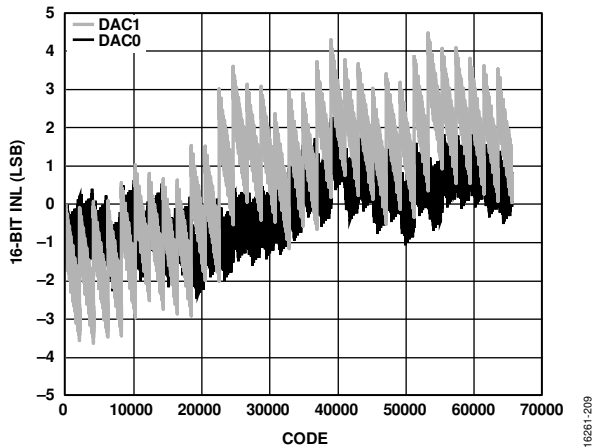


Figure 35. INL, $I_{OUTFS} = 26\text{ mA}$, 16-Bit Resolution

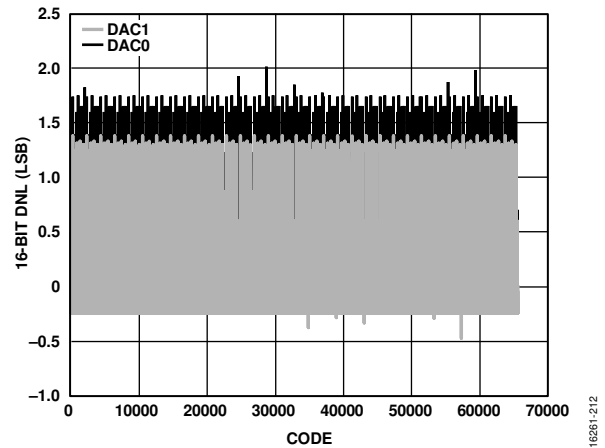


Figure 38. DNL, $I_{OUTFS} = 15.6\text{ mA}$, 16-Bit Resolution

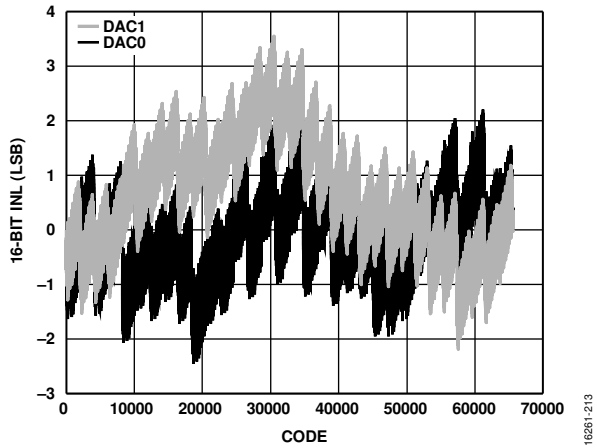


Figure 39. INL, $I_{OUTFS} = 15.6 \text{ mA}$, 16-Bit Resolution

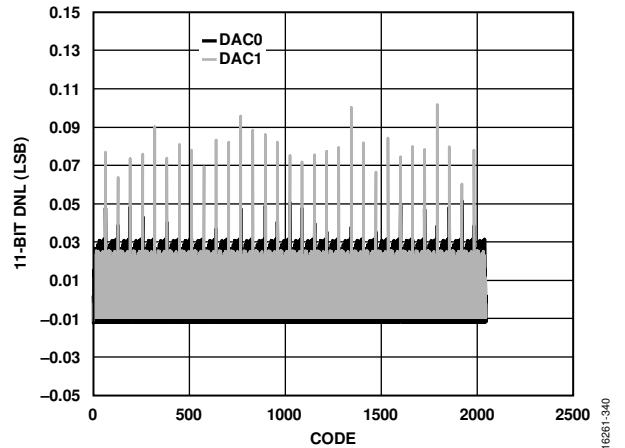


Figure 42. DNL, $I_{OUTFS} = 20 \text{ mA}$, 11-Bit Resolution

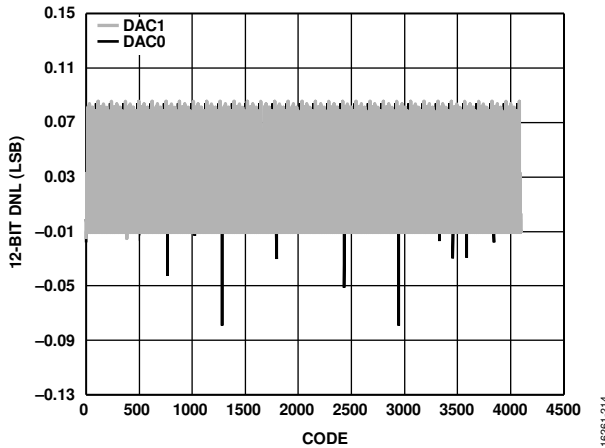


Figure 40. DNL, $I_{OUTFS} = 20 \text{ mA}$, 12-Bit Resolution

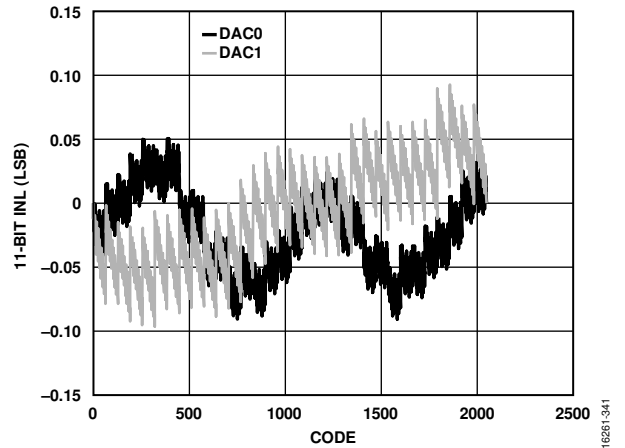


Figure 43. INL, $I_{OUTFS} = 20 \text{ mA}$, 11-Bit Resolution

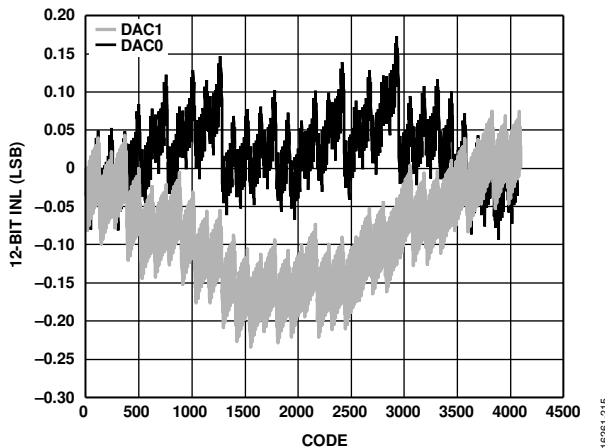


Figure 41. INL, $I_{OUTFS} = 20 \text{ mA}$, 12-Bit Resolution

TERMINOLOGY

Integral Nonlinearity (INL)

INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)

DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error

Offset error is the deviation of the output current from the ideal value of 0 mA. For DACx+, a 0 mA output is expected when all inputs are set to 0. For DACx-, a 0 mA output is expected when all inputs are set to 1.

Gain Error

Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when the input is at its minimum code and the output when the input is at its maximum code.

Output Compliance Range

The output compliance range is the range of allowable voltages at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift

Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX} . For offset and gain drift, the drift is reported in parts per million of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in parts per million per degrees Celsius.

Settling Time

Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter

If the digital inputs to the DAC are sampled at a multiple rate of the interpolation rate (f_{DATA}), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around the output data rate (f_{DAC}) can be greatly suppressed.

Channel Datapath

The channel datapaths, sometimes referred to as channelizers, are the complex data channel datapaths, before the summing node in the chip, that can be used or bypassed depending on the mode of operation chosen. When these channelizers are in use, complex data input is required. The channel datapaths include independently controlled optional gain stages and channel NCOs per channel. There is also a selectable channel interpolation block that is configurable (same setting for all channel interpolation blocks) depending on the mode of operation chosen.

Main Datapath

The main datapath refers to the portion of the digital datapath after the summing node in the chip, up to each of the main DAC analog cores. Each of these main datapaths includes an optional PA protection block with a feed forward to the ramp up/down gain stage block for muting the DAC outputs before damaging a power amplifier in the transmit path. There is a selectable main interpolation block that is configurable (same setting for both main interpolation blocks) depending on the mode of operation chosen. Each main datapath also contains an individually programmable main NCO per main DAC datapath that can be optionally used depending on the mode of operation.

Adjacent Channel Leakage Ratio (ACLR)

ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Adjusted DAC Update Rate

The adjusted DAC update rate is the DAC update rate divided by the smallest interpolating factor. For clarity on DACs with multiple interpolating factors, the adjusted DAC update rate for each interpolating factor may be given.

Physical (PHY) Lane

Physical Lane x refers to SERDINx±.

Logical Lane

Logical Lane x refers to physical lanes after optionally being remapped by the crossbar block (Register 0x308 to Register 0x30B).

Link Lane

Link Lane x refers to logical lanes considered per link. When paging Link 0 (Register 0x300, Bit 2 = 0), Link Lane x = Logical Lane x. When paging Link 1 (Register 0x300, Bit 2 = 1, dual link only), Link Lane x = Logical Lane x + 4.

THEORY OF OPERATION

The AD9173 is a 16-bit, dual RF DAC with a high speed JESD204B SERDES interface, compliant with Subclass 0 and Subclass 1 operation. Figure 1 shows a functional block diagram of the AD9173. Each DAC core has three individually bypassable channelizers that support up to 1.54 GSPS of complex data rate input per channel. Eight high speed serial lanes carry data at a maximum of 15.4 Gbps to the channel datapaths. The JESD204B interface supports both single-link and dual-link modes of operation, depending on the selected mode configuration. Compared to either LVDS or CMOS interfaces, the SERDES interface simplifies pin count, board layout, and input clock requirements to the device.

The clock for the input data is derived from the DAC clock, or device clock (required by the JESD204B specification). This device clock can be sourced with a PLL reference clock used by the on-chip PLL to generate a DAC clock, or a high fidelity, direct external DAC sampling clock. The device can be configured to operate in one-, two-, three-, four-, or eight-lane per link modes, depending on the required input data rate.

The digital datapath of the AD9173 offers bypassable (1×) interpolation modes for both the channel datapaths and the main datapaths. Additionally, depending on the selected mode, there are also 2×, 3×, 4×, 6×, and 8× interpolation options for the channel datapaths, and 2×, 4×, 6×, 8×, and 12× interpolation options for the main datapaths. See Table 13 for a summary of the various JESD204B modes available, as well as the respective interpolation options.

For each of the channel digital datapaths (when not using 1× interpolation for the channel), there are individually programmable gain stages and NCO blocks available. The NCO blocks have a 48-bit modulus NCO option to enable digital frequency shifts of signals with near infinite precision.

The NCO can operate alone in NCO only mode using a programmable dc value input via the SPI or with digital data from the SERDES interface and digital datapath. At the end of the three channelizer datapaths, a summation node combines the three channel datapaths together at a maximum of 1.54 GSPS to then pass along to each of the main DAC datapaths for further digital feature options.

Each of the main DAC datapaths contain an optional power amplifier (PA) protection block, a main datapath interpolation block, a main NCO with an optional modulus feature, and a ramp-up/ramp-down gain block that is fed by the PA protection block. Additionally, there is an optional calibration tone feature, as well as four modulator switch modes that are part of the main NCO block.

The AD9173 is capable of multichip synchronization that can both synchronize multiple DACs and establish a constant and deterministic latency (latency locking) path for the DACs. The latency for each of the DACs remains constant to within several DAC clock cycles from link establishment to link establishment. An external alignment signal (SYSREF±) makes the AD9173 JESD204B Subclass 1 compliant. Several modes of SYSREF± signal handling are available for use in the system.

An SPI configures the various functional blocks and monitors their statuses. The various functional blocks and the data interface must be set up in a specific sequence for proper operation (see the Start-Up Sequence section). Simple SPI initialization routines set up the JESD204B link and are included in the evaluation board software support.

This data sheet describes the various blocks of the AD9173 in detail. Descriptions of the JESD204B interface, control parameters, and various registers to set up and monitor the device are provided. The recommended start-up routine reliably sets up the data link.