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FEATURES

- 8 analog-to-digital converters (ADCs) integrated into 1 package**
- 100 mW ADC power per channel at 65 MSPS**
- SNR = 60.8 dB (to Nyquist)**
- ENOB = 9.8 bits**
- SFDR = 80 dBc (to Nyquist)**
- Excellent linearity**
 - DNL = ±0.3 LSB (typical); INL = ±0.4 LSB (typical)**
- Serial LVDS (ANSI-644, default)**
- Low power, reduced signal option (similar to IEEE 1596.3)**
- Data and frame clock outputs**
- 325 MHz, full-power analog bandwidth**
- 2 V p-p input voltage range**
- 1.8 V supply operation**
- Serial port control**
 - Full-chip and individual-channel power-down modes**
 - Flexible bit orientation**
 - Built-in and custom digital test pattern generation**
 - Programmable clock and data alignment**
 - Programmable output resolution**
 - Standby mode**

APPLICATIONS

- Medical imaging and nondestructive ultrasound**
- Portable ultrasound and digital beam-forming systems**
- Quadrature radio receivers**
- Diversity radio receivers**
- Tape drives**
- Optical networking**
- Test equipment**

GENERAL DESCRIPTION

The AD9212 is an octal, 10-bit, 40 MSPS/65 MSPS ADC with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. Operating at a conversion rate of up to 65 MSPS, it is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock (DCO) for capturing data on the output and a frame clock (FCO) for signaling a new output byte are provided. Individual channel power-down is supported and typically consumes less than 2 mW when all channels are disabled.

Rev. E

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FUNCTIONAL BLOCK DIAGRAM

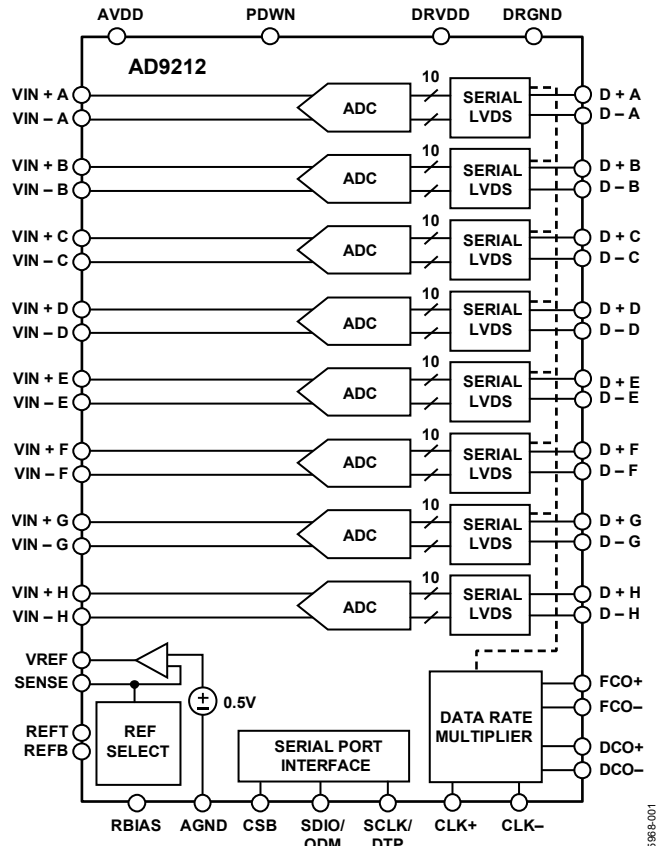


Figure 1.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9212 is available in a RoHS-compliant, 64-lead LFCSP. It is specified over the industrial temperature range of -40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Small Footprint. Eight ADCs are contained in a small package.
2. Low Power of 100 mW per Channel at 65 MSPS.
3. Ease of Use. A data clock output (DCO) operates up to 300 MHz and supports double data rate (DDR) operation.
4. User Flexibility. SPI control offers a wide range of flexible features to meet specific system requirements.
5. Pin-Compatible Family. This includes the [AD9222](#) (12-bit) and [AD9252](#) (14-bit).

AD9212* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9212 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9212: Octal, 10-Bit, 40 MSPS/65 MSPS, Serial LVDS, 1.8 V ADC Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog
- AD9212 IBIS Models

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9212 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9212 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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Added Endnote 2 in Ordering Guide	56

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10/06—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -0.5 dBFS, unless otherwise noted.

Table 1.

Parameter ¹	Temperature	AD9212-40			AD9212-65			Unit
		Min	Typ	Max	Min	Typ	Max	
RESOLUTION		10			10			Bits
ACCURACY		Guaranteed			Guaranteed			
No Missing Codes	Full	Guaranteed			Guaranteed			
Offset Error	Full	±1.5		±8	±1.5		±8	mV
Offset Matching	Full	±3		±8	±3		±8	mV
Gain Error	Full	±0.4		±1.2	±3.2		±4.3	% FS
Gain Matching	Full	±0.3		±0.7	±0.4		±0.9	% FS
Differential Nonlinearity (DNL)	Full	±0.1		±0.4	±0.3		±0.65	LSB
Integral Nonlinearity (INL)	Full	±0.15		±0.5	±0.4		±1	LSB
TEMPERATURE DRIFT								
Offset Error	Full	±2			±2			ppm/°C
Gain Error	Full	±17			±17			ppm/°C
Reference Voltage (1 V Mode)	Full	±21			±21			ppm/°C
REFERENCE								
Output Voltage Error (VREF = 1 V)	Full	±2		±30	±2		±30	mV
Load Regulation @ 1.0 mA (VREF = 1 V)	Full	3			3			mV
Input Resistance	Full	6			6			kΩ
ANALOG INPUTS								
Differential Input Voltage Range (VREF = 1 V)	Full	2			2			V p-p
Common-Mode Voltage	Full	AVDD/2			AVDD/2			V
Differential Input Capacitance	Full	7			7			pF
Analog Bandwidth, Full Power	Full	325			325			MHz
POWER SUPPLY								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
IAVDD	Full		252	260		390	405	mA
IDRVDD	Full		49.5	53		54	58	mA
Total Power Dissipation (Including Output Drivers)	Full		542	560		800	833	mW
Power-Down Dissipation	Full		3	11		3	11	mW
Standby Dissipation ²	Full		83			95		mW
CROSSTALK								
AIN = -0.5 dBFS	Full		-90			-90		dB
Overrange ³	Full		-90			-90		dB

¹ See the [AN-835 Application Note, Understanding High Speed ADC Testing and Evaluation](#), for a complete set of definitions and how these tests were completed.

² Can be controlled via the SPI.

³ Overrange condition is specific with 6 dB of the full-scale input range.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -0.5 dBFS, unless otherwise noted.

Table 2.

Parameter ¹	Temperature	AD9212-40			AD9212-65			Unit
		Min	Typ	Max	Min	Typ	Max	
SIGNAL-TO-NOISE RATIO (SNR)								
$f_{IN} = 2.4$ MHz	Full		61.2		60.8			dB
$f_{IN} = 19.7$ MHz	Full	60.2	61.2		60.8			dB
$f_{IN} = 35$ MHz	Full		61.2		58.5	60.8		dB
$f_{IN} = 70$ MHz	Full		61.0		60.7			dB
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)								
$f_{IN} = 2.4$ MHz	Full		61.2		60.7			dB
$f_{IN} = 19.7$ MHz	Full	60.0	61.0		60.6			dB
$f_{IN} = 35$ MHz	Full		61.0		57.0	60.5		dB
$f_{IN} = 70$ MHz	Full		60.8		60.4			dB
EFFECTIVE NUMBER OF BITS (ENOB)								
$f_{IN} = 2.4$ MHz	Full		9.87		9.81			Bits
$f_{IN} = 19.7$ MHz	Full	9.71	9.87		9.81			Bits
$f_{IN} = 35$ MHz	Full		9.87		9.43	9.81		Bits
$f_{IN} = 70$ MHz	Full		9.84		9.79			Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
$f_{IN} = 2.4$ MHz	Full		87		81			dBc
$f_{IN} = 19.7$ MHz	Full	72	85		79			dBc
$f_{IN} = 35$ MHz	Full		79		62	77		dBc
$f_{IN} = 35$ MHz	25°C				69	77		dBc
$f_{IN} = 70$ MHz	Full		74		72			dBc
WORST HARMONIC (SECOND OR THIRD)								
$f_{IN} = 2.4$ MHz	Full		-87		-81			dBc
$f_{IN} = 19.7$ MHz	Full		-85	-72	-79			dBc
$f_{IN} = 35$ MHz	Full		-79		-77	-62		dBc
$f_{IN} = 35$ MHz	25°C				-77	-69		dBc
$f_{IN} = 70$ MHz	Full		-74		-72			dBc
WORST OTHER (EXCLUDING SECOND OR THIRD)								
$f_{IN} = 2.4$ MHz	Full		-90		-86			dBc
$f_{IN} = 19.7$ MHz	Full		-85	-72	-86			dBc
$f_{IN} = 35$ MHz	Full		-85		-85	-70		dBc
$f_{IN} = 70$ MHz	Full		-85		-85			dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)— AIN1 AND AIN2 = -7.0 dBFS								
$f_{IN1} = 15$ MHz, $f_{IN2} = 16$ MHz	25°C		80.0		77.0			dBc
$f_{IN1} = 70$ MHz, $f_{IN2} = 71$ MHz	25°C		77.0		77.0			dBc

¹ See the [AN-835 Application Note](#), *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -0.5 dBFS, unless otherwise noted.

Table 3.

Parameter ¹	Temperature	AD9212-40			AD9212-65			Unit
		Min	Typ	Max	Min	Typ	Max	
CLOCK INPUTS (CLK+, CLK-)		CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL			
Logic Compliance								
Differential Input Voltage ²	Full	250			250			mV p-p
Input Common-Mode Voltage	Full		1.2			1.2		V
Input Resistance (Differential)	25°C		20			20		kΩ
Input Capacitance	25°C		1.5			1.5		pF
LOGIC INPUTS (PDWN, SCLK/DTP)								
Logic 1 Voltage	Full	1.2		3.6	1.2		3.6	V
Logic 0 Voltage	Full	0		0.3			0.3	V
Input Resistance	25°C		30			30		kΩ
Input Capacitance	25°C		0.5			0.5		pF
LOGIC INPUT (CSB)								
Logic 1 Voltage	Full	1.2		3.6	1.2		3.6	V
Logic 0 Voltage	Full	0		0.3			0.3	V
Input Resistance	25°C		70			70		kΩ
Input Capacitance	25°C		0.5			0.5		pF
LOGIC INPUT (SDIO/ODM)								
Logic 1 Voltage	Full	1.2		DRVDD + 0.3	1.2		DRVDD + 0.3	V
Logic 0 Voltage	Full	0		0.3	0		0.3	V
Input Resistance	25°C		30			30		kΩ
Input Capacitance	25°C		2			2		pF
LOGIC OUTPUT (SDIO/ODM) ³								
Logic 1 Voltage (I _{OH} = 800 μA)	Full	1.79			1.79			V
Logic 0 Voltage (I _{OL} = 50 μA)	Full			0.05			0.05	V
DIGITAL OUTPUTS (D + x, D - x), (ANSI-644)								
Logic Compliance		LVDS			LVDS			
Differential Output Voltage (V _{OD})	Full	247		454	247		454	mV
Output Offset Voltage (V _{OS})	Full	1.125		1.375	1.125		1.375	V
Output Coding (Default)		Offset binary			Offset binary			
DIGITAL OUTPUTS (D + x, D - x), (LOW POWER, REDUCED SIGNAL OPTION)								
Logic Compliance		LVDS			LVDS			
Differential Output Voltage (V _{OD})	Full	150		250	150		250	mV
Output Offset Voltage (V _{OS})	Full	1.10		1.30	1.10		1.30	V
Output Coding (Default)		Offset binary			Offset binary			

¹ See the [AN-835 Application Note, Understanding High Speed ADC Testing and Evaluation](#), for a complete set of definitions and how these tests were completed.

² This is specified for LVDS and LVPECL only.

³ This is specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -0.5 dBFS, unless otherwise noted.

Table 4.

Parameter ¹	Temp	AD9212-40			AD9212-65			Unit
		Min	Typ	Max	Min	Typ	Max	
CLOCK²								
Maximum Clock Rate	Full	40			65			MSPS
Minimum Clock Rate	Full			10			10	MSPS
Clock Pulse Width High (t _{EH})	Full		12.5			7.7		ns
Clock Pulse Width Low (t _{EL})	Full		12.5			7.7		ns
OUTPUT PARAMETERS^{2,3}								
Propagation Delay (t _{PD})	Full	1.5	2.3	3.1	1.5	2.3	3.1	ns
Rise Time (t _r) (20% to 80%)	Full		300			300		ps
Fall Time (t _f) (20% to 80%)	Full		300			300		ps
FCO Propagation Delay (t _{FCO})	Full	1.5	2.3	3.1	1.5	2.3	3.1	ns
DCO Propagation Delay (t _{CPD}) ⁴	Full		t _{FCO} + (t _{SAMPLE/20})			t _{FCO} + (t _{SAMPLE/20})		ns
DCO to Data Delay (t _{DATA}) ⁴	Full	(t _{SAMPLE/20}) - 300	(t _{SAMPLE/20})	(t _{SAMPLE/20}) + 300	(t _{SAMPLE/20}) - 300	(t _{SAMPLE/20})	(t _{SAMPLE/20}) + 300	ps
DCO to FCO Delay (t _{FRAME}) ⁴	Full	(t _{SAMPLE/20}) - 300	(t _{SAMPLE/20})	(t _{SAMPLE/20}) + 300	(t _{SAMPLE/20}) - 300	(t _{SAMPLE/20})	(t _{SAMPLE/20}) + 300	ps
Data-to-Data Skew (t _{DATA-MAX} - t _{DATA-MIN})	Full		±50	±200		±50	±200	ps
Wake-Up Time (Standby)	25°C		600			600		ns
Wake-Up Time (Power-Down)	25°C		375			375		μs
Pipeline Latency	Full		8			8		CLK cycles
APERTURE								
Aperture Delay (t _A)	25°C		750			750		ps
Aperture Uncertainty (Jitter)	25°C		<1			<1		ps rms
Out-of-Range Recovery Time	25°C		1			1		CLK cycles

¹ See the [AN-835 Application Note](#), *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.

² Can be adjusted via the SPI interface.

³ Measurements were made using a part soldered to FR-4 material.

⁴ t_{SAMPLE/20} is based on the number of bits divided by 2 because the delays are based on half duty cycles.

TIMING DIAGRAMS

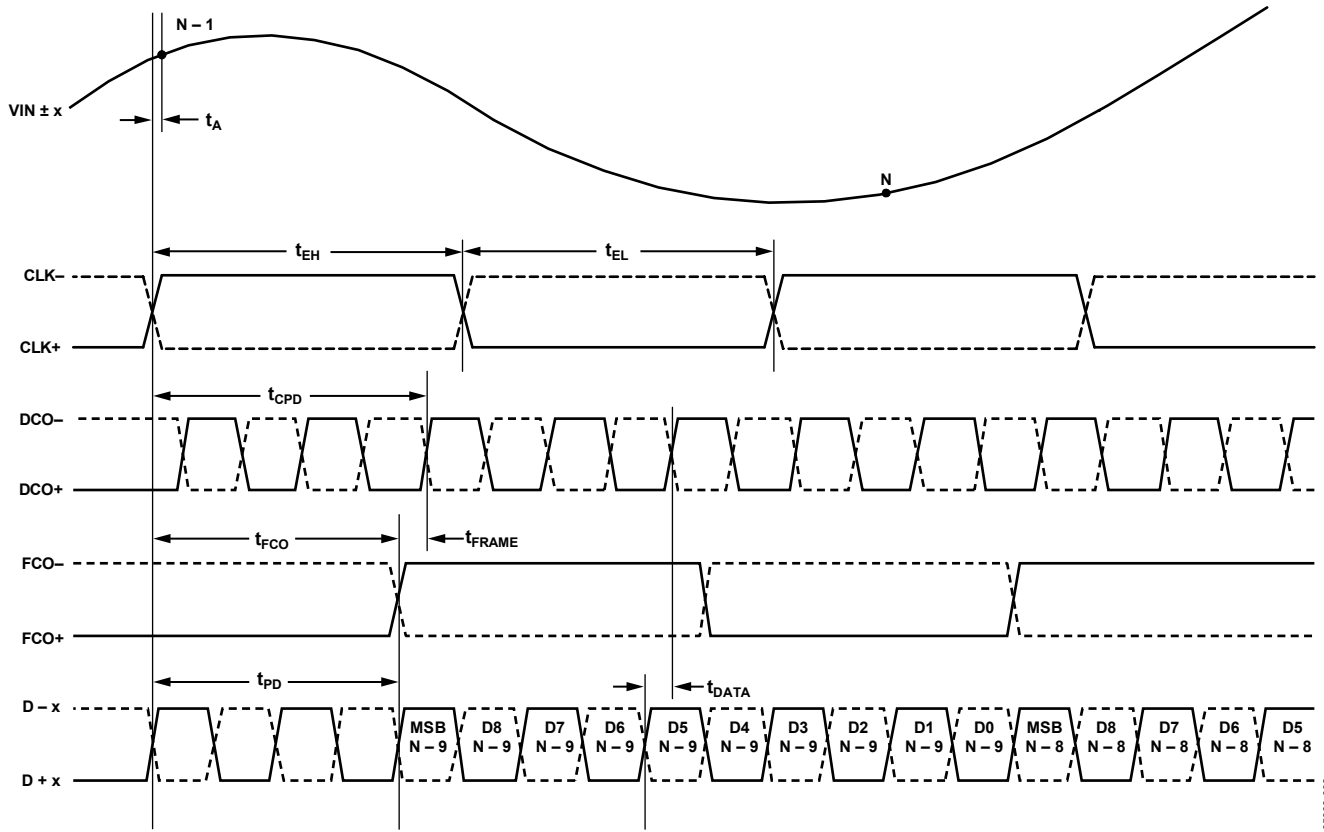


Figure 2. 10-Bit Data Serial Stream (Default), MSB First

0596B-002

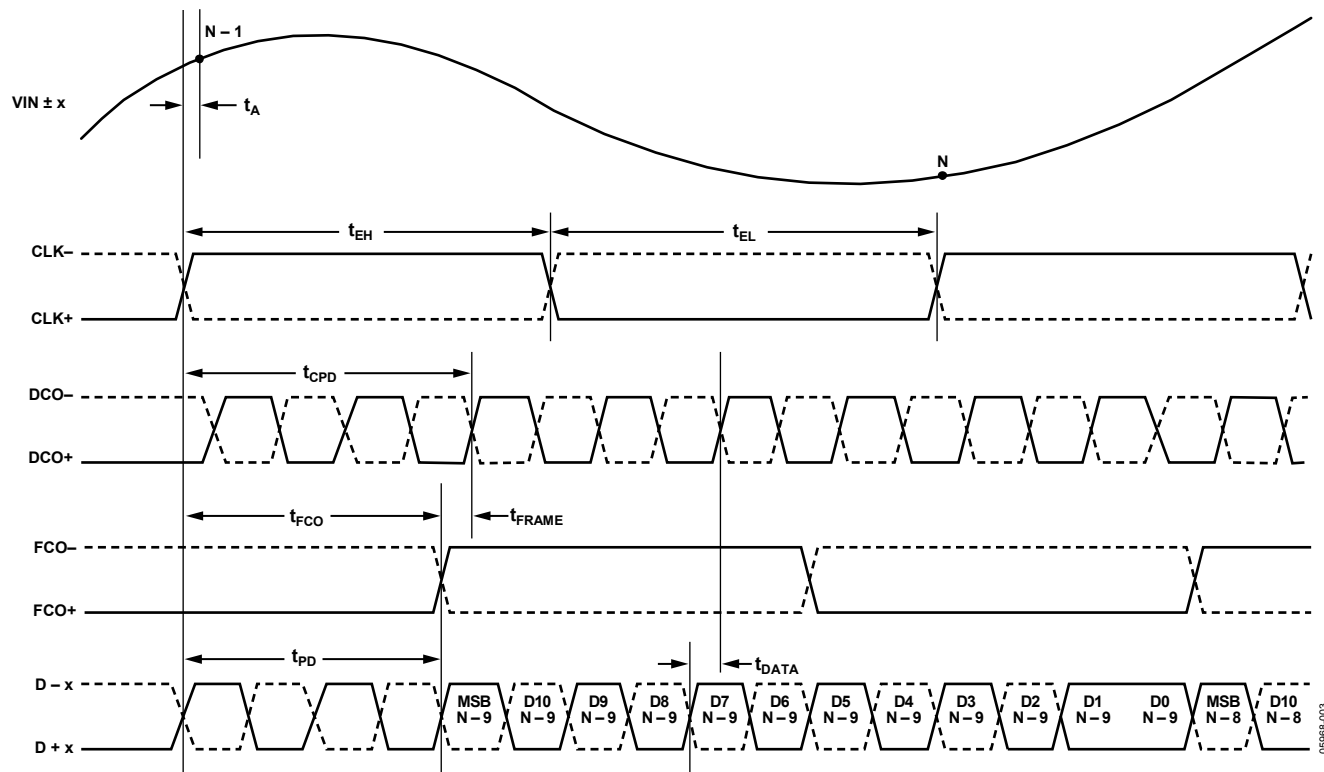
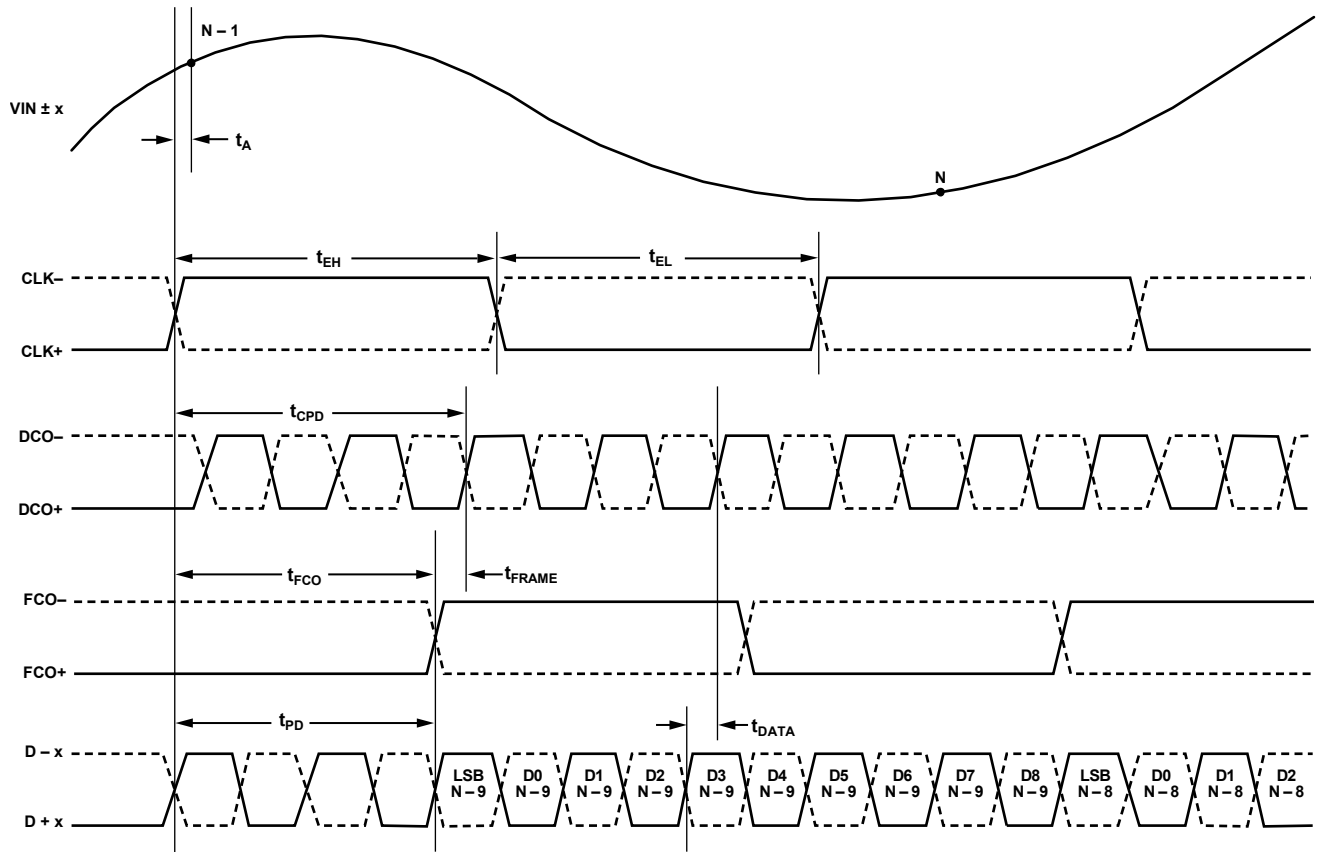


Figure 3. 12-Bit Data Serial Stream, MSB First

0596C-003



0598-004

Figure 4. 10-Bit Data Serial Stream, LSB First

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
ELECTRICAL		
AVDD	AGND	-0.3 V to +2.0 V
DRVDD	DRGND	-0.3 V to +2.0 V
AGND	DRGND	-0.3 V to +0.3 V
AVDD	DRVDD	-2.0 V to +2.0 V
Digital Outputs (D + x, D - x, DCO+, DCO-, FCO+, FCO-)	DRGND	-0.3 V to +2.0 V
CLK+, CLK-	AGND	-0.3 V to +3.9 V
VIN + x, VIN - x	AGND	-0.3 V to +2.0 V
SDIO/ODM	AGND	-0.3 V to +2.0 V
PDWN, SCLK/DTP, CSB	AGND	-0.3 V to +3.9 V
REFT, REFB, RBIAS	AGND	-0.3 V to +2.0 V
VREF, SENSE	AGND	-0.3 V to +2.0 V
ENVIRONMENTAL		
Operating Temperature Range (Ambient)		-40°C to +85°C
Storage Temperature Range (Ambient)		-65°C to +150°C
Maximum Junction Temperature		150°C
Lead Temperature (Soldering, 10 sec)		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE

Table 6.

Air Flow Velocity (m/s)	θ_{JA}^1	θ_{JB}	θ_{JC}	Unit
0.0	17.7			°C/W
1.0	15.5	8.7	0.6	°C/W
2.5	13.9			°C/W

¹ θ_{JA} for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.

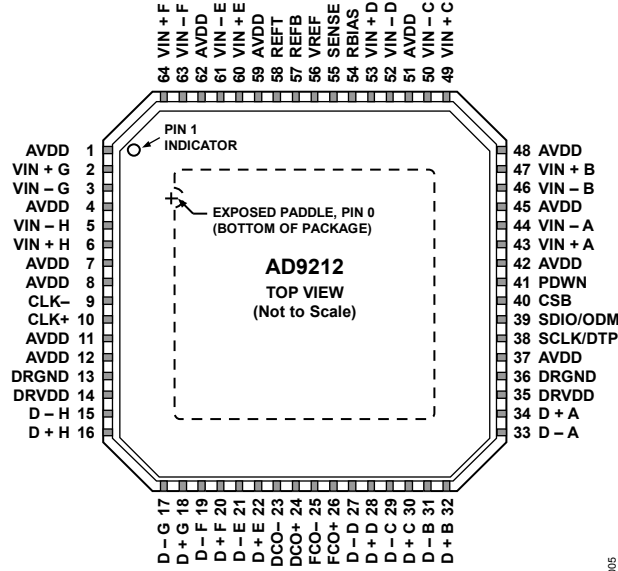
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. THE EXPOSED PAD MUST BE CONNECTED TO ANALOG GROUND

Figure 5. 64-Lead LFCSP Pin Configuration, Top View

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND	Analog Ground (Exposed Paddle)
1, 4, 7, 8, 11, 12, 37, 42, 45, 48, 51, 59, 62	AVDD	1.8 V Analog Supply
13, 36	DRGND	Digital Output Driver Ground
14, 35	DRVDD	1.8 V Digital Output Driver Supply
2	VIN + G	ADC G Analog Input True
3	VIN - G	ADC G Analog Input Complement
5	VIN - H	ADC H Analog Input Complement
6	VIN + H	ADC H Analog Input True
9	CLK-	Input Clock Complement
10	CLK+	Input Clock True
15	D - H	ADC H Digital Output Complement
16	D + H	ADC H Digital Output True
17	D - G	ADC G Digital Output Complement
18	D + G	ADC G Digital Output True
19	D - F	ADC F Digital Output Complement
20	D + F	ADC F Digital Output True
21	D - E	ADC E Digital Output Complement
22	D + E	ADC E Digital Output True
23	DCO-	Data Clock Digital Output Complement
24	DCO+	Data Clock Digital Output True
25	FCO-	Frame Clock Digital Output Complement
26	FCO+	Frame Clock Digital Output True
27	D - D	ADC D Digital Output Complement
28	D + D	ADC D Digital Output True
29	D - C	ADC C Digital Output Complement
30	D + C	ADC C Digital Output True
31	D - B	ADC B Digital Output Complement

Pin No.	Mnemonic	Description
32	D + B	ADC B Digital Output True
33	D – A	ADC A Digital Output Complement
34	D + A	ADC A Digital Output True
38	SCLK/DTP	Serial Clock/Digital Test Pattern
39	SDIO/ODM	Serial Data Input-Output/Output Driver Mode
40	CSB	Chip Select Bar
41	PDWN	Power-Down
43	VIN + A	ADC A Analog Input True
44	VIN – A	ADC A Analog Input Complement
46	VIN – B	ADC B Analog Input Complement
47	VIN + B	ADC B Analog Input True
49	VIN + C	ADC C Analog Input True
50	VIN – C	ADC C Analog Input Complement
52	VIN – D	ADC D Analog Input Complement
53	VIN + D	ADC D Analog Input True
54	RBIAS	External Resistor to Set the Internal ADC Core Bias Current
55	SENSE	Reference Mode Selection
56	VREF	Voltage Reference Input/Output
57	REFB	Negative Differential Reference
58	REFT	Positive Differential Reference
60	VIN + E	ADC E Analog Input True
61	VIN – E	ADC E Analog Input Complement
63	VIN – F	ADC F Analog Input Complement
64	VIN + F	ADC F Analog Input True

EQUIVALENT CIRCUITS

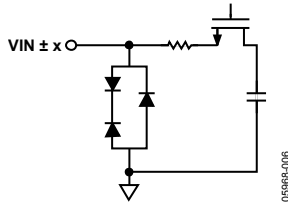


Figure 6. Equivalent Analog Input Circuit

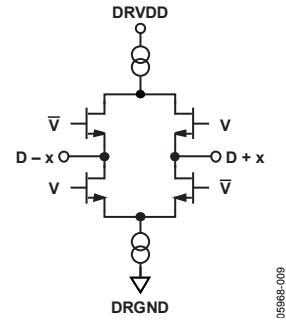


Figure 9. Equivalent Digital Output Circuit

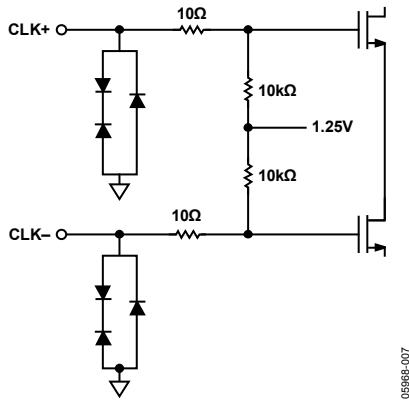


Figure 7. Equivalent Clock Input Circuit

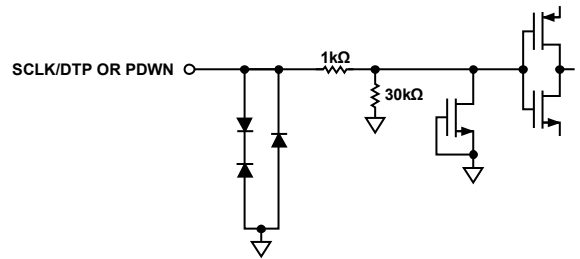


Figure 10. Equivalent SCLK/DTP or PDWN Input Circuit

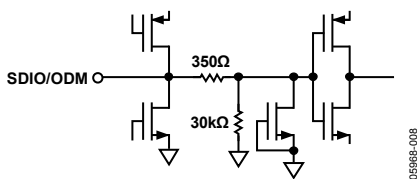


Figure 8. Equivalent SDIO/ODM Input Circuit

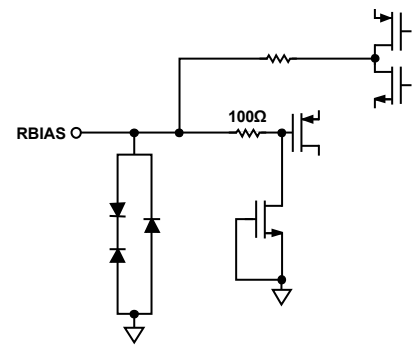


Figure 11. Equivalent RBIAS Circuit

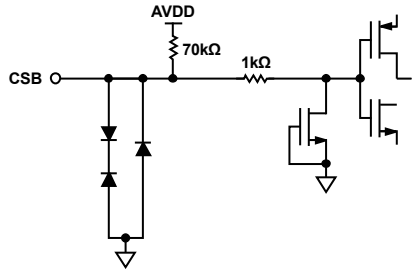


Figure 12. Equivalent CSB Input Circuit

05968-012

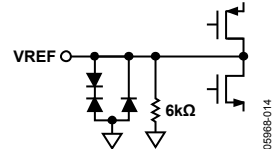


Figure 14. Equivalent VREF Circuit

05968-014

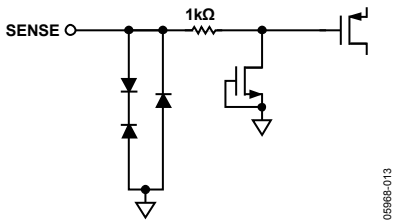


Figure 13. Equivalent SENSE Circuit

05968-013

TYPICAL PERFORMANCE CHARACTERISTICS

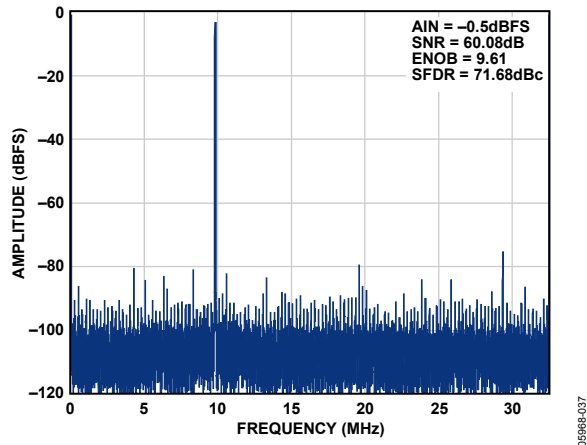


Figure 15. Single-Tone 32k FFT with $f_{IN} = 2.3$ MHz, AD9212-40

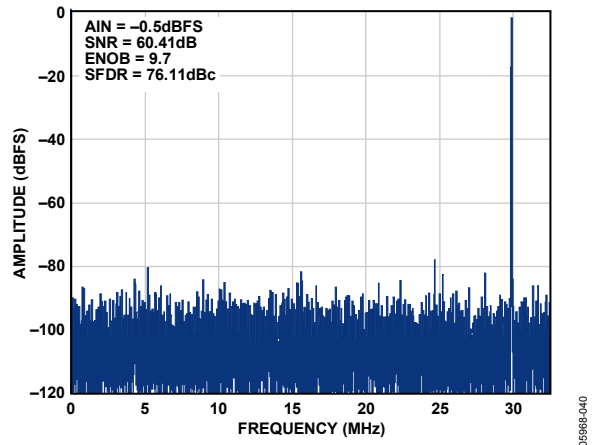


Figure 18. Single-Tone 32k FFT with $f_{IN} = 35$ MHz, AD9212-65

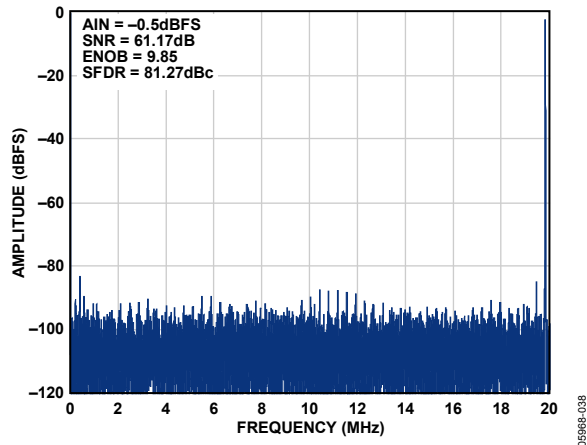


Figure 16. Single-Tone 32k FFT with $f_{IN} = 19.7$ MHz, AD9212-40

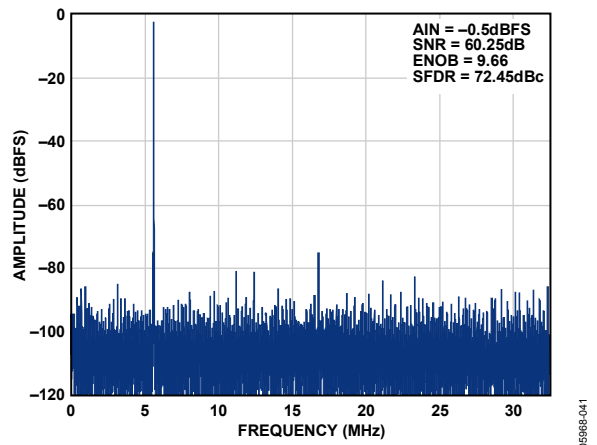


Figure 19. Single-Tone 32k FFT with $f_{IN} = 70$ MHz, AD9212-65

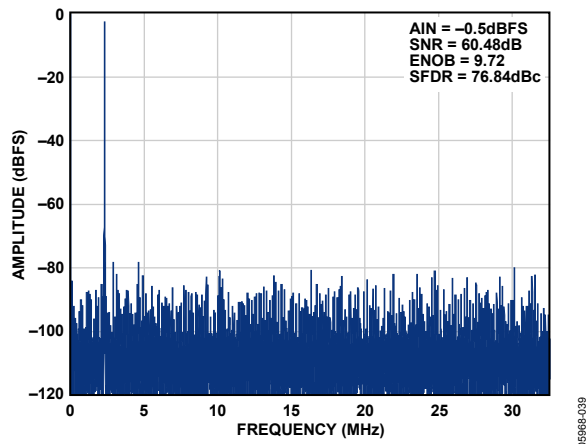


Figure 17. Single-Tone 32k FFT with $f_{IN} = 2.3$ MHz, AD9212-65

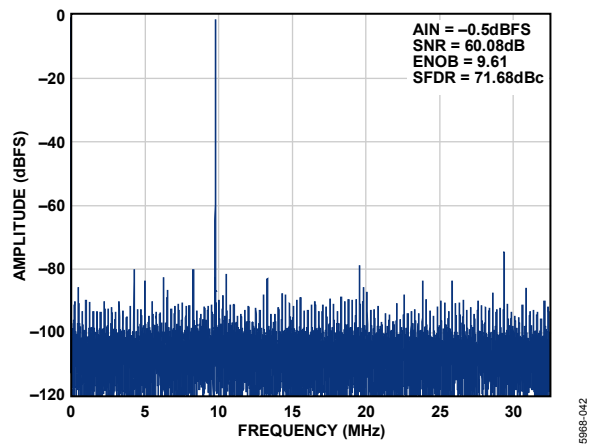


Figure 20. Single-Tone 32k FFT with $f_{IN} = 120$ MHz, AD9212-65

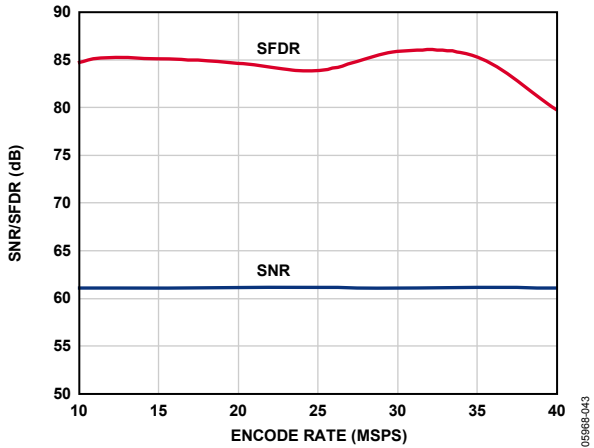


Figure 21. SNR/SFDR vs. f_{SAMPLE} , $f_{IN} = 10.3$ MHz, AD9212-40

05988-043

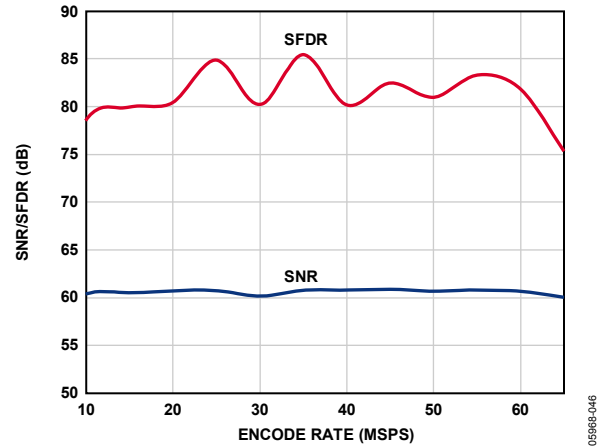


Figure 24. SNR/SFDR vs. f_{SAMPLE} , $f_{IN} = 35$ MHz, AD9212-65

05988-046

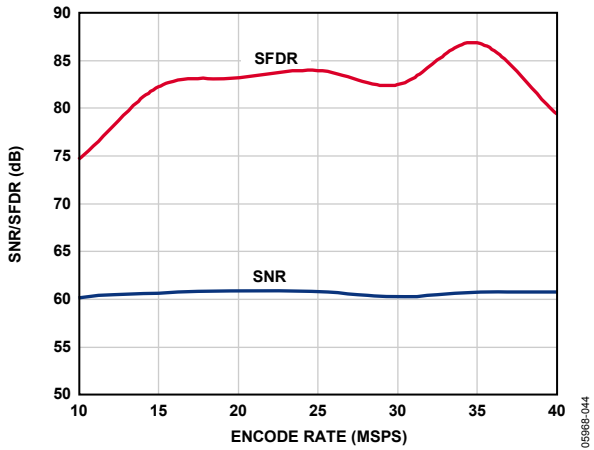


Figure 22. SNR/SFDR vs. f_{SAMPLE} , $f_{IN} = 19.7$ MHz, AD9212-40

05988-044

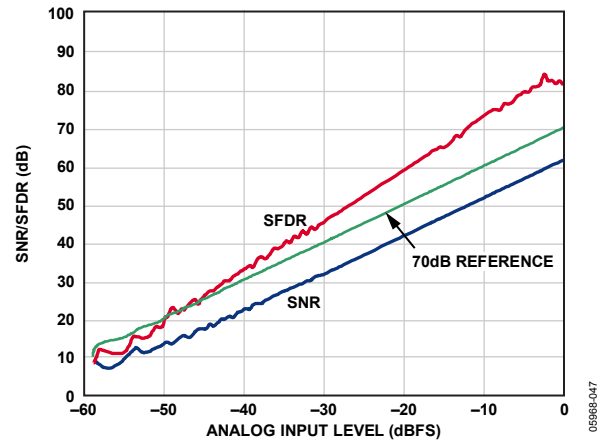


Figure 25. SNR/SFDR vs. Analog Input Level, $f_{IN} = 10.3$ MHz, AD9212-40

05988-047

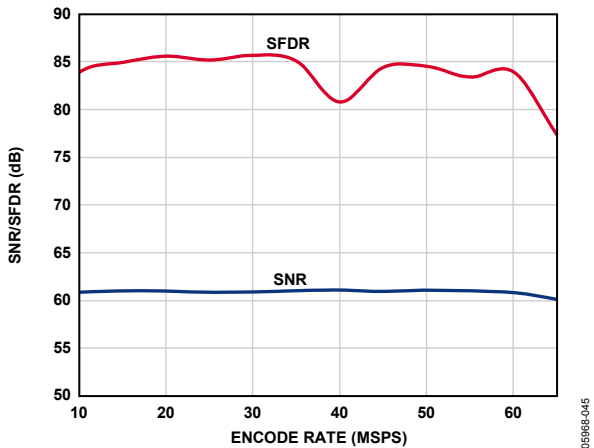


Figure 23. SNR/SFDR vs. f_{SAMPLE} , $f_{IN} = 10.3$ MHz, AD9212-65

05988-045

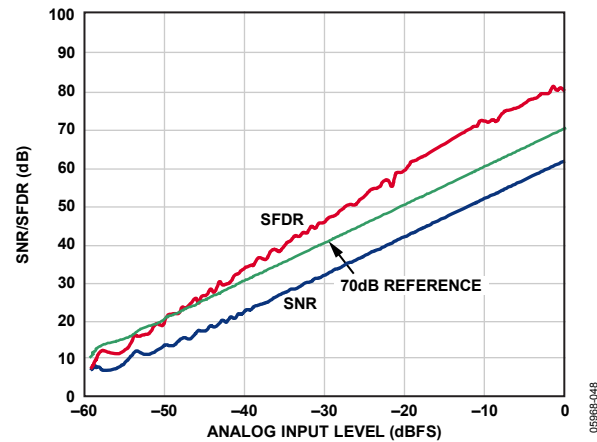


Figure 26. SNR/SFDR vs. Analog Input Level, $f_{IN} = 35$ MHz, AD9212-40

05988-048

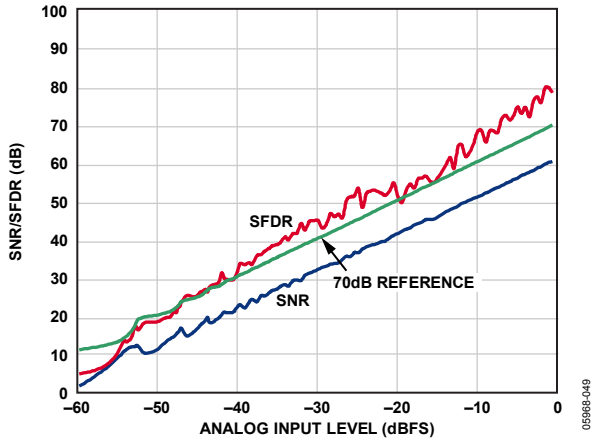


Figure 27. SNR/SFDR vs. Analog Input Level, $f_{IN} = 10.3$ MHz, AD9212-65

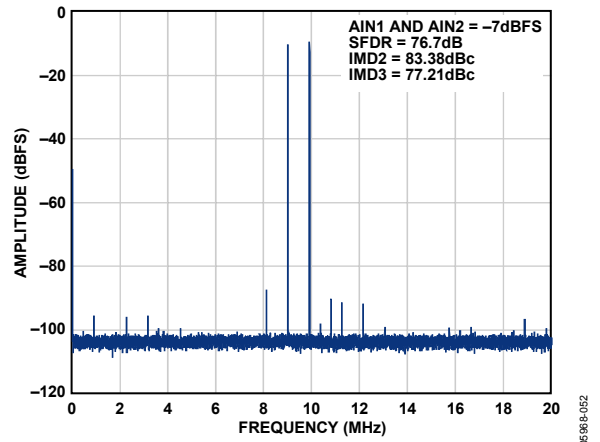


Figure 30. Two-Tone 32k FFT with $f_{IN1} = 70$ MHz and $f_{IN2} = 71$ MHz, AD9212-40

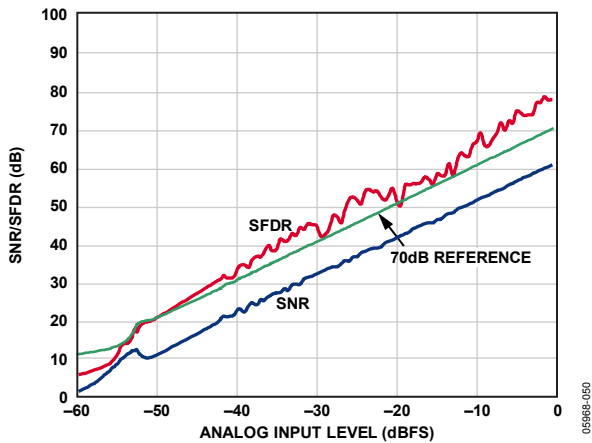


Figure 28. SNR/SFDR vs. Analog Input Level, $f_{IN} = 35$ MHz, AD9212-65

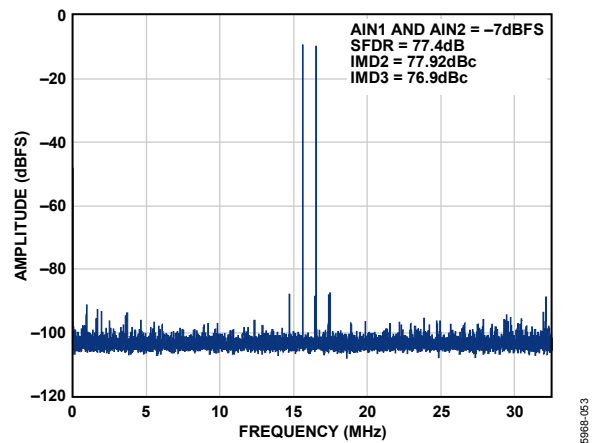


Figure 31. Two-Tone 32k FFT with $f_{IN1} = 15$ MHz and $f_{IN2} = 16$ MHz, AD9212-65

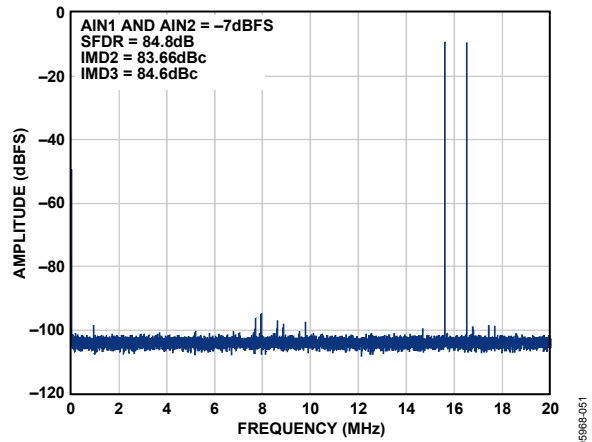


Figure 29. Two-Tone 32k FFT with $f_{IN1} = 15$ MHz and $f_{IN2} = 16$ MHz, AD9212-40

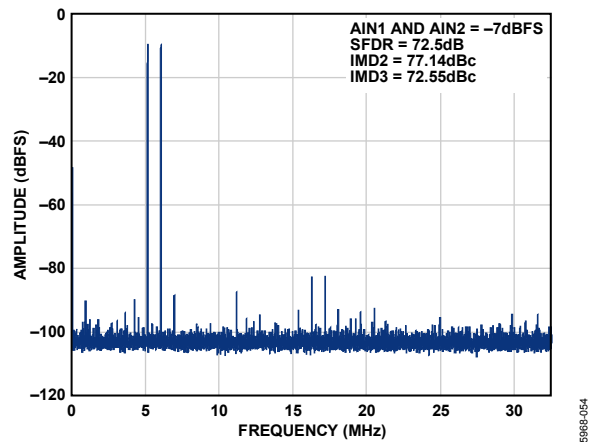


Figure 32. Two-Tone 32k FFT with $f_{IN1} = 70$ MHz and $f_{IN2} = 71$ MHz, AD9212-65

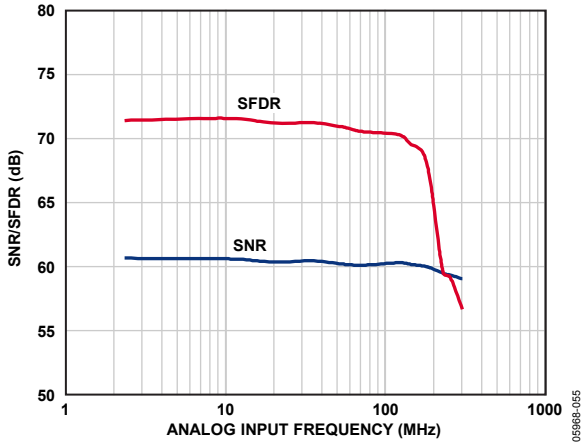


Figure 33. SNR/SFDR vs. f_{IN} , AD9212-65

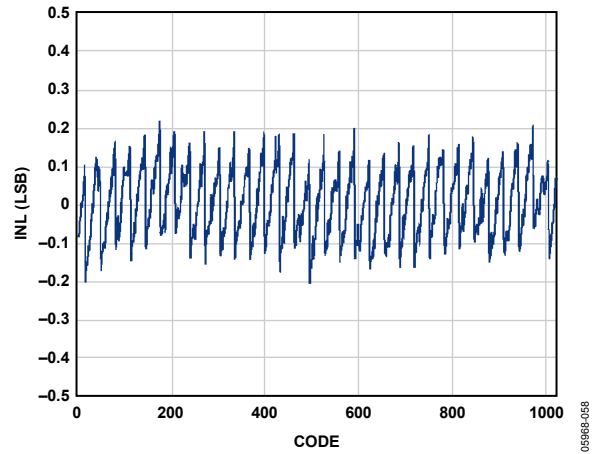


Figure 36. INL, $f_{IN} = 2.3$ MHz, AD9212-65

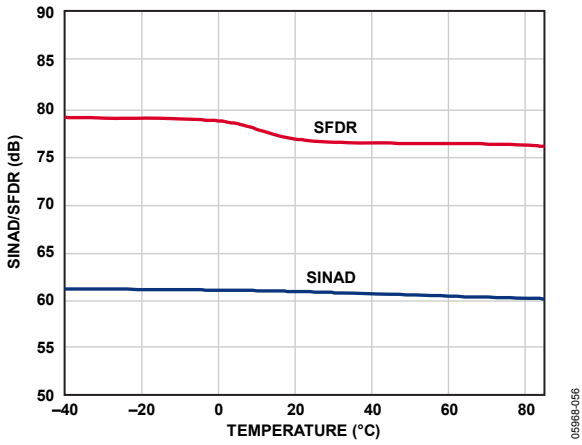


Figure 34. SINAD/SFDR vs. Temperature, $f_{IN} = 10.3$ MHz, AD9212-40

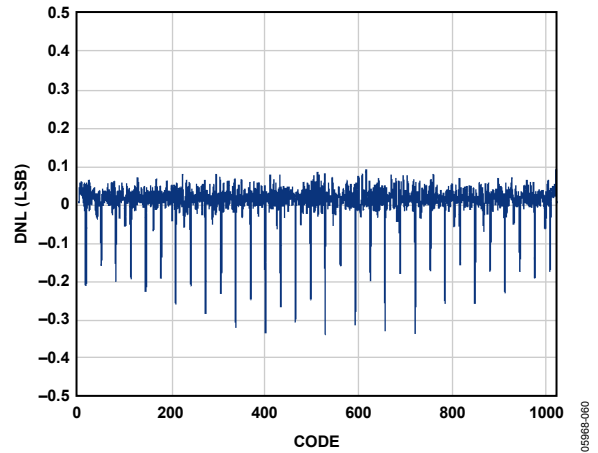


Figure 37. DNL, $f_{IN} = 2.3$ MHz, AD9212-65

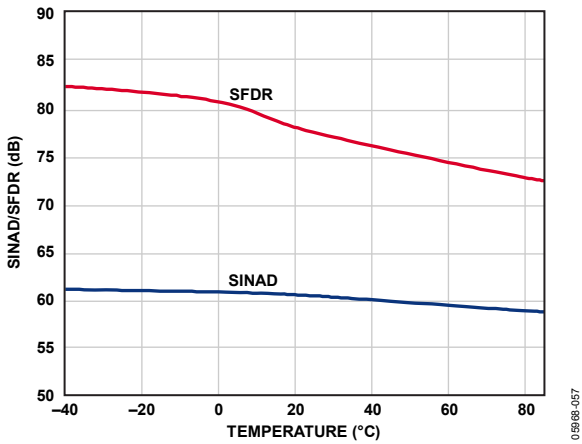


Figure 35. SINAD/SFDR vs. Temperature, $f_{IN} = 10.3$ MHz, AD9212-65

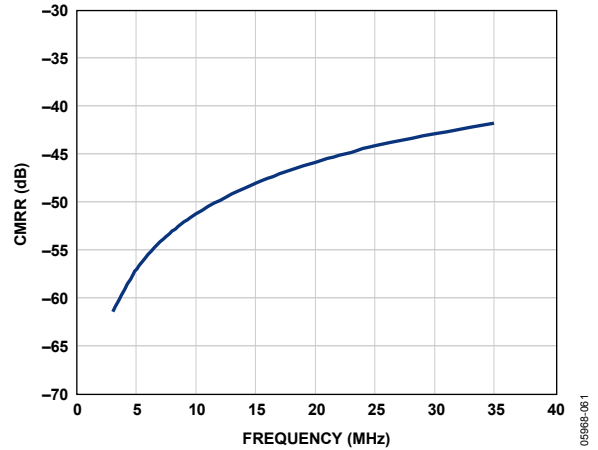


Figure 38. CMRR vs. Frequency, AD9212-65

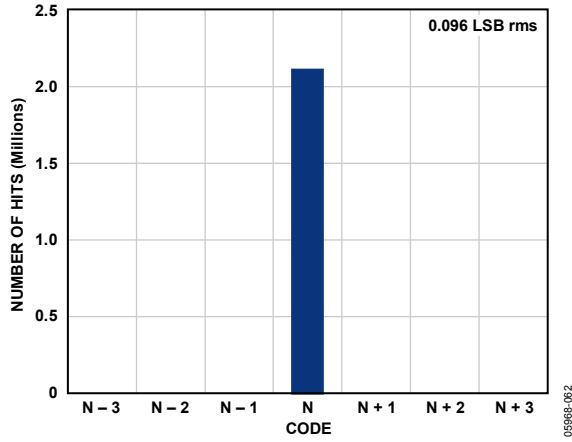


Figure 39. Input-Referred Noise Histogram, AD9212-65

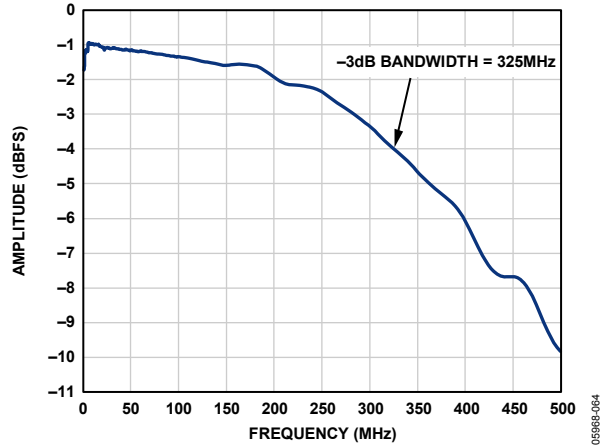


Figure 41. Full Power Bandwidth vs. Frequency, AD9212-65

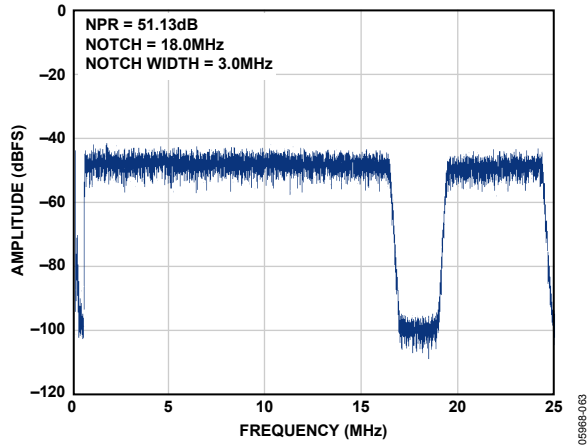


Figure 40. Noise Power Ratio (NPR), AD9212-65

THEORY OF OPERATION

The AD9212 architecture consists of a pipelined ADC divided into three sections: a 4-bit first stage followed by eight 1.5-bit stages and a 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 10-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9212 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. An input common-mode voltage of midsupply minimizes signal-dependent errors and provides optimum performance.

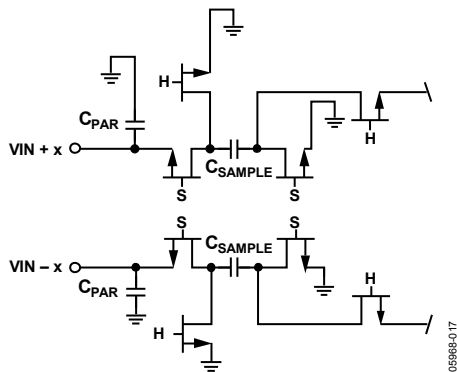


Figure 42. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 42). When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low-Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and therefore achieve the maximum bandwidth of the ADC. Such use of low-Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the [AN-742 Application Note, Frequency Domain Response of Switched-Capacitor ADCs](#); the [AN-827 Application Note, A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs](#); and the *Analog Dialogue* article “[Transformer-Coupled Front-End for Wideband A/D Converters](#)” (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

The analog inputs of the AD9212 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM} = AVDD/2$ is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 45 and Figure 46.

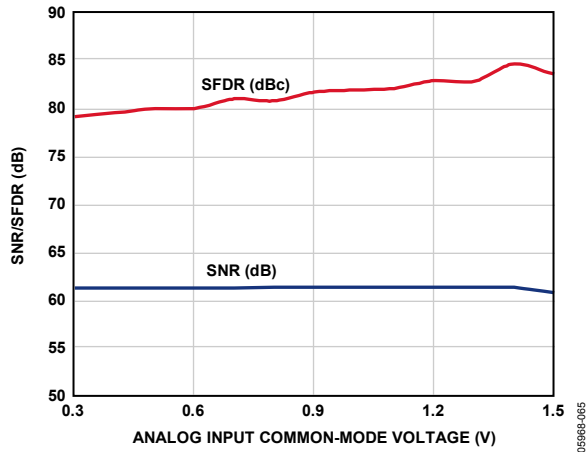


Figure 43. SNR/SFDR vs. Common-Mode Voltage, $f_{IN} = 2.3$ MHz, AD9212-40

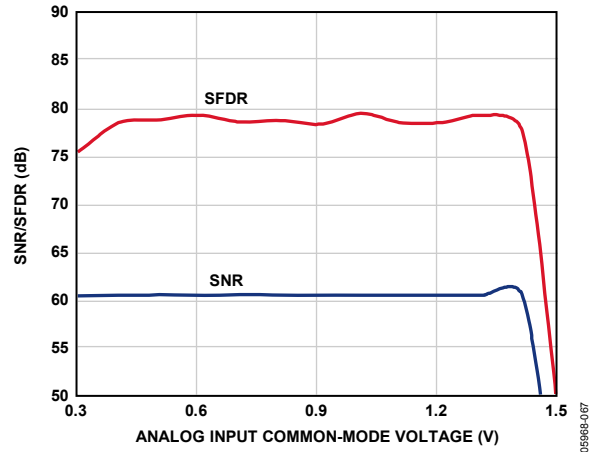


Figure 45. SNR/SFDR vs. Common-Mode Voltage, $f_{IN} = 2.3$ MHz, AD9212-65

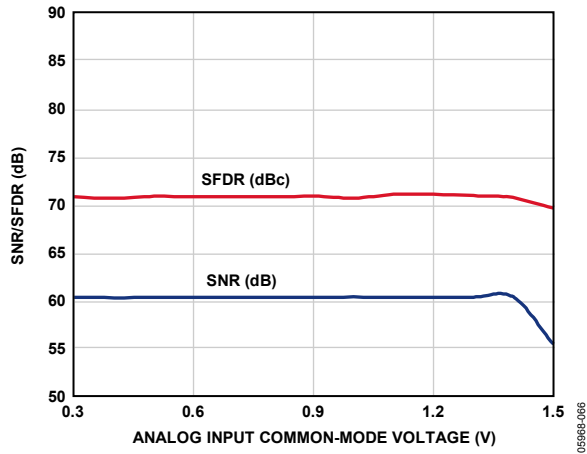


Figure 44. SNR/SFDR vs. Common-Mode Voltage, $f_{IN} = 19.7$ MHz, AD9212-40

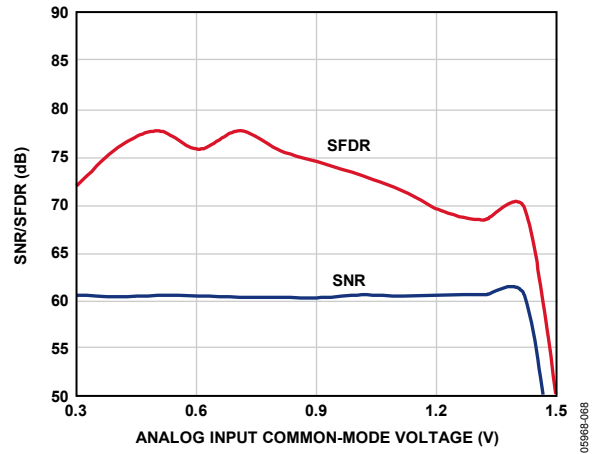


Figure 46. SNR/SFDR vs. Common-Mode Voltage, $f_{IN} = 35$ MHz, AD9212-65

For best dynamic performance, the source impedances driving $VIN + x$ and $VIN - x$ should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates the positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as

$$REFT = 1/2 (AVDD + VREF)$$

$$REFB = 1/2 (AVDD - VREF)$$

$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from these equations that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9212, the largest input span available is 2 V p-p.

Differential Input Configurations

There are several ways to drive the AD9212 either actively or passively; however, optimum performance is achieved by driving the analog input differentially. For example, using the AD8334 differential driver to drive the AD9212 provides excellent performance and a flexible interface to the ADC (see Figure 50) for baseband applications. This configuration is commonly used for medical ultrasound systems.

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 47 and Figure 48), because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9212.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

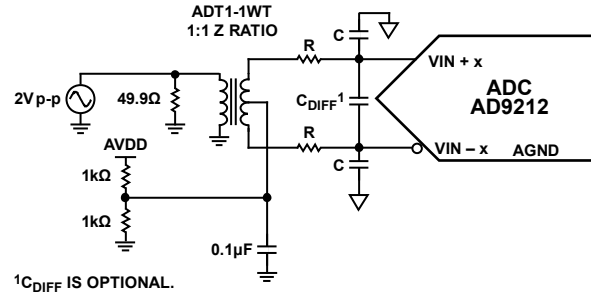


Figure 47. Differential Transformer-Coupled Configuration for Baseband Applications

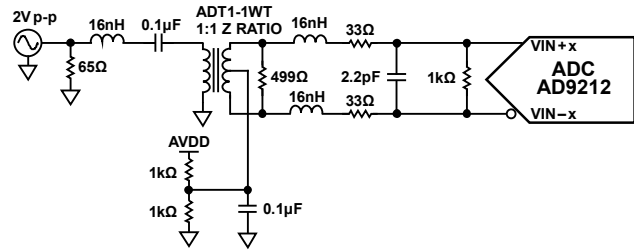


Figure 48. Differential Transformer-Coupled Configuration for IF Applications

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the application requires a single-ended input configuration, ensure that the source impedances on each input are well matched in order to achieve the best possible performance. A full-scale input of 2 V p-p can still be applied to the ADC's $VIN + x$ pin while the $VIN - x$ pin is terminated. Figure 49 details a typical single-ended input configuration.

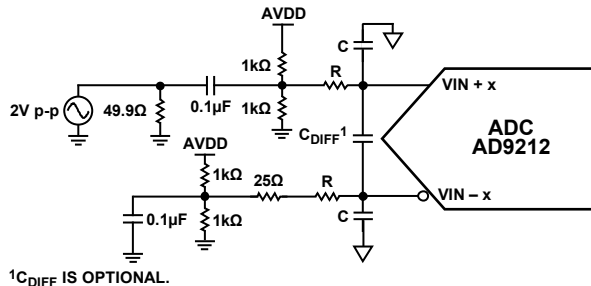


Figure 49. Single-Ended Input Configuration

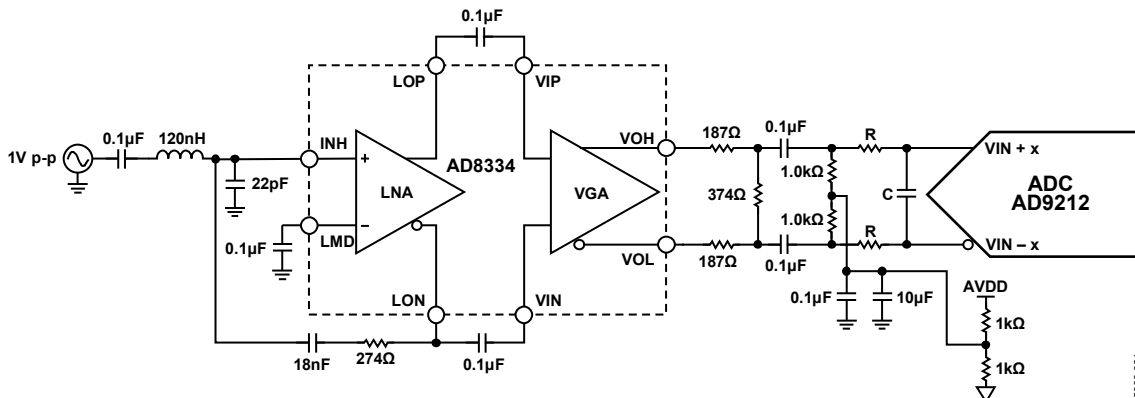


Figure 50. Differential Input Configuration Using the AD8334

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9212 sample clock inputs (CLK+ and CLK-) should be clocked with a differential signal. This signal is typically ac-coupled into the CLK+ and CLK- pins via a transformer or capacitors. These pins are biased internally and require no additional biasing.

Figure 51 shows the preferred method for clocking the AD9212. The low jitter clock source is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9212 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9212, and it preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

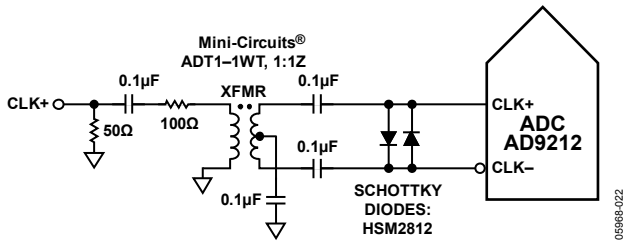


Figure 51. Transformer-Coupled Differential Clock

Another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 52. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

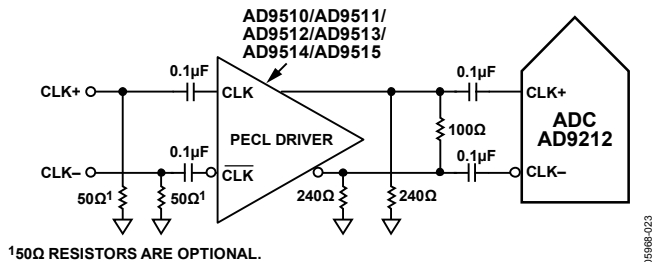


Figure 52. Differential PECL Sample Clock

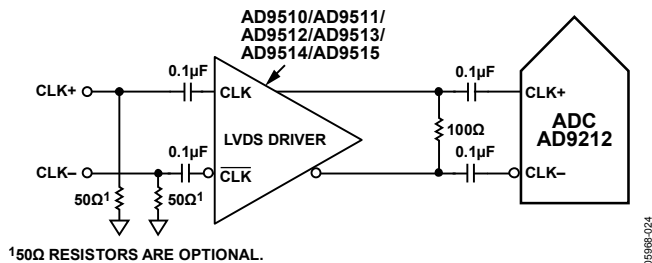


Figure 53. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be driven directly from a CMOS gate, and the CLK- pin should be bypassed to ground with a 0.1 μF capacitor in parallel with a 39 kΩ resistor (see Figure 54). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages of up to 3.3 V, making the selection of the drive logic voltage very flexible.

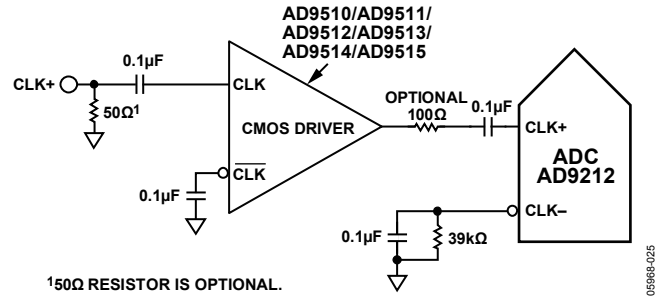


Figure 54. Single-Ended 1.8 V CMOS Sample Clock

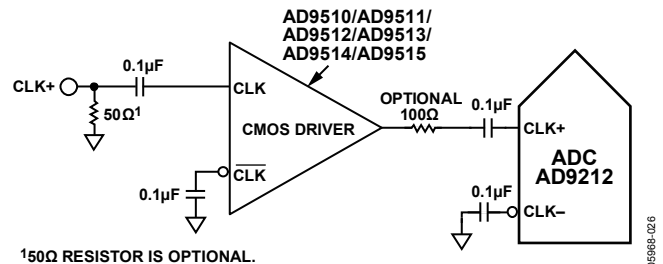


Figure 55. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9212 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9212. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See the Memory Map section for more details on using this feature.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_j) can be calculated by

$$SNR \text{ Degradation} = 20 \times \log_{10}(1/2 \times \pi \times f_A \times t_j)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 56).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9212. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the [AN-501 Application Note](#) and the [AN-756 Application Note](#) for more in-depth information about jitter performance as it relates to ADCs.

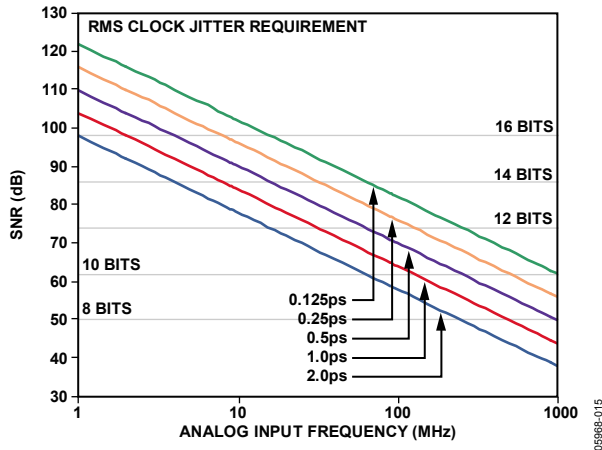


Figure 56. Ideal SNR vs. Input Frequency and Jitter

Power Dissipation and Power-Down Mode

As shown in Figure 57 and Figure 58, the power dissipated by the AD9212 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

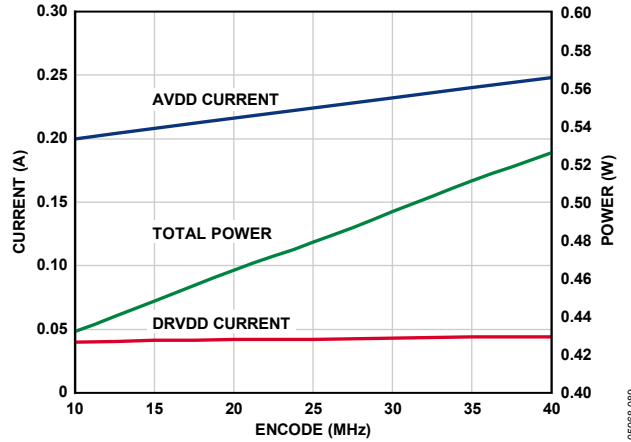


Figure 57. Supply Current vs. f_{SAMPLE} for $f_{IN} = 10.3 \text{ MHz}$, AD9212-40

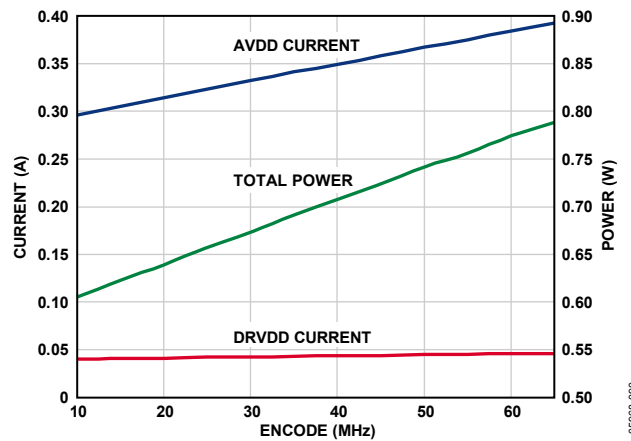


Figure 58. Supply Current vs. f_{SAMPLE} for $f_{IN} = 10.3 \text{ MHz}$, AD9212-65