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Quad, 12-Bit, 40/65 MSPS
Serial LVDS 1.8 V A/D Converter

Data Sheet

AD9228

FEATURES

4 ADCs integrated into 1 package
119 mW ADC power per channel at 65 MSPS
SNR = 70 dB (to Nyquist)
ENOB = 11.3 bits
SFDR = 82 dBc (to Nyquist)
Excellent linearity
- **DNL = ±0.3 LSB (typical)**
- **INL = ±0.4 LSB (typical)**

Serial LVDS (ANSI-644, default)
- **Low power, reduced signal option (similar to IEEE 1596.3)**

Data and frame clock outputs
315 MHz full-power analog bandwidth
2 V p-p input voltage range
1.8 V supply operation
Serial port control
- **Full-chip and individual-channel power-down modes**
- **Flexible bit orientation**
- **Built-in and custom digital test pattern generation**
- **Programmable clock and data alignment**
- **Programmable output resolution**
- **Standby mode**

APPLICATIONS

Medical imaging and nondestructive ultrasound
Portable ultrasound and digital beam-forming systems
Quadrature radio receivers
Diversity radio receivers
Tape drives
Optical networking
Test equipment

GENERAL DESCRIPTION

The AD9228 is a quad, 12-bit, 40/65 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 65 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual-channel power-down is supported and typically consumes less than 2 mW when all channels are disabled.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9228 is available in an RoHS compliant, 48-lead LFCSP. It is specified over the industrial temperature range of –40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

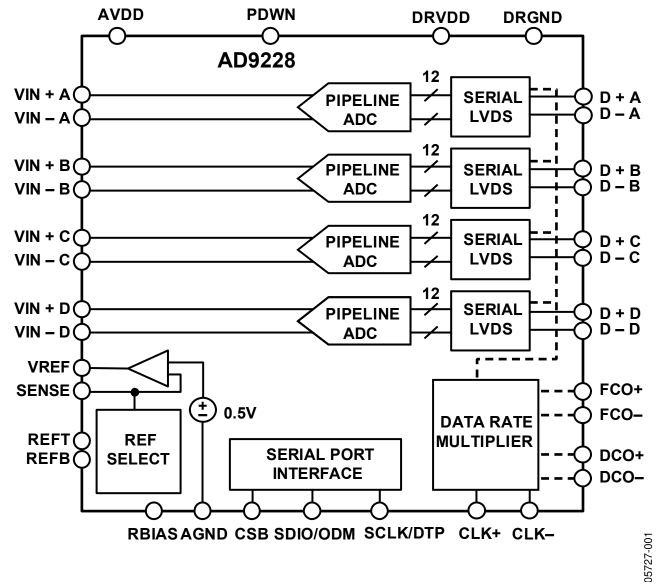

Figure 1.

PRODUCT HIGHLIGHTS

1. Small Footprint. Four ADCs are contained in a small, space-saving package.
2. Low power of 119 mW/channel at 65 MSPS.
3. Ease of Use. A data clock output (DCO) is provided that operates at frequencies of up to 390 MHz and supports double data rate (DDR) operation.
4. User Flexibility. The SPI control offers a wide range of flexible features to meet specific system requirements.
5. Pin-Compatible Family. This includes the AD9287 (8-bit), AD9219 (10-bit), and AD9259 (14-bit).

Rev. E

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AD9228* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9228 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9228: Quad, 12-Bit, 40/65 MSPS Serial LVDS 1.8 V A/D Converter Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog
- AD9228 IBIS Model

REFERENCE MATERIALS

Technical Articles

- Matching An ADC To A Transformer
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9228 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9228 EngineerZone Discussions.

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REVISION HISTORY

SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 1.

Parameter[1]	Temperature	AD9228-40 Min	AD9228-40 Typ	AD9228-40 Max	AD9228-65 Min	AD9228-65 Typ	AD9228-65 Max	Unit
RESOLUTION		12			12			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full		±1	±8		±1	±8	mV
Offset Matching	Full		±2	±8		±2	±8	mV
Gain Error	Full		±0.4	±1.2		±2	±3.5	% FS
Gain Matching	Full		±0.3	±0.7		±0.3	±0.7	% FS
Differential Nonlinearity (DNL)	Full		±0.25	±0.5		±0.3	±0.65	LSB
Integral Nonlinearity (INL)	Full		±0.4	±1		±0.4	±1	LSB
TEMPERATURE DRIFT								
Offset Error	Full		±2			±2		ppm/°C
Gain Error	Full		±17			±17		ppm/°C
Reference Voltage (1 V Mode)	Full		±21			±21		ppm/°C
REFERENCE								
Output Voltage Error (V_{REF} = 1 V)	Full		±2	±30		±2	±30	mV
Load Regulation at 1.0 mA (V_{REF} = 1 V)	Full		3			3		mV
Input Resistance	Full		6			6		kΩ
ANALOG INPUTS								
Differential Input Voltage (V_{REF} = 1 V)	Full		2			2		V p-p
Common-Mode Voltage	Full		AVDD/2			AVDD/2		V
Differential Input Capacitance	Full		7			7		pF
Analog Bandwidth, Full Power	Full		315			315		MHz
POWER SUPPLY								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{AVDD}	Full		155	170		232	245	mA
I_{DRVDD}	Full		31	34		34	38	mA
Total Power Dissipation (Including Output Drivers)	Full		335	367		478	510	mW
Power-Down Dissipation	Full		2	5.8		2	5.8	mW
Standby Dissipation[2]	Full		72			72		mW
CROSSTALK	Full		−100			−100		dB
CROSSTALK (Overrange Condition)[3]	Full		−100			−100		dB

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Can be controlled via the SPI.
[3] Overrange condition is specific with 6 dB of the full-scale input range.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	AD9228-40 Min	AD9228-40 Typ	AD9228-40 Max	AD9228-65 Min	AD9228-65 Typ	AD9228-65 Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 2.4 MHz	Full		70.5			70.2		dB
f_{IN} = 19.7 MHz	Full	68.5	70.2			70.0		dB
f_{IN} = 35 MHz	Full		70.2		68.5	70.0		dB
f_{IN} = 70 MHz	Full		70.0			69.5		dB
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)								
f_{IN} = 2.4 MHz	Full		70.3			70.0		dB
f_{IN} = 19.7 MHz	Full	68.0	69.8			70.0		dB
f_{IN} = 35 MHz	Full		69.7		68.0	69.8		dB
f_{IN} = 70 MHz	Full		69.5			69.0		dB
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 2.4 MHz	Full		11.42			11.37		Bits
f_{IN} = 19.7 MHz	Full	11.1	11.37			11.33		Bits
f_{IN} = 35 MHz	Full		11.37		11.1	11.33		Bits
f_{IN} = 70 MHz	Full		11.33			11.25		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 2.4 MHz	Full		85			85		dBc
f_{IN} = 19.7 MHz	Full	72	82			85		dBc
f_{IN} = 35 MHz	Full		80		73	84		dBc
f_{IN} = 70 MHz	Full		80			74		dBc
WORST HARMONIC (Second or Third)								
f_{IN} = 2.4 MHz	Full		−85			−85		dBc
f_{IN} = 19.7 MHz	Full		−82	−72		−85		dBc
f_{IN} = 35 MHz	Full		−80			−84	−73	dBc
f_{IN} = 70 MHz	Full		−80			−74		dBc
WORST OTHER (Excluding Second or Third)								
f_{IN} = 2.4 MHz	Full		−90			−90		dBc
f_{IN} = 19.7 MHz	Full		−90	−80		−90		dBc
f_{IN} = 35 MHz	Full		−90			−90	−79	dBc
f_{IN} = 70 MHz	Full		−90			−88		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS								
f_{IN1} = 15 MHz, f_{IN2} = 16 MHz	25°C		80.8			77.8		dBc
f_{IN1} = 70 MHz, f_{IN2} = 71 MHz	25°C		75.0			77.0		dBc

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 3.

Parameter[1]	Temperature	AD9228-40 Min	AD9228-40 Typ	AD9228-40 Max	AD9228-65 Min	AD9228-65 Typ	AD9228-65 Max	Unit
CLOCK INPUTS (CLK+, CLK−)								
Logic Compliance			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			250			mV p-p
Input Common-Mode Voltage	Full		1.2			1.2		V
Input Resistance (Differential)	25°C		20			20		kΩ
Input Capacitance	25°C		1.5			1.5		pF
LOGIC INPUTS (PDWN, SCLK/DTP)								
Logic 1 Voltage	Full	1.2		3.6	1.2		3.6	V
Logic 0 Voltage	Full	0		0.3			0.3	V
Input Resistance	25°C		30			30		kΩ
Input Capacitance	25°C		0.5			0.5		pF
LOGIC INPUT (CSB)								
Logic 1 Voltage	Full	1.2		3.6	1.2		3.6	V
Logic 0 Voltage	Full	0		0.3			0.3	V
Input Resistance	25°C		70			70		kΩ
Input Capacitance	25°C		0.5			0.5		pF
LOGIC INPUT (SDIO/ODM)								
Logic 1 Voltage	Full	1.2		DRVDD + 0.3	1.2		DRVDD + 0.3	V
Logic 0 Voltage	Full	0		0.3	0		0.3	V
Input Resistance	25°C		30			30		kΩ
Input Capacitance	25°C		2			2		pF
LOGIC OUTPUT (SDIO/ODM)[3]								
Logic 1 Voltage (I_{OH} = 800 μA)	Full		1.79			1.79		V
Logic 0 Voltage (I_{OL} = 50 μA)	Full			0.05			0.05	V
DIGITAL OUTPUTS (D + x, D − x), (ANSI-644)								
Logic Compliance			LVDS			LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	1.125		1.375	V
Output Coding (Default)			Offset binary			Offset binary		
DIGITAL OUTPUTS (D + x, D − x), (Low Power, Reduced Signal Option)								
Logic Compliance			LVDS			LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	1.10		1.30	V
Output Coding (Default)			Offset binary			Offset binary		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] This is specified for LVDS and LVPECL only.
[3] This is specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 4.

Parameter[1, 2]	Temp	AD9228-40 Min	AD9228-40 Typ	AD9228-40 Max	AD9228-65 Min	AD9228-65 Typ	AD9228-65 Max	Unit
CLOCK[3]								
Maximum Clock Rate	Full	40			65			MSPS
Minimum Clock Rate	Full			10			10	MSPS
Clock Pulse Width High (t_{EH})	Full		12.5			7.7		ns
Clock Pulse Width Low (t_{EL})	Full		12.5			7.7		ns
OUTPUT PARAMETERS[3]								
Propagation Delay (t_{PD})	Full	2.0	2.7	3.5	2.0	2.7	3.5	ns
Rise Time (t_R) (20% to 80%)	Full		300			300		ps
Fall Time (t_F) (20% to 80%)	Full		300			300		ps
FCO Propagation Delay (t_{FCO})	Full	2.0	2.7	3.5	2.0	2.7	3.5	ns
DCO Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/24)			t_{FCO} + (t_{SAMPLE}/24)		ns
DCO to Data Delay (t_{DATA})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
DCO to FCO Delay (t_{FRAME})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
Data to Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±50	±150		±50	±150	ps
Wake-Up Time (Standby)	25°C		600			600		ns
Wake-Up Time (Power-Down)	25°C		375			375		µs
Pipeline Latency	Full		8			8		CLK cycles
APERTURE								
Aperture Delay (t_A)	25°C		500			500		ps
Aperture Uncertainty (Jitter)	25°C		<1			<1		ps rms
Out-of-Range Recovery Time	25°C		1			2		CLK cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] Can be adjusted via the SPI.
[4] t_{SAMPLE}/24 is based on the number of bits divided by 2 because the delays are based on half duty cycles.

TIMING DIAGRAMS

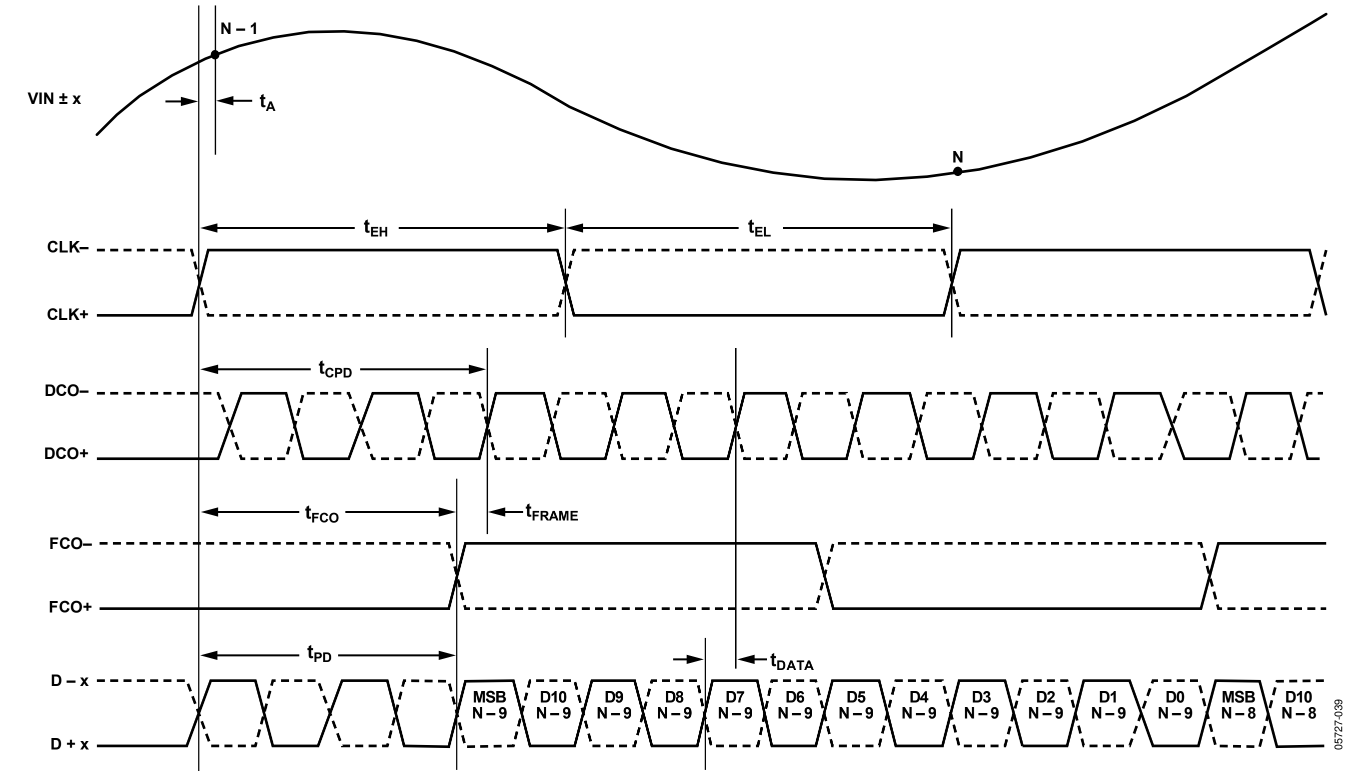


Figure 2. 12-Bit Data Serial Stream, MSB First (Default)

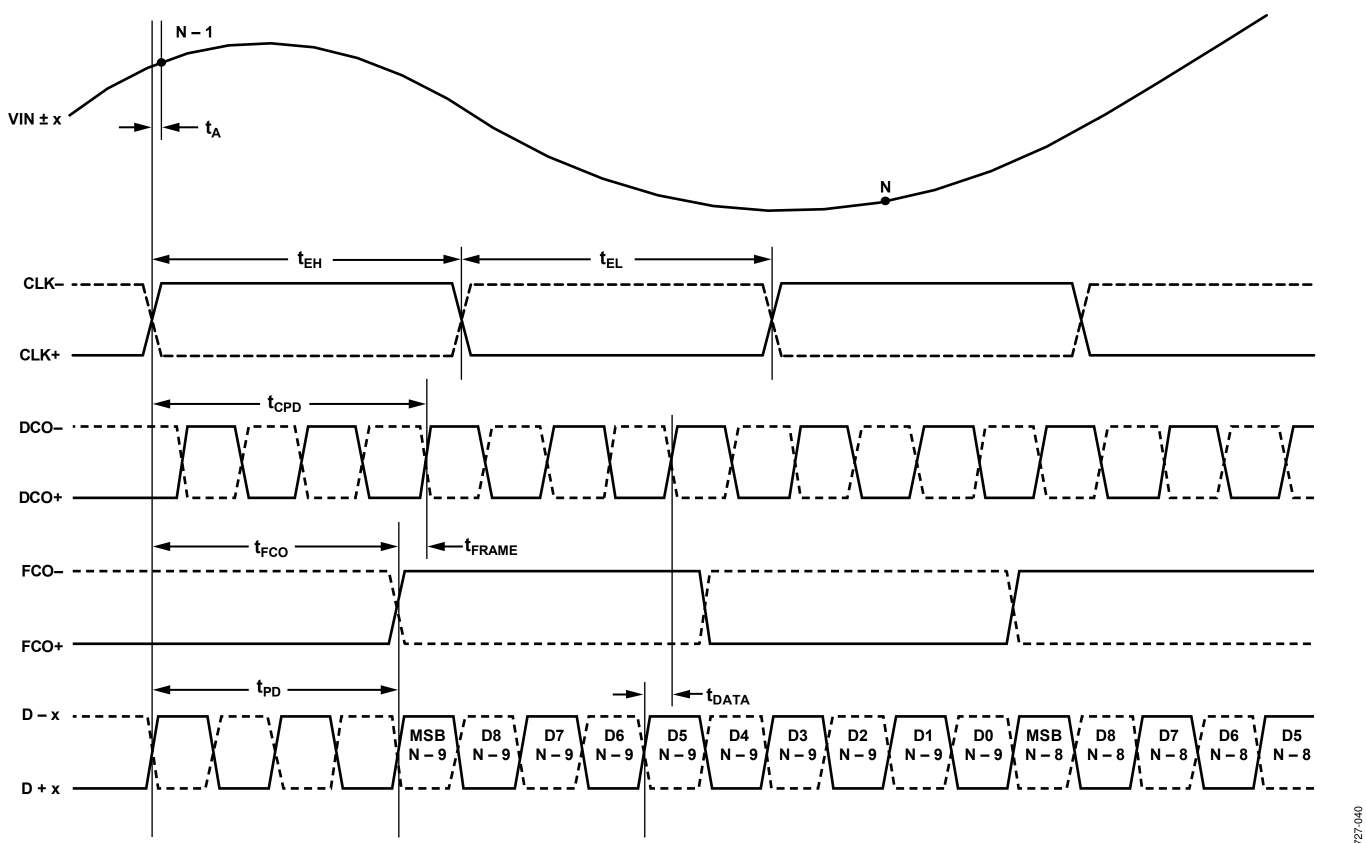


Figure 3. 10-Bit Data Serial Stream, MSB First

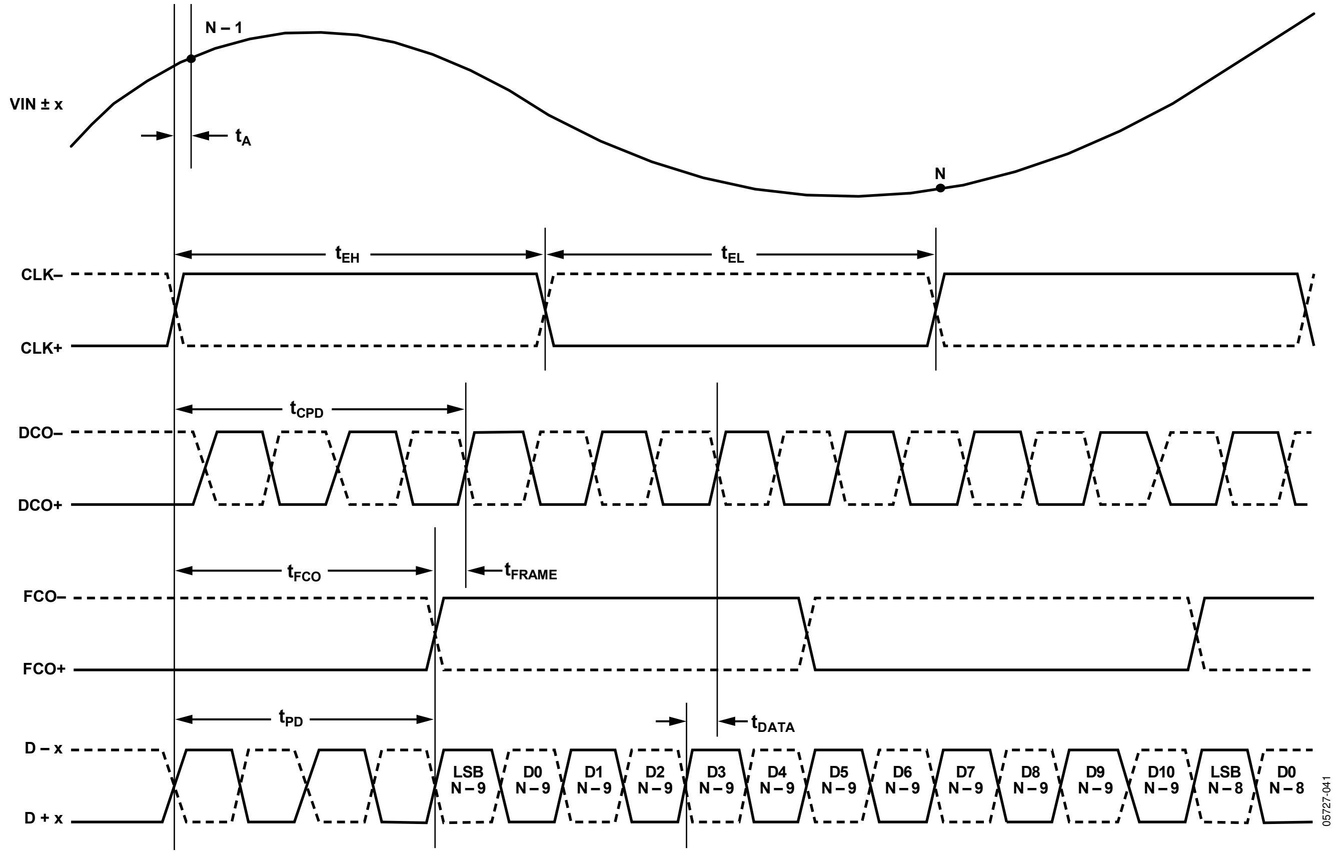


Figure 4. 12-Bit Data Serial Stream, LSB First

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
ELECTRICAL		
AVDD	AGND	−0.3 V to +2.0 V
DRVDD	DRGND	−0.3 V to +2.0 V
AGND	DRGND	−0.3 V to +0.3 V
AVDD	DRVDD	−2.0 V to +2.0 V
Digital Outputs (D + x, D − x, DCO+, DCO−, FCO+, FCO−)	DRGND	−0.3 V to +2.0 V
CLK+, CLK−	AGND	−0.3 V to +3.9 V
VIN + x, VIN − x	AGND	−0.3 V to +2.0 V
SDIO/ODM	AGND	−0.3 V to +2.0 V
PDWN, SCLK/DTP, CSB	AGND	−0.3 V to +3.9 V
REFT, REFB, RBIAS	AGND	−0.3 V to +2.0 V
VREF, SENSE	AGND	−0.3 V to +2.0 V
ENVIRONMENTAL		
Operating Temperature Range (Ambient)		−40°C to +85°C
Maximum Junction Temperature		150°C
Lead Temperature (Soldering, 10 sec)		300°C
Storage Temperature Range (Ambient)		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

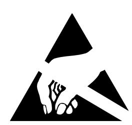
THERMAL IMPEDANCE

Table 6.

Air Flow Velocity (m/sec)	θ_{JA}[1]	θ_{JB}	θ_{JC}	Unit
0.0	24			°C/W
1.0	21	12.6	1.2	°C/W
2.5	19			°C/W

[1] θ_{JA} for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

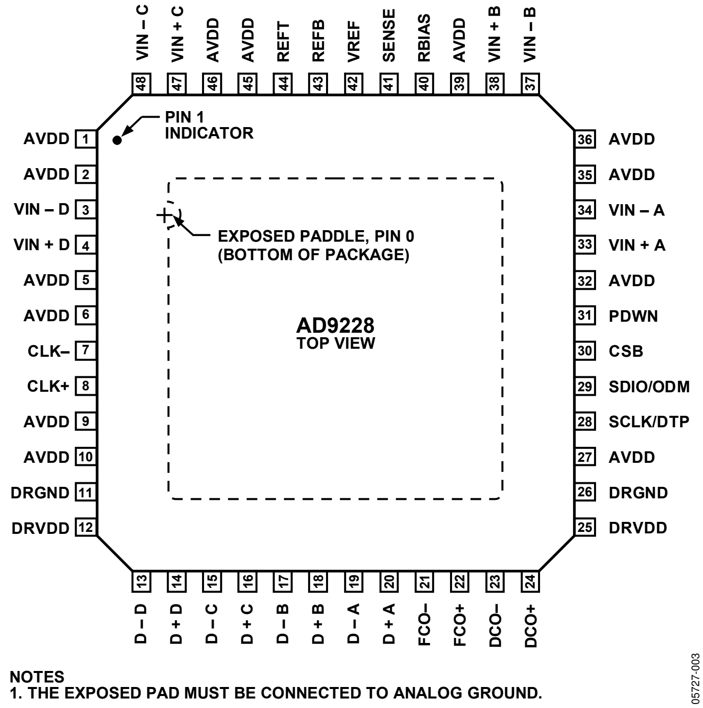


Figure 5. 48-Lead LFCSP Pin Configuration, Top View

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND	Analog Ground (Exposed Paddle)
1, 2, 5, 6, 9, 10, 27, 32, 35, 36, 39, 45, 46	AVDD	1.8 V Analog Supply
11, 26	DRGND	Digital Output Driver Ground
12, 25	DRVDD	1.8 V Digital Output Driver Supply
3	VIN – D	ADC D Analog Input Complement
4	VIN + D	ADC D Analog Input True
7	CLK–	Input Clock Complement
8	CLK+	Input Clock True
13	D – D	ADC D Digital Output Complement
14	D + D	ADC D Digital Output True
15	D – C	ADC C Digital Output Complement
16	D + C	ADC C Digital Output True
17	D – B	ADC B Digital Output Complement
18	D + B	ADC B Digital Output True
19	D – A	ADC A Digital Output Complement
20	D + A	ADC A Digital Output True
21	FCO–	Frame Clock Output Complement
22	FCO+	Frame Clock Output True
23	DCO–	Data Clock Output Complement
24	DCO+	Data Clock Output True
28	SCLK/DTP	Serial Clock/Digital Test Pattern
29	SDIO/ODM	Serial Data IO/Output Driver Mode
30	CSB	Chip Select Bar
31	PDWN	Power-Down

Pin No.	Mnemonic	Description
33	VIN + A	ADC A Analog Input True
34	VIN − A	ADC A Analog Input Complement
37	VIN − B	ADC B Analog Input Complement
38	VIN + B	ADC B Analog Input True
40	RBIAS	External resistor sets the internal ADC core bias current
41	SENSE	Reference Mode Selection
42	VREF	Voltage Reference Input/Output
43	REFB	Differential Reference (Negative)
44	REFT	Differential Reference (Positive)
47	VIN + C	ADC C Analog Input True
48	VIN − C	ADC C Analog Input Complement

EQUIVALENT CIRCUITS

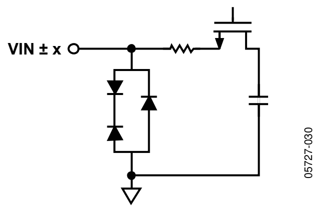


Figure 6. Equivalent Analog Input Circuit

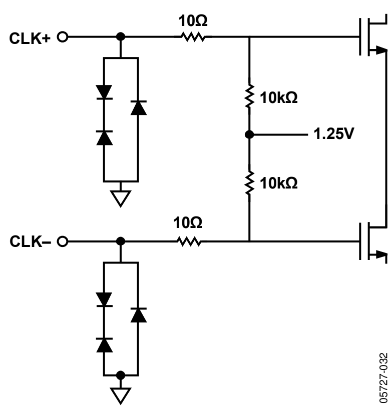


Figure 7. Equivalent Clock Input Circuit

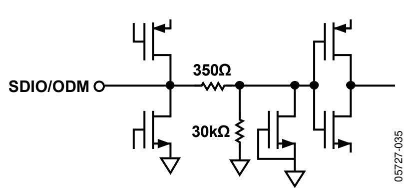


Figure 8. Equivalent SDIO/ODM Input Circuit

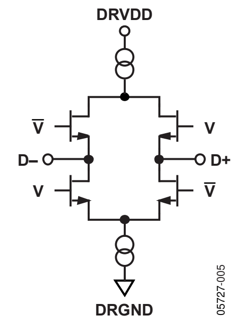


Figure 9. Equivalent Digital Output Circuit

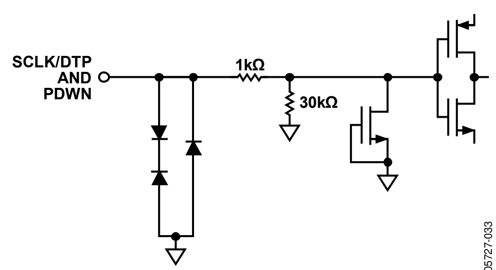


Figure 10. Equivalent SCLK/DTP and PDWN Input Circuit

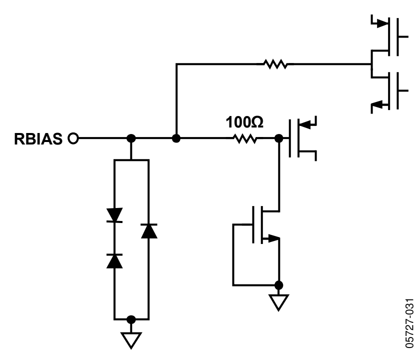


Figure 11. Equivalent RBIAS Circuit

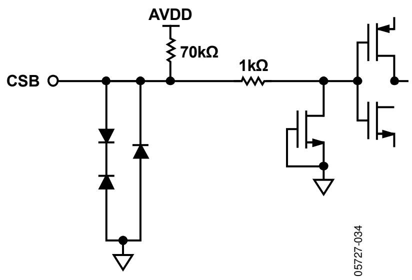


Figure 12. Equivalent CSB Input Circuit

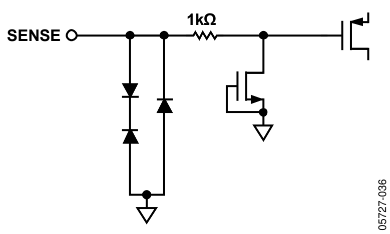


Figure 13. Equivalent SENSE Circuit

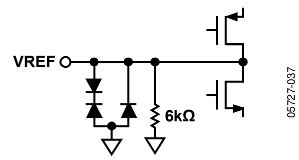


Figure 14. Equivalent VREF Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

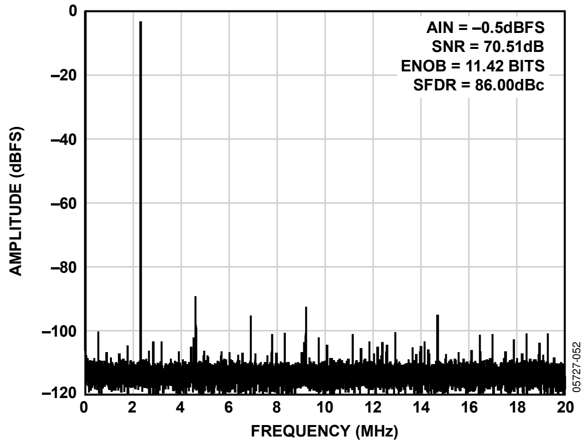


Figure 15. Single-Tone 32k FFT with f_{IN} = 2.4 MHz, f_{SAMPLE} = 40 MSPS

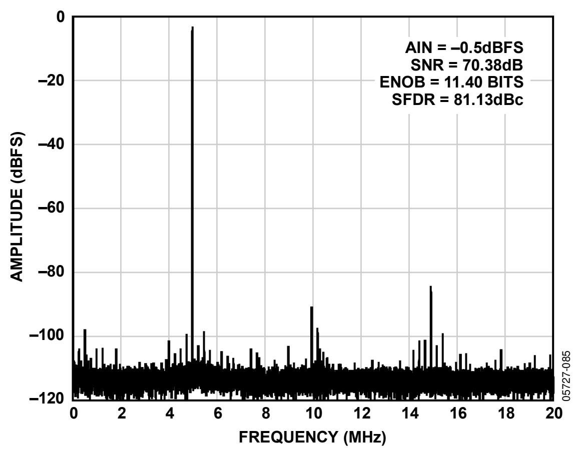


Figure 16. Single-Tone 32k FFT with f_{IN} = 35 MHz, f_{SAMPLE} = 40 MSPS

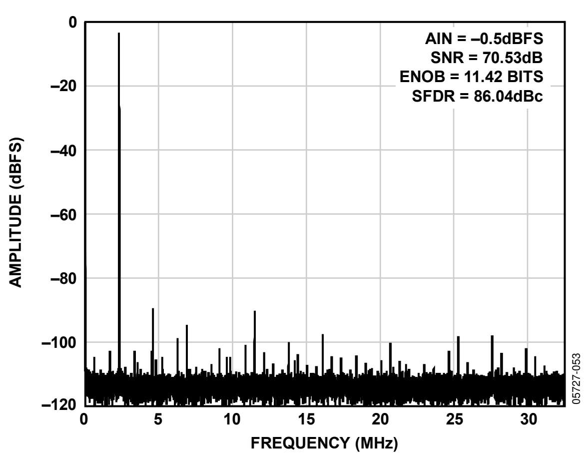


Figure 17. Single-Tone 32k FFT with f_{IN} = 2.3 MHz, f_{SAMPLE} = 65 MSPS

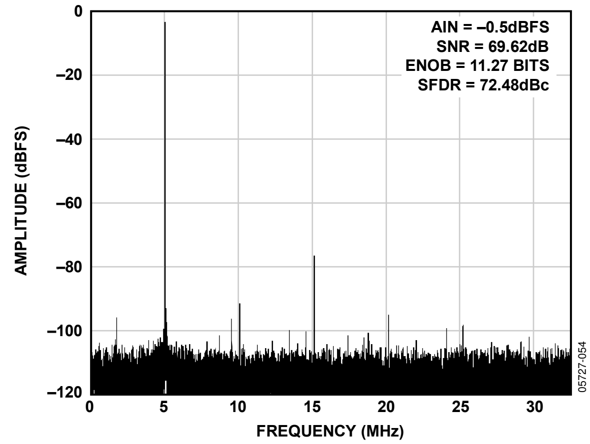


Figure 18. Single-Tone 32k FFT with f_{IN} = 70 MHz, f_{SAMPLE} = 65 MSPS

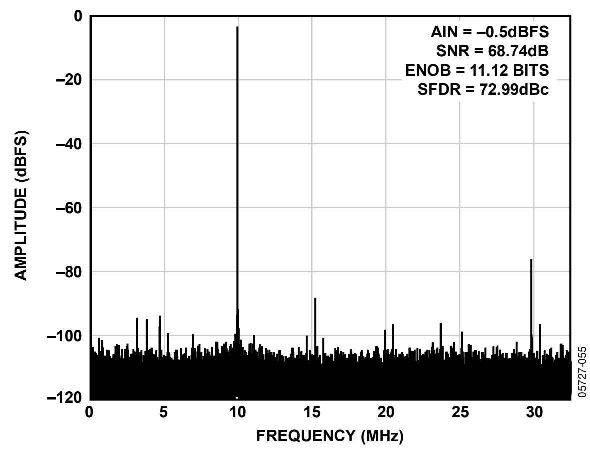


Figure 19. Single-Tone 32k FFT with f_{IN} = 120 MHz, f_{SAMPLE} = 65 MSPS

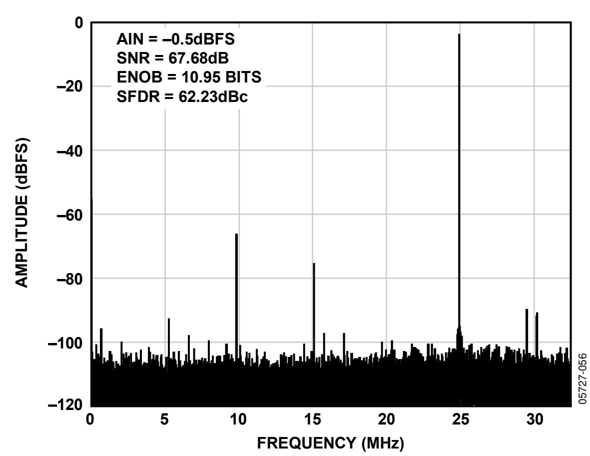


Figure 20. Single-Tone 32k FFT with f_{IN} = 170 MHz, f_{SAMPLE} = 65 MSPS

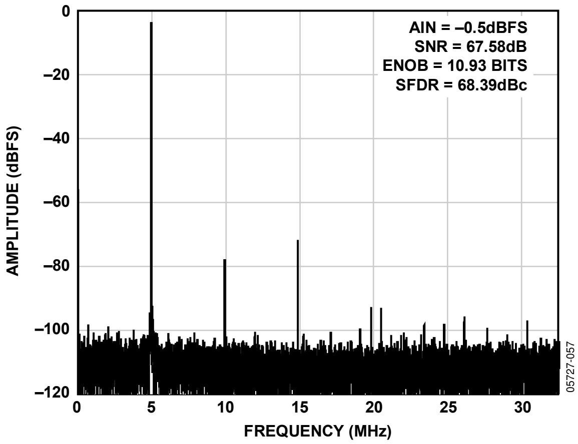


Figure 21. Single-Tone 32k FFT with f_{IN} = 190 MHz, f_{SAMPLE} = 65 MSPS

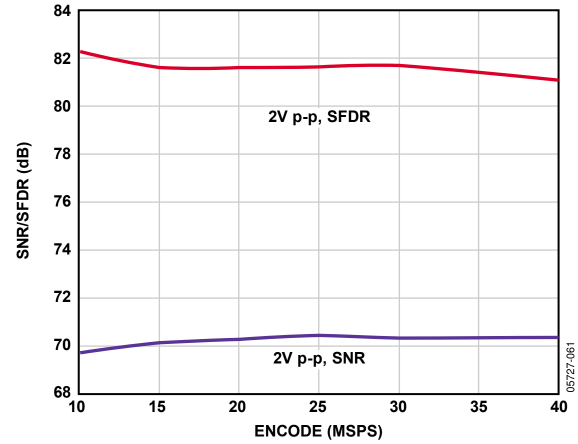


Figure 24. SNR/SFDR vs. Encode, f_{IN} = 35 MHz, f_{SAMPLE} = 40 MSPS

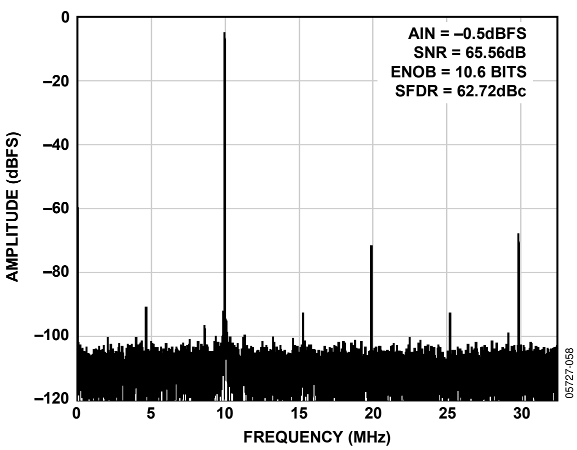


Figure 22. Single-Tone 32k FFT with f_{IN} = 250 MHz, f_{SAMPLE} = 65 MSPS

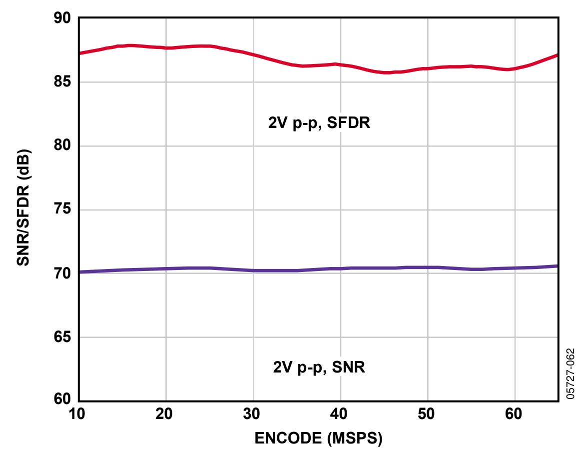


Figure 25. SNR/SFDR vs. Encode, f_{IN} = 10.3 MHz, f_{SAMPLE} = 65 MSPS

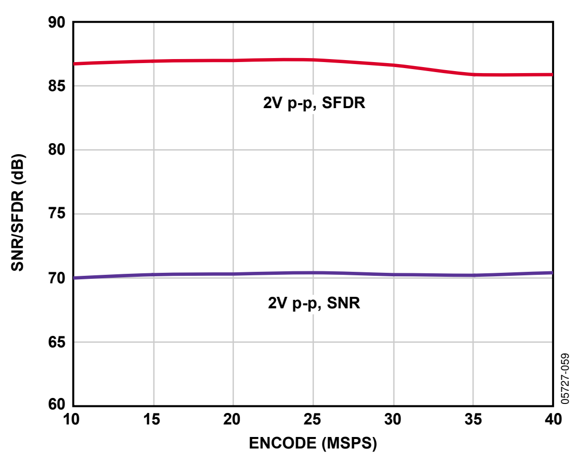


Figure 23. SNR/SFDR vs. Encode, f_{IN} = 10.3 MHz, f_{SAMPLE} = 40 MSPS

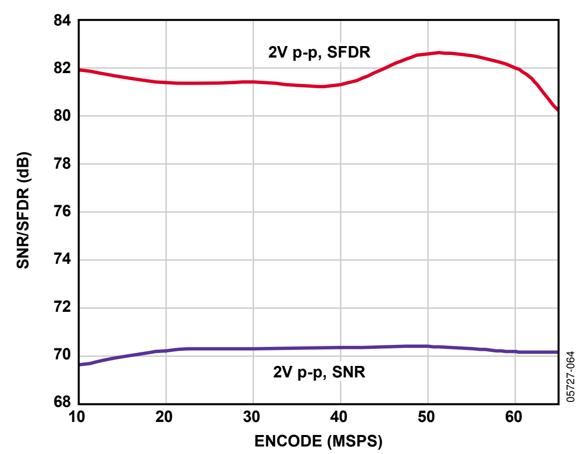


Figure 26. SNR/SFDR vs. Encode, f_{IN} = 35 MHz, f_{SAMPLE} = 65 MSPS

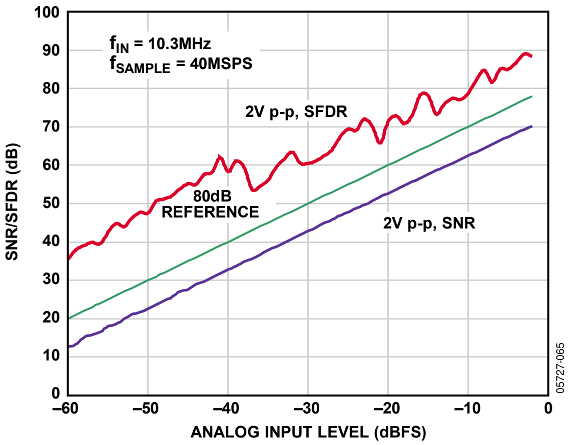


Figure 27. SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz, f_{SAMPLE} = 40 MSPS

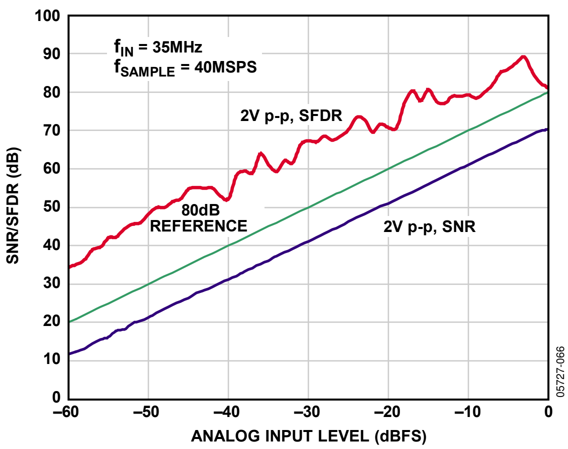


Figure 28. SNR/SFDR vs. Analog Input Level, f_{IN} = 35 MHz, f_{SAMPLE} = 40 MSPS

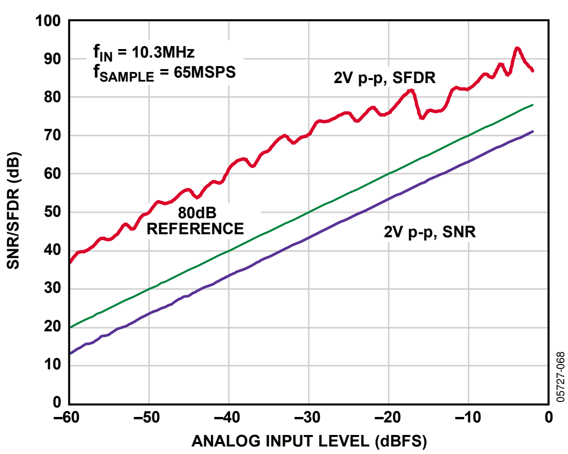


Figure 29. SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz, f_{SAMPLE} = 65 MSPS

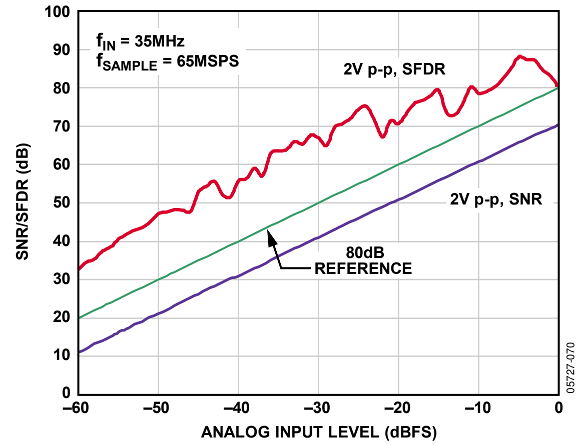


Figure 30. SNR/SFDR vs. Analog Input Level, f_{IN} = 35 MHz, f_{SAMPLE} = 65 MSPS

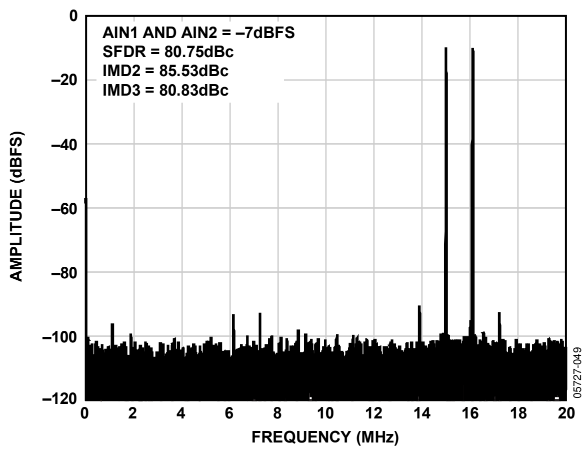


Figure 31. Two-Tone 32k FFT with f_{IN1} = 15 MHz and f_{IN2} = 16 MHz, f_{SAMPLE} = 40 MSPS

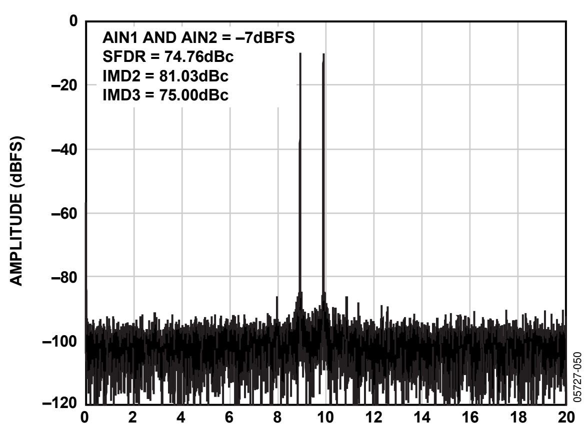


Figure 32. Two-Tone 32k FFT with f_{IN1} = 70 MHz and f_{IN2} = 71 MHz, f_{SAMPLE} = 40 MSPS

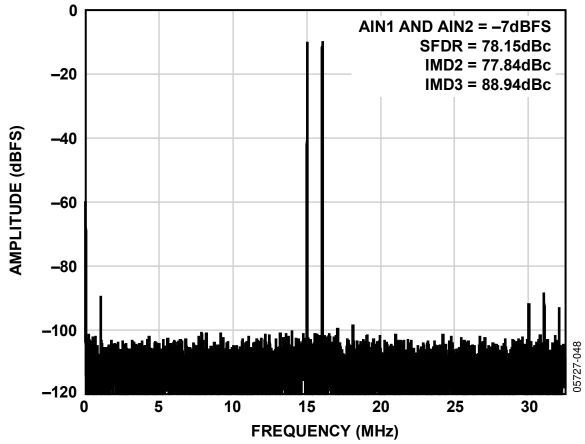


Figure 33. Two-Tone 32k FFT with f_{IN1} = 15 MHz and f_{IN2} = 16 MHz, f_{SAMPLE} = 65 MSPS

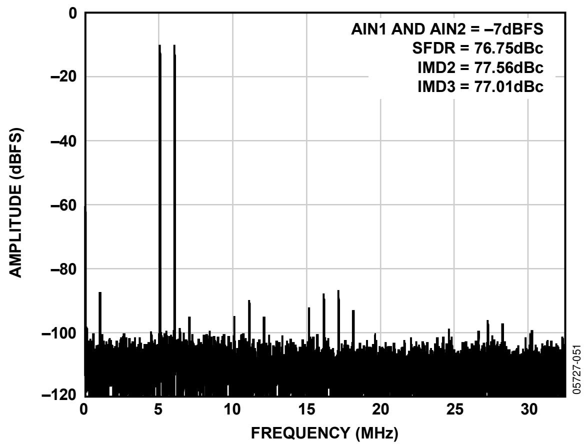


Figure 34. Two-Tone 32k FFT with f_{IN1} = 70 MHz and f_{IN2} = 71 MHz, f_{SAMPLE} = 65 MSPS

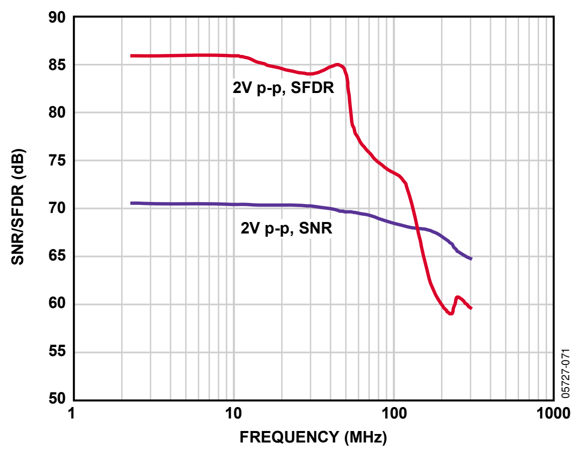


Figure 35. SNR/SFDR vs. Frequency, f_{SAMPLE} = 65 MSPS

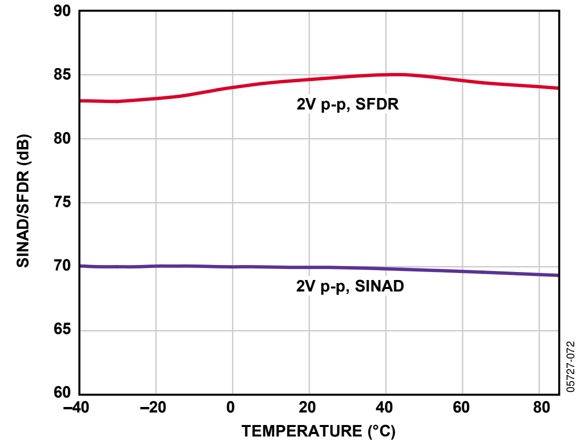


Figure 36. SINAD/SFDR vs. Temperature, f_{IN} = 10.3 MHz, f_{SAMPLE} = 65 MSPS

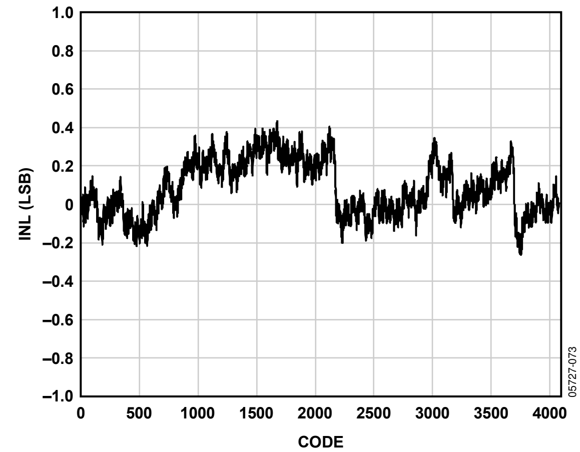


Figure 37. INL, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

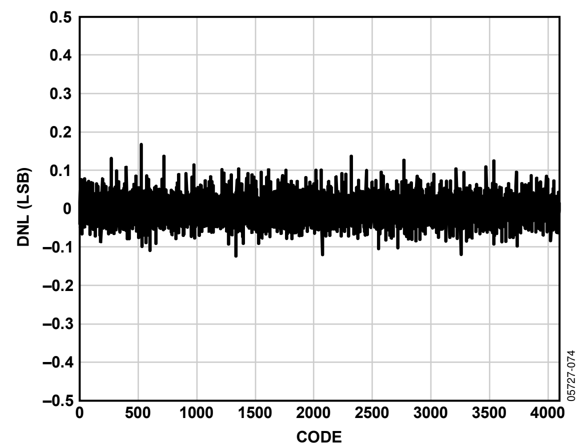


Figure 38. DNL, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

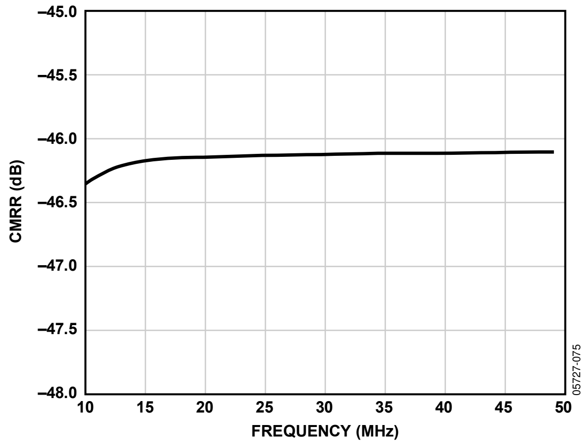


Figure 39. CMRR vs. Frequency, f_{SAMPLE} = 65 MSPS

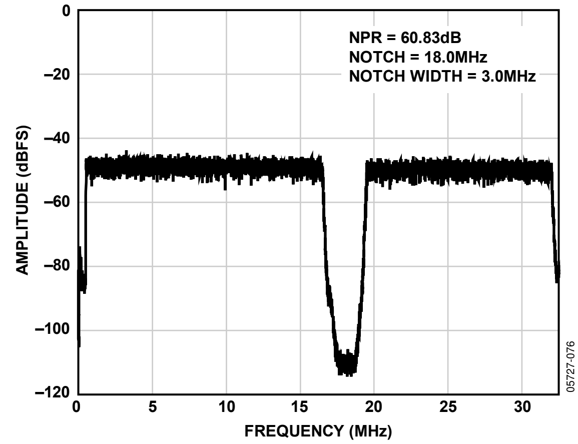


Figure 41. Noise Power Ratio (NPR), f_{SAMPLE} = 65 MSPS

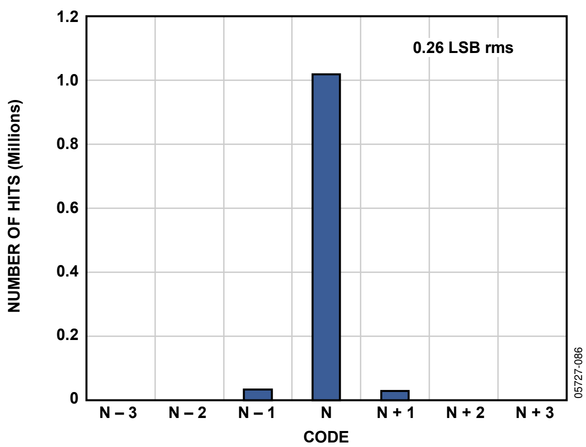


Figure 40. Input-Referred Noise Histogram, f_{SAMPLE} = 65 MSPS

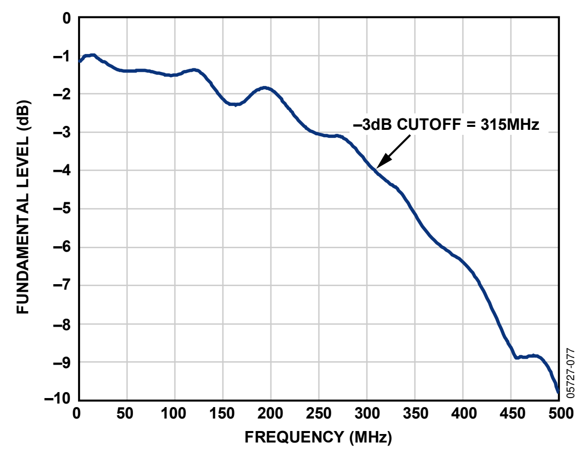


Figure 42. Full-Power Bandwidth vs. Frequency, f_{SAMPLE} = 65 MSPS

THEORY OF OPERATION

The AD9228 architecture consists of a pipelined ADC divided into three sections: a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9228 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

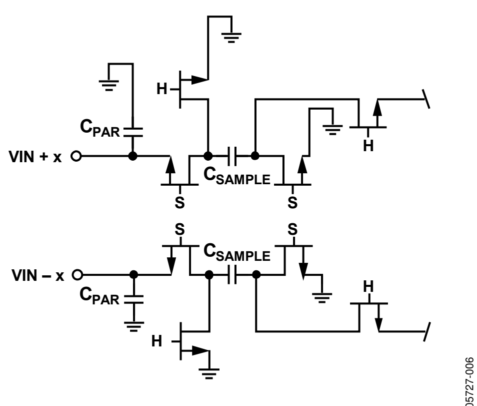


Figure 43. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 43). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low-Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and therefore achieve the maximum bandwidth of the ADC. Such use of low-Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

The analog inputs of the AD9228 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 44 to Figure 47.

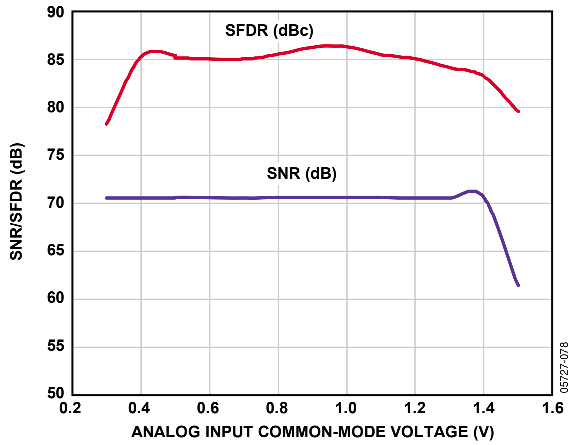


Figure 44. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

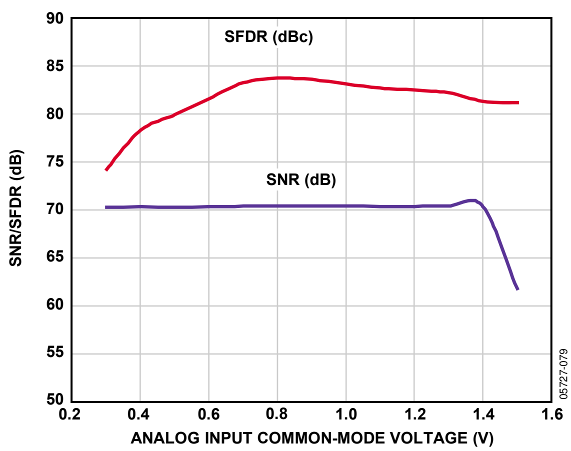


Figure 45. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 30 MHz, f_{SAMPLE} = 65 MSPS

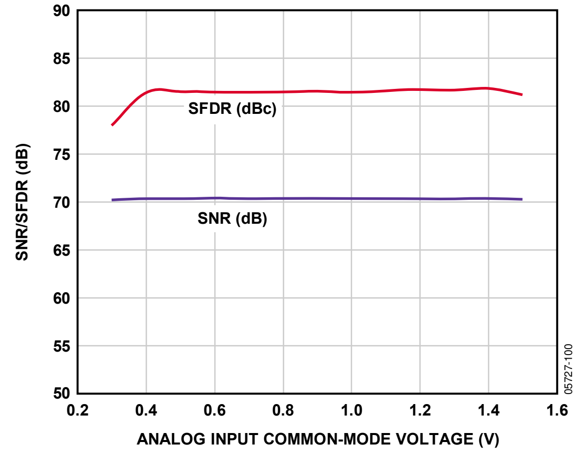


Figure 46. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 2.4 MHz, f_{SAMPLE} = 40 MSPS

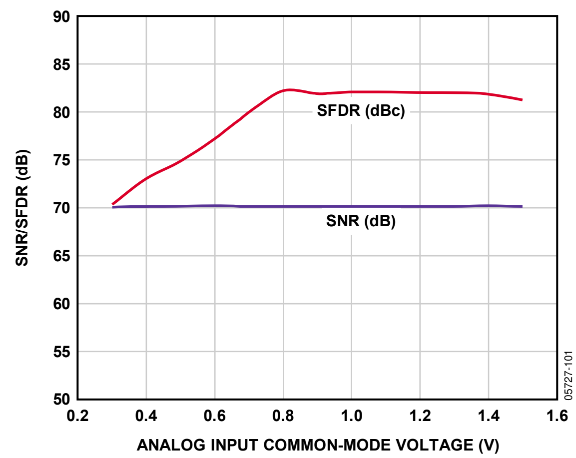


Figure 47. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 30 MHz, f_{SAMPLE} = 40 MSPS

For best dynamic performance, the source impedances driving VIN + x and VIN − x should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates the positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common-mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as

$$REFT = 1/2\ (AVDD + VREF)$$
$$REFB = 1/2\ (AVDD - VREF)$$
$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from these equations that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9228, the largest input span available is 2 V p-p.

Differential Input Configurations

There are several ways to drive the AD9228 either actively or passively; however, optimum performance is achieved by driving the analog input differentially. For example, using the AD8332 differential driver to drive the AD9228 provides excellent performance and a flexible interface to the ADC (see Figure 51) for baseband applications. This configuration is commonly used for medical ultrasound systems.

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 48 and Figure 49), because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9228.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

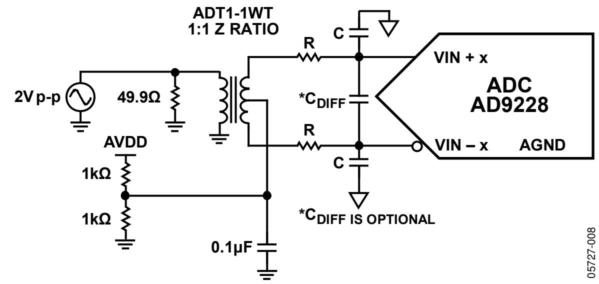


Figure 48. Differential Transformer-Coupled Configuration for Baseband Applications

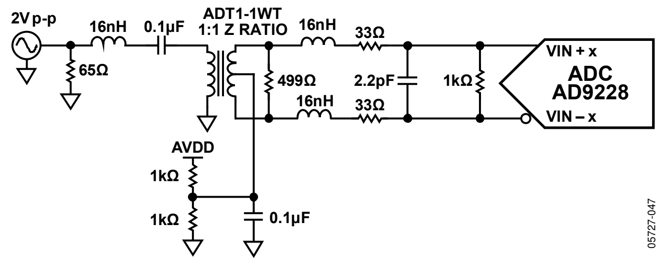


Figure 49. Differential Transformer-Coupled Configuration for IF Applications

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the application requires a single-ended input configuration, ensure that the source impedances on each input are well matched in order to achieve the best possible performance. A full-scale input of 2 V p-p can be applied to the ADC's VIN + x pin while the VIN − x pin is terminated. Figure 50 details a typical single-ended input configuration.

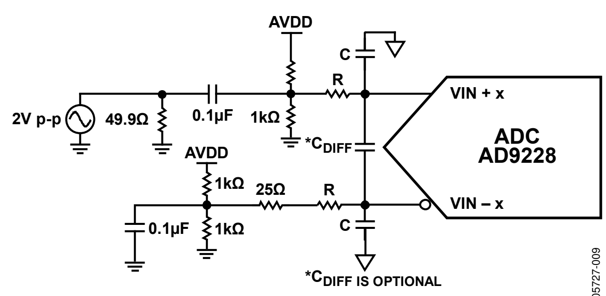


Figure 50. Single-Ended Input Configuration

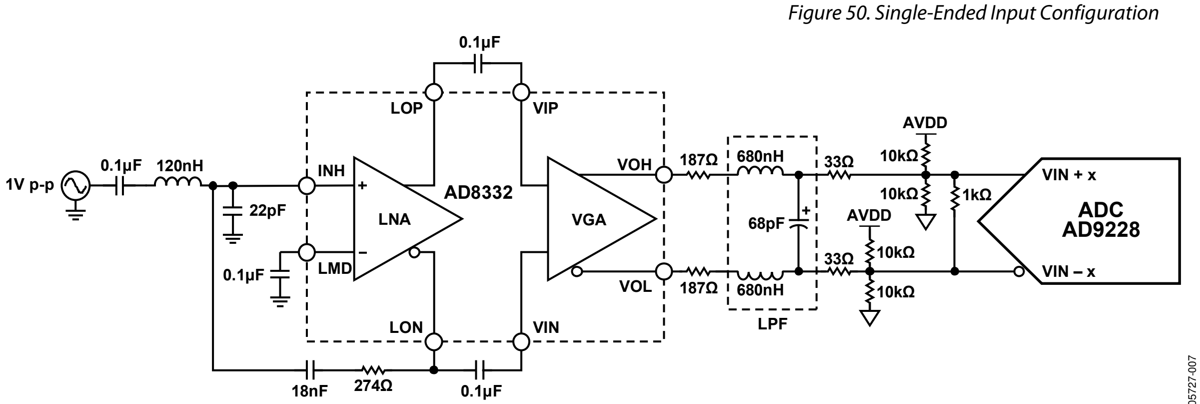


Figure 51. Differential Input Configuration Using the AD8332 with Two-Pole, 16 MHz Low-Pass Filter

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9228 sample clock inputs (CLK+ and CLK–) should be clocked with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally and require no additional biasing.

Figure 52 shows a preferred method for clocking the AD9228. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9228 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9228, and it preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

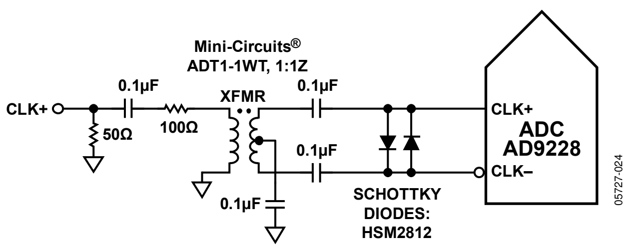


Figure 52. Transformer-Coupled Differential Clock

Another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 53. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

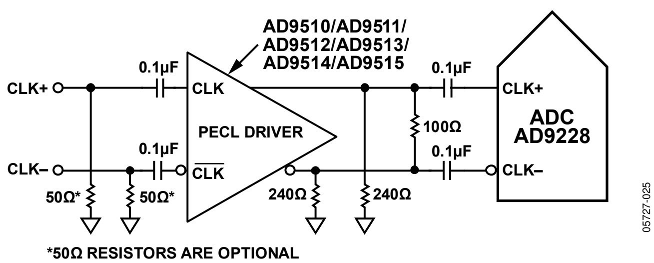


Figure 53. Differential PECL Sample Clock

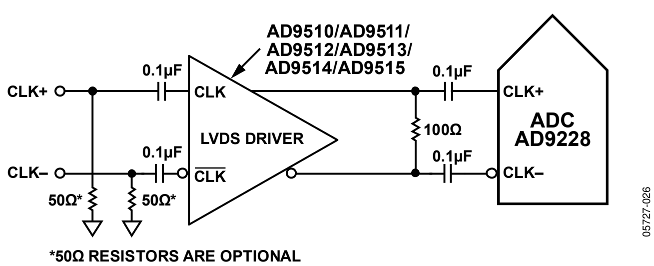


Figure 54. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be driven directly from a CMOS gate, and the CLK– pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 55). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages of up to 3.3 V and therefore offers several selections for the drive logic voltage.

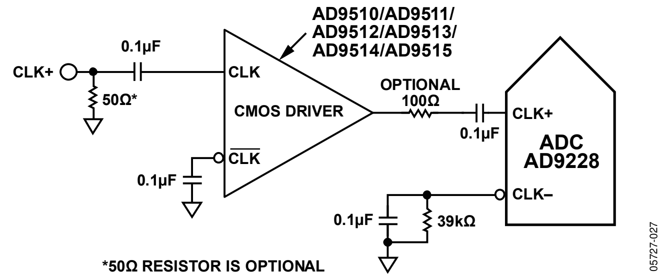


Figure 55. Single-Ended 1.8 V CMOS Sample Clock

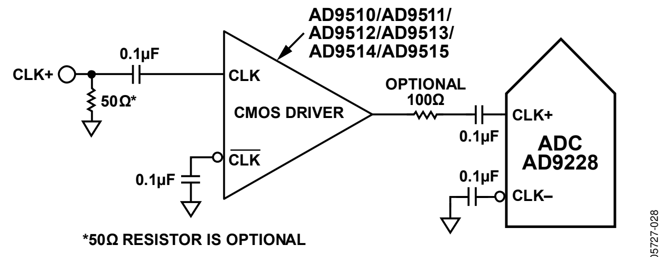


Figure 56. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9228 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9228. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See the Memory Map section for more details on using this feature.

Jitter in the rising edge of the input is an important concern, and it is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 20 MHz nominal. The loop has a time constant associated with it that must be considered in applications where the clock rate can change dynamically. This requires a wait time of 1.5 µs to 5 µs after a dynamic clock frequency increase (or decrease) before the DCS loop is relocked to the input signal. During the period that the loop is not locked, the DCS loop is bypassed and the internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20 \times \log 10(1/2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter (see Figure 57).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9228. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators are the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock during the last step.

Refer to the AN-501 Application Note and to the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

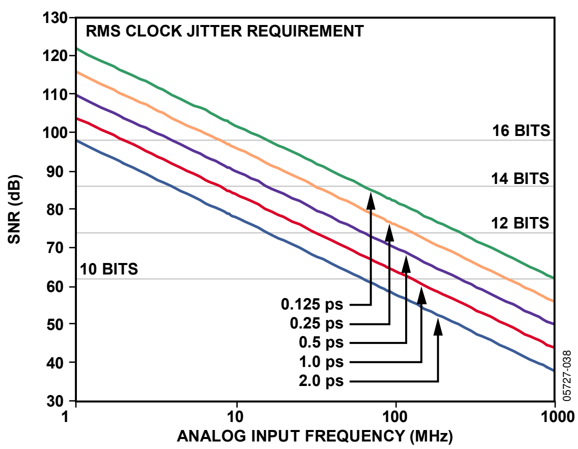


Figure 57. Ideal SNR vs. Input Frequency and Jitter

Power Dissipation and Power-Down Mode

As shown in Figure 58 and Figure 59, the power dissipated by the AD9228 is proportional to its sample rate. The digital power dissipation does not vary significantly because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

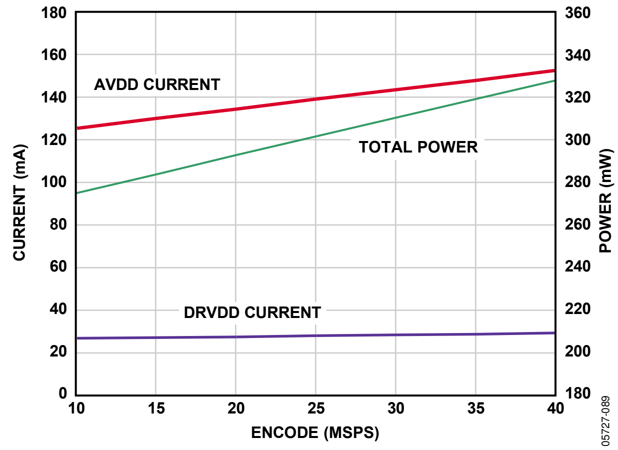


Figure 58. Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz, f_{SAMPLE} = 40 MSPS

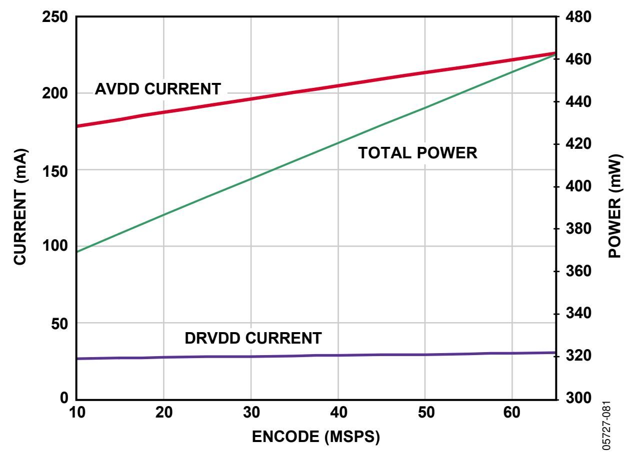


Figure 59. Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz, f_{SAMPLE} = 65 MSPS