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12-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter

AD9230

FEATURES

- SNR = 64.9 dBFS @ f_{IN} up to 70 MHz @ 250 MSPS
- ENOB of 10.4 @ f_{IN} up to 70 MHz @ 250 MSPS (−1.0 dBFS)
- SFDR = −79 dBc @ f_{IN} up to 70 MHz @ 250 MSPS (−1.0 dBFS)
- Excellent linearity
  - DNL = ±0.3 LSB typical
  - INL = ±0.5 LSB typical
- LVDS at 250 MSPS (ANSI-644 levels)
- 700 MHz full power analog bandwidth
- On-chip reference, no external decoupling required
- Integrated input buffer and track-and-hold
- Low power dissipation
  - 434 mW @ 250 MSPS—LVDS SDR mode
  - 400 mW @ 250 MSPS—LVDS DDR mode
- Programmable input voltage range
  - 1.0 V to 1.5 V, 1.25 V nominal
- 1.8 V analog and digital supply operation
- Selectable output data format (offset binary, twos complement, Gray code)
- Clock duty cycle stabilizer
- Integrated data capture clock

APPLICATIONS

- Wireless and wired broadband communications
- Cable reverse path
- Communications test equipment
- Radar and satellite subsystems
- Power amplifier linearization

FUNCTIONAL BLOCK DIAGRAM

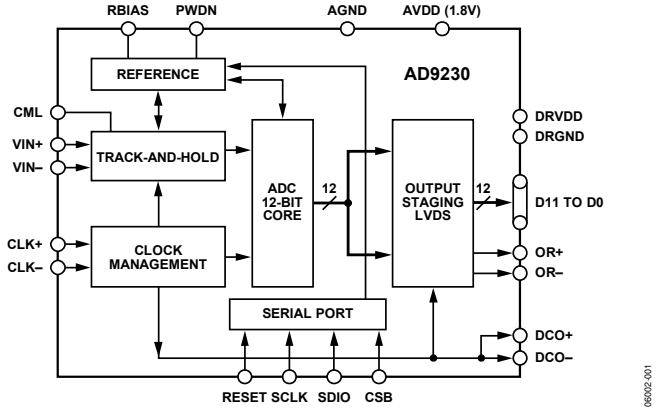

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD9230 is a 12-bit monolithic sampling analog-to-digital converter optimized for high performance, low power, and ease of use. The product operates at up to a 250 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier and broadband systems. All necessary functions, including a track-and-hold (T/H) and voltage reference, are included on the chip to provide a complete signal conversion solution.

The ADC requires a 1.8 V analog voltage supply and a differential clock for full performance operation. The digital outputs are LVDS (ANSI-644) compatible and support either twos complement, offset binary format, or Gray code. A data clock output is available for proper output data timing.

Fabricated on an advanced CMOS process, the AD9230 is available in a 56-lead LFCSP, specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. High Performance—Maintains 64.9 dBFS SNR @ 250 MSPS with a 70 MHz input.
2. Low Power—Consumes only 434 mW @ 250 MSPS.
3. Ease of Use—LVDS output data and output clock signal allow interface to current FPGA technology. The on-chip reference and sample and hold provide flexibility in system design. Use of a single 1.8 V supply simplifies system power supply design.
4. Serial Port Control—Standard serial port interface supports various product functions, such as data formatting, disabling the clock duty cycle stabilizer, power-down, gain adjust, and output test pattern generation.
5. Pin-Compatible Family—10-bit pin-compatible family offered as AD9211.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

AD9230* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9230 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9230: 12-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog
- AD9230 (11-Bit) IBIS Model
- AD9230 IBIS Models

REFERENCE MATERIALS

Technical Articles

- Improve The Design Of Your Passive Wideband ADC Front-End Network
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9230 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9230 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

2/07—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

Table 1.

		AD9230-170			AD9230-210			AD9230-250			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION			12			12			12		Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	25°C		4.2			4.3			4.5		mV
	Full	−12		12	−12		12	−12		12	mV
Gain Error	25°C		0.89			1.0			1.1		mV
	Full	−1.5		3.5	−1.5		3.5	−1.5		3.5	% FS
Differential Nonlinearity	25°C		±0.3			±0.3			±0.3		LSB
(DNL)	Full	−0.5		0.5	−0.5		0.5	−0.6		0.6	LSB
Integral Nonlinearity (INL)	25°C		±0.5			±0.4			±0.5		LSB
	Full	−0.75		0.75	−0.75		0.75	−1.0		+1.0	LSB
TEMPERATURE DRIFT											
Offset Error	Full		±9			±8			±7		µV/°C
Gain Error	Full		0.019			0.021			0.018		%/°C
ANALOG INPUTS (VIN+, VIN−)											
Differential Input Voltage Range[2]	Full	0.98	1.25	1.5	0.98	1.25	1.5	0.98	1.25	1.5	V p-p
Input Common-Mode Voltage	Full		1.4			1.4			1.4		V
Input Resistance (Differential)	Full		4.3			4.3			4.3		kΩ
Input Capacitance	25°C		2			2			2		pF
POWER SUPPLY											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9				V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9				V
Supply Currents											
I_{AVDD}[3]	Full		136	145		154	164		181	194	mA
I_{DRVDD}[3]/SDR Mode[4]	Full		58	61		59	62		60	63	mA
I_{DRVDD}[3]/DDR Mode[5]	Full		39			40			41		mA
Power Dissipation[3]	Full										mW
SDR Mode[4]	Full		349	371		383	407		434	463	mW
DDR Mode[5]	Full		315			349			400		mW

[1] See the AN-835 Application Note, "Understanding High Speed ADC Testing and Evaluation," for a complete set of definitions and how these tests were completed.
[2] The input range is programmable through the SPI, and the range specified reflects the nominal values of each setting. See the Memory Map section.
[3] I_{AVDD} and I_{DRVDD} are measured with a −1 dBFS, 10.3 MHz sine input at rated sample rate.
[4] Single data rate mode; this is the default mode of the AD9230.
[5] Double data rate mode; user-programmable feature. See the Memory Map section.

AC SPECIFICATIONS[1]

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

Table 2.

		AD9230-170			AD9230-210			AD9230-250			
Parameter[2]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SNR											
f_{IN} = 10 MHz	25°C	63.8	64.6		63.7	64.5		63.3	64.1		dB
	Full	63.5			63.4			62.5			dB
f_{IN} = 70 MHz	25°C	63.5	64.3		63.3	64.2		63.0	63.9		dB
	Full	63.3			63.1			62.3			dB
f_{IN} = 170 MHz[3]	25°C		63.5			63.4			63.3		dB
f_{IN} = 225 MHz	25°C		63.0			61.5			63.3		dB
SINAD											
f_{IN} = 10 MHz	25°C	63.7	64.5		63.6	64.4		63.3	64.0		dB
	Full	63.4			63.4			62.4			dB
f_{IN} = 70 MHz	25°C	63.3	64.1		63.2	64.0		62.9	63.7		dB
	Full	63.1			63.0			62.2			dB
f_{IN} = 170 MHz[3]	25°C		63.3			63.1			63.0		dB
f_{IN} = 225 MHz	25°C		61.8			61.1			62.8		dB
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 10 MHz	25°C		10.6			10.6			10.5		Bits
f_{IN} = 70 MHz	25°C		10.5			10.5			10.4		Bits
f_{IN} = 170 MHz[3]	25°C		10.4			10.4			10.3		Bits
f_{IN} = 225 MHz	25°C		10.1			10.0			10.3		Bits
WORST HARMONIC (Second or Third)											
f_{IN} = 10 MHz	25°C		−82	−78		−86	−80		−84	−79	dBc
	Full			−78			−78			−76	dBc
f_{IN} = 70 MHz	25°C		−78	−76		−80	−77		−79	−76	dBc
	Full			−75			−75			−75	dBc
f_{IN} = 170 MHz[3]	25°C		−78			−79			−78		dBc
f_{IN} = 225 MHz	25°C		−68			−70			−75		dBc
WORST OTHER (SFDR Excluding Second and Third)											
f_{IN} = 10 MHz	25°C		−89	−84		−89	−84		−84	−79	dBc
	Full			−83			−83			−76	dBc
f_{IN} = 70 MHz	25°C		−89	−83		−86	−81		−83	−79	dBc
	Full			−83			−81			−75	dBc
f_{IN} = 170 MHz[3]	25°C		−89			−79			−83		dBc
f_{IN} = 225 MHz	25°C		−80			−79			−80		dBc
TWO-TONE IMD											
140.2 MHz/141.3 MHz @ −7 dBFS	25°C		73			75			78		dBc
170.2 MHz/171.3 MHz @ −7 dBFS	25°C					67			73		dBc
ANALOG INPUT BANDWIDTH	25°C		700			700			700		MHz

[1] All ac specifications tested by driving CLK+ and CLK− differentially.
[2] See the AN-835 Application Note, "Understanding High Speed ADC Testing and Evaluation," for a complete set of definitions and how these tests were completed.
[3] 140 MHz for the AD9230-170 speed grade, 170 MHz for the AD9230-210 and AD9230-250 speed grades.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

Table 3.

		AD9230-170			AD9230-210			AD9230-250			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUTS											
Logic Compliance	Full		CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		1.2			1.2			1.2		V
Differential Input Voltage	Full	0.2		6	0.2		6	0.2		6	V p-p
Input Voltage Range	Full	AVDD − 0.3		AVDD + 1.6	AVDD − 0.3		AVDD + 1.6	AVDD − 0.3		AVDD + 1.6	V
Input Common-Mode Range	Full	1.1		AVDD	1.1		AVDD	1.1		AVDD	V
High Level Input Voltage (V_{IH})	Full	1.2		3.6	1.2		3.6	1.2		3.6	V
Low Level Input Voltage (V_{IL})	Full	0		0.8	0		0.8	0		0.8	V
High Level Input Current (I_{IH})	Full	−10		+10	−10		+10	−10		+10	µA
Low Level Input Current (I_{IL})	Full	−10		+10	−10		+10	−10		+10	µA
Input Resistance (Differential)	Full	16	20	24	16	20	24	16	20	24	kΩ
Input Capacitance	Full		4			4			4		pF
LOGIC INPUTS											
Logic 1 Voltage	Full	0.8 × VDD			0.8 × VDD			0.8 × VDD			V
Logic 0 Voltage	Full			0.2 × AVDD			0.2 × AVDD			0.2 × AVDD	V
Logic 1 Input Current (SDIO)	Full		0			0			0		µA
Logic 0 Input Current (SDIO)	Full		−60			−60			−60		µA
Logic 1 Input Current (SCLK, PDWN, CSB, RESET)	Full		55			55			50		µA
Logic 0 Input Current (SCLK, PDWN, CSB, RESET)	Full		0			0			0		µA
Input Capacitance	25°C		4			4			4		pF
LOGIC OUTPUTS[2]											
V_{OD} Differential Output Voltage	Full	247		454	247		454	247		454	mV
V_{OS} Output Offset Voltage	Full	1.125		1.375	1.125		1.375	1.125		1.375	V
Output Coding		Twos complement, Gray code, or offset binary (default)									

[1] See the AN-835 Application Note, "Understanding High Speed ADC Testing and Evaluation," for a complete set of definitions and how these tests were completed.
[2] LVDS $R_{TERMINATION}$ = 100 Ω.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

Table 4.

		AD9230-170			AD9230-210			AD9230-250			
Parameter (Conditions)	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**				**Unit**
Maximum Conversion Rate	Full	170			210			250			MSPS
Minimum Conversion Rate	Full			40			40			40	MSPS
CLK+ Pulse Width High (t_{CH})	Full	2.65	2.9		2.15	2.4		1.8	2.0		ns
CLK+ Pulse Width Low (t_{CL})	Full	2.65	2.9		2.15	2.4		1.8	2.0		ns
Output (LVDS – SDR Mode)[1]											
Data Propagation Delay (t_{PD})	Full		3.0			3.0			3.0		ns
Rise Time (t_R) (20% to 80%)	25°C		0.2			0.2			0.2		ns
Fall Time (t_F) (20% to 80%)	25°C		0.2			0.2			0.2		ns
DCO Propagation Delay (t_{CPD})	Full		3.9			3.9			3.9		ns
Data to DCO Skew (t_{SKEW})	Full	−0.3	0.1	0.5	−0.3	0.1	0.5	−0.3	0.1	0.5	ns
Latency	Full		7			7			7		Cycles
Output (LVDS – DDR Mode)[2]											
Data Propagation Delay (t_{PD})	Full		3.8			3.8			3.8		ns
Rise Time (t_R) (20% to 80%)	25°C		0.2			0.2			0.2		ns
Fall Time (t_F) (20% to 80%)	25°C		0.2			0.2			0.2		ns
DCO Propagation Delay (t_{CPD})	Full		3.9			3.9			3.9		ns
Data to DCO Skew (t_{SKEW})	Full	−0.5	0.1	0.3	−0.5	0.1	0.3	−0.5	0.1	0.3	ns
Latency	Full		7			7			7		Cycles
Aperture Uncertainty (Jitter, t_J)	25°C		0.2			0.2					ps rms

[1] See Figure 2.
[2] See Figure 3.

TIMING DIAGRAMS

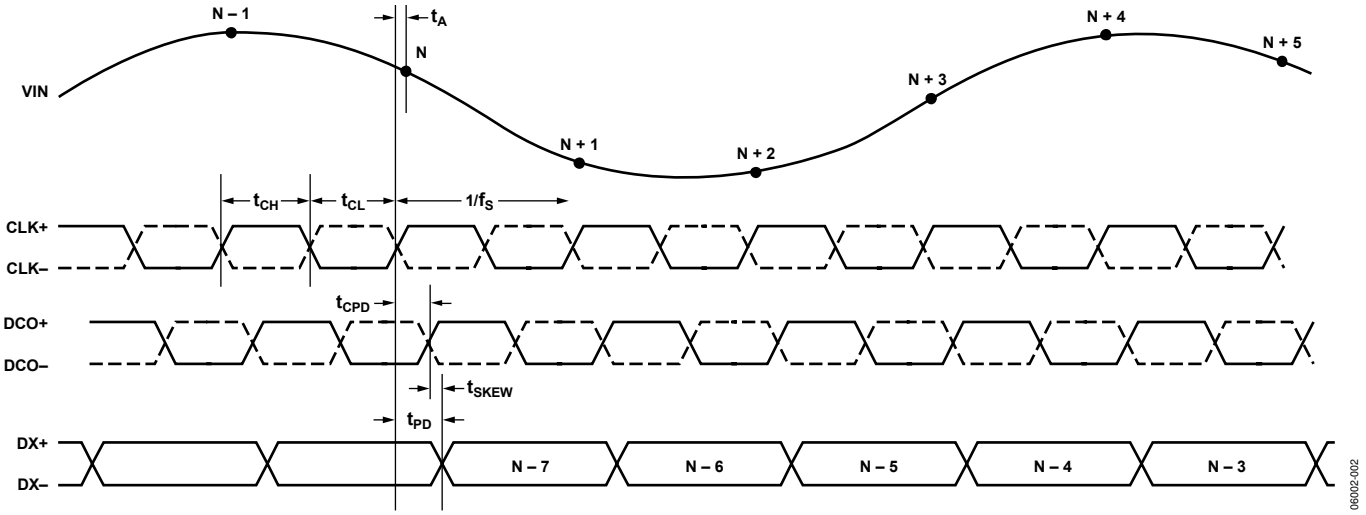

Figure 2. Single Data Rate Mode

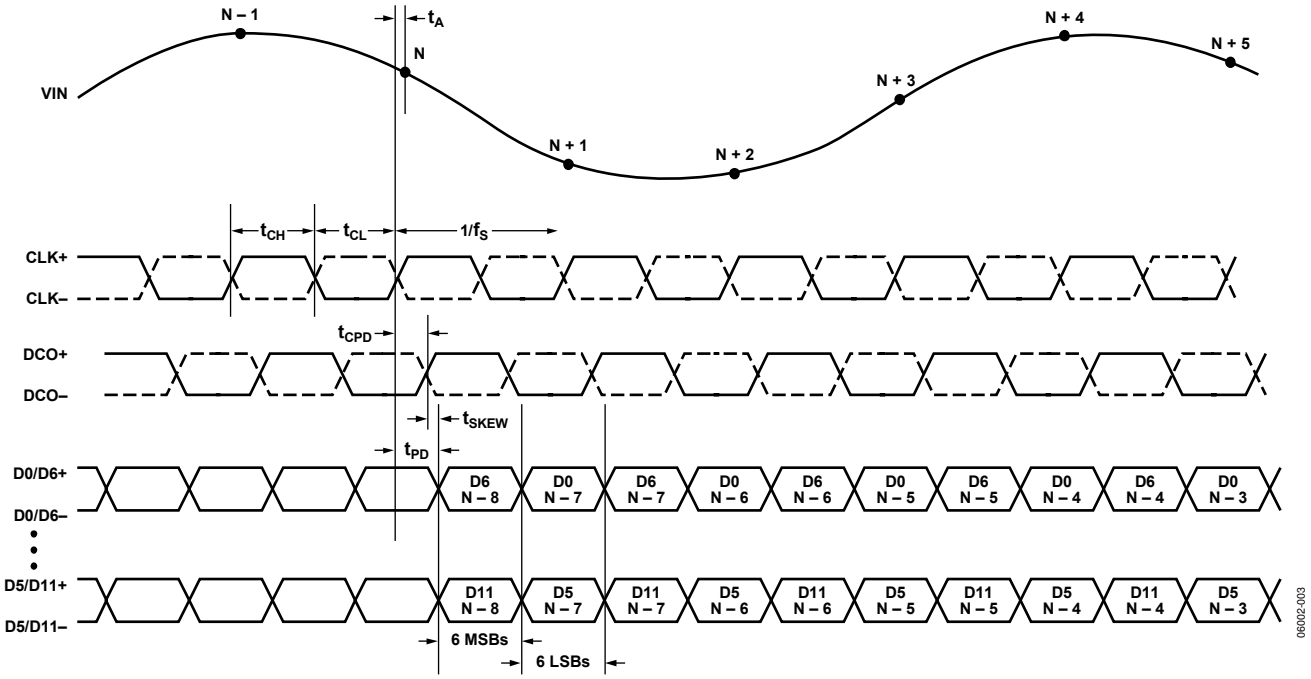

Figure 3. Double Data Rate Mode

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +2.0 V
AGND to DRGND	−0.3 V to +0.3 V
AVDD to DRVDD	−2.0 V to +2.0 V
D0+/D0− through D13+/D13− to DRGND	−0.3 V to DRVDD + 0.3 V
DCO to DRGND	−0.3 V to DRVDD + 0.3 V
OR to DGND	−0.3 V to DRVDD + 0.3 V
CLK+ to AGND	−0.3 V to +3.9 V
CLK− to AGND	−0.3 V to +3.9 V
VIN+ to AGND	−0.3 V to AVDD + 0.2 V
VIN− to AGND	−0.3 V to AVDD + 0.2 V
SDIO/DCS to DGND	−0.3 V to DRVDD + 0.3 V
PDWN to AGND	−0.3 V to +3.9 V
CSB to AGND	−0.3 V to +3.9 V
SCLK/DFS to AGND	−0.3 V to +3.9 V
ENVIRONMENTAL	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 6.

Package Type	θ_{JA}	θ_{JC}	Unit
56-Lead LFCSP (CP-48-3)	30.4	2.9	°C/W

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, and through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

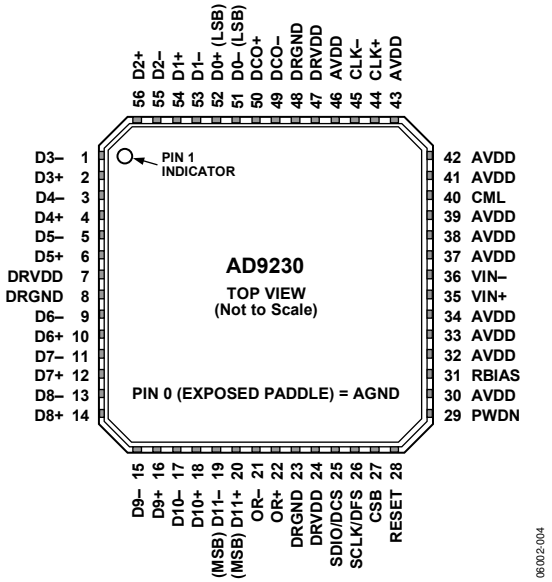

Figure 4. Single Data Rate Mode

Table 7. Single Data Rate Mode Pin Function Descriptions

Pin No.	Mnemonic	Description
30, 32 to 34, 37 to 39, 41 to 43, 46	AVDD	1.8 V Analog Supply.
7, 24, 47	DRVDD	1.8 V Digital Output Supply.
0	AGND[1]	Analog Ground.
8, 23, 48	DRGND[1]	Digital Output Ground.
35	VIN+	Analog Input—True.
36	VIN–	Analog Input—Complement.
40	CML	Common-Mode Output Pin. Enabled through the SPI, this pin provides a reference for the optimized internal bias voltage for VIN+/VIN–.
44	CLK+	Clock Input—True.
45	CLK–	Clock Input—Complement.
31	RBIAS	Set Pin for Chip Bias Current. (Place 1% 10 kΩ resistor terminated to ground.) Nominally 0.5 V.
28	RESET	CMOS-Compatible Chip Reset (Active Low).
25	SDIO/DCS	Serial Port Interface (SPI®) Data Input/Output (Serial Port Mode); Duty Cycle Stabilizer Select (External Pin Mode).
26	SCLK/DFS	Serial Port Interface Clock (Serial Port Mode); Data Format Select Pin (External Pin Mode).
27	CSB	Serial Port Chip Select (Active Low).
29	PWDN	Chip Power-Down.
49	DCO–	Data Clock Output—Complement.
50	DCO+	Data Clock Output—True.
51	D0–	D0 Complement Output Bit (LSB).
52	D0+	D0 True Output Bit (LSB).
53	D1–	D1 Complement Output Bit.
54	D1+	D1 True Output Bit.
55	D2–	D2 Complement Output Bit.
56	D2+	D2 True Output Bit.
1	D3–	D3 Complement Output Bit.
2	D3+	D3 True Output Bit.
3	D4–	D4 Complement Output Bit.
4	D4+	D4 True Output Bit.

Pin No.	Mnemonic	Description
5	D5–	D5 Complement Output Bit.
6	D5+	D5 True Output Bit.
9	D6–	D6 Complement Output Bit.
10	D6+	D6 True Output Bit.
11	D7–	D7 Complement Output Bit.
12	D7+	D7 True Output Bit.
13	D8–	D8 Complement Output Bit.
14	D8+	D8 True Output Bit.
15	D9–	D9 Complement Output Bit.
16	D9+	D9 True Output Bit.
17	D10–	D10 Complement Output Bit.
18	D10+	D10 True Output Bit.
19	D11–	D11 Complement Output Bit (MSB).
20	D11+	D11 True Output Bit (MSB).
21	OR–	Overrange Complement Output Bit.
22	OR+	Overrange True Output Bit.

[1] AGND and DRGND should be tied to a common quiet ground plane.

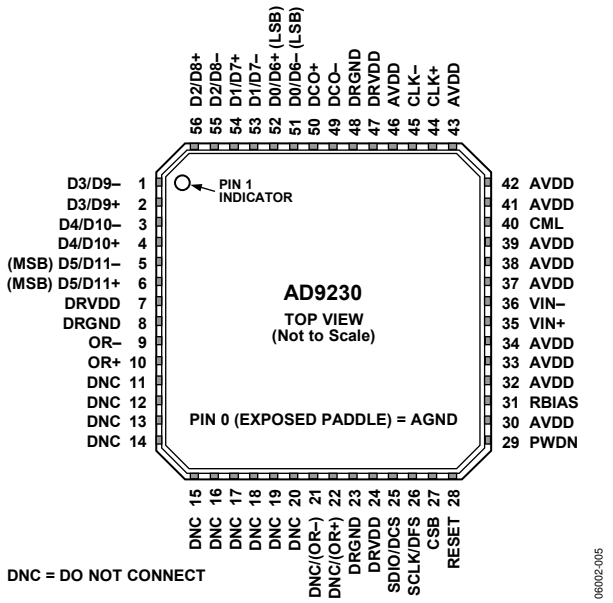

Figure 5. Double Data Rate

Table 8. Double Data Rate Mode Pin Function Descriptions

Pin No.	Mnemonic	Description
30, 32 to 34, 37 to 39, 41 to 43, 46	AVDD	1.8 V Analog Supply.
7, 24, 47	DRVDD	1.8 V Digital Output Supply.
0	AGND[1]	Analog Ground.
8, 23, 48	DRGND[1]	Digital Output Ground.
35	VIN+	Analog Input—True.
36	VIN–	Analog Input—Complement.
40	CML	Common-Mode Output Pin. Enabled through the SPI, this pin provides a reference for the optimized internal bias voltage for VIN+/VIN–.
44	CLK+	Clock Input—True.
45	CLK–	Clock Input—Complement.
31	RBIAS	Set Pin for Chip Bias Current. (Place 1% 10 kΩ resistor terminated to ground.) Nominally 0.5 V.
28	RESET	CMOS-Compatible Chip Reset (Active Low).
25	SDIO/DCS	Serial Port Interface (SPI) Data Input/Output (Serial Port Mode); Duty Cycle Stabilizer Select (External Pin Mode).
26	SCLK/DFS	Serial Port Interface Clock (Serial Port Mode); Data Format Select Pin (External Pin Mode).
27	CSB	Serial Port Chip Select (Active Low).
29	PWDN	Chip Power-Down.
49	DCO–	Data Clock Output—Complement.
50	DCO+	Data Clock Output—True.
51	D0/D6–	D0/D6 Complement Output Bit (LSB).
52	D0/D6+	D0/D6 True Output Bit (LSB).
53	D1/D7–	D1/D7 Complement Output Bit.
54	D1/D7+	D1/D7 True Output Bit.
55	D2/D8–	D2/D8 Complement Output Bit.
56	D2/D8+	D2/D8 True Output Bit.
1	D3/D9–	D3/D9 Complement Output Bit.
2	D3/D9+	D3/D9 True Output Bit.
3	D4/D10–	D4/D10 Complement Output Bit.
4	D4/D10+	D4/D10 True Output Bit.
5	D5/D11–	D5/D11 Complement Output Bit (MSB).
6	D5/D11+	D5/D11 True Output Bit (MSB).

Pin No.	Mnemonic	Description
9	OR–	D6 Complement Output Bit. (This pin is disabled if Pin 21 is reconfigured through the SPI to be OR–.)
10	OR+	D6 True Output Bit. (This pin is disabled if Pin 22 is reconfigured through the SPI to be OR+.)
11 to 20	DNC	Do Not Connect.
21	DNC/(OR–)	Do Not Connect. (This pin can be reconfigured as the Overrange Complement Output Bit through the serial port register.)
22	DNC/(OR+)	Do Not Connect. (This pin can be reconfigured as the Overrange True Output Bit through the serial port register.)

[1] AGND and DRGND should be tied to a common quiet ground plane.

EQUIVALENT CIRCUITS

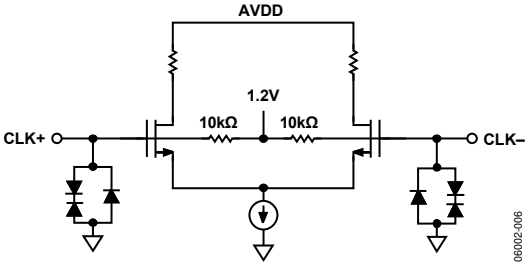

Figure 6. Clock Inputs

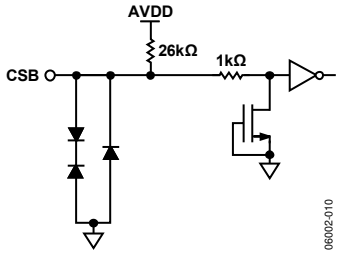

Figure 9. Equivalent CSB Input Circuit

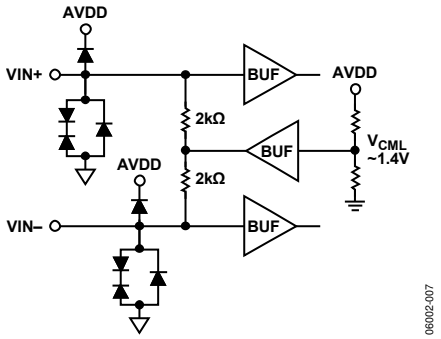

Figure 7. Analog Inputs (V_{CML} = ~1.4 V)

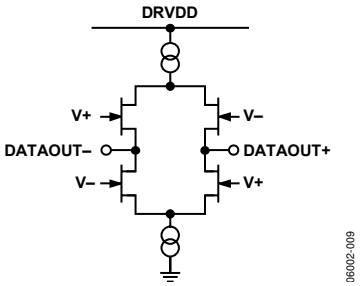

Figure 10. LVDS Outputs (Dx+, Dx–, OR+, OR–, DCO+, DCO–)

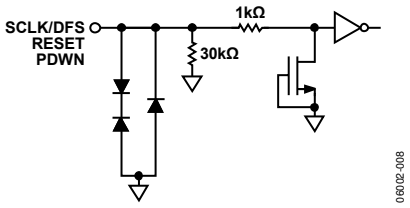

Figure 8. Equivalent SCLK/DFS, RESET, PDWN Input Circuit

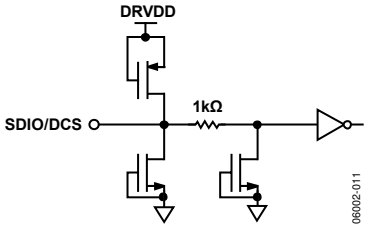

Figure 11. Equivalent SDIO/DCS Input Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, rated sample rate, DCS enabled, T_A = 25°C, 1.25 V p-p differential input, AIN = −1 dBFS, unless otherwise noted.

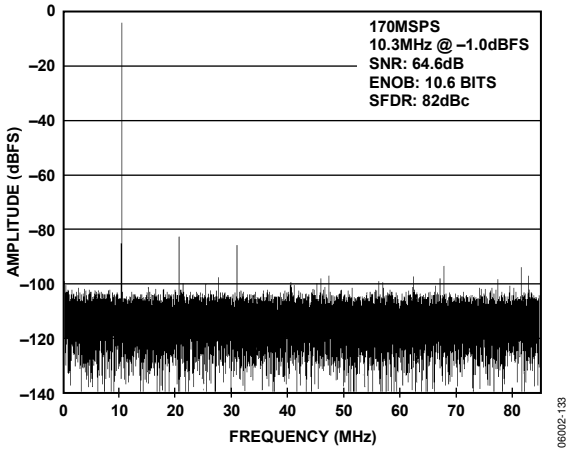

Figure 12. AD9230-170 64k Point Single-Tone FFT; 170 MSPS, 10.3 MHz

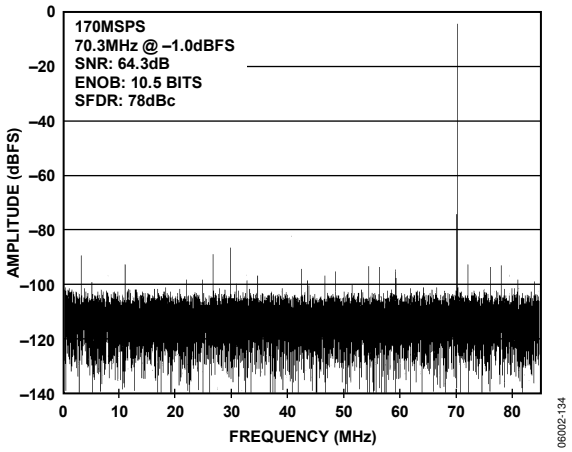

Figure 13. AD9230-170 64k Point Single-Tone FFT; 170 MSPS, 70.3 MHz

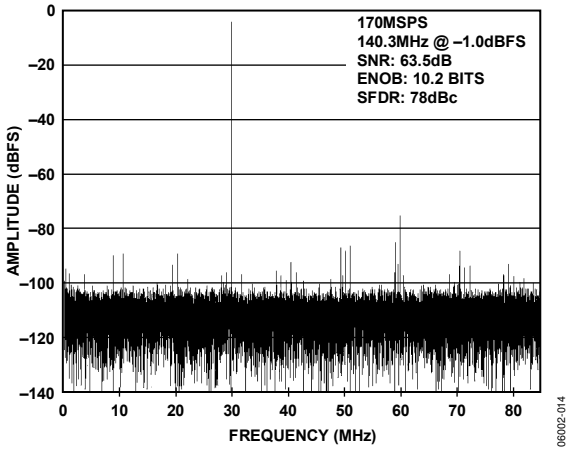

Figure 14. AD9230-170 64k Point Single-Tone FFT; 170 MSPS, 140.3 MHz

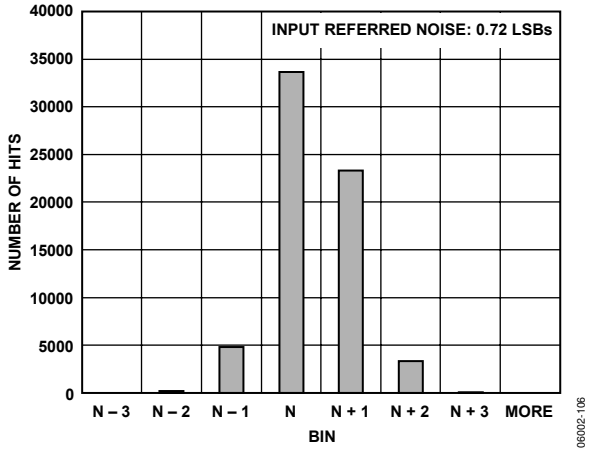

Figure 15. AD9230-170 Grounded Input Histogram; 170 MSPS

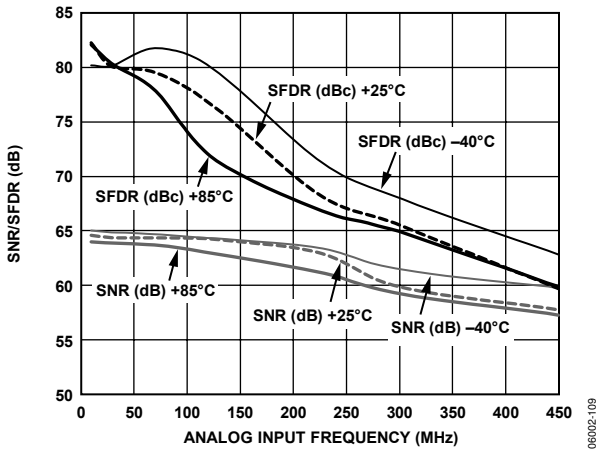

Figure 16. AD9230-170 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1.25 V p-p Full Scale; 170 MSPS

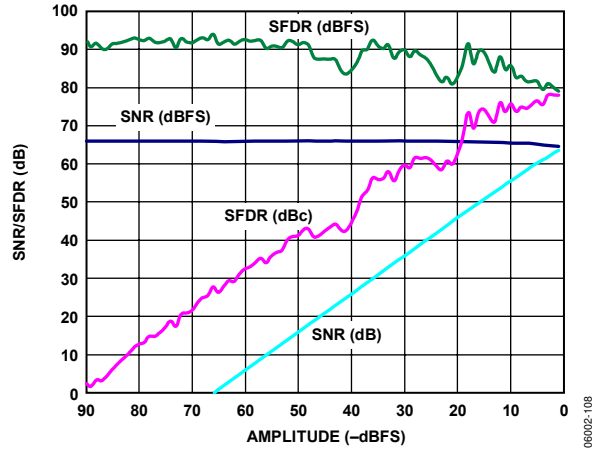

Figure 17. AD9230-170 SNR/SFDR vs. Input Amplitude; 140.3 MHz

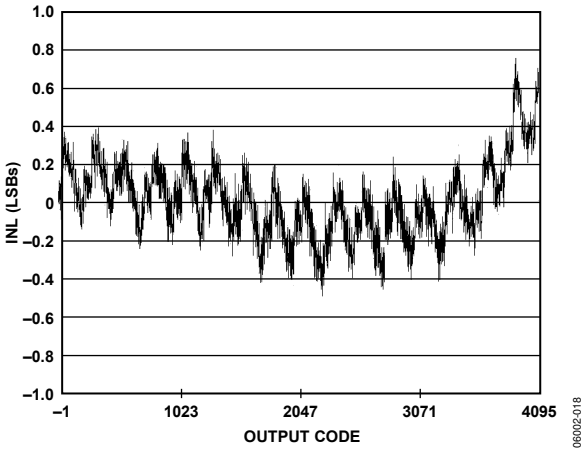

Figure 18. AD9230-170 INL; 170 MSPS

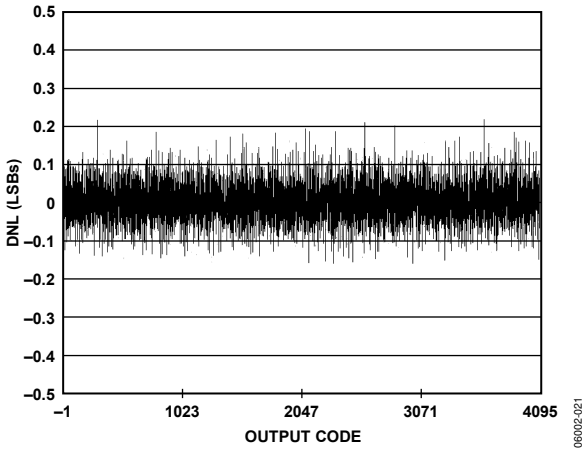

Figure 21. AD9230-170 DNL; 170 MSPS

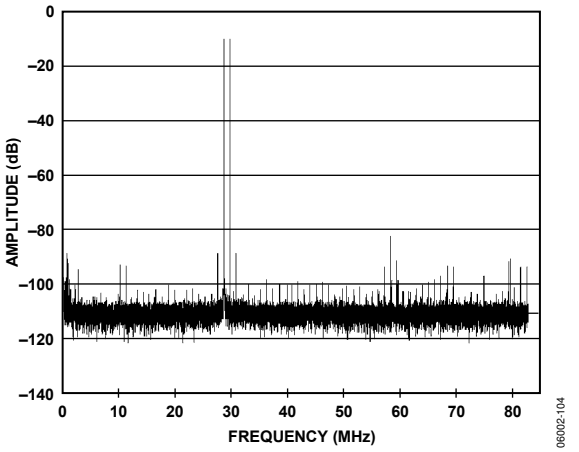

Figure 19. AD9230-170 64k Point, Two-Tone FFT; 170 MSPS, 140.1 MHz, 141.1 MHz

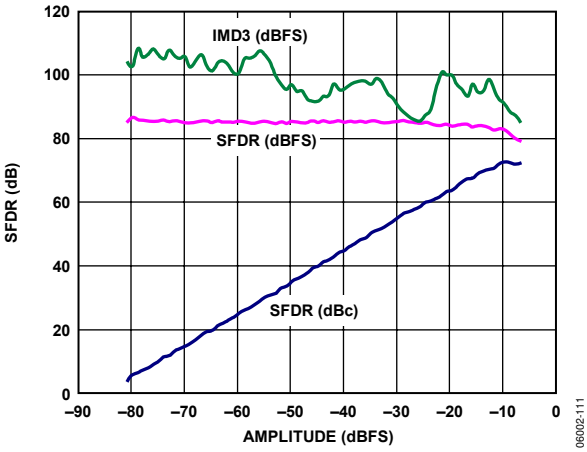

Figure 22. AD9230-170 Two-Tone SFDR vs. Input Amplitude; 170 MSPS, 140.1 MHz, 141.1 MHz

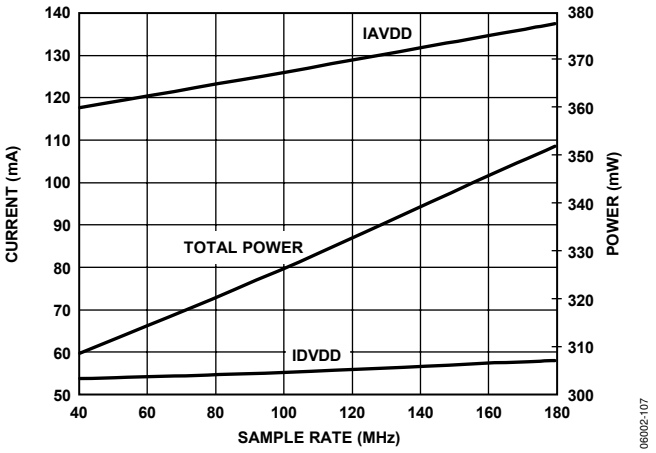

Figure 20. AD9230-170 Power Supply Current vs. Sample Rate

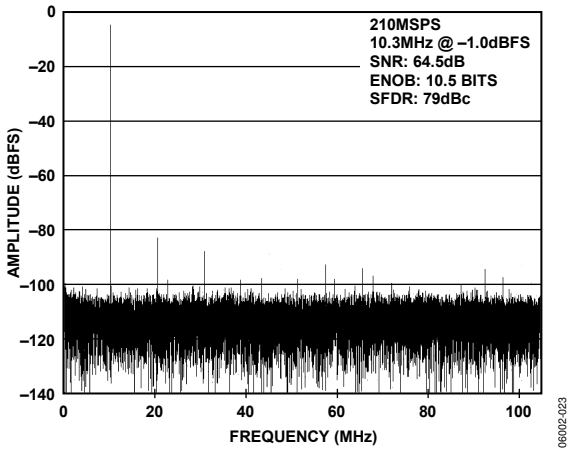

Figure 23. AD9230-210 64k Point Single-Tone FFT; 210 MSPS, 10.3 MHz

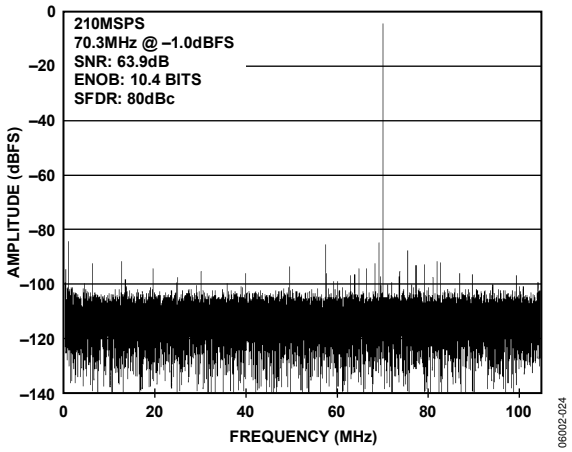

Figure 24. AD9230-210 64k Point Single-Tone FFT; 210 MSPS, 70.3 MHz

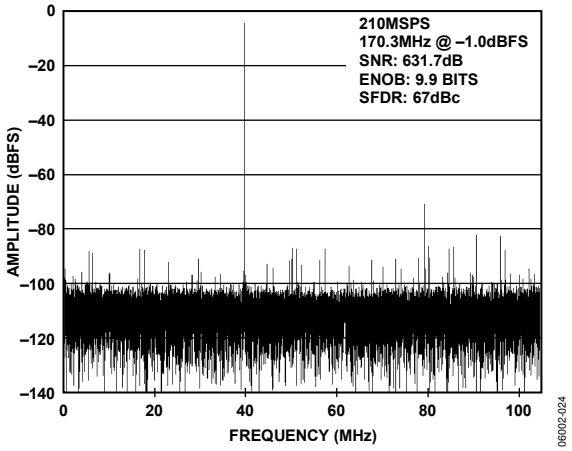

Figure 25. AD9230-210 64k Point Single-Tone FFT; 210 MSPS, 170.3 MHz

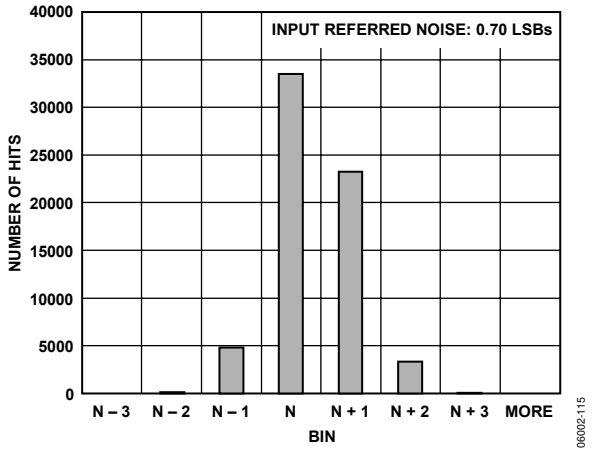

Figure 26. AD9230-210 Grounded Input Histogram; 210 MSPS

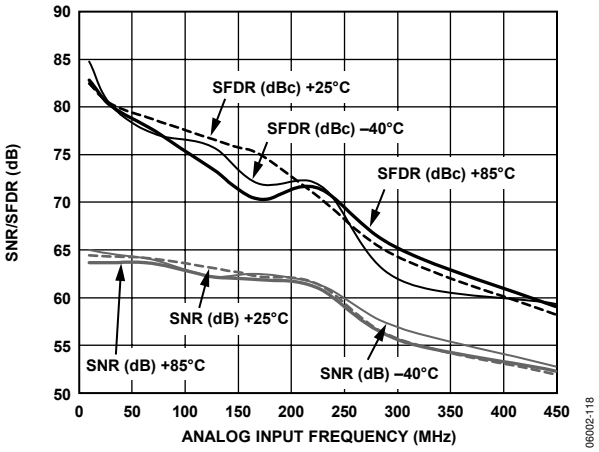

Figure 27. AD9230-210 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1.25 V p-p Full Scale; 210 MSPS

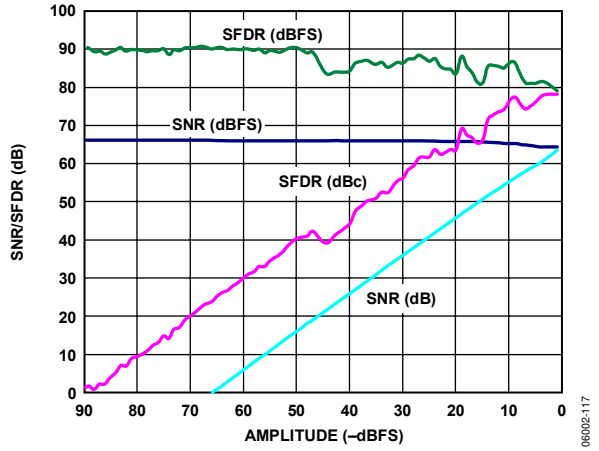

Figure 28. AD9230-210 SNR/SFDR vs. Input Amplitude; 210 MSPS, 170.3 MHz

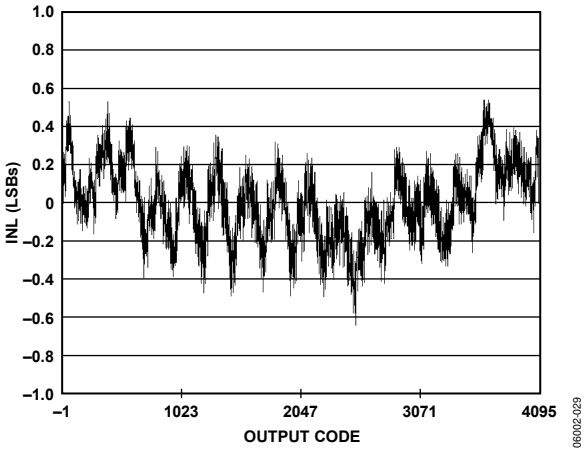

Figure 29. AD9230-210 INL; 210 MSPS

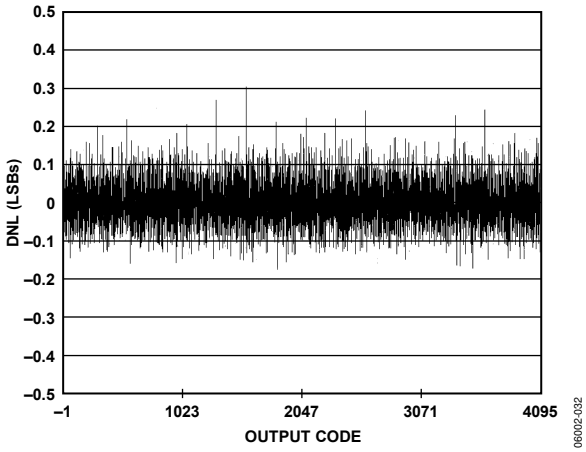

Figure 32. AD9230-210 DNL; 210 MSPS

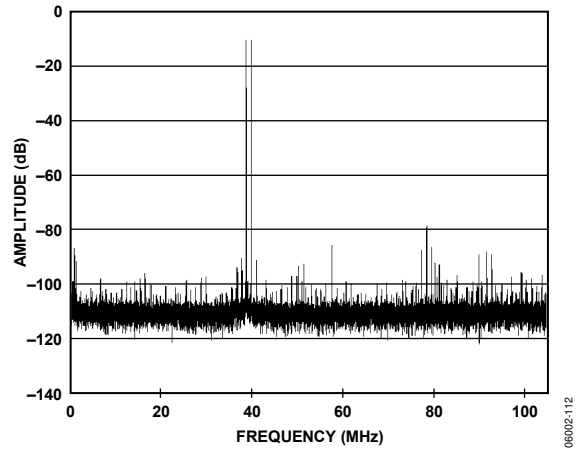

Figure 30. AD9230-210 64 Point, Two-Tone FFT; 210 MSPS, 170.1 MHz, 171.1 MHz

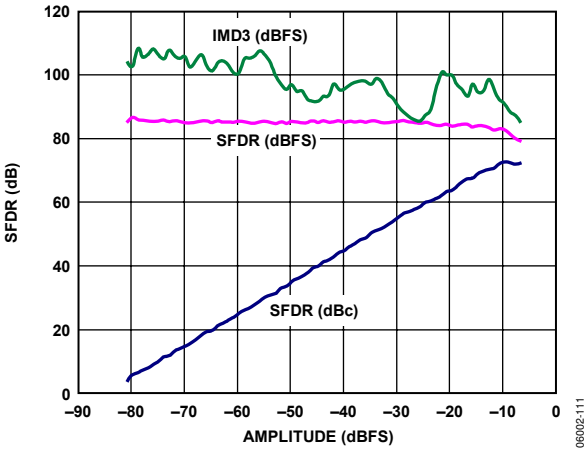

Figure 33. AD9230-210 Two-Tone SFDR vs. Input Amplitude; 210 MSPS, 170.1 MHz, 171.1 MHz

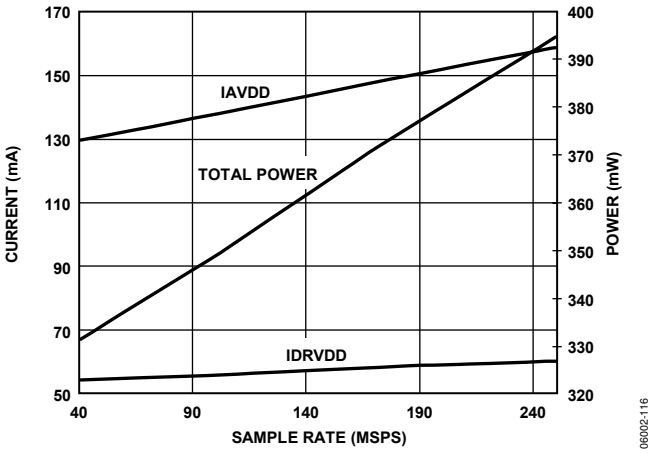

Figure 31. AD9230-210 Power Supply Current vs. Sample Rate

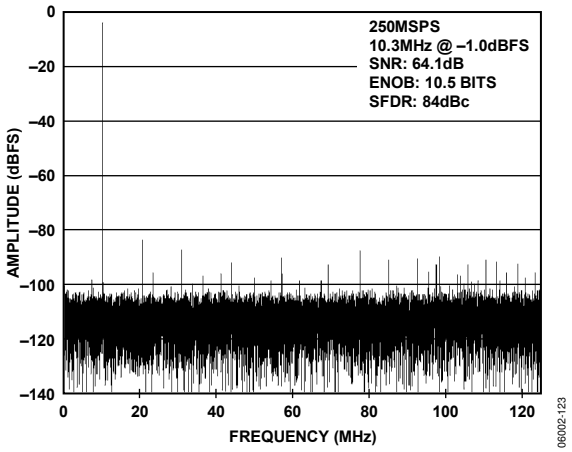

Figure 34. AD9230-250 64k Point Single-Tone FFT; 250 MSPS, 10.3 MHz

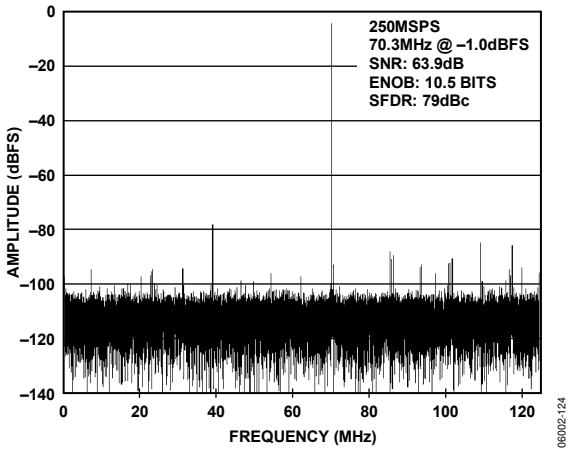

Figure 35. AD9230-250 64k Point Single-Tone FFT; 250 MSPS, 70.3 MHz

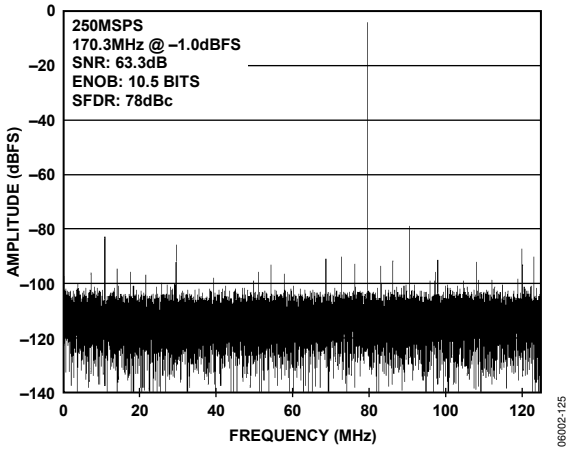

Figure 36. AD9230-250 64k Point Single-Tone FFT; 250 MSPS, 170.3 MHz

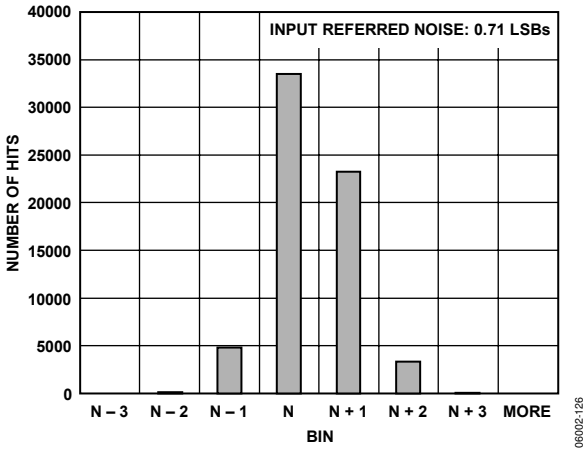

Figure 37. AD9230-250 Grounded Input Histogram; 250 MSPS

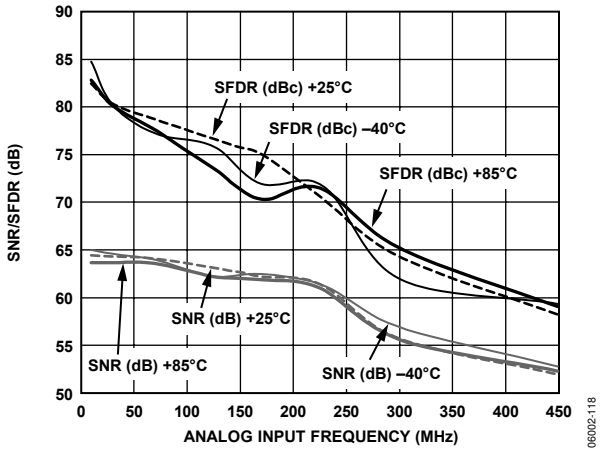

Figure 38. AD9230-250 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1.25 V p-p Full Scale; 250 MSPS

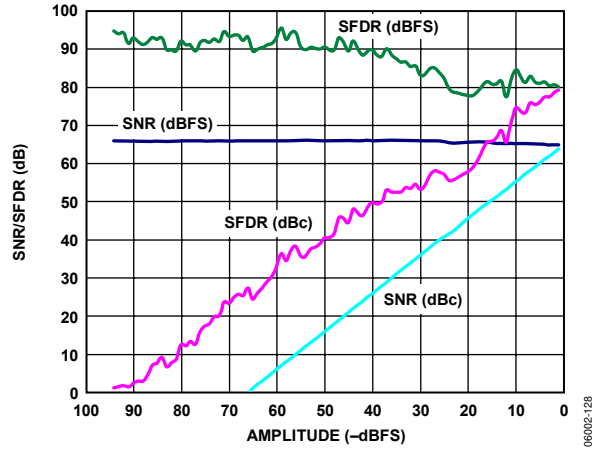

Figure 39. AD9230-250 SNR/SFDR vs. Input Amplitude; 250 MSPS, 170.3 MHz

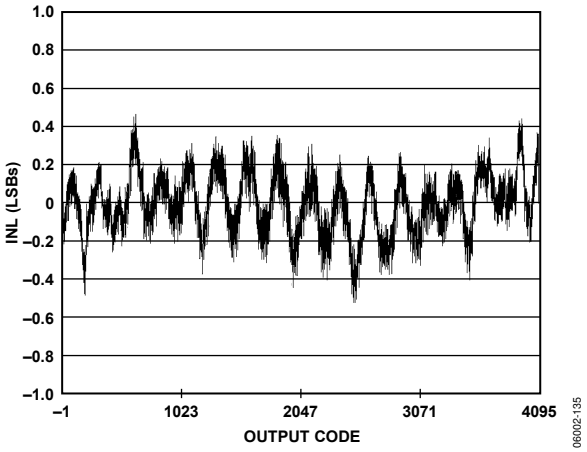

Figure 40. AD9230-250 INL; 250 MSPS

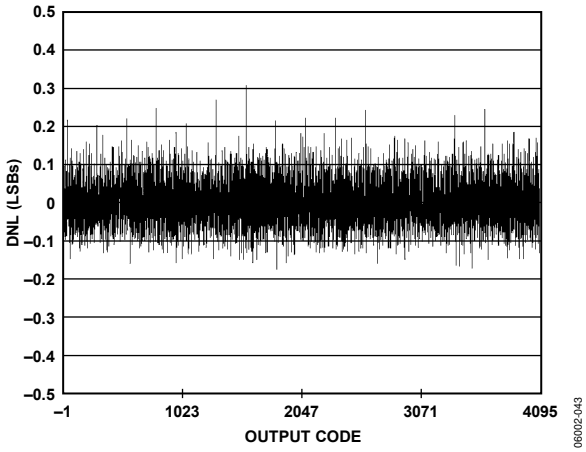

Figure 43. AD9230-250 DNL; 250 MSPS

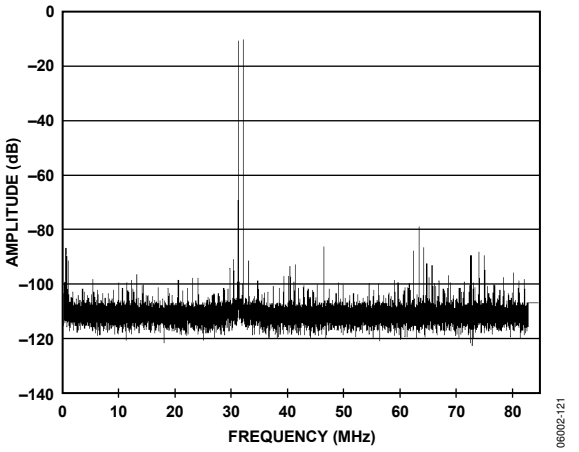

Figure 41. AD9230-250 64k Point, Two-Tone FFT; 250 MSPS, 170.1 MHz, 171.1 MHz

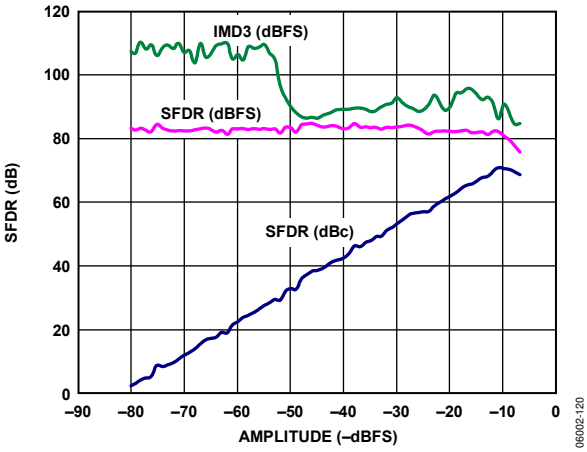

Figure 44. AD9230-250 Two-Tone SFDR vs. Input Amplitude; 250 MSPS, 170.1 MHz, 171.1 MHz

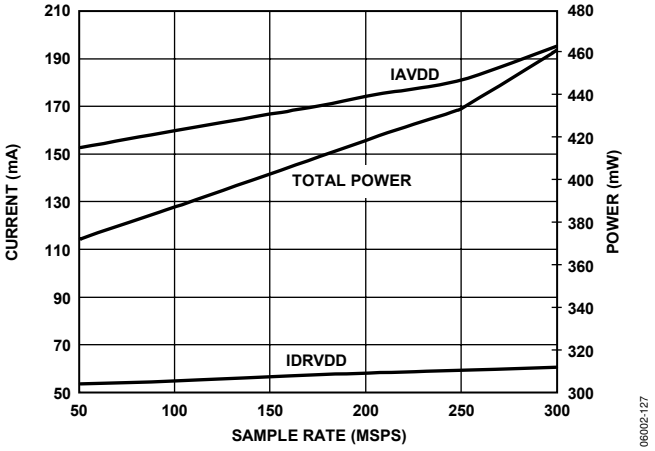

Figure 42. AD9230 Power Supply Current vs. Sample Rate

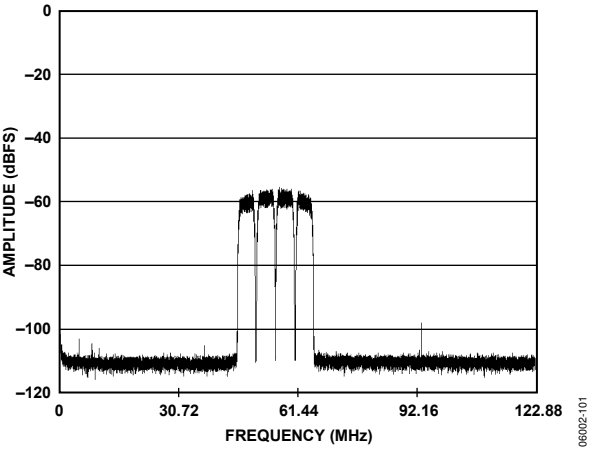

Figure 45. AD9230-250 64k Point FFT; Four W-CDMA Carriers, IF = 184 MHz, 245.6 MSPS

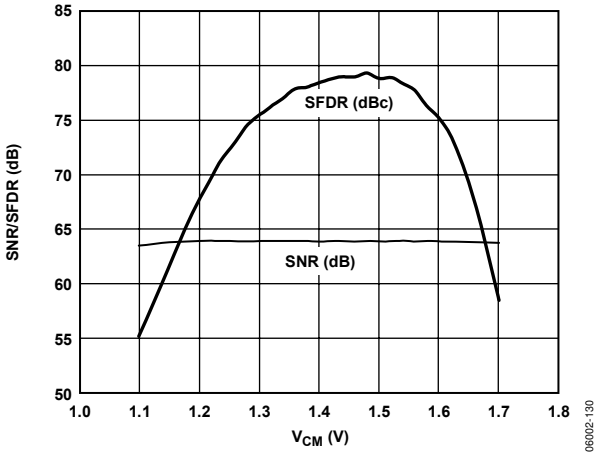

Figure 46. SNR/SFDR vs. Common-Mode Voltage; 250 MSPS, 70.3 MHz @ −1 dBFS

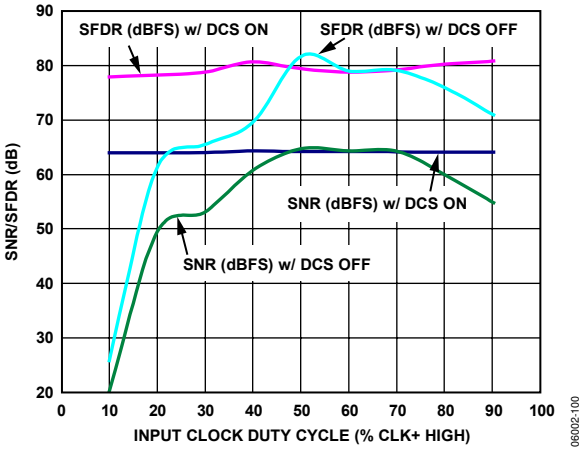

Figure 49. SNR/SFDR vs. Sample Clock Duty Cycle; 250 MSPS, 170.3 MHz @ −1 dBFS

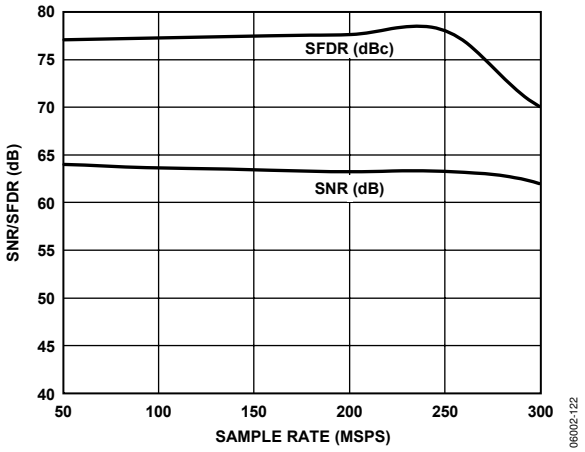

Figure 47. SNR/SFDR vs. Sample Rate; 250 MSPS, 170.3 MHz @ −1 dBFS

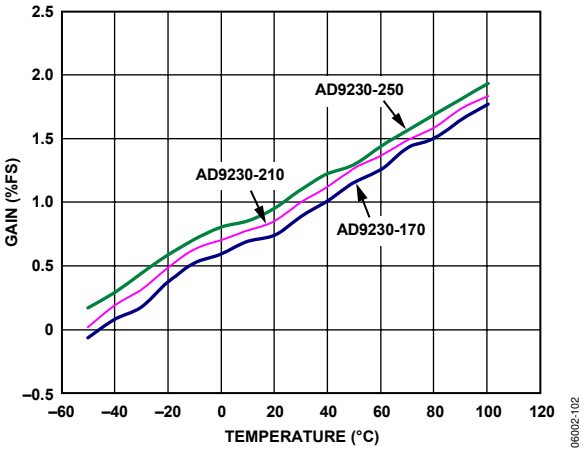

Figure 50. Gain vs. Temperature

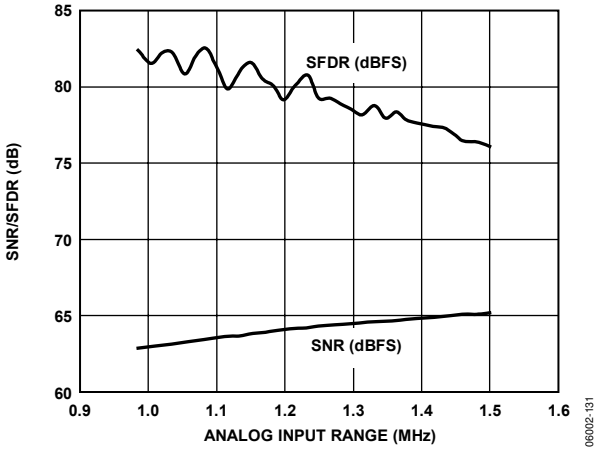

Figure 48. SNR/SFDR vs. Analog Input Range; 250 MSPS, 170.3 MHz @ −1 dBFS

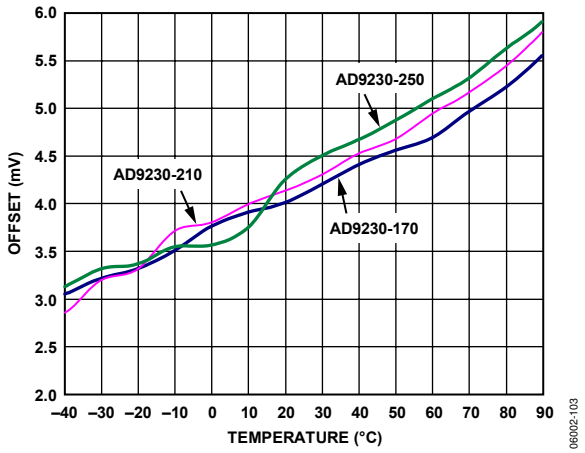

Figure 51. Offset vs. Temperature

THEORY OF OPERATION

The AD9230 architecture consists of a front-end sample and hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled in differential or single-ended mode. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT AND VOLTAGE REFERENCE

The analog input to the AD9230 is a differential buffer. For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched such that common-mode settling errors are symmetrical. The analog input is optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. SNR and SINAD performance degrades significantly if the analog input is driven with a single-ended signal.

A wideband transformer, such as Mini-Circuits® ADT1-1WT, can provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Both analog inputs are self-biased by an on-chip resistor divider to a nominal 1.3 V.

An internal differential voltage reference creates positive and negative reference voltages that define the 1.25 V p-p fixed span of the ADC core. This internal voltage reference can be adjusted by means of SPI control. See the AD9230 Configuration Using the SPI section for more details.

Differential Input Configurations

Optimum performance is achieved while driving the AD9230 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to AVDD/2 + 0.5 V, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

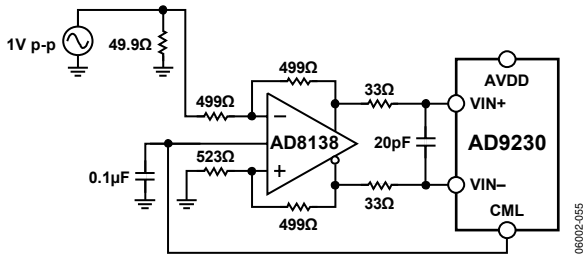

Figure 52. Differential Input Configuration Using the AD8138

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers may not be adequate to achieve the true performance of the AD9230. This is especially true in IF undersampling applications where frequencies in the 70 MHz to 100 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration. The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

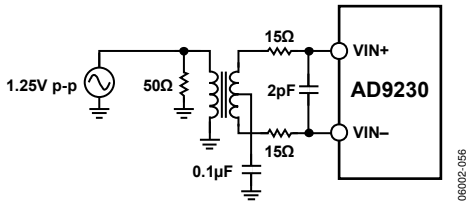

Figure 53. Differential Transformer—Coupled Configuration

As an alternative to using a transformer-coupled input at frequencies in the second Nyquist zone, the AD8352 differential driver can be used (see Figure 54).

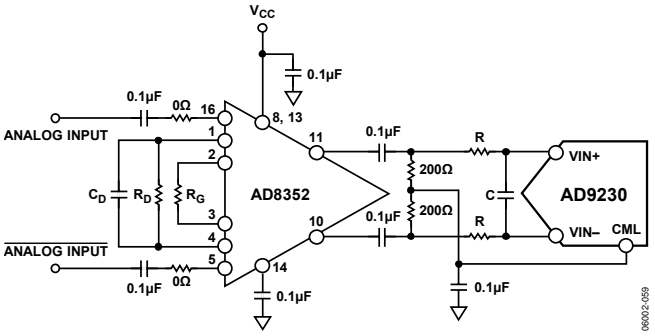

Figure 54. Differential Input Configuration Using the AD8352

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9230 sample clock inputs (CLK+ and CLK–) should be clocked with a differential signal. This signal is typically ac-coupled into the CLK+ pin and CLK– pin via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 55 shows one preferred method for clocking the AD9230. The low jitter clock source is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9230 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9230 and preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

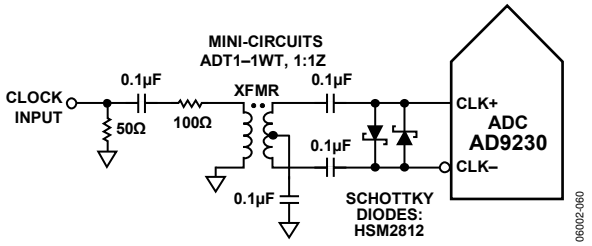

Figure 55. Transformer-Coupled Differential Clock

If a low jitter clock is available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 56. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

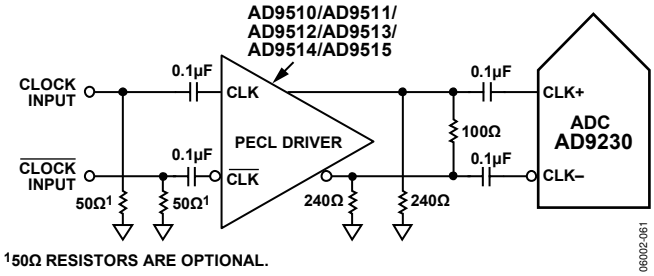

Figure 56. Differential PECL Sample Clock

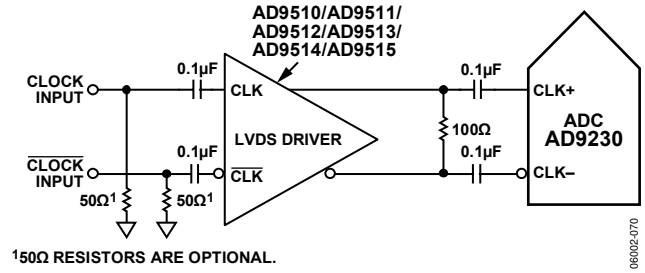

Figure 57. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be directly driven from a CMOS gate, and the CLK– pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 58). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages up to 3.3 V, making the selection of the drive logic voltage very flexible.

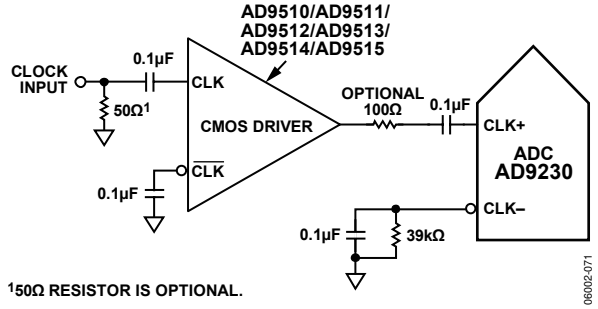

Figure 58. Single-Ended 1.8 V CMOS Sample Clock

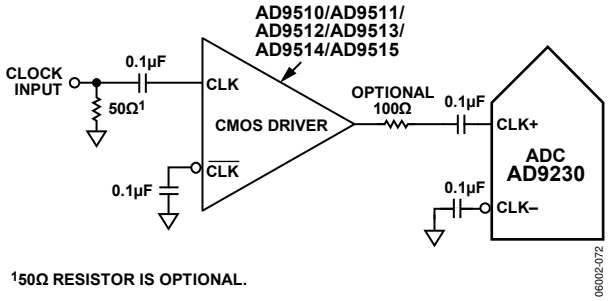

Figure 59. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9230 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9230. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See the AD9230 Configuration Using the SPI section for more details on using this feature.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20 \times \log_{10}[1/2 \times \pi \times f_A \times t_J]$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 60).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9230. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs (visit www.analog.com).

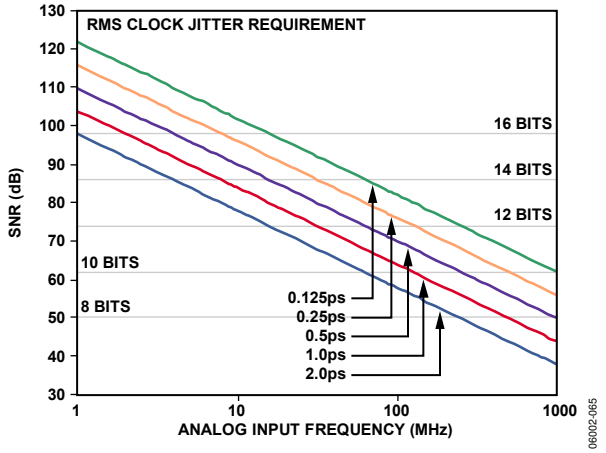

Figure 60. Ideal SNR vs. Input Frequency and Jitter

POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 42, the power dissipated by the AD9230 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

By asserting PDWN (Pin 29) high, the AD9230 is placed in standby mode or full power-down mode, as determined by the contents of Serial Port Register 08. Reasserting the PDWN pin low returns the AD9230 into its normal operational mode.

An additional standby mode is supported by means of varying the clock input. When the clock rate falls below 20 MHz, the AD9230 assumes a standby state. In this case, the biasing network and internal reference remain on, but digital circuitry is powered down. Upon reactivating the clock, the AD9230 resumes normal operation after allowing for the pipeline latency.

DIGITAL OUTPUTS

Digital Outputs and Timing

The AD9230 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This can be changed to a low power, reduced signal option similar to the IEEE 1596.3 standard using the SPI. This LVDS standard can further reduce the overall power dissipation of the device, which reduces the power by ~39 mW. See the Memory Map section for more information. The LVDS driver current is derived on-chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver.

The AD9230 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. No far-end receiver termination and poor differential trace routing may result in timing errors. It is recommended that the trace length is no longer than 24 inches and that the differential output traces are kept close together and at equal lengths.

An example of the LVDS output using the ANSI standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths less than 24 inches on regular FR-4 material is shown in Figure 61. Figure 62 shows an example of when the trace lengths exceed 24 inches on regular FR-4 material. Notice that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position. It is up to the user to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches.

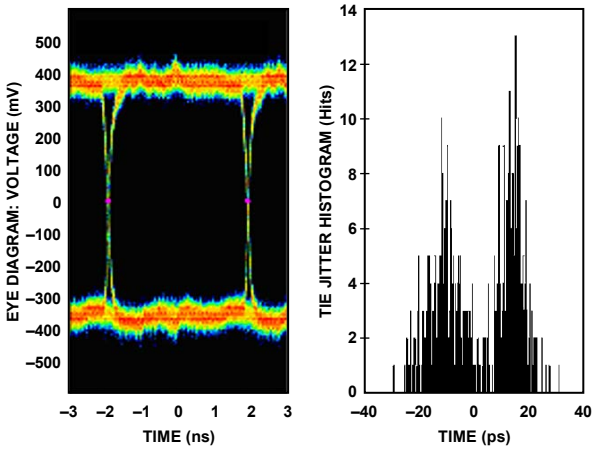

Figure 61. Data Eye for LVDS Outputs in ANSI Mode with Trace Lengths Less than 24 Inches on Standard FR-4, AD9230-250

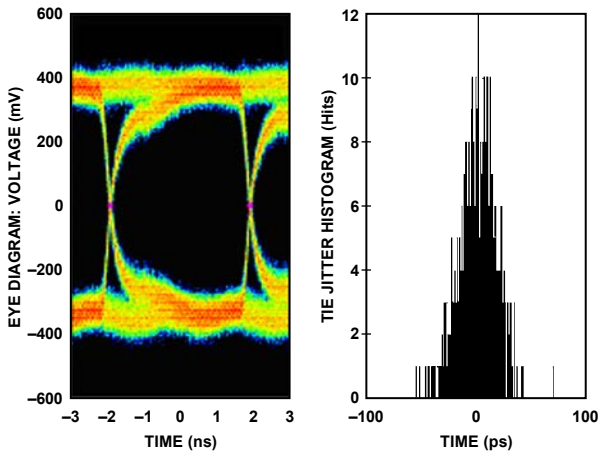

Figure 62. Data Eye for LVDS Outputs in ANSI Mode with Trace Lengths Greater than 24 Inches on Standard FR-4, AD9230-250

The format of the output data is offset binary by default. An example of the output coding format can be found in Table 12. If it is desired to change the output data format to twos complement, see the AD9230 Configuration Using the SPI section.

An output clock signal is provided to assist in capturing data from the AD9230. The DCO is used to clock the output data and is equal to the sampling clock (CLK) rate. In single data rate mode (SDR), data is clocked out of the AD9230 and must be captured on the rising edge of the DCO. In double data rate mode (DDR), data is clocked out of the AD9230 and must be captured on the rising and falling edges of the DCO See the timing diagrams shown in Figure 2 and Figure 3 for more information.

Output Data Rate and Pinout Configuration

The output data of the AD9230 can be configured to drive 12 pairs of LVDS outputs at the same rate as the input clock signal (single data rate, or SDR, mode), or six pairs of LVDS outputs at 2× the rate of the input clock signal (double data rate, or DDR, mode). SDR is the default mode; the device may be reconfigured for DDR by setting Bit 3 in Register 14 (see Table 13).

Out-of-Range (OR)

An out-of-range condition exists when the analog input voltage is beyond the input range of the ADC. OR is a digital output that is updated along with the data output corresponding to the particular sampled input voltage. Thus, OR has the same pipeline latency as the digital data. OR is low when the analog input voltage is within the analog input range and high when the analog input voltage exceeds the input range, as shown in Figure 63. OR remains high until the analog input returns to within the input range and another conversion is completed. By logically AND-ing OR with the MSB and its complement, overrange high or underrange low conditions can be detected.

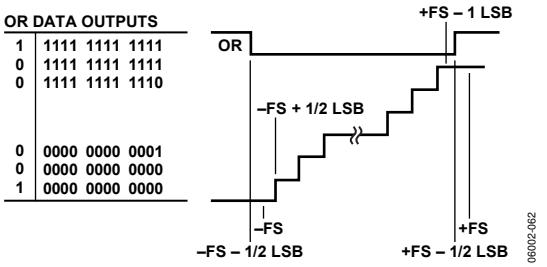

Figure 63. OR Relation to Input Voltage and Output Data

TIMING

The AD9230 provides latched data outputs with a pipeline delay of seven clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9230. These transients can degrade the converter's dynamic performance. The AD9230 also provides data clock output (DCO) intended for capturing the data in an external register. The data outputs are valid on the rising edge of DCO.

The lowest typical conversion rate of the AD9230 is 40 MSPS. At clock rates below 1 MSPS, the AD9230 assumes the standby mode.

RBIAS

The AD9230 requires the user to place a 10 kΩ resistor between the RBIAS pin and ground. This resister should have a 1% tolerance and is used to set the master current reference of the ADC core.

AD9230 CONFIGURATION USING THE SPI

The AD9230 SPI allows the user to configure the converter for specific functions or operations through a structured register space inside the ADC. This gives the user added flexibility to customize device operation depending on the application. Addresses are accessed (programmed or readback) serially in one-byte words. Each byte may be further divided down into fields, which are documented in the Memory Map section.

There are three pins that define the serial port interface or SPI to this particular ADC. They are the SPI SCLK/DFS, SPI SDIO/DCS, and CSB pins. The SCLK/DFS (serial clock) is used to synchronize the read and write data presented the ADC. The SDIO/DCS (serial data input/output) is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB is an active low control that enables or disables the read and write cycles (see Table 9).