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12-Bit, 1 GSPS/500 MSPS JESD204B, Dual Analog-to-Digital Converter

Data Sheet **AD9234**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
- 1.5 W total power per channel at 1 GSPS (default settings)
- SFDR
  - 79 dBFS at 340 MHz (1 GSPS)
  - 86 dBFS at 340 MHz (500 MSPS)
- SNR
  - 63.4 dBFS at 340 MHz (A_{IN} = −1.0 dBFS, 1 GSPS)
  - 65.6 dBFS at 340 MHz (A_{IN} = −1.0 dBFS, 500 MSPS)
- ENOB = 10.4 bits at 10 MHz
- DNL = ±0.16 LSB; INL = ±0.35 LSB
- Noise density
  - −151 dBFS/Hz (1 GSPS)
  - −150 dBFS/Hz (500 MSPS)
- 1.25 V, 2.5 V, and 3.3 V dc supply operation
- Low swing full scale input
  - 1.34 V p-p nominal (1 GSPS)
  - 1.63 V p-p nominal (500 MSPS)
- No missing codes
- Internal ADC voltage reference
- Flexible termination impedance
  - 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- 2 GHz usable analog input full power bandwidth
- 95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation
- Differential clock input
- Optional decimate-by-2 DDC per channel
- Differential clock input
- Integer clock divide by 1, 2, 4, or 8
- Flexible JESD204B lane configurations
- Small signal dither

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE
- Point-to-point radio systems
- Digital predistortion observation path
- General-purpose software radios
- Ultrawideband satellite receiver
- Instrumentation (spectrum analyzers, network analyzers, integrated RF test solutions)
- Digital oscilloscopes
- High speed data acquisition systems
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

FUNCTIONAL BLOCK DIAGRAM

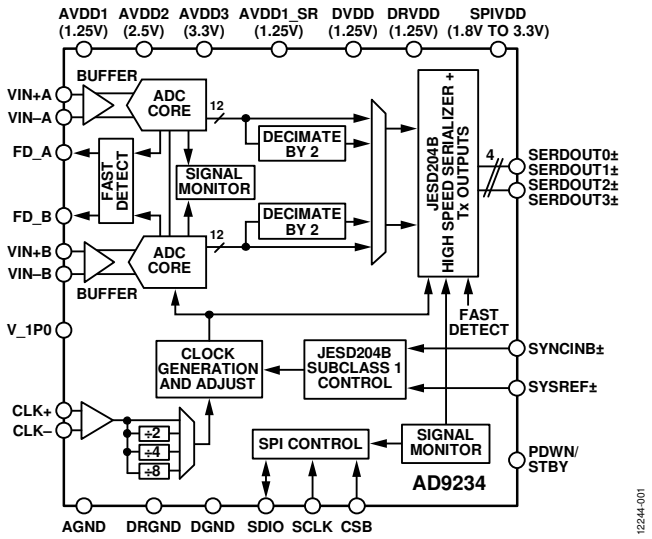

Figure 1.

PRODUCT HIGHLIGHTS

1. Low power consumption analog core, 12-bit, 1.0 GSPS dual analog-to-digital converter (ADC) with 1.5 W per channel.
2. Wide full power bandwidth supports IF sampling of signals up to 2 GHz.
3. Buffered inputs with programmable input termination eases filter design and implementation.
4. Flexible serial port interface (SPI) controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection.
6. 9 mm × 9 mm 64-lead LFCSP.
7. Pin compatible with the AD9680 14-bit, 1 GSPS/500 MSPS dual ADC.

Rev. A
Document Feedback

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Technical Support www.analog.com

AD9234* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9680/AD9234/AD9690 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9234: 12-Bit, 1 GSPS JESD204B, Dual Analog-to-Digital Converter Data Sheet

TOOLS AND SIMULATIONS

- AD9234 IBIS Model

REFERENCE MATERIALS

Technical Articles

- Clocking Wideband GSPS JESD204B ADCs

DESIGN RESOURCES

- AD9234 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9234 EngineerZone Discussions.

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8/14—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9234 is a dual, 12-bit, 1 GSPS/500 MSPS ADC. The device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed for sampling wide bandwidth analog signals. The AD9234 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth buffered inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. Each ADC data output is internally connected to an optional decimate-by-2 block.

The AD9234 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD9234 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

Users can configure the Subclass 1 JESD204B-based high speed serialized output in a variety of one-, two-, or four-lane configurations, depending on the acceptable lane rate of the receiving logic device and the sampling rate of the ADC. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD9234 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V to 3.3 V capable 3-wire SPI.

The AD9234 is available in a Pb-free, 64-lead LFCSP and is specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 1.

		AD9234-500			AD9234-1000			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	12			12			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full	−0.22	0	+0.20	−0.22	0	+0.20	% FSR
Offset Matching	Full		0	+0.19		0	+0.19	% FSR
Gain Error	Full	−13.8	−5.1	+3.6		0		% FSR
Gain Matching	Full	−3.9	+1	+5.9		1	+4.8	% FSR
Differential Nonlinearity (DNL)	Full	−0.3		+0.3	−0.3	±0.16	+0.3	LSB
Integral Nonlinearity (INL)	Full	−0.8		+1.1	−1.2	±35	+1.4	LSB
TEMPERATURE DRIFT								
Offset Error	25°C		±2.6			±6		ppm/°C
Gain Error	25°C		±36			±36		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Voltage	Full		1.0			1.0		V
INPUT-REFERRED NOISE								
V_{REF} = 1.0 V	25°C		0.74			1.02		LSB rms
ANALOG INPUTS								
Differential Input Voltage Range	Full		1.63			1.34		V p-p
Common-Mode Voltage (V_{CM})	25°C		2.05			2.05		V
Differential Input Capacitance[1]	25°C		1.5			1.5		pF
Analog Input Full Power Bandwidth	25°C		2			2		GHz
POWER SUPPLY								
AVDD1	Full	1.22	1.25	1.28	1.22	1.25	1.28	V
AVDD2	Full	2.44	2.50	2.56	2.44	2.50	2.56	V
AVDD3	Full	3.2	3.3	3.4	3.2	3.3	3.4	V
AVDD1_SR	Full	1.22	1.25	1.28	1.22	1.25	1.28	V
DVDD	Full	1.22	1.25	1.28	1.22	1.25	1.28	V
DRVDD	Full	1.22	1.25	1.28	1.22	1.25	1.28	V
SPIVDD	Full	1.7	1.8	3.4	1.7	1.8	3.4	V
I_{AVDD1}	Full		430	480		675	740	mA
I_{AVDD2}	Full		380	430		525	590	mA
I_{AVDD3}	Full		65	75		75	91	mA
I_{AVDD1_SR}	Full		15	18		16	18	mA
I_{DVDD}[2]	Full		140	152		230	236	mA
I_{DRVDD}[1]	Full		190	246		205	225	mA
I_{DRVDD} (L = 2 mode)	25°C		140			N/A[3]		mA
I_{SPIVDD}	Full		5	6		5	6	mA

Parameter	Temp	AD9234-500 Min	AD9234-500 Typ	AD9234-500 Max	AD9234-1000 Min	AD9234-1000 Typ	AD9234-1000 Max	Unit
POWER CONSUMPTION								
Total Power Dissipation (Including Output Drivers)[2]	Full		2.15	2.5		3.0	3.3	W
Total Power Dissipation (L = 2 Mode)	25°C		2.08			N/A[3]		W
Power-Down Dissipation	Full		670			750		mW
Standby[4]	Full		1.1			1.25		W

[1] All lanes running. Power dissipation on DRVDD changes with lane rate and number of lanes used.
[2] Default mode. No DDCs used. L = 4, M = 2, F = 1.
[3] N/A = not applicable. At the maximum sample rate, it is not applicable to use L = 2 mode on the JESD204B output interface because this exceeds the maximum lane rate of 12.5 Gbps. L = 2 mode is supported when the equation ((M × N′ × (10/8) × f_{OUT})/L) results in a line rate that is ≤12.5 Gbps. f_{OUT} is the output sample rate and is denoted by f_S/DCM, where DCM = decimation ratio.
[4] Can be controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Temp	AD9234-500 Min	AD9234-500 Typ	AD9234-500 Max	AD9234-1000 Min	AD9234-1000 Typ	AD9234-1000 Max	Unit
ANALOG INPUT FULL SCALE	Full		1.63			1.34		V p-p
NOISE DENSITY[2]	Full		−150			−151		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]								
f_{IN} = 10 MHz	25°C		65.9			64.2		dBFS
f_{IN} = 170 MHz	Full	65.1	65.8		61.6	63.9		dBFS
f_{IN} = 340 MHz	25°C		65.6			63.4		dBFS
f_{IN} = 450 MHz	25°C		65.3			63.1		dBFS
f_{IN} = 737 MHz	25°C		64.2			61.6		dBFS
f_{IN} = 985 MHz	25°C		63.6			60.7		dBFS
f_{IN} = 1410 MHz	25°C		62.2			58.8		dBFS
SNR AND DISTORTION RATIO (SINAD)[3]								
f_{IN} = 10 MHz	25°C		65.8			64.1		dBFS
f_{IN} = 170 MHz	Full	65.0	65.7		61.2	63.8		dBFS
f_{IN} = 340 MHz	25°C		65.5			63.3		dBFS
f_{IN} = 450 MHz	25°C		65.2			63.0		dBFS
f_{IN} = 737 MHz	25°C		63.7			61.5		dBFS
f_{IN} = 985 MHz	25°C		63.1			60.6		dBFS
f_{IN} = 1410 MHz	25°C		61.2			58.7		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 10 MHz	25°C		10.7			10.4		Bits
f_{IN} = 170 MHz	Full	10.5	10.6		9.9	10.3		Bits
f_{IN} = 340 MHz	25°C		10.6			10.2		Bits
f_{IN} = 450 MHz	25°C		10.5			10.2		Bits
f_{IN} = 737 MHz	25°C		10.3			9.9		Bits
f_{IN} = 985 MHz	25°C		10.2			9.8		Bits
f_{IN} = 1410 MHz	25°C		9.9			9.5		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)[3]								
f_{IN} = 10 MHz	25°C		84			89		dBFS
f_{IN} = 170 MHz	Full	77	85		70	80		dBFS
f_{IN} = 340 MHz	25°C		85			79		dBFS
f_{IN} = 450 MHz	25°C		87			80		dBFS
f_{IN} = 737 MHz	25°C		75			81		dBFS
f_{IN} = 985 MHz	25°C		75			79		dBFS
f_{IN} = 1410 MHz	25°C		71			78		dBFS

Parameter[1]	Temp	AD9234-500 Min	AD9234-500 Typ	AD9234-500 Max	AD9234-1000 Min	AD9234-1000 Typ	AD9234-1000 Max	Unit
WORST HARMONIC, SECOND OR THIRD[3]								
f_{IN} = 10 MHz	25°C		−84			−89		dBFS
f_{IN} = 170 MHz	Full		−85	−77		−80	−70	dBFS
f_{IN} = 340 MHz	25°C		−85			−79		dBFS
f_{IN} = 450 MHz	25°C		−87			−80		dBFS
f_{IN} = 737 MHz	25°C		−75			−82		dBFS
f_{IN} = 985 MHz	25°C		−75			−79		dBFS
f_{IN} = 1410 MHz	25°C		−71			−78		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC[3]								
f_{IN} = 10 MHz	25°C		−96			−89		dBFS
f_{IN} = 170 MHz	Full	−82	−95			−85	−76	dBFS
f_{IN} = 340 MHz	25°C		−94			−83		dBFS
f_{IN} = 450 MHz	25°C		−93			−82		dBFS
f_{IN} = 737 MHz	25°C		−88			−81		dBFS
f_{IN} = 985 MHz	25°C		−89			−85		dBFS
f_{IN} = 1410 MHz	25°C		−86			−80		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −7 dBFS								
f_{IN1} = 187 MHz, f_{IN2} = 190 MHz	25°C		−90			−81		dBFS
f_{IN1} = 338 MHz, f_{IN2} = 341 MHz	25°C		−86			−78		dBFS
CROSSTALK[4]	25°C		95			95		dB
FULL POWER BANDWIDTH[5]	25°C		2			2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (30 MHz).
[3] See Table 9 for recommended settings for the buffer current setting optimized for SFDR.
[4] Crosstalk is measured at 170 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[5] Measured with circuit shown in Figure 64.

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	600	1200	1800	mV p-p
Input Common-Mode Voltage	Full		0.85		V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
SYSTEM REFERENCE INPUTS (SYSREF+, SYSREF−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance (Differential)	Full			2.5	pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0		0.5	V
Input Resistance	Full		30		kΩ
LOGIC OUTPUT (SDIO)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage (I_{OH} = 800 µA)	Full	0.8 × SPIVDD			V
Logic 0 Voltage (I_{OL} = 50 µA)	Full	0		0.5	V
SYNC INPUTS (SYNCINB+, SYNCINB−)					
Logic Compliance	Full		LVDS/LVPECL/CMOS		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
LOGIC OUTPUTS (FD_A, FD_B)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0		0.5	V
Input Resistance	Full		30		kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 3)					
Logic Compliance	Full		CML		
Differential Output Voltage	Full	360		770	mV p-p
Output Common-Mode Voltage (V_{CM})					
AC-Coupled	25°C	0		1.8	V
Short-Circuit Current (I_{Dshort})	25°C	−100		+100	mA
Differential Return Loss (RL_{DIFF})[1]	25°C	8			dB
Common-Mode Return Loss (RL_{CM})[1]	25°C	6			dB
Differential Termination Impedance	Full	80	100	120	Ω

[1] Differential and common-mode return loss is measured from 100 MHz to 0.75 MHz × baud rate.

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate, A_{IN} = −1.0 dBFS, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 4.

		AD9234-500			AD9234-1000			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK								
Clock Rate (at CLK+/CLK− Pins)	Full	0.3		4	0.3		4	GHz
Maximum Sample Rate[1]	Full	500			1000			MSPS
Minimum Sample Rate[2]	Full	300			300			MSPS
Clock Pulse Width High	Full	1000			500			ps
Clock Pulse Width Low	Full	1000			500			ps
OUTPUT PARAMETERS								
Unit Interval (UI)[3]	Full	80	200		80	100		ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)	25°C	24	32		24	32		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)	25°C	24	32		24	32		ps
PLL Lock Time	25°C		2			2		ms
Data Rate per Channel (NRZ)[4]	25°C	3.125	5	12.5	3.125	10	12.5	Gbps
LATENCY[5]								
Pipeline Latency	Full		55			55		Clock cycles
Fast Detect Latency	Full			28			28	Clock cycles
Wake-Up Time[6]								
Standby	25°C		1			1		ms
Power-Down	25°C			4			4	ms
APERTURE								
Aperture Delay (t_A)	Full		530			530		ps
Aperture Uncertainty (Jitter, t_j)	Full		55			55		fs rms
Out-of-Range Recovery Time	Full		1			1		Clock Cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 300 MSPS with L = 2 or L = 1.
[3] Baud rate = 1/UI. A subset of this range can be supported.
[4] Default L = 4. This number can be changed based on the sample rate and decimation ratio.
[5] No DDCs used. L = 4, M = 2, F = 1.
[6] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Unit**
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 2				
t_{SU_SR}	Device clock to SYSREF+ setup time		117		ps
t_{H_SR}	Device clock to SYSREF+ hold time		−96		ps
SPI TIMING REQUIREMENTS	See Figure 3				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 3)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 3)	10			ns

Timing Diagrams

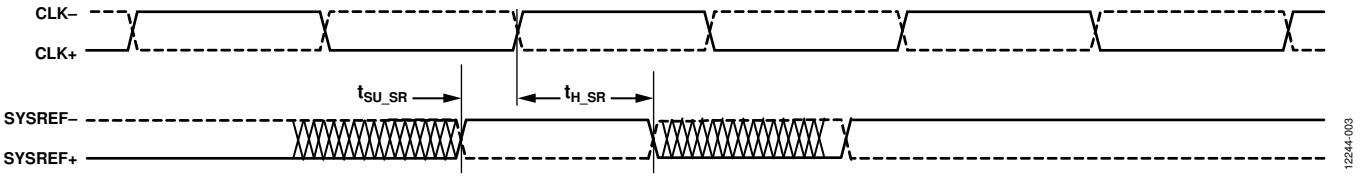

Figure 2. SYSREF± Setup and Hold Timing

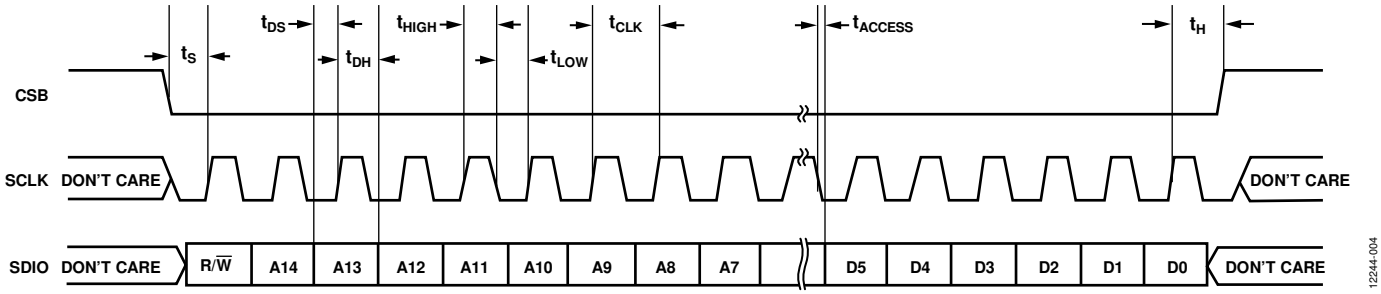

Figure 3. Serial Port Interface Timing Diagram

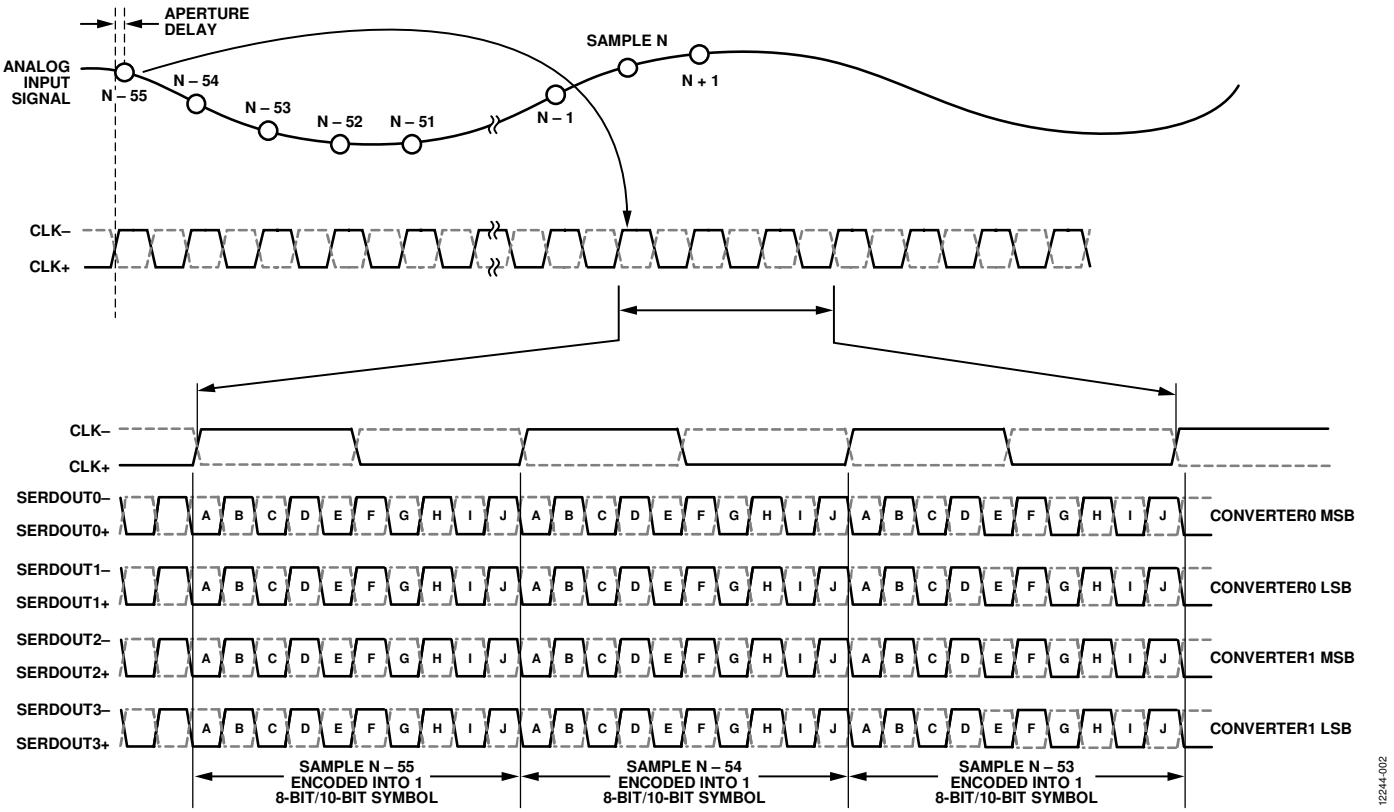

Figure 4. Data Output Timing (Full Bandwidth Mode; L = 4; M = 2; F = 1)

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD1_SR to AGND	1.32 V
AVDD2 to AGND	2.75 V
AVDD3 to AGND	3.63 V
DVDD to DGND	1.32 V
DRVDD to DRGND	1.32 V
SPIVDD to AGND	3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	3.2 V
SCLK, SDIO, CSB to AGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to AGND	−0.3 V to SPIVDD + 0.3 V
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−40°C to +115°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and θ_{JB}. In addition, metal in direct contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes, reduces the θ_{JA}. Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 6.

Table 7. Thermal Resistance Values

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	Ψ_{JB}	θ_{JC_TOP}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	17.8[1, 2]	6.3[1, 3]	4.7[1, 5]	1.2[1, 5]	°C/W
	1.0	15.6[1, 2]	5.9[1, 3]	N/A[4]		°C/W
	2.5	15.0[1, 2]	5.7[1, 3]	N/A[4]		°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per JEDEC JESD51-8 (still air).
[4] N/A = not applicable.
[5] Per MIL-STD 883, Method 1012.1.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

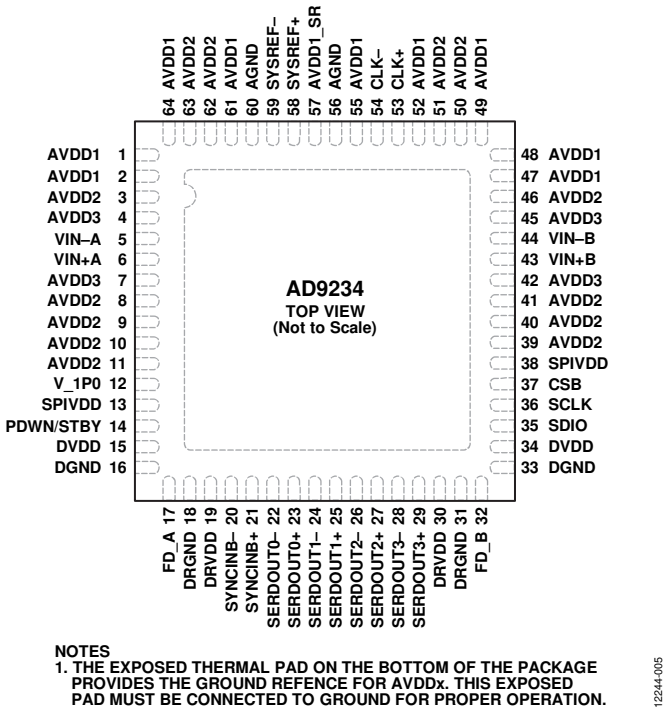

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
Power Supplies			
0	EPAD	Ground	Exposed Pad. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx. This exposed pad must be connected to ground for proper operation.
1, 2, 47, 48, 49, 52, 55, 61, 64	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
3, 8, 9, 10, 11, 39, 40, 41, 46, 50, 51, 62, 63	AVDD2	Supply	Analog Power Supply (2.5 V Nominal).
4, 7, 42, 45	AVDD3	Supply	Analog Power Supply (3.3 V Nominal).
13, 38	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V to 3.3 V).
15, 34	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
16, 33	DGND	Ground	Ground Reference for DVDD.
18, 31	DRGND	Ground	Ground Reference for DRVDD.
19, 30	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
56, 60	AGND[1]	Ground	Ground Reference for SYSREF±.
57	AVDD1_SR[1]	Supply	Analog Power Supply for SYSREF± (1.25 V Nominal).
Analog			
5, 6	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
12	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
43, 44	VIN+B, VIN−B	Input	ADC B Analog Input True/Complement.
53, 54	CLK+, CLK−	Input	Clock Input True/Complement.
CMOS Outputs			
17, 32	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B.

Pin No.	Mnemonic	Type	Description
Digital Inputs			
20, 21	SYNCINB−, SYNCINB+	Input	Active Low JESD204B LVDS Sync Input Complement/True.
58, 59	SYSREF+, SYSREF−	Input	Active High JESD204B LVDS System Reference Input True/Complement.
Data Outputs			
22, 23	SERDOUT0−, SERDOUT0+	Output	Lane 0 Output Data Complement/True.
24, 25	SERDOUT1−, SERDOUT1+	Output	Lane 1 Output Data Complement/True.
26, 27	SERDOUT2−, SERDOUT2+	Output	Lane 2 Output Data Complement/True.
28, 29	SERDOUT3−, SERDOUT3+	Output	Lane 3 Output Data Complement/True.
Device Under Test (DUT) Controls			
14	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
35	SDIO	Input/output	SPI Serial Data Input/Output.
36	SCLK	Input	SPI Serial Clock.
37	CSB	Input	SPI Chip Select (Active Low).

[1] To ensure proper ADC operation, connect AVDD1_SR and AGND separately from the AVDD1 and EPAD connection. For more information, refer to the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9234-1000

AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, 1.34 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, clock divider = 2, T_A = 25°C, 128k FFT sample, unless otherwise noted.

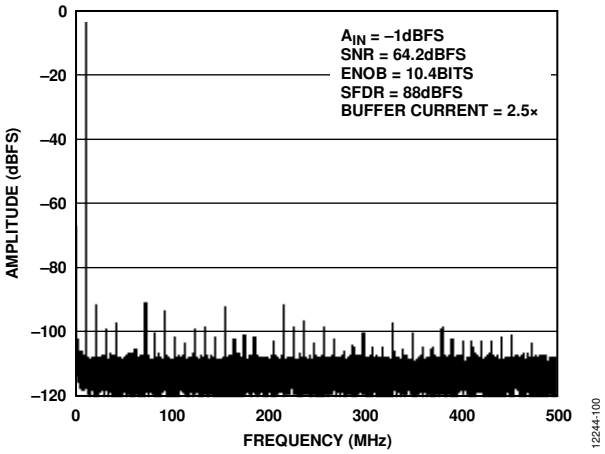

Figure 6. Single-Tone FFT with f_{IN} = 10.3 MHz

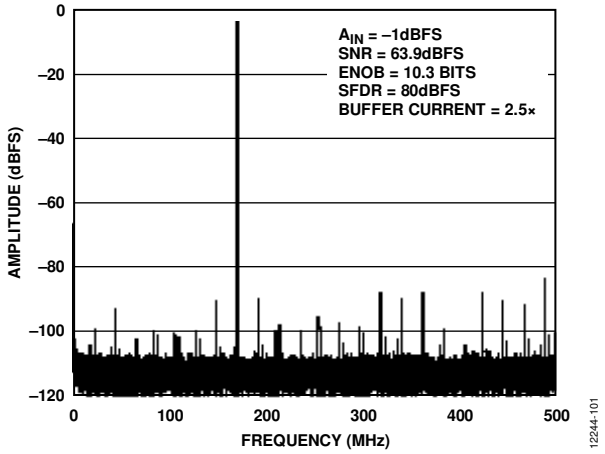

Figure 7. Single-Tone FFT with f_{IN} = 170.3 MHz

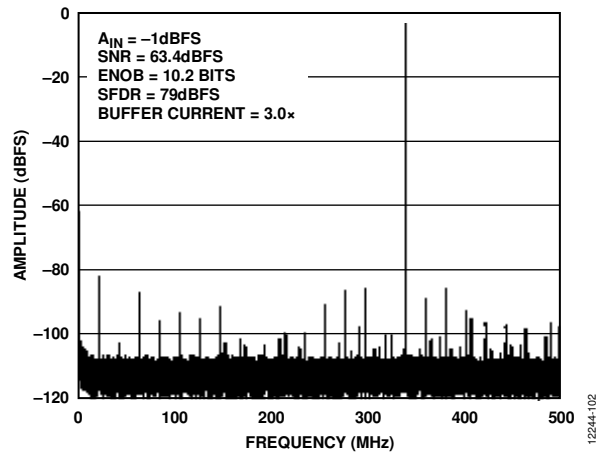

Figure 8. Single-Tone FFT with f_{IN} = 340.3 MHz

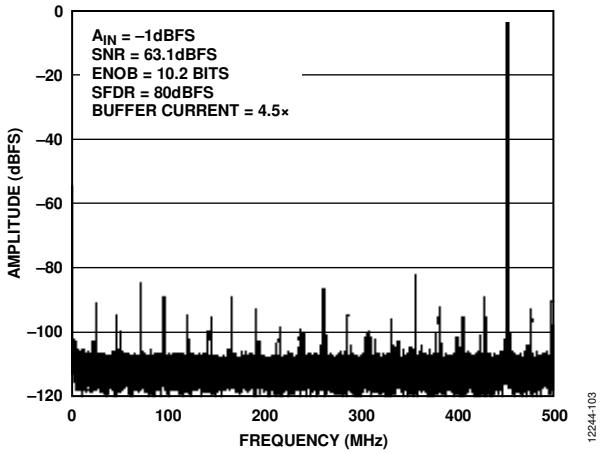

Figure 9. Single-Tone FFT with f_{IN} = 450.3 MHz

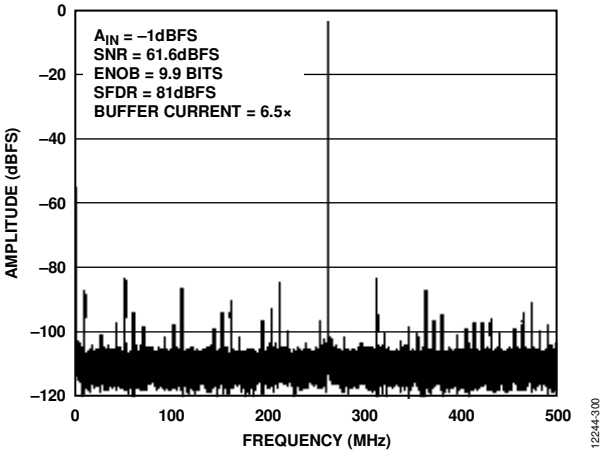

Figure 10. Single-Tone FFT with f_{IN} = 737.3 MHz

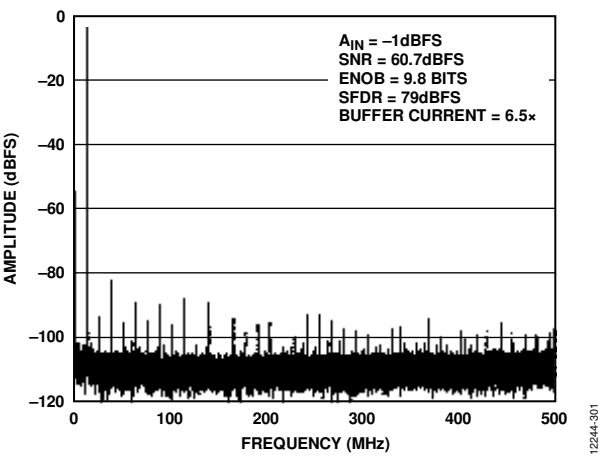

Figure 11. Single-Tone FFT with f_{IN} = 985.3 MHz

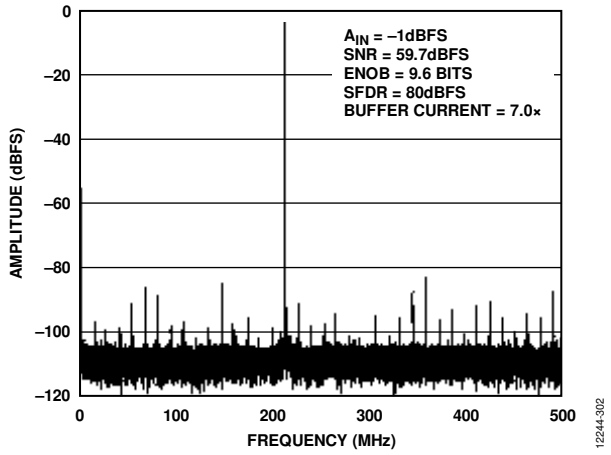

Figure 12. Single-Tone FFT with f_{IN} = 1213.3 MHz

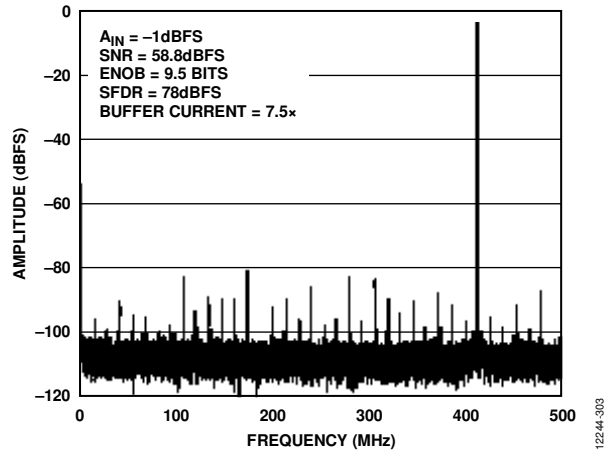

Figure 13. Single-Tone FFT with f_{IN} = 1413.3 MHz

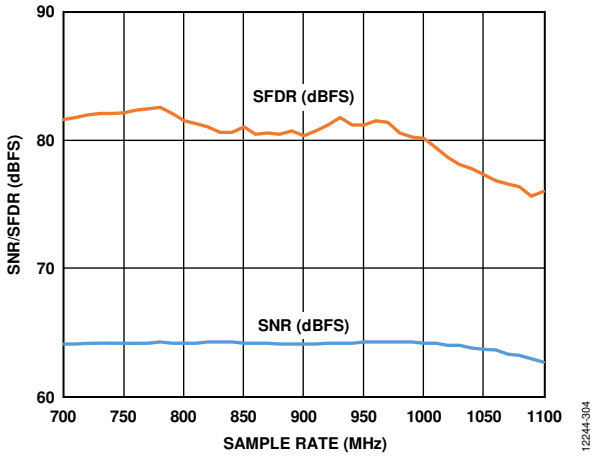

Figure 14. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 170.3 MHz ; Buffer Current = 3.0×

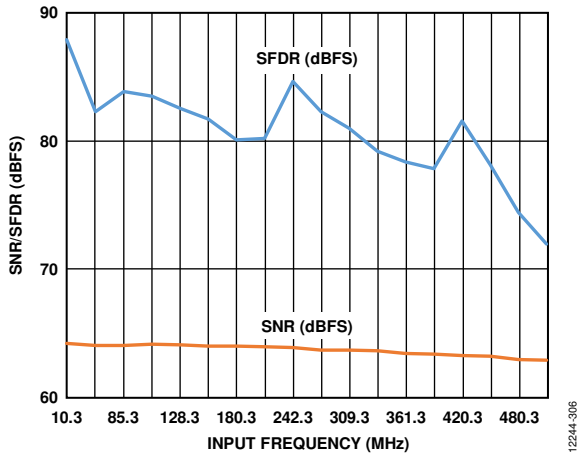

Figure 15. SNR/SFDR vs. Input Frequency (f_{IN}); f_{IN} < 500 MHz ; Buffer Current = 3.5× (Uses Circuit Shown in Figure 63)

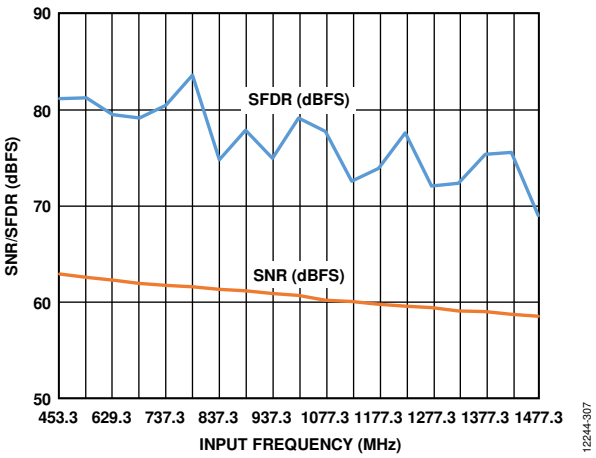

Figure 16. SNR/SFDR vs. Input Frequency (f_{IN}); 450 MHz < f_{IN} < 1500 MHz; Buffer Current = 7.5× (Uses Circuit Shown in Figure 64)

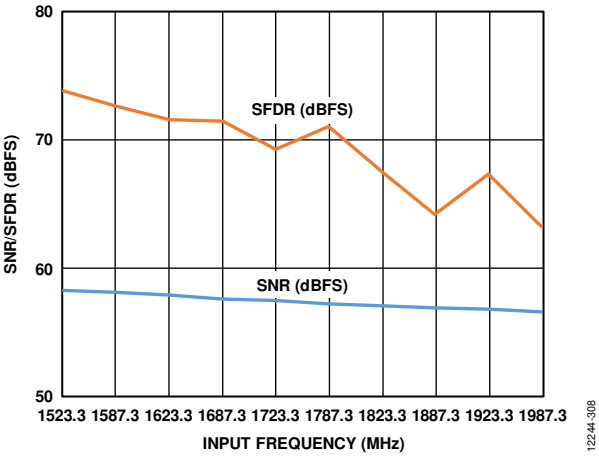

Figure 17. SNR/SFDR vs. Input Frequency (f_{IN}); 1500 MHz < f_{IN} < 2000 MHz; Buffer Current = 8.5× (Uses Circuit Shown in Figure 64)

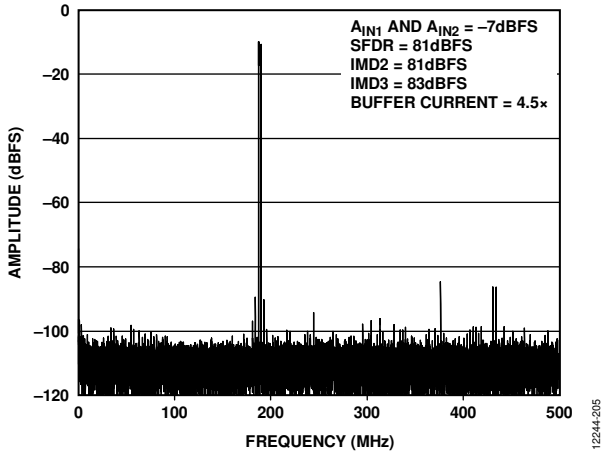

Figure 18. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

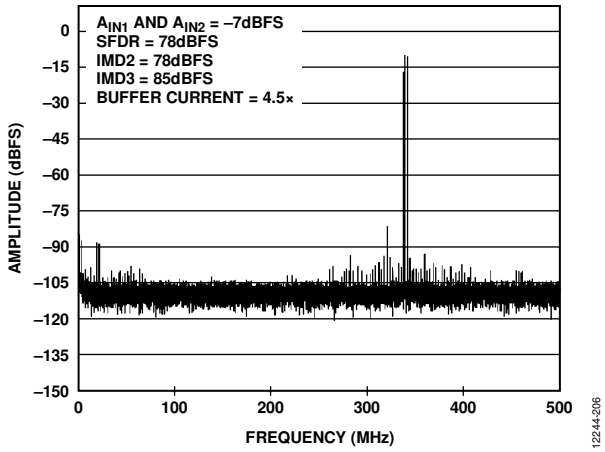

Figure 19. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

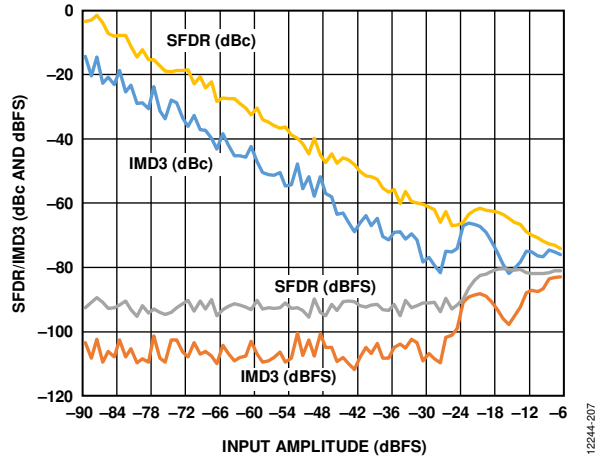

Figure 20. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

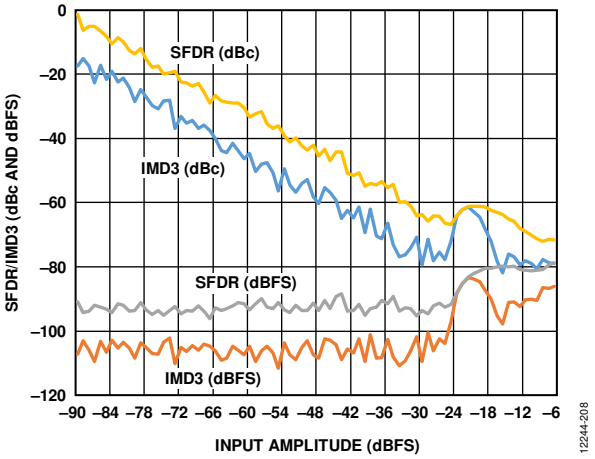

Figure 21. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

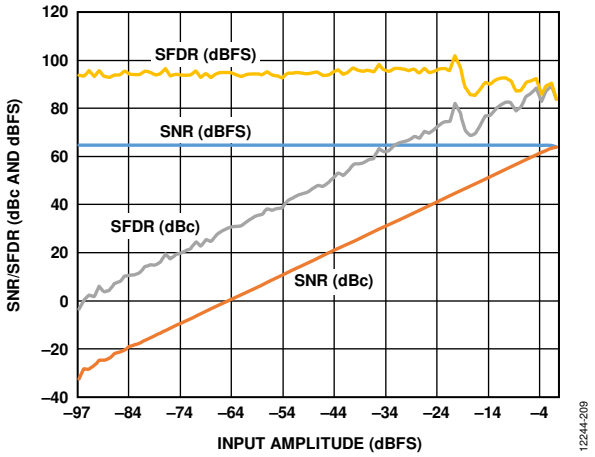

Figure 22. SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz; Buffer Current = 2.0×

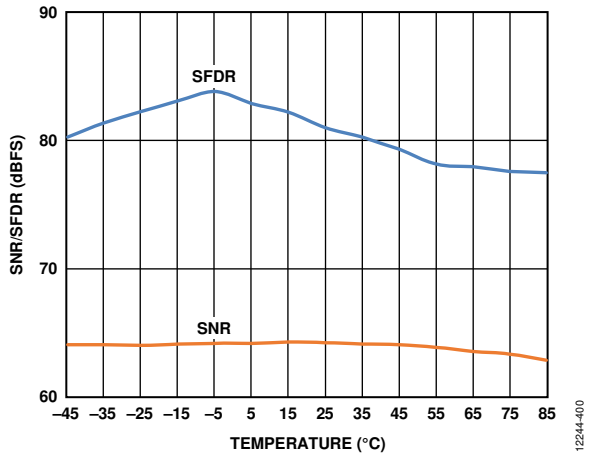

Figure 23. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

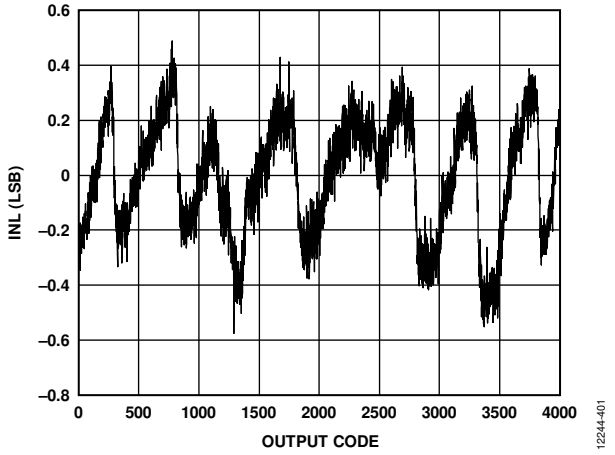

Figure 24. INL, f_{IN} = 10.3 MHz

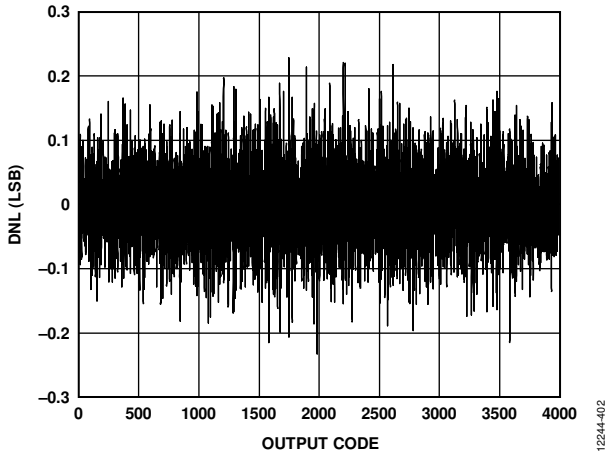

Figure 25. DNL, f_{IN} = 10 MHz

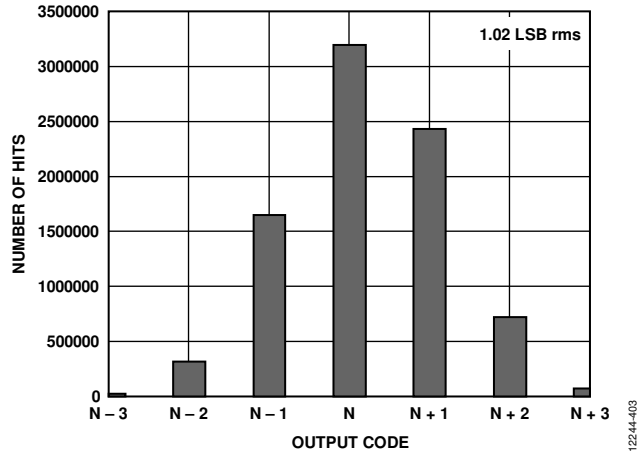

Figure 26. Input-Referred Noise Histogram

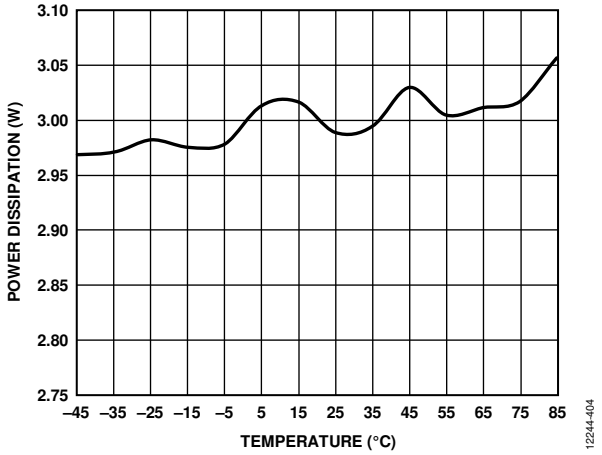

Figure 27. Power Dissipation vs. Temperature

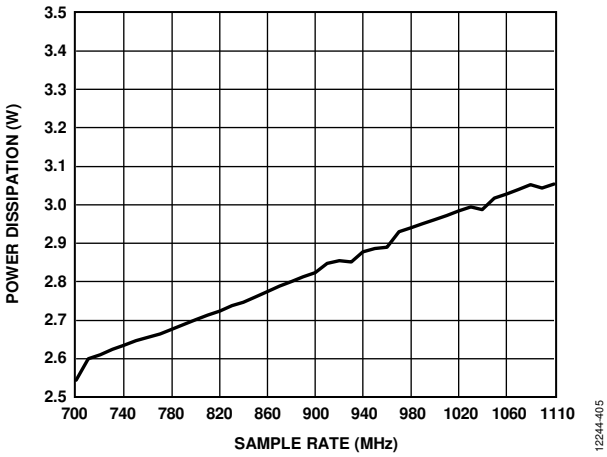

Figure 28. Power Dissipation vs. Sample Rate (f_S)

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AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.5 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, 1.63 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, clock divider = 2, T_A = 25°C, 128k FFT sample, unless otherwise noted.

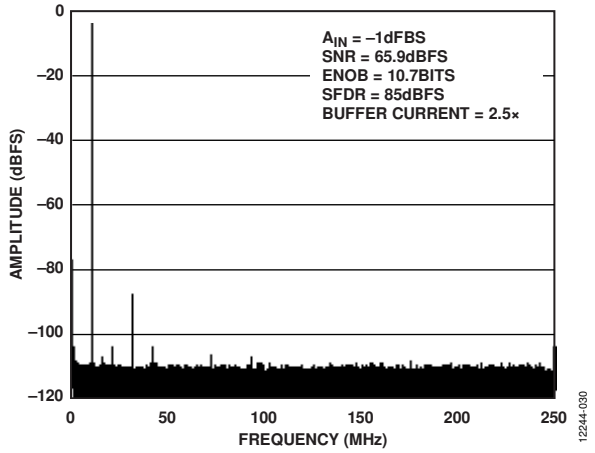

Figure 29. Single-Tone FFT with f_{IN} = 10.3 MHz

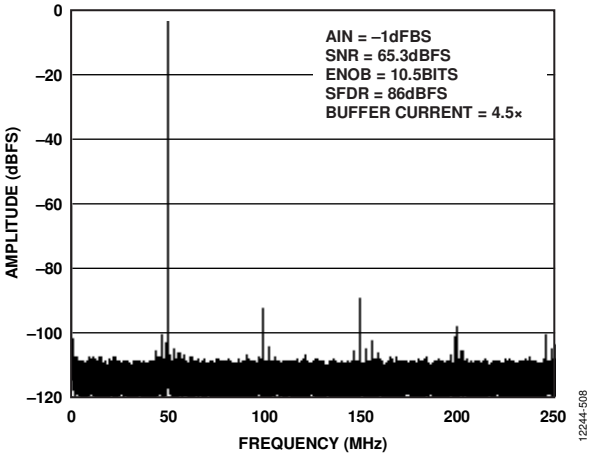

Figure 32. Single-Tone FFT with f_{IN} = 450.3 MHz

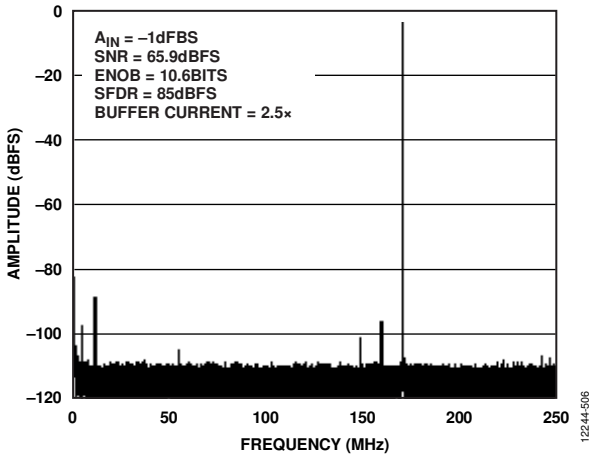

Figure 30. Single-Tone FFT with f_{IN} = 170.3 MHz

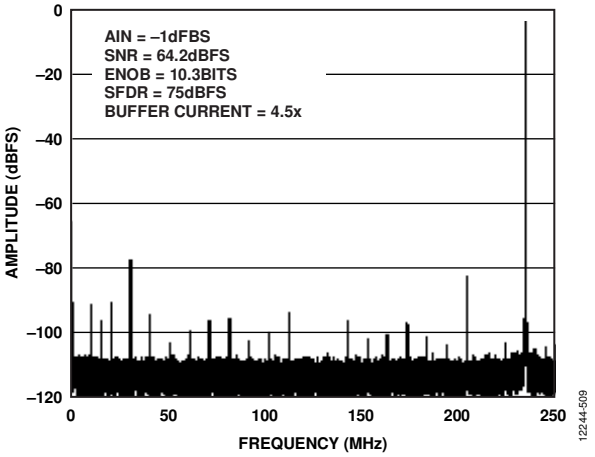

Figure 33. Single-Tone FFT with f_{IN} = 737.3 MHz

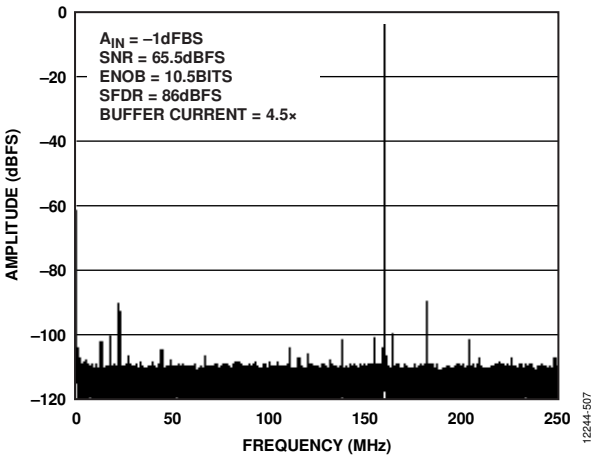

Figure 31. Single-Tone FFT with f_{IN} = 340.3 MHz

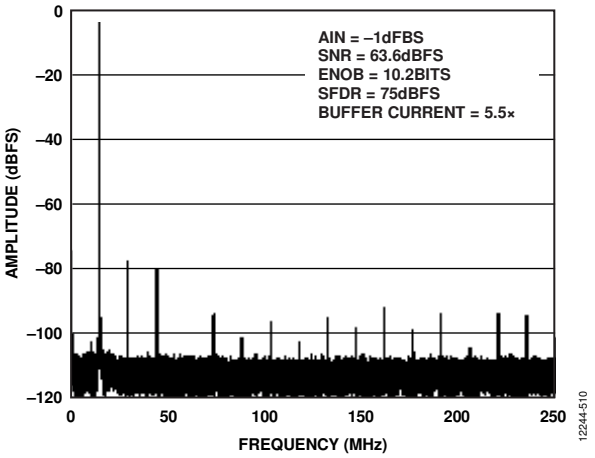

Figure 34. Single-Tone FFT with f_{IN} = 985.3 MHz

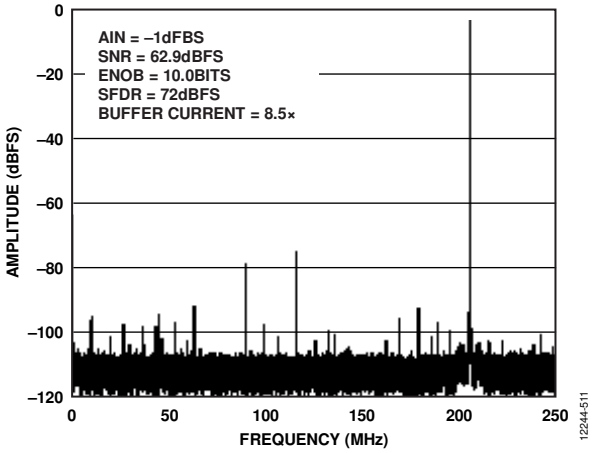

Figure 35. Single-Tone FFT with f_{IN} = 1213.3 MHz

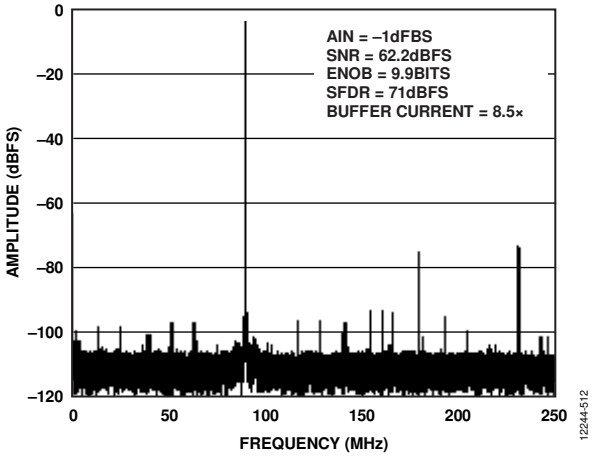

Figure 36. Single-Tone FFT with f_{IN} = 1413.3 MHz

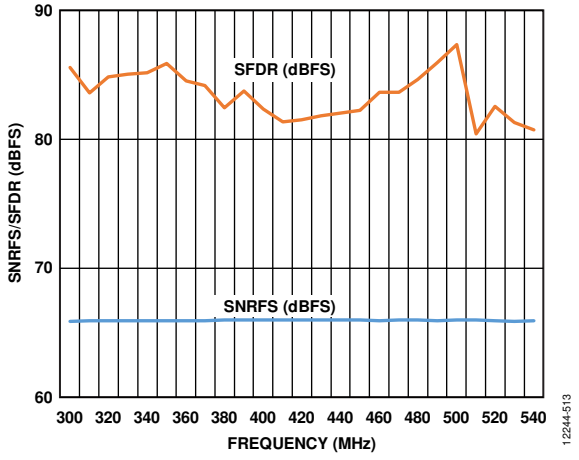

Figure 37. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 170.3 MHz ; Buffer Current = 3.0×

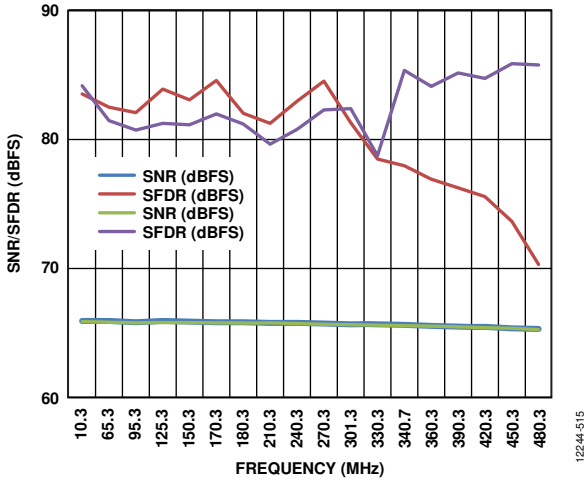

Figure 38. SNR/SFDR vs. Input Frequency (f_{IN}); f_{IN} < 500 MHz; Buffer Current = 2.5× and 4.5× (Uses Circuit Shown in Figure 63)

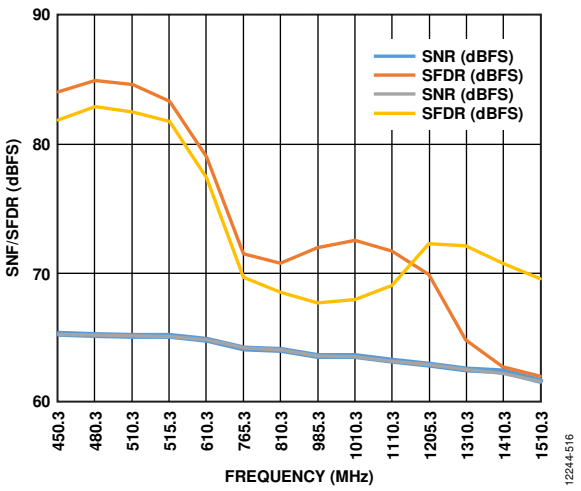

Figure 39. SNR/SFDR vs. Input Frequency (f_{IN}); 450 MHz < f_{IN} < 1500 MHz; Buffer Current = 6.5× and 8.5× (Uses Circuit Shown in Figure 64)

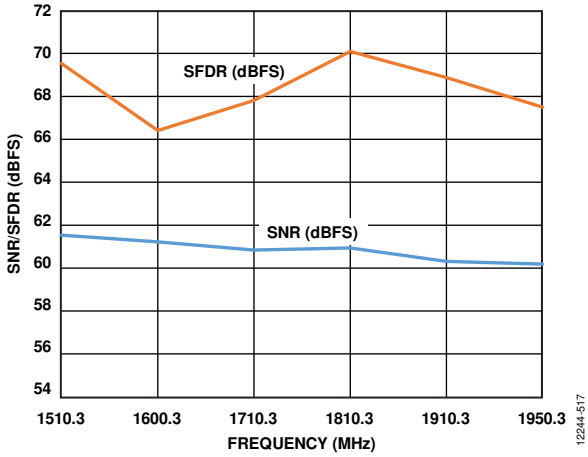

Figure 40. SNR/SFDR vs. Input Frequency (f_{IN}); 1500 MHz < f_{IN} < 2000 MHz; Buffer Current = 8.5× (Uses Circuit Shown in Figure 64)

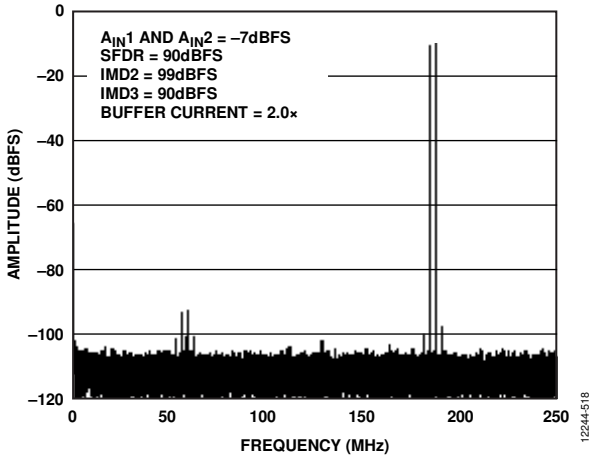

Figure 41. Two-Tone FFT; f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

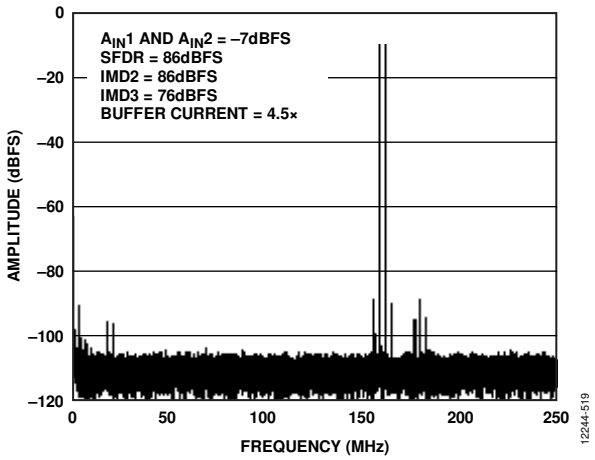

Figure 42. Two-Tone FFT; f_{IN1} = 338 MHz, f_{IN2} = 341 MHz

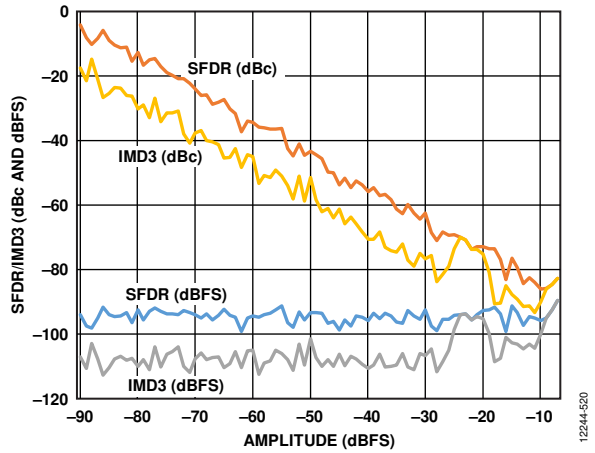

Figure 43. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

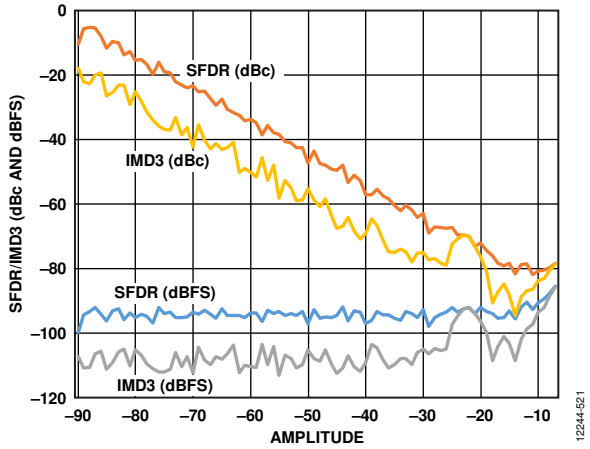

Figure 44. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 338 MHz and f_{IN2} = 341 MHz

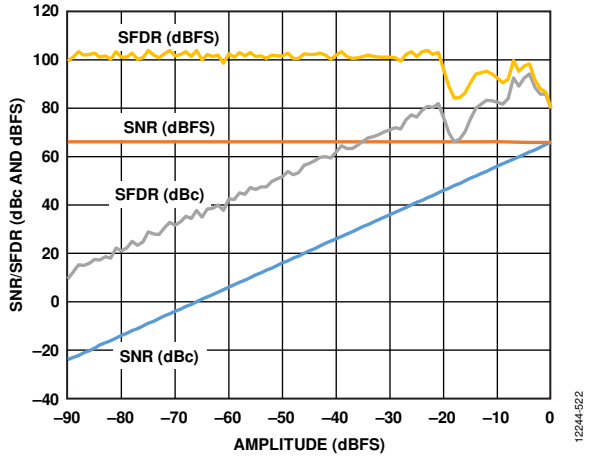

Figure 45. SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz; Buffer Current = 2.0×

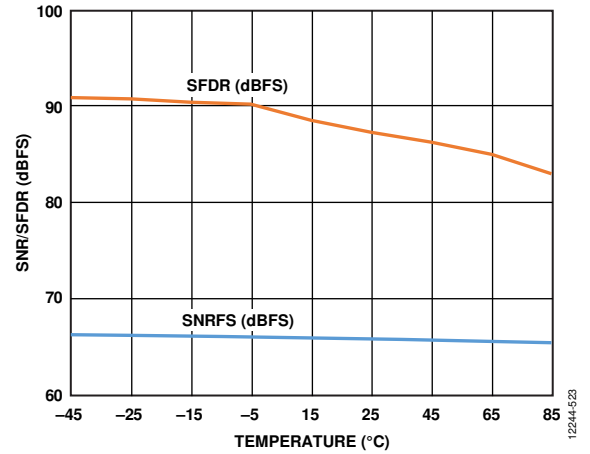

Figure 46. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

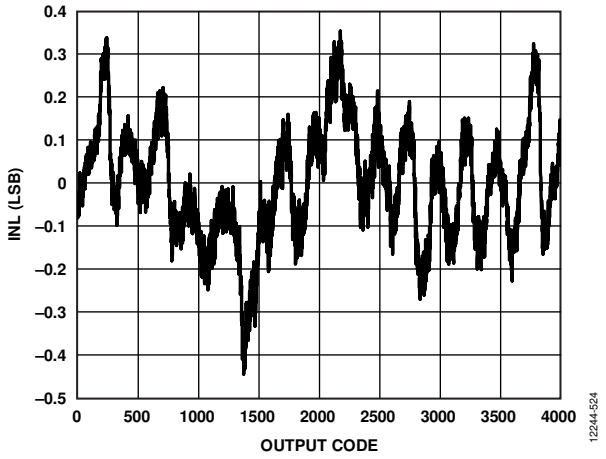

Figure 47. INL, f_{IN} = 10.3 MHz

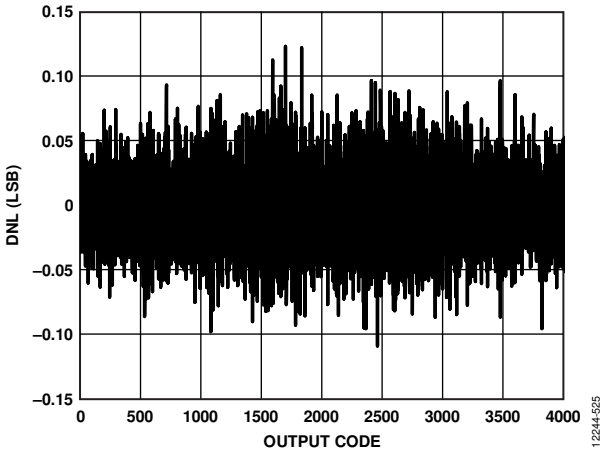

Figure 48. DNL, f_{IN} = 10 MHz

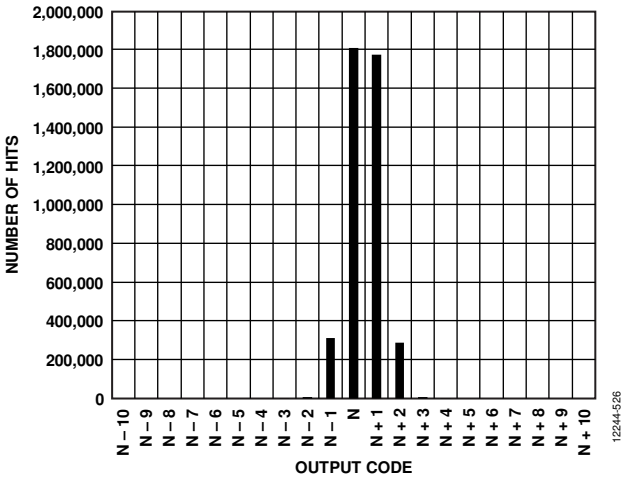

Figure 49. Input-Referred Noise Histogram

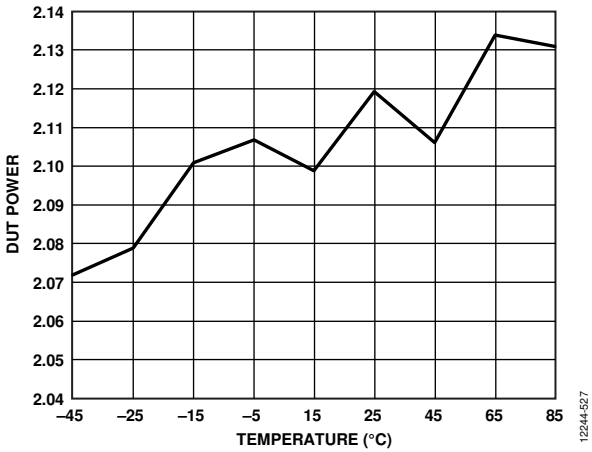

Figure 50. Power Dissipation vs. Temperature

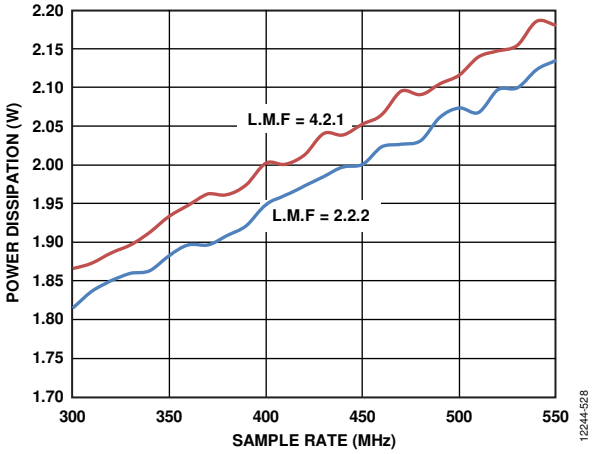

Figure 51. Power Dissipation vs. Sample Rate (f_S)

EQUIVALENT CIRCUITS

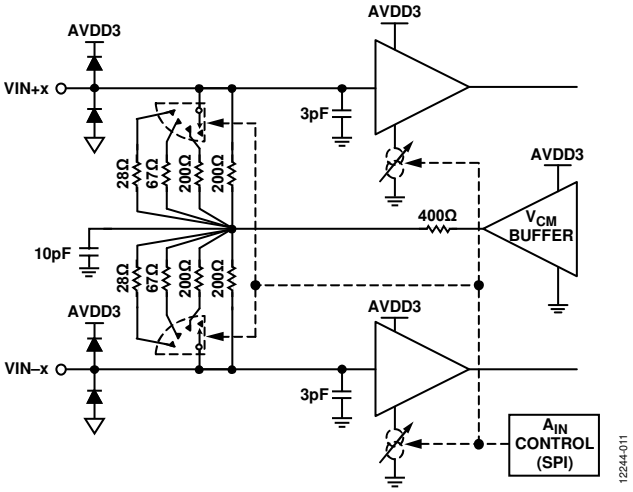

Figure 52. Analog Inputs

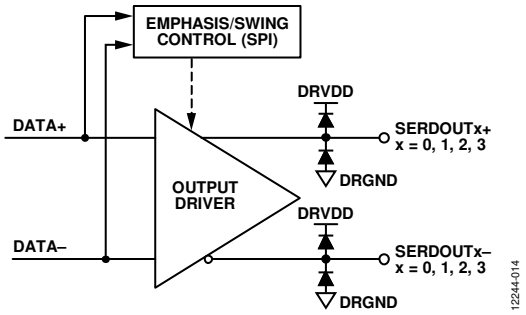

Figure 55. Digital Outputs

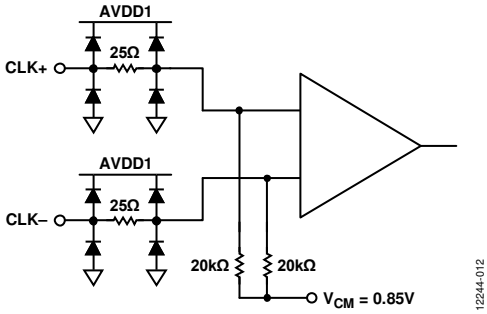

Figure 53. Clock Inputs

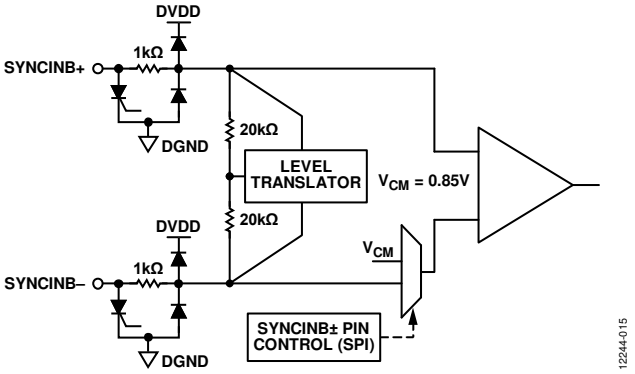

Figure 56. SYNCINB± Inputs

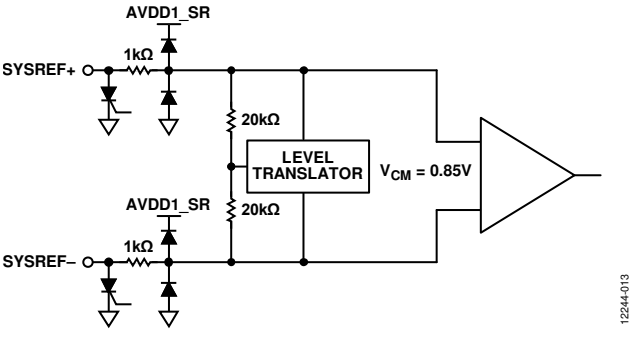

Figure 54. SYSREF± Inputs

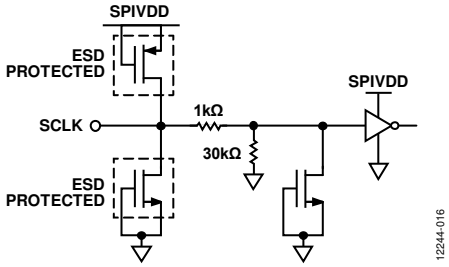

Figure 57. SCLK Input

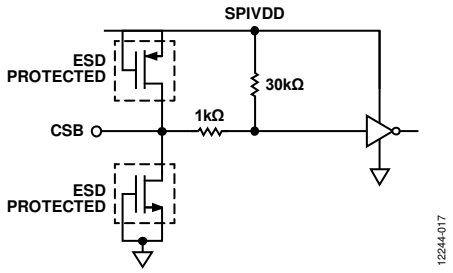

Figure 58. CSB Input

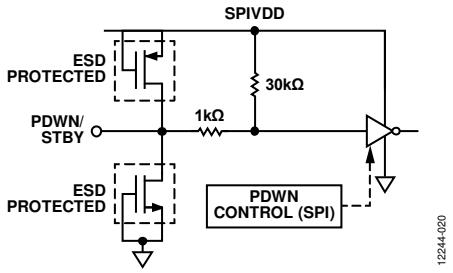

Figure 61. PDWN/STBY Input

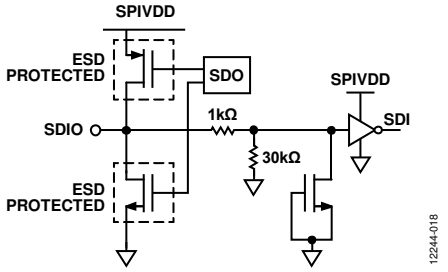

Figure 59. SDIO Input

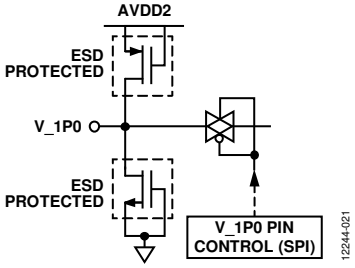

Figure 62. V_1P0 Input

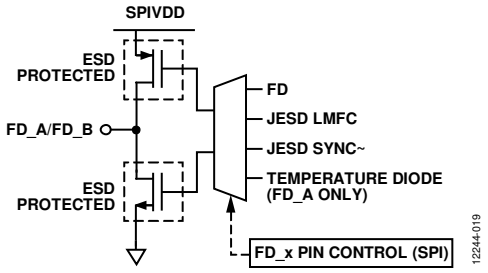

Figure 60. FD_A/FD_B Outputs

THEORY OF OPERATION

The AD9234 has two analog input channels and four JESD204B output lane pairs. The ADC is designed to sample wide bandwidth analog signals of up to 2 GHz. The AD9234 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The AD9234 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

The Subclass 1 JESD204B-based high speed serialized output data rate can be configured in one-lane (L = 1), two-lane (L = 2), and four-lane (L = 4) configurations, depending on the sample rate and the decimation ratio. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

ADC ARCHITECTURE

The architecture of the AD9234 consists of an input buffered pipelined ADC. The input buffer is designed to provide a termination impedance to the analog input signal. This termination impedance can be changed using the SPI to meet the termination needs of the driver/amplifier. The default termination value is set to 400 Ω. The equivalent circuit diagram of the analog input termination is shown in Figure 52. The input buffer is optimized for high linearity, low noise, and low power.

The input buffer provides a linear high input impedance (for ease of drive) and reduces kickback from the ADC. The buffer is optimized for high linearity, low noise, and low power. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample; at the same time, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9234 is a differential buffer. The internal common-mode voltage of the buffer is 2.05 V. The clock signal alternately switches the input circuit between sample mode and hold mode. When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, helps reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, thus, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input, which limits unwanted broadband noise. For more information, refer to the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005). In general, the precise values depend on the application.

For best dynamic performance, the source impedances driving VIN+x and VIN−x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9234, the available span is 1.34 V p-p differential for AD9234-1000 and 1.63 V p-p differential for AD9234-500.

Differential Input Configurations

There are several ways to drive the AD9234, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 63 and Figure 64) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9234.

For low to midrange frequencies, a double balun or double transformer network (see Figure 63) is recommended for optimum performance of the AD9234. For higher frequencies in the second and third Nyquist zones, it is better to remove some of the front-end passive components to ensure wideband operation (see Figure 64).