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FEATURES

- 1.8 V analog supply operation**
- 1.8 V to 3.3 V output supply**
- SNR = 71.7 dBc (72.7 dBFS) to 70 MHz input**
- SFDR = 85 dBc to 70 MHz input**
- Low power: 395 mW @ 125 MSPS**
- Differential input with 650 MHz bandwidth**
- On-chip voltage reference and sample-and-hold amplifier**
- DNL = ± 0.4 LSB**
- Flexible analog input: 1 V p-p to 2 V p-p range**
- Offset binary, Gray code, or twos complement data format**
- Clock duty cycle stabilizer**
- Data output clock**
- Serial port control**
 - Built-in selectable digital test pattern generation**
 - Programmable clock and data alignment**

APPLICATIONS

- Ultrasound equipment**
- IF sampling in communications receivers**
 - IS-95, CDMA-One, IMT-2000**
- Battery-powered instruments**
- Hand-held scopometers**
- Low cost digital oscilloscopes**

GENERAL DESCRIPTION

The AD9246 is a monolithic, single 1.8 V supply, 14-bit, 80 MSPS/105 MSPS/125 MSPS analog-to-digital converter (ADC), featuring a high performance sample-and-hold amplifier (SHA) and on-chip voltage reference. The product uses a multistage differential pipeline architecture with output error correction logic to provide 14-bit accuracy at 125 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The wide bandwidth, truly differential SHA allows a variety of user-selectable input ranges and offsets, including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available ADCs, the AD9246 is suitable for applications in communications, imaging, and medical ultrasound.

A differential clock input controls all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance.

Rev. A

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FUNCTIONAL BLOCK DIAGRAM

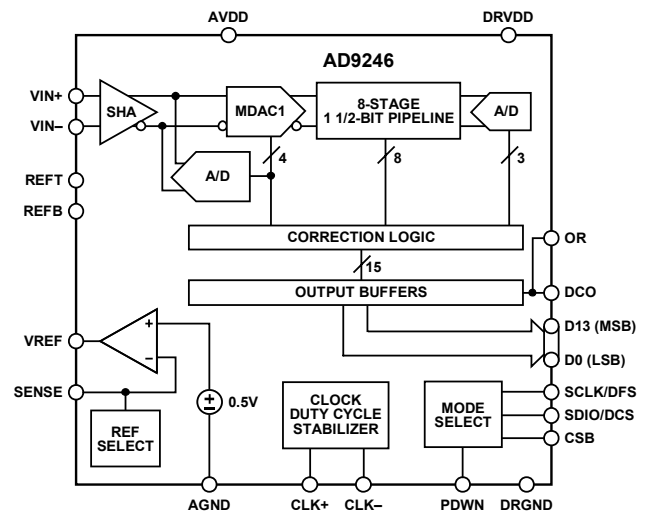


Figure 1.

The digital output data is presented in offset binary, Gray code, or twos complement formats. A data output clock (DCO) is provided to ensure proper latch timing with receiving logic.

The AD9246 is available in a 48-lead LFCSP_VQ and is specified over the industrial temperature range (-40°C to $+85^{\circ}\text{C}$).

PRODUCT HIGHLIGHTS

1. The AD9246 operates from a single 1.8 V power supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
2. The patented SHA input maintains excellent performance for input frequencies up to 225 MHz.
3. The clock DCS maintains overall ADC performance over a wide range of clock pulse widths.
4. A standard serial port interface supports various product features and functions, such as data formatting (offset binary, twos complement, or Gray coding), enabling the clock DCS, power-down, and voltage reference mode.
5. The AD9246 is pin-compatible with the AD9233, allowing a simple migration from 12 bits to 14 bits.

AD9246* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9246 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-1408: Using the AD8376 VGA to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9246: 14-Bit, 80 MSPS/105 MSPS/125 MSPS, 1.8 V Analog-to-Digital Converter Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog
- AD9246 IBIS Models

REFERENCE DESIGNS

- CN0051

REFERENCE MATERIALS

Technical Articles

- Improve The Design Of Your Passive Wideband ADC Front-End Network
- Matching An ADC To A Transformer
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9246 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9246 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

8/06—Rev. 0 to Rev. A

Added 80 MSPS	Universal
Changes to Features	1
Deleted Figures 19, 20, 22, 23	11
Deleted Figures 24, 25, 27 to 29.....	12
Deleted Figures 31, 34.....	13
Deleted Figures 37, 38, 40, 41	14
Deleted Figure 46	15

Deleted Figure 52	16
Changes to Figure 41	17
Changes to Figure 46	19
Inserted Figure 54	21
Added Data Clock Output (DCO) Section	22
Changes to Table 15	25
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4/06—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 2.5 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, DCS enabled, unless otherwise noted.

Table 1.

Parameter	Temp	AD9246BCPZ-80			AD9246BCPZ-105			AD9246BCPZ-125			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION	Full	14			14			14			Bits
ACCURACY		Guaranteed			Guaranteed			Guaranteed			
No Missing Codes	Full	Guaranteed			Guaranteed			Guaranteed			
Offset Error	Full		±0.3	±0.5		±0.3	±0.8		±0.3	±0.8	% FSR
Gain Error	Full		±0.6	±4.7		±0.6	±5.0		±0.6	±4.2	% FSR
Differential Nonlinearity (DNL) ¹	Full			±1.0			±1.0			±1.0	LSB
	25°C		±0.4			±0.4			±0.4		LSB
Integral Nonlinearity (INL) ¹	Full			±5.0			±5.0			±5.0	LSB
	25°C		±1.5			±1.3			±1.5		LSB
TEMPERATURE DRIFT											
Offset Error	Full		±15			±15			±15		ppm/°C
Gain Error	Full		±95			±95			±95		ppm/°C
INTERNAL VOLTAGE REFERENCE											
Output Voltage Error (1 V Mode)	Full		±5	±20		±5	±35		±5	±35	mV
Load Regulation @ 1.0 mA	Full		7			7			7		mV
INPUT REFERRED NOISE											
VREF = 1.0 V	25°C		1.3			1.3			1.3		LSB rms
ANALOG INPUT											
Input Span, VREF = 1.0 V	Full		2			2			2		V p-p
Input Capacitance ²	Full		8			8			8		pF
REFERENCE INPUT RESISTANCE	Full		6			6			6		kΩ
POWER SUPPLIES											
Supply Voltage											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	2.5	3.6	1.7	2.5	3.6	1.7	2.5	3.6	V
Supply Current											
IAVDD ¹	Full		138	155		178	194		220	236	mA
IDRVDD ¹ (DRVDD = 1.8 V)	Full		7			9			11		mA
IDRVDD ¹ (DRVDD = 3.3 V)	Full		12			16			19		mA
POWER CONSUMPTION											
DC Input	Full		248	279		320	350		395	425	mW
Sine Wave Input ¹ (DRVDD = 1.8 V)	Full		261			337			415		mW
Sine Wave Input ¹ (DRVDD = 3.3 V)	Full		288			373			458		mW
Standby Power ³	Full		40			40			40		mW
Power-Down Power	Full		1.8			1.8			1.8		mW

¹ Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.

² Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 4 for the equivalent analog input structure.

³ Standby power is measured with a dc input, the CLK pin inactive (set to AVDD or AGND).

AC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 2.5 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, DCS enabled, unless otherwise noted.

Table 2.

Parameter ¹	Temp	AD9246BCPZ-80			AD9246BCPZ-105			AD9246BCPZ-125			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SIGNAL-TO-NOISE-RATIO (SNR)											
$f_{IN} = 2.4$ MHz	25°C		71.9			71.9			71.9		dBc
$f_{IN} = 70$ MHz	25°C		71.9			71.9			71.7		dBc
	Full	70.8			69.5			69.5			dBc
$f_{IN} = 100$ MHz	25°C		71.6			71.6			71.6		dBc
$f_{IN} = 170$ MHz	25°C		70.9			70.9			70.8		dBc
SIGNAL-TO-NOISE AND DISTORTION (SINAD)											
$f_{IN} = 2.4$ MHz	25°C		71.1			71.1			71.1		dBc
$f_{IN} = 70$ MHz	25°C		71.5			70.8			70.6		dBc
	Full	70.4			68.5			68.5			dBc
$f_{IN} = 100$ MHz	25°C		70.6			70.6			70.6		dBc
$f_{IN} = 170$ MHz	25°C		69.9			69.9			69.8		dBc
EFFECTIVE NUMBER OF BITS (ENOB)											
$f_{IN} = 2.4$ MHz	25°C		11.7			11.7			11.7		Bits
$f_{IN} = 70$ MHz	25°C		11.6			11.6			11.6		Bits
$f_{IN} = 100$ MHz	25°C		11.6			11.6			11.6		Bits
$f_{IN} = 170$ MHz	25°C		11.5			11.5			11.5		Bits
WORST SECOND OR THIRD HARMONIC											
$f_{IN} = 2.4$ MHz	25°C		-90			-90			-90		dBc
$f_{IN} = 70$ MHz	25°C		-85			-85			-85		dBc
	Full			-76			-73			-73	dBc
$f_{IN} = 100$ MHz	25°C		-85			-85			-85		dBc
$f_{IN} = 170$ MHz	25°C		-83.5			-83.5			-83		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)											
$f_{IN} = 2.4$ MHz	25°C		90			90			90		dBc
$f_{IN} = 70$ MHz	25°C		85			85			85		dBc
	Full	76			73			73			dBc
$f_{IN} = 100$ MHz	25°C		85			85			85		dBc
$f_{IN} = 170$ MHz	25°C		83.5			83.5			83		dBc
WORST OTHER HARMONIC OR SPUR											
$f_{IN} = 2.4$ MHz	25°C		-90			-90			-90		dBc
$f_{IN} = 70$ MHz	25°C		-90			-90			-90		dBc
	Full			-85			-80			-80	dBc
$f_{IN} = 100$ MHz	25°C		-90			-90			-90		dBc
$f_{IN} = 170$ MHz	25°C		-90			-90			-90		dBc
TWO-TONE SFDR											
$f_{IN} = 29$ MHz (-7 dBFS), 32 MHz (-7 dBFS)	25°C		87			87			85		dBc
$f_{IN} = 169$ MHz (-7 dBFS), 172 MHz (-7 dBFS)	25°C		83			83			84		dBc
ANALOG INPUT BANDWIDTH	25°C		650			650			650		MHz

¹ See AN-835, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.

AD9246

DIGITAL SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 2.5 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temp	AD9246BCPZ-80/105/125			Unit
		Min	Typ	Max	
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK-)					
Logic Compliance		CMOS/LVDS/LVPECL			
Internal Common-Mode Bias	Full	1.2			V
Differential Input Voltage	Full	0.2		6	V p-p
Input Voltage Range	Full	AVDD - 0.3		AVDD + 1.6	V
Input Common-Mode Range	Full	1.1		AVDD	V
High Level Input Voltage (V _{IH})	Full	1.2		3.6	V
Low Level Input Voltage (V _{IL})	Full	0		0.8	V
High Level Input Current (I _{IH})	Full	-10		+10	μA
Low Level Input Current (I _{IL})	Full	-10		+10	μA
Input Resistance	Full	8	10	12	kΩ
Input Capacitance	Full	4			pF
LOGIC INPUTS (SCLK/DFS, OEB, PWDN)					
High Level Input Voltage (V _{IH})	Full	1.2		3.6	V
Low Level Input Voltage (V _{IL})	Full	0		0.8	V
High Level Input Current (I _{IH})	Full	-50		-75	μA
Low Level Input Current (I _{IL})	Full	-10		+10	μA
Input Resistance	Full	30			kΩ
Input Capacitance	Full	2			pF
LOGIC INPUTS (CSB)					
High Level Input Voltage (V _{IH})	Full	1.2		3.6	V
Low Level Input Voltage (V _{IL})	Full	0		0.8	V
High Level Input Current (I _{IH})	Full	-10		+10	μA
Low Level Input Current (I _{IL})	Full	+40		+135	μA
Input Resistance	Full	26			kΩ
Input Capacitance	Full	2			pF
LOGIC INPUTS (SDIO/DCS)					
High Level Input Voltage (V _{IH})	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage (V _{IL})	Full	0		0.8	V
High Level Input Current (I _{IH})	Full	-10		+10	μA
Low Level Input Current (I _{IL})	Full	+40		+130	μA
Input Resistance	Full	26			kΩ
Input Capacitance	Full	5			pF
DIGITAL OUTPUTS					
DRVDD = 3.3 V					
High Level Output Voltage (V _{OH} , I _{OH} = 50 μA)	Full	3.29			V
High Level Output Voltage (V _{OH} , I _{OH} = 0.5 mA)	Full	3.25			V
Low Level Output Voltage (V _{OL} , I _{OL} = 1.6 mA)	Full	0.2			V
Low Level Output Voltage (V _{OL} , I _{OL} = 50 μA)	Full	0.05			V
DRVDD = 1.8 V					
High Level Output Voltage (V _{OH} , I _{OH} = 50 μA)	Full	1.79			V
High Level Output Voltage (V _{OH} , I _{OH} = 0.5 mA)	Full	1.75			V
Low Level Output Voltage (V _{OL} , I _{OL} = 1.6 mA)	Full	0.2			V
Low Level Output Voltage (V _{OL} , I _{OL} = 50 μA)	Full	0.05			V

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 2.5 V, unless otherwise noted.

Table 4.

Parameter ¹	Temp	AD9246BCPZ-80			AD9246BCPZ-105			AD9246BCPZ-125			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CLOCK INPUT PARAMETERS											
Conversion Rate, DCS Enabled	Full	20		80	20		105	20		125	MSPS
Conversion Rate, DCS Disabled	Full	10		80	10		105	10		125	MSPS
CLK Period	Full	12.5			9.5			8			ns
CLK Pulse Width High, DCS Enabled	Full	3.75	6.25	8.75	2.85	4.75	6.65	2.4	4	5.6	ns
CLK Pulse Width High, DCS Disabled	Full	5.63	6.25	6.88	4.28	4.75	5.23	3.6	4	4.4	ns
DATA OUTPUT PARAMETERS											
Data Propagation Delay (t_{PD}) ²	Full	3.1	3.9	4.8	3.1	3.9	4.8	3.1	3.9	4.8	ns
DCO Propagation Delay (t_{DCO})	Full		4.4			4.4			4.4		ns
Setup Time (t_s)	Full	4.9	5.7		3.4	4.3		2.6	3.5		ns
Hold Time (t_H)	Full	5.9	6.8		4.4	5.3		3.7	4.5		ns
Pipeline Delay (Latency)	Full		12			12			12		cycles
Aperture Delay (t_A)	Full		0.8			0.8			0.8		ns
Aperture Uncertainty (Jitter, t_j)	Full		0.1			0.1			0.1		ps rms
Wake-Up Time ³	Full		350			350			350		μ s
OUT-OF-RANGE RECOVERY TIME	Full		2			2			3		Cycles
SERIAL PORT INTERFACE⁴											
SCLK Period (t_{CLK})	Full	40			40			40			ns
SCLK Pulse Width High Time (t_{HI})	Full	16			16			16			ns
SCLK Pulse Width Low Time (t_{LO})	Full	16			16			16			ns
SDIO to SCLK Setup Time (t_{DS})	Full	5			5			5			ns
SDIO to SCLK Hold Time (t_{DH})	Full	2			2			2			ns
CSB to SCLK Setup Time (t_s)	Full	5			5			5			ns
CSB to SCLK Hold Time (t_H)	Full	2			2			2			ns

¹ See AN-835, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
² Output propagation delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load.
³ Wake-up time is dependent on the value of the decoupling capacitors, values shown with 0.1 μ F capacitor across REFT and REFB.
⁴ See Figure 57 and the Serial Port Interface (SPI) section.

TIMING DIAGRAM

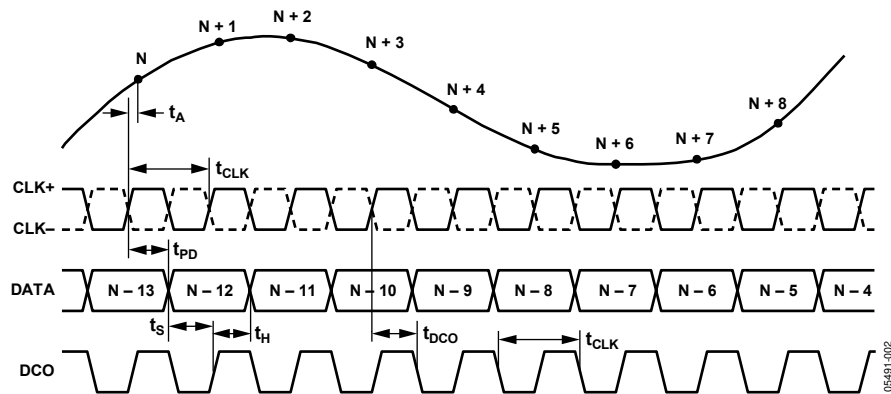


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to DGND	−0.3 V to +3.9 V
AGND to DGND	−0.3 V to +0.3 V
AVDD to DRVDD	−3.9 V to +2.0 V
D0 through D13 to DGND	−0.3 V to DRVDD + 0.3 V
DCO to DGND	−0.3 V to DRVDD + 0.3 V
OR to DGND	−0.3 V to DRVDD + 0.3 V
CLK+ to AGND	−0.3 V to +3.9 V
CLK− to AGND	−0.3 V to +3.9 V
VIN+ to AGND	−0.3 V to AVDD + 0.2 V
VIN− to AGND	−0.3 V to AVDD + 0.2 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
REFT to AGND	−0.3 V to AVDD + 0.2 V
REFB to AGND	−0.3 V to AVDD + 0.2 V
SDIO/DCS to DGND	−0.3 V to DRVDD + 0.3 V
PDWN to AGND	−0.3 V to +3.9 V
CSB to AGND	−0.3 V to +3.9 V
SCLK/DFS to AGND	−0.3 V to +3.9 V
OEB to AGND	−0.3 V to +3.9 V
ENVIRONMENTAL	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 Sec)	+300°C
Junction Temperature	+150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP_VQ package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-lead LFCSP_VQ (CP-48-3)	26.4	2.4	°C/W

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation effectively reducing θ_{JA} . In addition, metal in direct contact with the package leads from metal traces, and through holes, ground, and power planes, reduces the θ_{JA} .

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

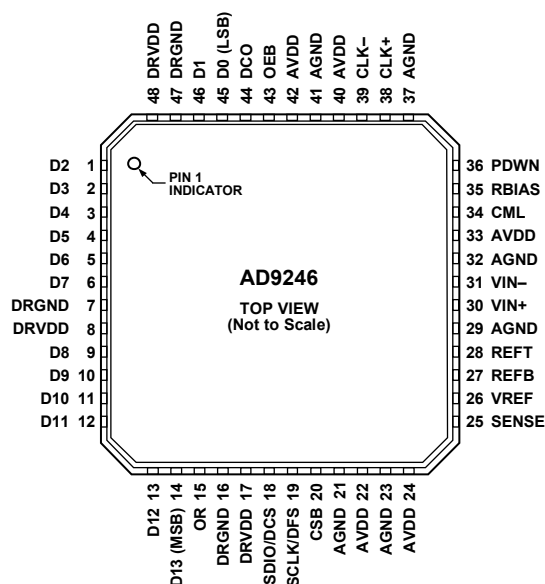


Figure 3. Pin Configuration

05481-003

Table 7. Pin Function Description

Pin No.	Mnemonic	Description
0, 21, 23, 29, 32, 37, 41	AGND	Analog Ground. (Pin 0 is the exposed thermal pad on the bottom of the package.)
45, 46, 1 to 6, 9 to 14	D0 (LSB) to D13 (MSB)	Data Output Bits.
7, 16, 47	DRGND	Digital Output Ground.
8, 17, 48	DRVDD	Digital Output Driver Supply (1.8 V to 3.3 V).
15	OR	Out-of-Range Indicator.
18	SDIO/DCS	Serial Port Interface (SPI) [®] Data Input/Output (Serial Port Mode); Duty Cycle Stabilizer Select (External Pin Mode). See Table 10.
19	SCLK/DFS	Serial Port Interface Clock (Serial Port Mode); Data Format Select Pin (External Pin Mode).
20	CSB	Serial Port Interface Chip Select (Active Low). See Table 10.
22, 24, 33, 40, 42	AVDD	Analog Power Supply.
25	SENSE	Reference Mode Selection. See Table 9.
26	VREF	Voltage Reference Input/Output.
27	REFB	Differential Reference (-).
28	REFT	Differential Reference (+).
30	VIN+	Analog Input Pin (+).
31	VIN-	Analog Input Pin (-).
34	CML	Common-Mode Level Bias Output.
35	RBIAS	External Bias Resistor Connection. A 10 k Ω resistor must be connected between this pin and analog ground (AGND).
36	PDWN	Power-Down Function Select.
38	CLK+	Clock Input (+).
39	CLK-	Clock Input (-).
43	OEB	Output Enable (Active Low).
44	DCO	Data Clock Output.

EQUIVALENT CIRCUITS

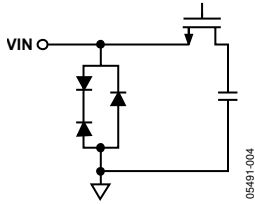


Figure 4. Equivalent Analog Input Circuit

05491-004

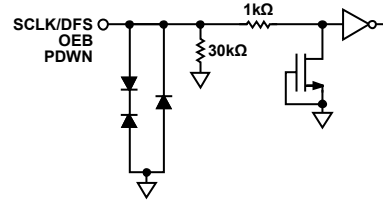


Figure 8. Equivalent SCLK/DFS, OEB, PDWN Input Circuit

05491-008

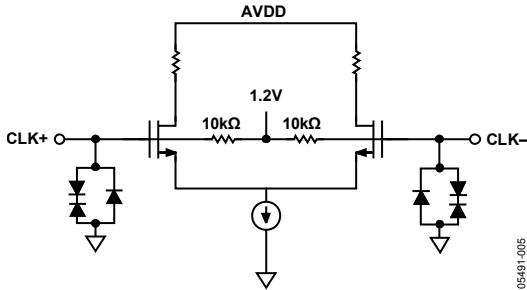


Figure 5. Equivalent Clock Input Circuit

05491-005

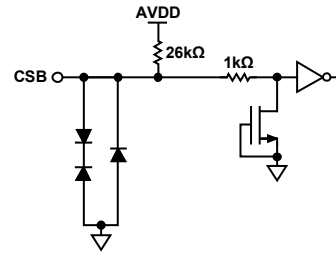


Figure 9. Equivalent CSB Input Circuit

05491-010

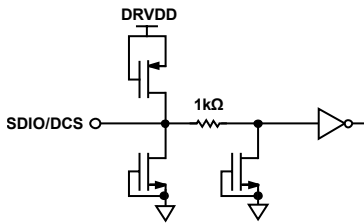


Figure 6. Equivalent SDIO/DCS Input Circuit

05491-006

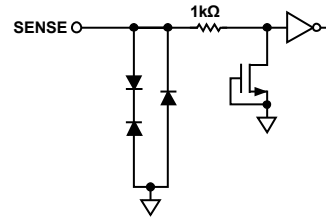


Figure 10. Equivalent Sense Circuit

05491-011

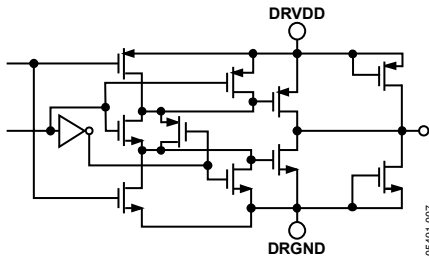


Figure 7. Equivalent Digital Output Circuit

05491-007

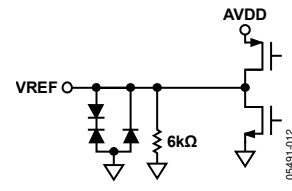


Figure 11. Equivalent VREF Circuit

05491-012

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V; DRVDD = 2.5 V; maximum sample rate, DCS enabled, 1 V internal reference; 2 V p-p differential input; AIN = -1.0 dBFS; 64k sample; T_A = 25°C, unless otherwise noted. All figures show typical performance for all speed grades.

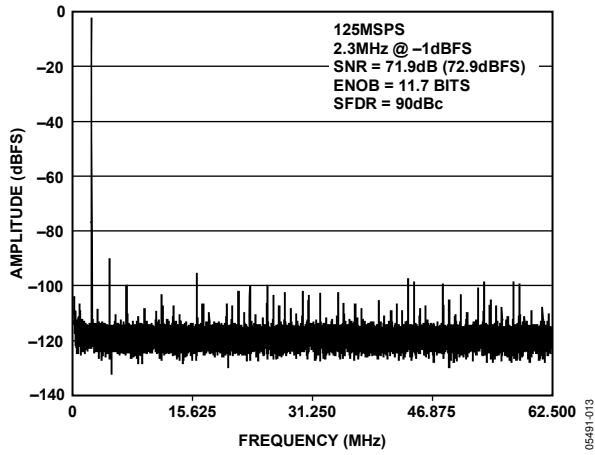


Figure 12. AD9246-125 Single-Tone FFT with $f_{IN} = 2.3$ MHz

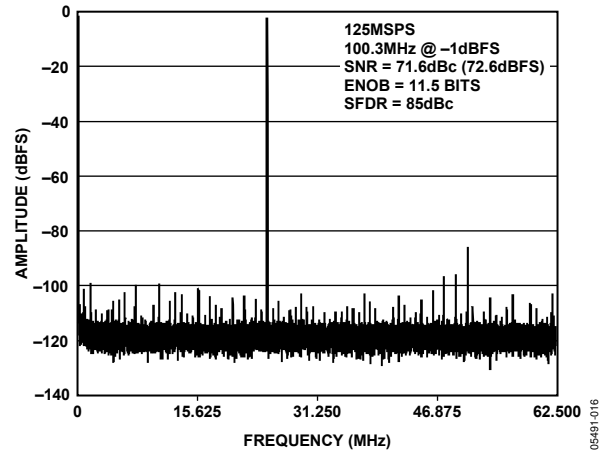


Figure 15. AD9246-125 Single-Tone FFT with $f_{IN} = 100.3$ MHz

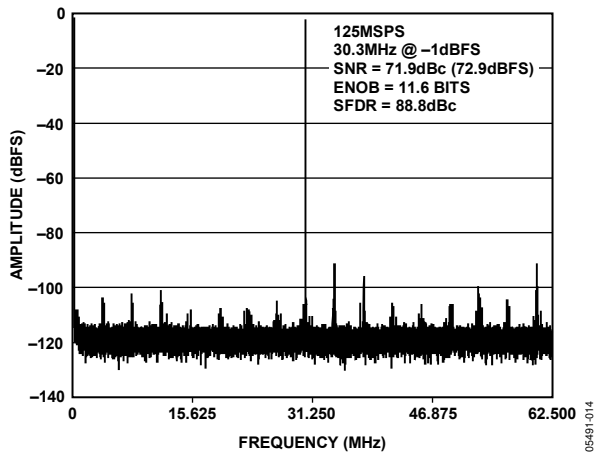


Figure 13. AD9246-125 Single-Tone FFT with $f_{IN} = 30.3$ MHz

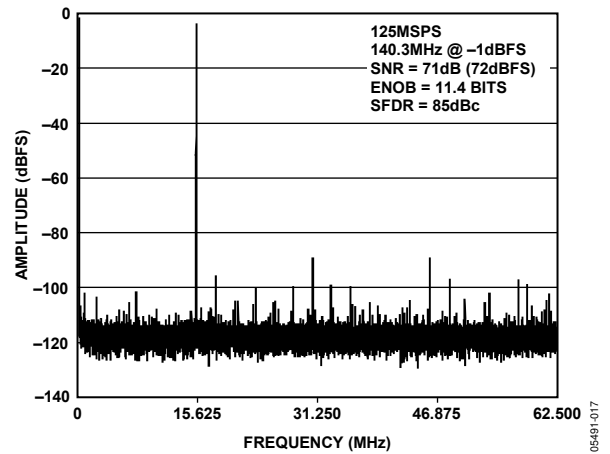


Figure 16. AD9246-125 Single-Tone FFT with $f_{IN} = 140.3$ MHz

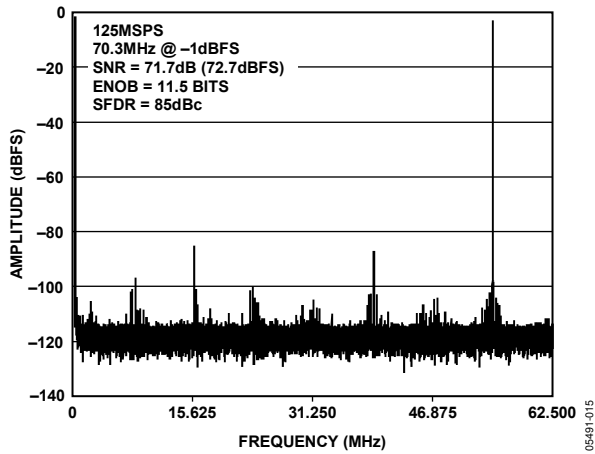


Figure 14. AD9246-125 Single-Tone FFT with $f_{IN} = 70.3$ MHz

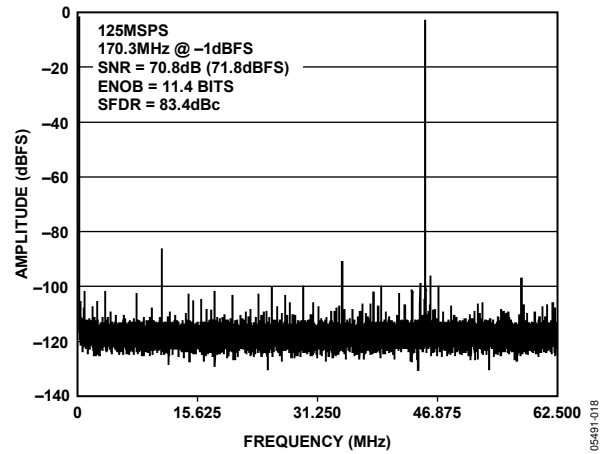


Figure 17. AD9246-125 Single-Tone FFT with $f_{IN} = 170.3$ MHz

AD9246

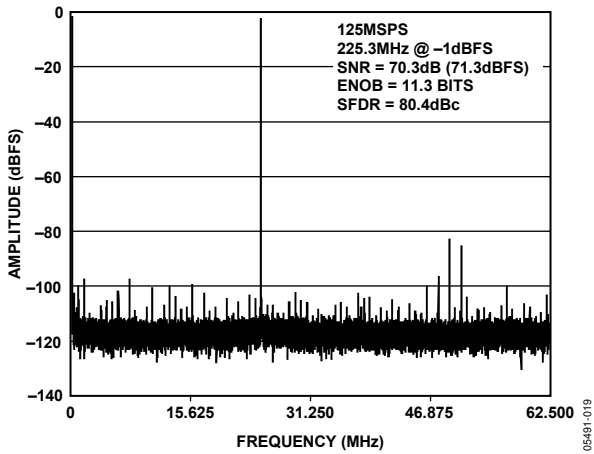


Figure 18. AD9246-125 Single-Tone FFT with $f_{IN} = 225.3$ MHz

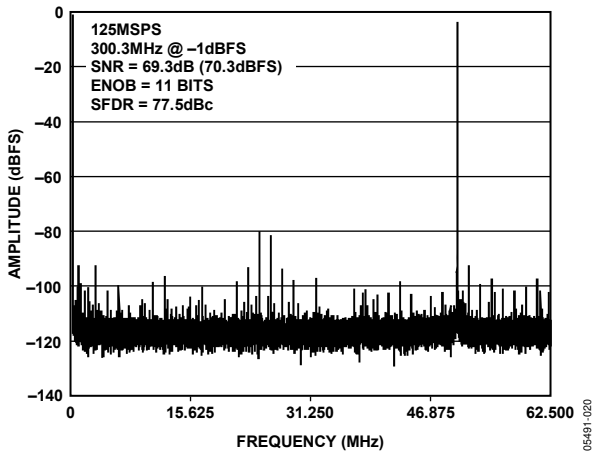


Figure 19. AD9246-125 Single-Tone FFT with $f_{IN} = 300.3$ MHz

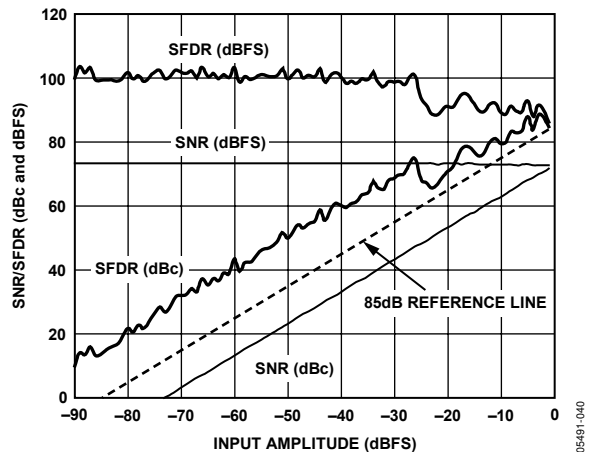


Figure 20. AD9246 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with $f_{IN} = 2.4$ MHz

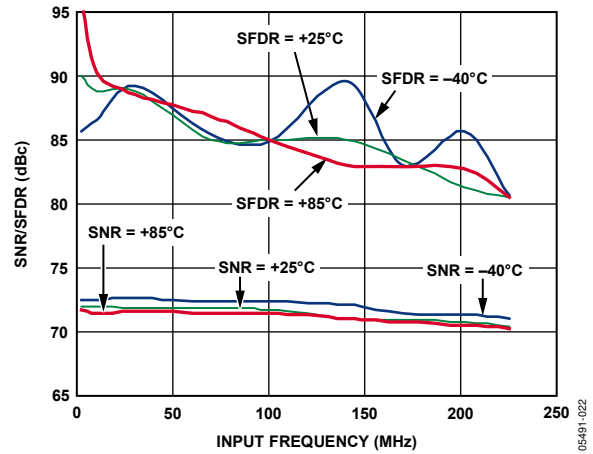


Figure 21. AD9246 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2V p-p Full Scale

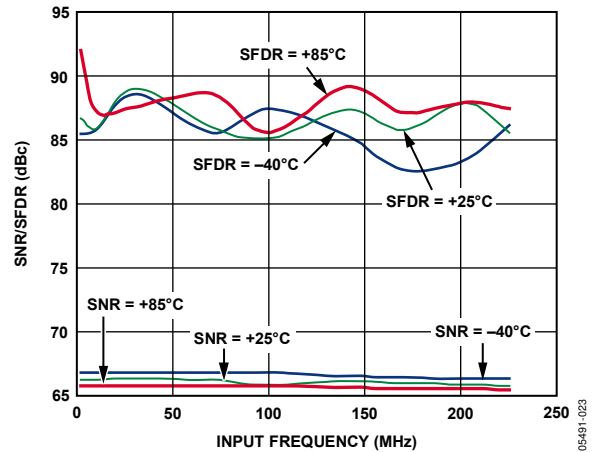


Figure 22. AD9246 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1V p-p Full Scale

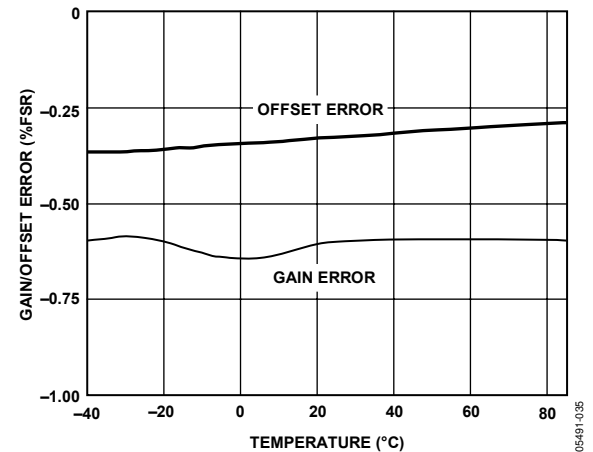


Figure 23. AD9246 Gain and Offset vs. Temperature

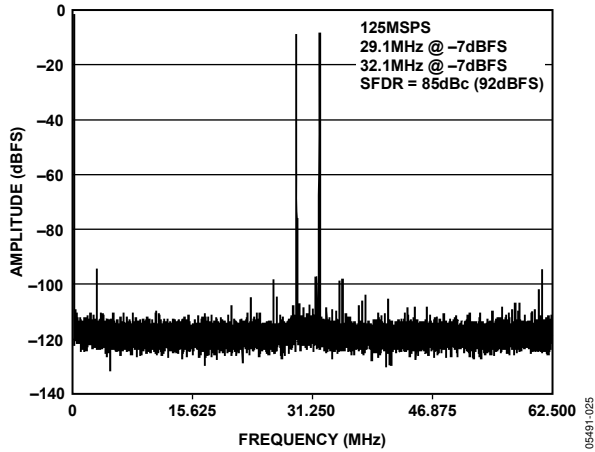


Figure 24. AD9246-125 Two-Tone FFT with $f_{IN1} = 29.1$ MHz, $f_{IN2} = 32.1$ MHz

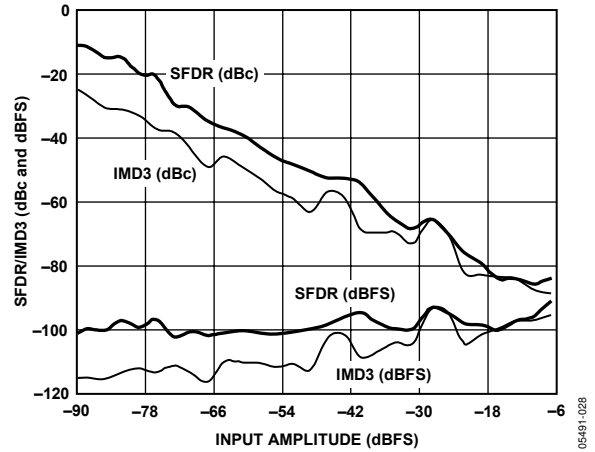


Figure 27. AD9246 Two-Tone SFDR/IMD vs. Input Amplitude (A_{IN}) with $F_{IN1} = 29.1$ MHz, $F_{IN2} = 32.1$ MHz

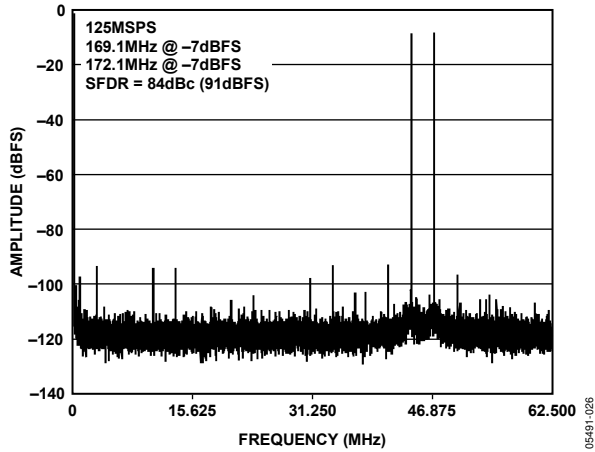


Figure 25. AD9246-125 Two-Tone FFT with $f_{IN1} = 169.1$ MHz, $f_{IN2} = 172.1$ MHz

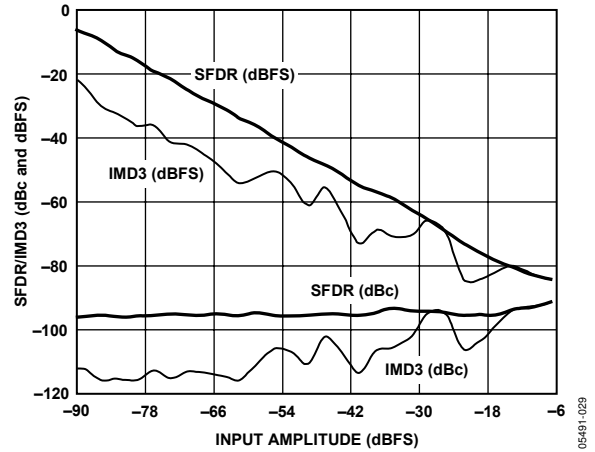


Figure 28. AD9246 Two-Tone SFDR/IMD vs. Input Amplitude (A_{IN}) with $F_{IN1} = 169.1$ MHz, $F_{IN2} = 172.1$ MHz

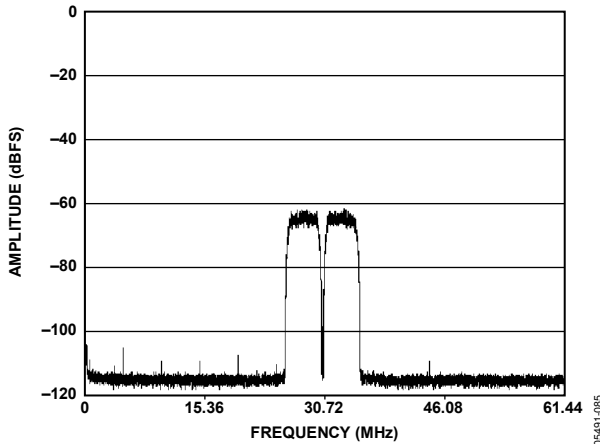


Figure 26. AD9246-125 Two 64k WCDMA Carriers with $f_{IN} = 215.04$ MHz, $f_s = 122.88$ MSPS

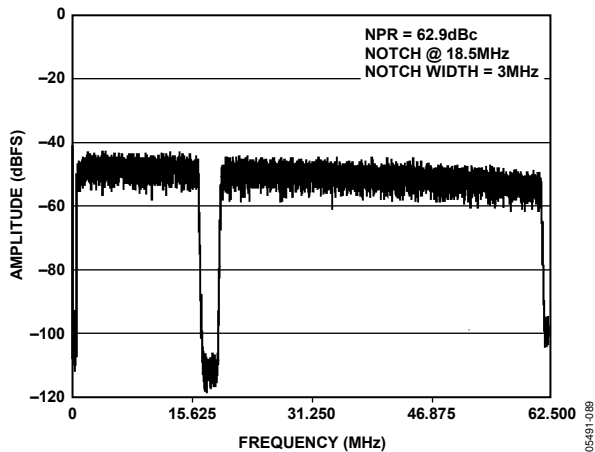


Figure 29. AD9246 Noise Power Ratio (NPR)

AD9246

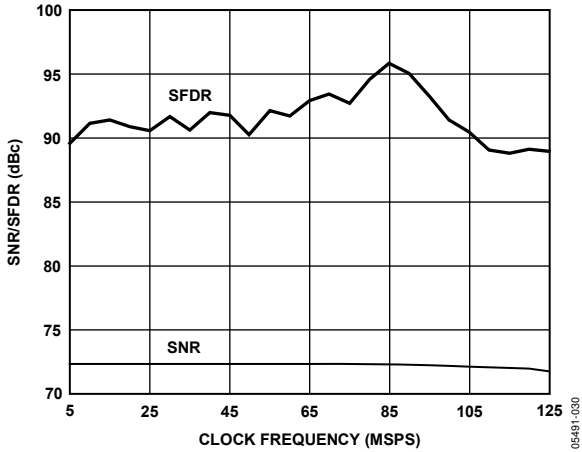


Figure 30. AD9246 Single-Tone SNR/SFDR vs. Clock Frequency (f_s) with $f_{IN} = 2.4$ MHz

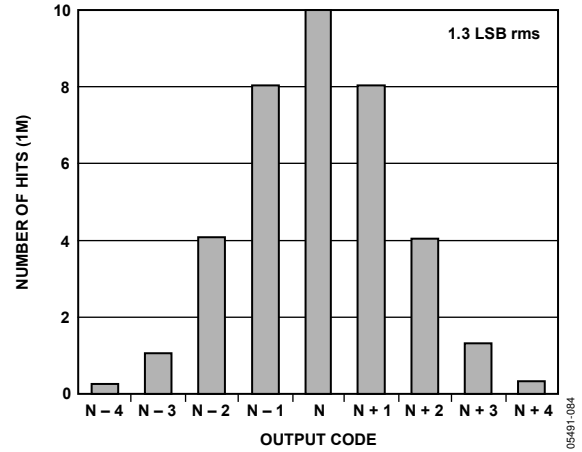


Figure 33. AD9246 Grounded Input Histogram

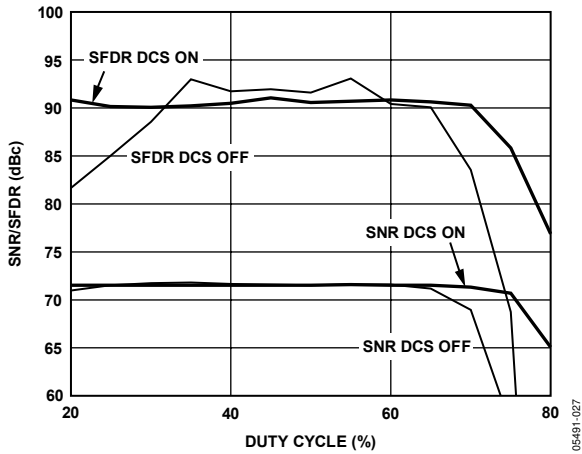


Figure 31. AD9246 SNR/SFDR vs. Duty Cycle with $f_{IN} = 10.3$ MHz

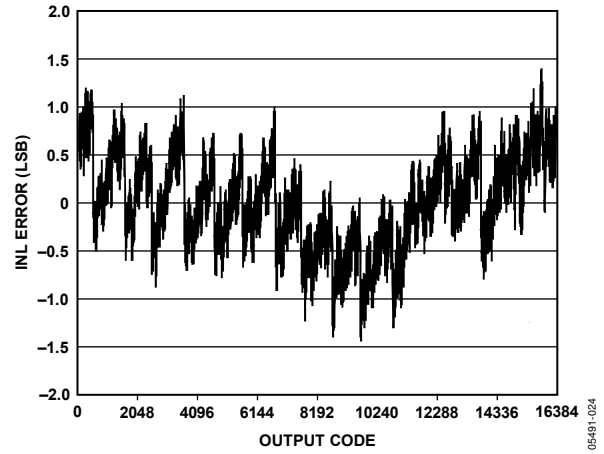


Figure 34. AD9246 INL with $f_{IN} = 10.3$ MHz

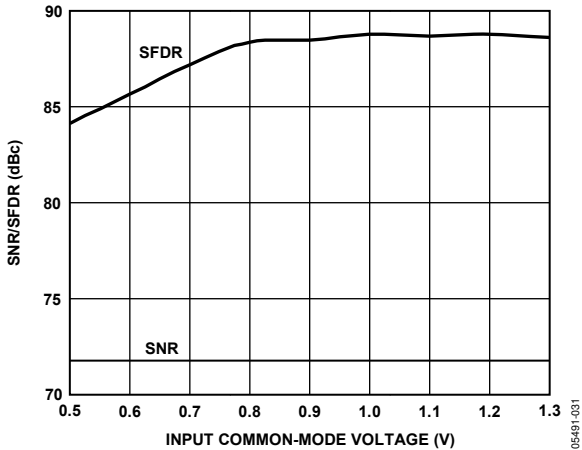


Figure 32. AD9246 SNR/SFDR vs. Input Common Mode (VCM) with $f_{IN} = 30$ MHz

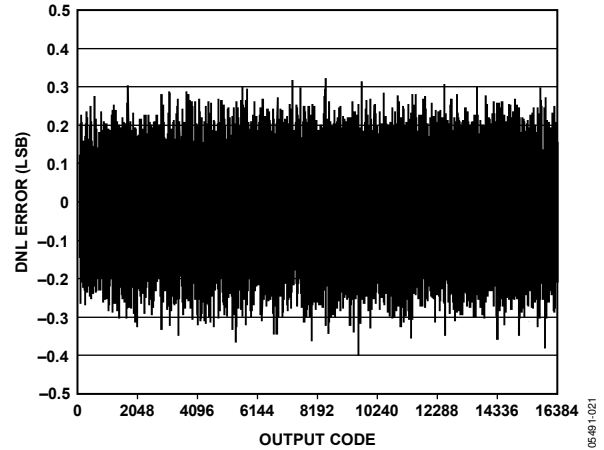


Figure 35. AD9246 DNL with $f_{IN} = 10.3$ MHz

THEORY OF OPERATION

The AD9246 architecture consists of a front-end sample-and-hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipeline architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9246 is a differential switched capacitor SHA that has been designed for optimum performance while processing a differential input signal.

The clock signal alternately switches the SHA between sample mode and hold mode (see Figure 36). When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source.

A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In IF undersampling applications, any shunt capacitors should be reduced. In combination with the driving source impedance, these capacitors would limit the input bandwidth.

For more information, see Application Notes [AN-742, Frequency Domain Response of Switched-Capacitor ADCs](#); and [AN-827, A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs](#), and the *Analog Dialogue* article, “[Transformer-Coupled Front-End for Wideband A/D Converters](#).”

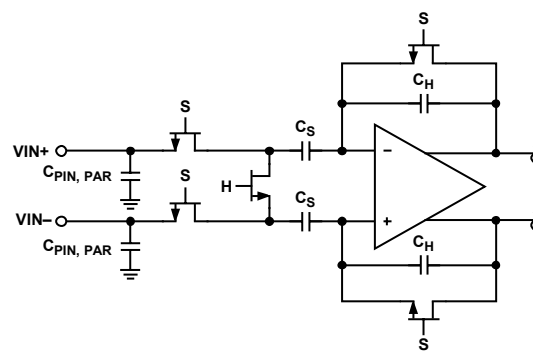


Figure 36. Switched Capacitor SHA Input

For best dynamic performance, the source impedances driving V_{IN+} and V_{IN-} should match such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

An internal differential reference buffer creates two reference voltages used to define the input span of the ADC core. The span of the ADC core is set by the buffer to be $2 \times V_{REF}$. The reference voltages are not available to the user. Two bypass points, REFT and REFB, are brought out for decoupling to reduce the noise contributed by the internal reference buffer. It is recommended that REFT be decoupled to REFB by a 0.1 μF capacitor, as described in the Layout Considerations section.

Input Common Mode

The analog inputs of the AD9246 are not internally dc-biased. In ac-coupled applications, the user must provide this bias externally. Setting the device such that $V_{CM} = 0.55 \times AV_{DD}$ is recommended for optimum performance; however, the device functions over a wider range with reasonable performance (see Figure 32). An on-board, common-mode voltage reference is included in the design and is available from the CML pin. Optimum performance is achieved when the common-mode voltage of the analog input is set by the CML pin voltage (typically $0.55 \times AV_{DD}$). The CML pin must be decoupled to ground by a 0.1 μF capacitor, as described in the Layout Considerations section.

DIFFERENTIAL INPUT CONFIGURATIONS

Optimum performance is achieved by driving the AD9246 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set with the CML pin of the AD9246 (see Figure 37), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

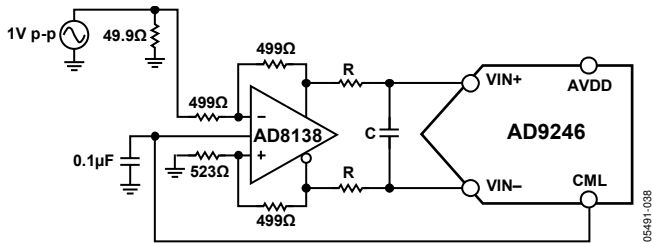


Figure 37. Differential Input Configuration Using the AD8138

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 38). The CML voltage can be connected to the center tap of the secondary winding of the transformer to bias the analog input.

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can cause core saturation, which leads to distortion.

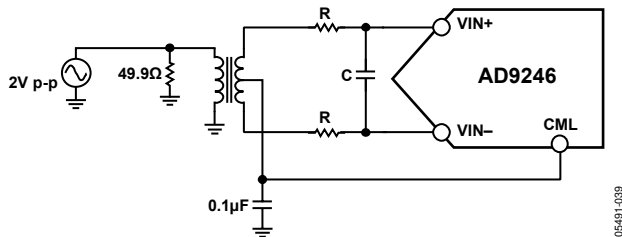


Figure 38. Differential Transformer-Coupled Configuration

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9246. For applications where SNR is a key parameter, transformer coupling is the recommended input.

For applications where SFDR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 40).

As an alternative to using a transformer-coupled input at frequencies in the second Nyquist zone, the AD8352 differential driver can be used (see Figure 41).

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 8 displays recommended values to set the RC network. However, these values are dependent on the input signal and should only be used as a starting guide.

Table 8. RC Network Recommended Values

Frequency Range (MHz)	R Series (Ω)	C Differential (pF)
0 to 70	33	15
70 to 200	33	5
200 to 300	15	5
>300	15	Open

Single-Ended Input Configuration

Although not recommended, it is possible to operate the AD9246 in a single-ended input configuration, as long as the input voltage swing is within the AVDD supply. Single-ended operation can provide adequate performance in cost-sensitive applications.

In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the source impedances on each input are matched, there should be little effect on SNR performance. Figure 39 details a typical single-ended input configuration.

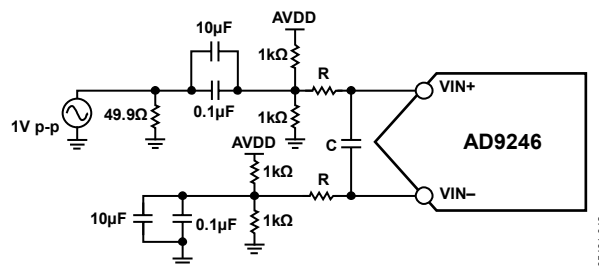


Figure 39. Single-Ended Input Configuration

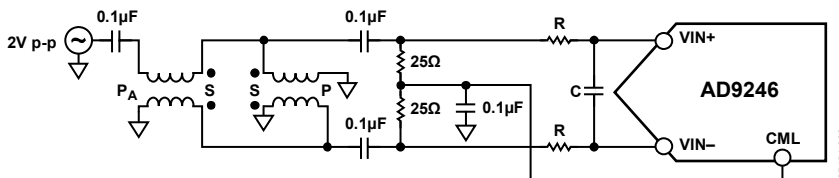


Figure 40. Differential Double Balun Input Configuration

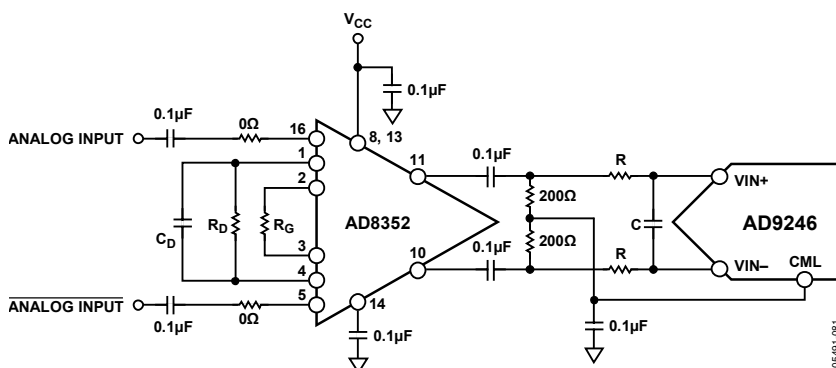


Figure 41. Differential Input Configuration Using the AD8352

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × External Reference
Internal Fixed Reference	VREF	0.5	1.0
Programmable Reference	0.2 V to VREF	$0.5 \times \left(1 + \frac{R2}{R1}\right)$ (see Figure 43)	2 × VREF
Internal Fixed Reference	AGND to 0.2 V	1.0	2.0

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9246. The input range is adjustable by varying the reference voltage applied to the AD9246, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly. The various reference modes are summarized in the following sections. The Reference Decoupling section describes the best practices and requirements for PCB layout of the reference.

Internal Reference Connection

A comparator within the AD9246 detects the potential at the SENSE pin and configures the reference into four possible states, as summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 42), setting VREF to 1 V.

Connecting the SENSE pin to VREF switches the reference amplifier input to the SENSE pin, completing the loop and providing a 0.5 V reference output.

If a resistor divider is connected external to the chip as shown in Figure 43, the switch sets to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$VREF = 0.5 \left(1 + \frac{R2}{R1}\right)$$

If the SENSE pin is connected to AVDD, the reference amplifier is disabled, and an external reference voltage can be applied to the VREF pin (see the External Reference Operation section).

The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

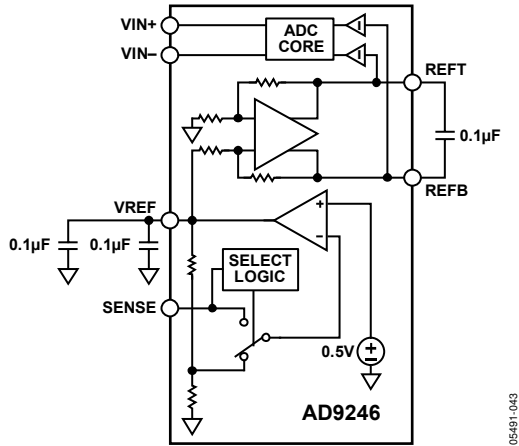


Figure 42. Internal Reference Configuration

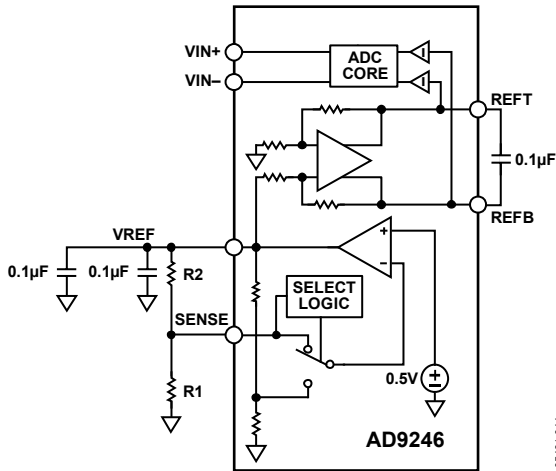


Figure 43. Programmable Reference Configuration

If the internal reference of the AD9246 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 44 depicts how the internal reference voltage is affected by loading.

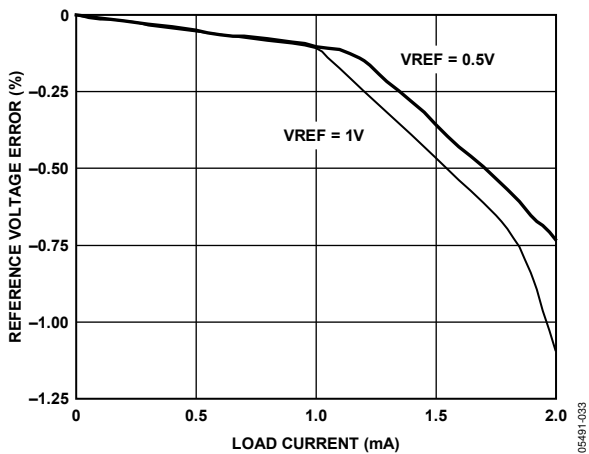


Figure 44. VREF Accuracy vs. Load

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 45 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes.

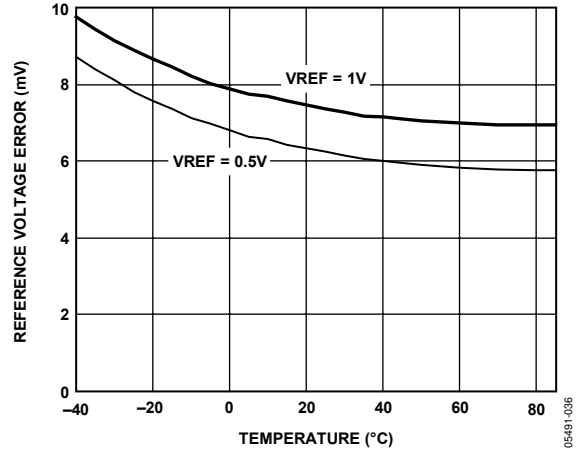


Figure 45. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal resistor divider loads the external reference with an equivalent 6 kΩ load (see Figure 11). In addition, an internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1 V.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9246 sample clock inputs (CLK+ and CLK-) should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ pin and the CLK- pin via a transformer or capacitors. These pins are biased internally (see Figure 5) and require no external bias.

Clock Input Options

The AD9246 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal used, the jitter of the clock source is of the most concern (see the Jitter Considerations section).

Figure 46 shows one preferred method for clocking the AD9246. A low jitter clock source is converted from single-ended to a differential signal using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD9246 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9246, while preserving the fast rise and fall times of the signal, which are critical to a low jitter performance.

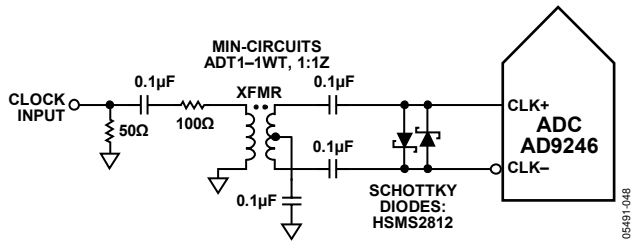


Figure 46. Transformer Coupled Differential Clock

If a low jitter clock source is not available, another option is to ac-couple a differential PECL signal to the sample clock input pins, as shown in Figure 47. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

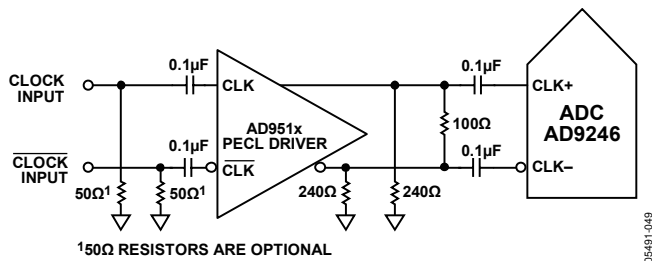


Figure 47. Differential PECL Sample Clock

A third option is to ac-couple a differential LVDS signal to the sample clock input pins, as shown in Figure 48. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

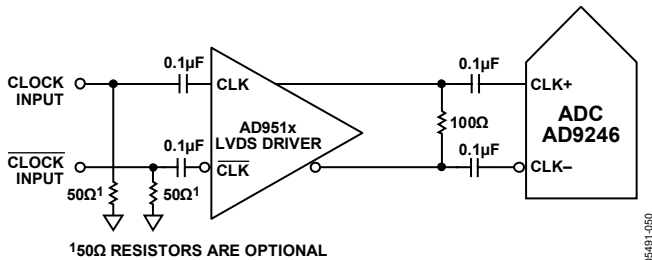


Figure 48. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, directly drive CLK+ from a CMOS gate, while bypassing the CLK- pin to ground using a 0.1 μF capacitor in parallel with a 39 kΩ resistor (see Figure 49). CLK+ may be directly driven from a CMOS gate. This input is designed to withstand input voltages up to 3.6 V, making the selection of the drive logic voltage very flexible. When driving CLK+ with a 1.8 V CMOS signal, biasing the CLK- pin with a 0.1 μF capacitor in parallel with a 39 kΩ resistor (see Figure 49) is required. The 39 kΩ resistor is not required when driving CLK+ with a 3.3 V CMOS signal (see Figure 50).

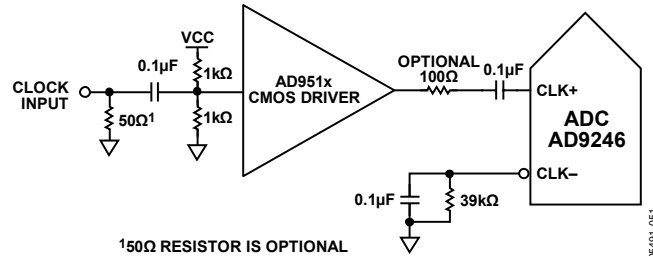


Figure 49. Single-Ended 1.8 V CMOS Sample Clock

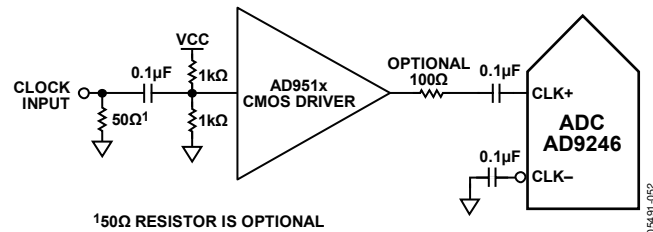


Figure 50. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9246 contains a duty cycle stabilizer (DCS) that retimes the nonsampling, or falling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9246. Noise and distortion performance are nearly flat for a wide range of duty cycles when the DCS is on, as shown in Figure 31.

Jitter in the rising edge of the input is still of paramount concern and is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 20 MHz nominally. The loop has a time constant associated with it that needs to be considered in applications where the clock rate can change dynamically. This requires a wait time of 1.5 μs to 5 μs after a dynamic clock frequency increase (or decrease) before the DCS loop is relocked to the input signal. During the time period the loop is not locked, the DCS loop is bypassed, and the internal device timing is dependent on the duty cycle of the input clock signal. In such an application, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

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The DCS can be enabled or disabled by setting the SDIO/DCS pin when operating in the external pin mode (see Table 10), or via the SPI, as described in Table 13.

Table 10. Mode Selection (External Pin Mode)

Voltage at Pin	SCLK/DFS	SDIO/DCS
AGND	Binary (default)	DCS disabled
AVDD	Twos complement	DCS enabled (default)

JITTER CONSIDERATIONS

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{IN}) due to jitter (t_j) is calculated as follows:

$$SNR = -20 \log(2\pi \times f_{IN} \times t_j)$$

In the equation, the rms aperture jitter represents the root mean square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. IF under-sampling applications are particularly sensitive to jitter, as illustrated in Figure 51.

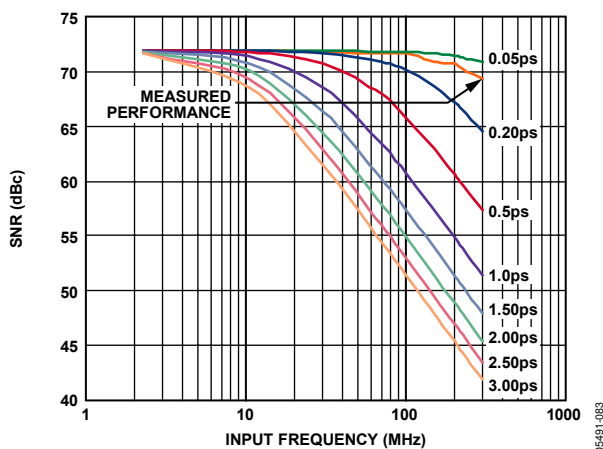


Figure 51. SNR vs. Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9246. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. The power supplies should also not be shared with analog input circuits, such as buffers, to avoid the clock modulating onto the input signal or vice versa. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to Application Notes [AN-501, Aperture Uncertainty and ADC System Performance](#), and [AN-756, Sampled Systems and the Effects of Clock Phase Noise and Jitter](#), for more in-depth information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 52 and Figure 53, the power dissipated by the AD9246 is proportional to its sample rate. The digital power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The maximum DRVDD current (I_{DRVDD}) can be calculated as:

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times \frac{f_{CLK}}{2} \times N$$

where N is the number of output bits, 14 in the case of the AD9246.

This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency, $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the sample rate and the characteristics of the analog input signal. Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 52 and Figure 53 was taken under the same operating conditions as the data for the Typical Performance Characteristics section, with a 5 pF load on each output driver.

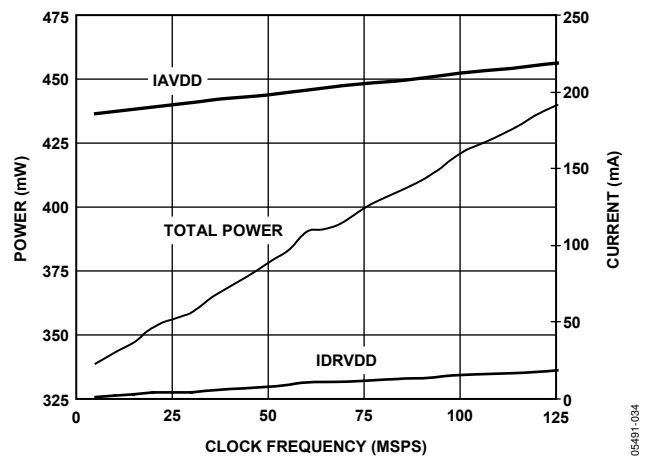


Figure 52. AD9246-125 Power and Current vs. Clock Frequency $f_{IN} = 30$ MHz

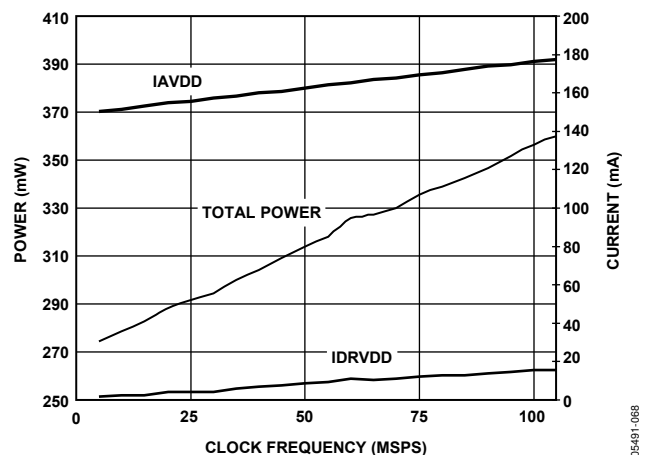


Figure 53. AD9246-105 Power and Current vs. Clock Frequency $f_{IN} = 30$ MHz

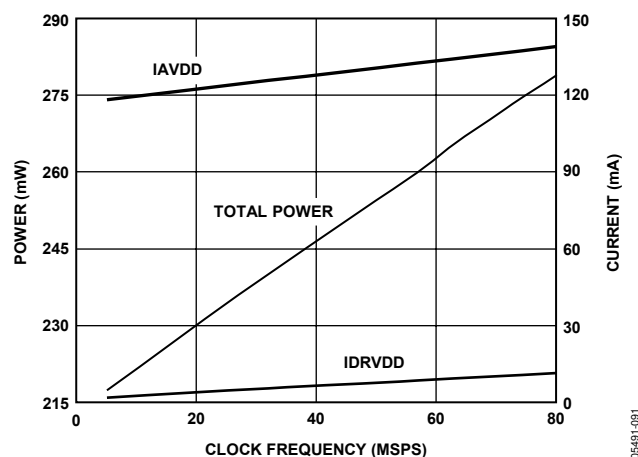


Figure 54. AD9246-80 Power and Current vs. Clock Frequency $f_{IN} = 30$ MHz

Power-Down Mode

By asserting the PDWN pin high, the AD9246 is placed in power-down mode. In this state, the ADC typically dissipates 1.8 mW. During power-down, the output drivers are placed in a high impedance state. Reasserting the PDWN pin low returns the AD9246 to its normal operational mode. This pin is both 1.8 V and 3.3 V tolerant.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. The decoupling capacitors on REFT and REFB are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in power-down mode; and shorter power-down cycles result in proportionally shorter wake-up times. With the recommended 0.1 μ F decoupling capacitors on REFT and REFB, it takes approximately 0.25 ms to fully discharge the reference buffer decoupling capacitors and 0.35 ms to restore full operation.

Standby Mode

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required (see the Memory Map section).

DIGITAL OUTPUTS

The AD9246 output drivers can be configured to interface with 1.8 V to 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fan-outs may require external buffers or latches.

The output data format can be selected for either offset binary or twos complement by setting the SCLK/DFS pin when operating in the external pin mode (see Table 10).

As detailed in the [Interfacing to High Speed ADCs via SPI User Manual](#), the data format can be selected for either offset binary, twos complement, or Gray code when using the SPI control.

Out-of-Range (OR) Condition

An out-of-range condition exists when the analog input voltage is beyond the input range of the ADC. OR is a digital output that is updated along with the data output corresponding to the particular sampled input voltage. Thus, OR has the same pipeline latency as the digital data.

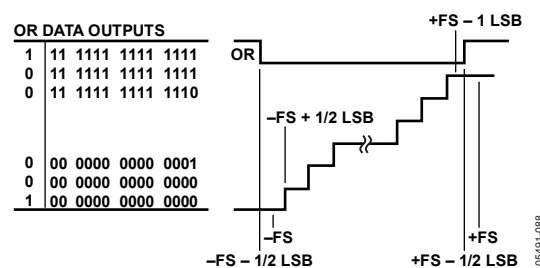


Figure 55. OR Relation to Input Voltage and Output Data

OR is low when the analog input voltage is within the analog input range and high when the analog input voltage exceeds the input range, as shown in Figure 55. OR remains high until the analog input returns to within the input range, and another conversion is completed. By logically AND'ing the OR bit with the MSB and its complement, overrange high or underrange low conditions can be detected. Table 11 is a truth table for the overrange/underrange circuit in Figure 56, which uses NAND gates.

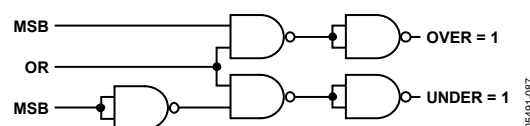


Figure 56. Overrange/Underrange Logic

Table 11. Overrange/Underrange Truth Table

OR	MSB	Analog Input Is:
0	0	Within range
0	1	Within range
1	0	Underrange
1	1	Overrange

Digital Output Enable Function (OEB)

The AD9246 has three-state ability. If the OEB pin is low, the output data drivers are enabled. If the OEB pin is high, the output data drivers are placed in a high impedance state. This is not intended for rapid access to the data bus. Note that OEB is referenced to the digital supplies (DRVDD) and should not exceed that supply voltage.

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TIMING

The lowest typical conversion rate of the AD9246 is 10 MSPS. At clock rates below 10 MSPS, dynamic performance can degrade.

The AD9246 provides latched data outputs with a pipeline delay of 12 clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9246. These transients can degrade the dynamic performance of the converter.

Data Clock Output (DCO)

The AD9246 provides a data clock output (DCO) intended for capturing the data in an external register. The data outputs are valid on the rising edge of DCO, unless the DCO clock polarity has been changed via the SPI. See Figure 2 for a graphical timing description.

Table 12. Output Data Format

Input (V)	Condition (V)	Binary Output Mode	Twos Complement Mode	Gray Code Mode (SPI accessible)	OR
VIN+ – VIN–	< –VREF – 0.5 LSB	00 0000 0000 0000	10 0000 0000 0000	11 0000 0000 0000	1
VIN+ – VIN–	= –VREF	00 0000 0000 0000	10 0000 0000 0000	11 0000 0000 0000	0
VIN+ – VIN–	= 0	10 0000 0000 0000	00 0000 0000 0000	00 0000 0000 0000	0
VIN+ – VIN–	= +VREF – 1.0 LSB	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000	0
VIN+ – VIN–	> +VREF – 0.5 LSB	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000	1

SERIAL PORT INTERFACE (SPI)

The AD9246 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. This provides the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that are further divided into fields, as documented in the Memory Map section. For detailed operational information, see the [Interfacing to High Speed ADCs via SPI User Manual](#).

CONFIGURATION USING THE SPI

As summarized in Table 13, three pins define the SPI of this ADC. The SCLK/DFS pin synchronizes the read and write data presented to the ADC. The SDIO/DCS dual purpose pin allows data to be sent and read from the internal ADC memory map registers. The CSB pin is an active low control that enables or disables the read and write cycles.

Table 13. Serial Port Interface Pins

Pin Name	Function
SCLK/DFS	SCLK (serial clock) is the serial shift clock in. SCLK synchronizes serial interface reads and writes.
SDIO/DCS	SDIO (serial data input/output) is a dual purpose pin. The typical role for this pin is an input and output, depending on the instruction being sent and the relative position in the timing frame.
CSB	CSB (chip select bar) is an active low control that gates the read and write cycles.

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing. Figure 57 and Table 14 provide examples of the serial timing and its definitions.

Other modes involving the CSB are available. The CSB can be held low indefinitely to permanently enable the device (this is called streaming). The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and the length is determined by the W0 bit and the W1 bit. All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip as well as read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB- or in LSB-first mode. MSB first is the default on power up and can be changed via the configuration register. For more information, see the [Interfacing to High Speed ADCs via SPI User Manual](#).

Table 14. SPI Timing Diagram Specifications

Name	Description
t _{DS}	Setup time between data and rising edge of SCLK
t _{DH}	Hold time between data and rising edge of SCLK
t _{CLK}	Period of the clock
t _S	Setup time between CSB and SCLK
t _H	Hold time between CSB and SCLK
t _{HI}	Minimum period that SCLK should be in a logic high state
t _{LO}	Minimum period that SCLK should be in a logic low state

HARDWARE INTERFACE

The pins described in Table 13 comprise the physical interface between the user's programming device and the serial port of the AD9246. The SCLK and CSB pins function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either PROM or PIC microcontrollers. This provides the user with the ability to use an alternate method to program the ADC. One method is described in detail in the Application Note [AN-812, Microcontroller-based Serial Port Interface Boot Circuit](#).

When the SPI interface is not used, some pins serve a dual function. When strapped to AVDD or ground during device power-on, the pins are associated with a specific function.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO/DCS and SCLK/DFS pins serve as stand-alone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the output data format and duty cycle stabilizer (see Table 10). In this mode, the CSB chip select should be connected to AVDD, which disables the serial port interface. For more information, see the [Interfacing to High Speed ADCs via SPI User Manual](#).

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight address locations. The memory map is roughly divided into three sections: the chip configuration registers map (Address 0x00 to Address 0x02), the device index and transfer registers map (Address 0xFF), and the ADC functions map (Address 0x08 to Address 0x18).

Table 15 displays the register address number in hexadecimal in the first column. The last column displays the default value for each hexadecimal address. The Bit 7 (MSB) column is the start of the default hexadecimal value given. For example, Hexadecimal Address 0x14, output_phase, has a hexadecimal default value of 0x00. This means Bit 3 = 0, Bit 2 = 0, Bit 1 = 1, and Bit 0 = 1 or 0011 in binary. This setting is the default output clock or DCO phase adjust option. The default value adjusts the DCO phase 90° relative to the nominal DCO edge and 180° relative to the data edge. For more information on this function, consult the [Interfacing to High Speed ADCs via SPI User Manual](#).

Open Locations

Locations marked as open are currently not supported for this device. When required, these locations should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x14). If the entire address location is open (Address 0x13), then the address location does not need to be written.

Default Values

Coming out of reset, critical registers are loaded with default values. The default values for the registers are shown in Table 15.

Logic Levels

An explanation of two registers follows:

- “Bit is set” is synonymous with “Bit is set to Logic 1” or “Writing Logic 1 for the bit.”
- “Clear a bit” is synonymous with “Bit is set to Logic 0” or “Writing Logic 0 for the bit.”

SPI-Accessible Features

A list of features accessible via the SPI and a brief description of what the user can do with these features follow. These features are described in detail in the [Interfacing to High Speed ADCs via SPI User Manual](#).

- **Modes:** Set either power-down or standby mode.
- **Clock:** Access the DCS via the SPI.
- **Offset:** Digitally adjust the converter offset.
- **Test I/O:** Set test modes to have known data on output bits.
- **Output Mode:** Set up outputs; vary the strength of the output drivers.
- **Output Phase:** Set the output clock polarity.
- **VREF:** Set the reference voltage.

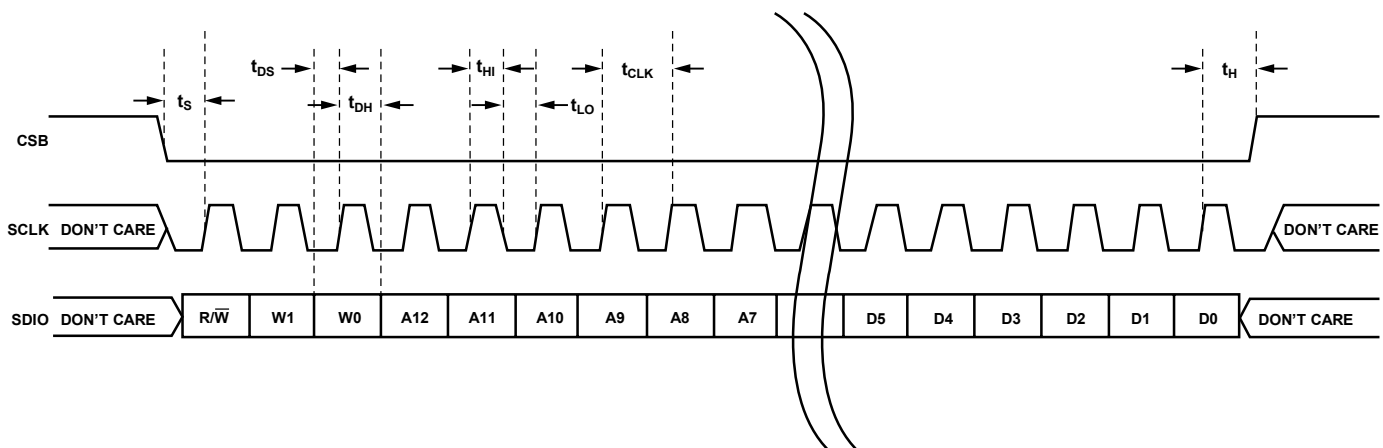


Figure 57. Serial Port Interface Timing Diagram

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