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16 Channel, 14-Bit, 65 MSPS, Serial LVDS, 1.8 V ADC

Data Sheet **AD9249**

FEATURES

- **Low power**
  - **16 ADC channels integrated into 1 package**
  - **58 mW per channel at 65 MSPS with scalable power options**
  - **35 mW per channel at 20 MSPS**
- **SNR: 75 dBFS (to Nyquist); SFDR: 90 dBc (to Nyquist)**
- **DNL: ±0.6 LSB (typical); INL: ±0.9 LSB (typical)**
- **Crosstalk, worst adjacent channel, 10 MHz, −1 dBFS: −90 dB typical**
- **Serial LVDS (ANSI-644, default)**
  - **Low power, reduced signal option (similar to IEEE 1596.3)**
- **Data and frame clock outputs**
- **650 MHz full power analog bandwidth**
- **2 V p-p input voltage range**
- **1.8 V supply operation**
- **Serial port control**
  - **Flexible bit orientation**
  - **Built in and custom digital test pattern generation**
  - **Programmable clock and data alignment**
  - **Power-down and standby modes**

APPLICATIONS

- **Medical imaging**
- **Communications receivers**
- **Multichannel data acquisition**

GENERAL DESCRIPTION

The AD9249 is a 16-channel, 14-bit, 65 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit that is designed for low cost, low power, small size, and ease of use. The device operates at a conversion rate of up to 65 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and an LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The AD9249 automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. Data clock outputs (DCO±1, DCO±2) for capturing data on the output and frame clock outputs (FCO±1, FCO±2) for signaling a new output byte are provided. Individual channel power-down is supported, and the device typically consumes less than 2 mW when all channels are disabled.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

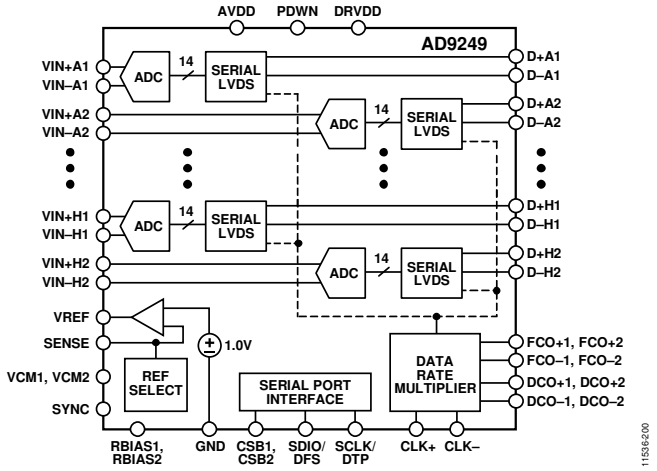

Figure 1.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation.

The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9249 is available in an RoHS-compliant, 144-ball CSP-BGA. It is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Small Footprint. Sixteen ADCs are contained in a small, 10 mm × 10 mm package.
2. Low Power. 35 mW/channel at 20 MSPS with scalable power options.
3. Ease of Use. Data clock outputs (DCO±1, DCO±2) operate at frequencies of up to 455 MHz and support double data rate (DDR) operation.
4. User Flexibility. SPI control offers a wide range of flexible features to meet specific system requirements.

Rev. 0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **Technical Support**

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AD9249* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9249 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9249: 16 Channel, 14-Bit, 65 MSPS, Serial LVDS, 1.8 V ADC Data Sheet

TOOLS AND SIMULATIONS

- AD9249 ADISimADC model
- AD9249 Input Impedance

REFERENCE MATERIALS

Press

- Low-Power 14-bit A/D Converters Enable High-Performance, Multi-Channel Data Acquisition in Compact Package

DESIGN RESOURCES

- AD9249 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9249 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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TABLE OF CONTENTS

REVISION HISTORY

10/13—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

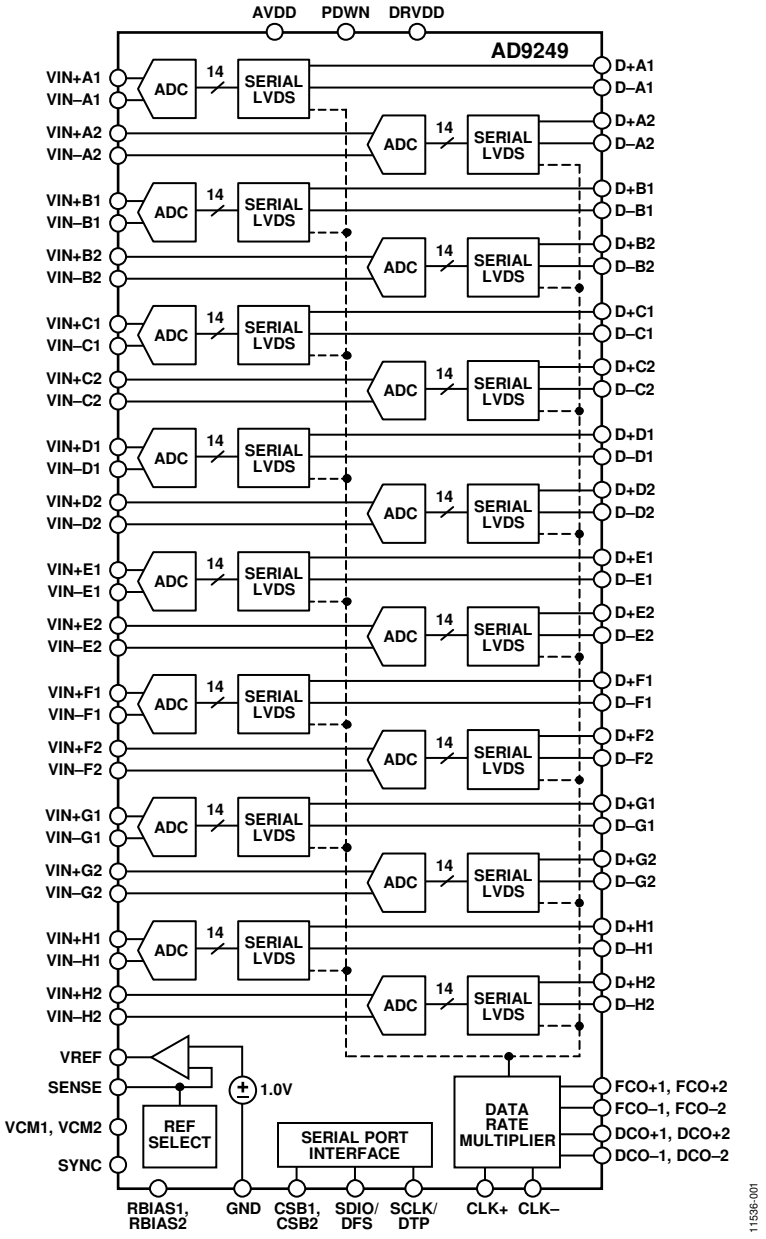

Figure 2.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	0	0.24	0.8	% FSR
Offset Matching	Full	0	0.24	0.7	% FSR
Gain Error	Full	−7.2	−3.5	+0.2	% FSR
Gain Matching	Full	0	1.8	6.0	% FSR
Differential Nonlinearity (DNL)	Full	−0.9	±0.6	+1.6	LSB
Integral Nonlinearity (INL)	Full	−3.0	±0.9	+3.0	LSB
TEMPERATURE DRIFT					
Offset Error	Full		−1.8		ppm/°C
Gain Error	Full		3.6		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	Full	0.98	1.0	1.01	V
Load Regulation at 1.0 mA (V_{REF} = 1 V)	25°C		3		mV
Input Resistance	Full		7.5		kΩ
INPUT REFERRED NOISE					
V_{REF} = 1.0 V	25°C		0.98		LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1 V)	Full		2		V p-p
Common-Mode Voltage	Full		0.9		V
Common-Mode Range	Full	0.5		1.3	V
Differential Input Resistance	Full		5.2		kΩ
Differential Input Capacitance	Full		3.5		pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD}	Full		395	429	mA
I_{DRVDD} (ANSI-644 Mode)	Full		118	124	mA
I_{DRVDD} (Reduced Range Mode)	25°C		88		mA
TOTAL POWER CONSUMPTION					
Total Power Dissipation (16 Channels, ANSI-644 Mode)	Full		924	995	mW
Total Power Dissipation (16 Channels, Reduced Range Mode)	25°C		869		mW
Power-Down Dissipation	25°C		2		mW
Standby Dissipation[2]	25°C		199		mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for information about how these tests were completed.
[2] Controlled via the SPI.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		75.4		dBFS
f_{IN} = 19.7 MHz	Full	74.4	75.3		dBFS
f_{IN} = 48 MHz	25°C		74.7		dBFS
f_{IN} = 69.5 MHz	25°C		74.4		dBFS
f_{IN} = 118 MHz	25°C		72.8		dBFS
f_{IN} = 139.5 MHz	25°C		72.2		dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25°C		75.4		dBFS
f_{IN} = 19.7 MHz	Full	74.0	75.3		dBFS
f_{IN} = 48 MHz	25°C		74.7		dBFS
f_{IN} = 69.5 MHz	25°C		74.4		dBFS
f_{IN} = 118 MHz	25°C		72.6		dBFS
f_{IN} = 139.5 MHz	25°C		71.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.2		Bits
f_{IN} = 19.7 MHz	Full	12.0	12.2		Bits
f_{IN} = 48 MHz	25°C		12.1		Bits
f_{IN} = 69.5 MHz	25°C		12.1		Bits
f_{IN} = 118 MHz	25°C		11.8		Bits
f_{IN} = 139.5 MHz	25°C		11.6		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		95		dBc
f_{IN} = 19.7 MHz	Full	85	93		dBc
f_{IN} = 48 MHz	25°C		94		dBc
f_{IN} = 69.5 MHz	25°C		92		dBc
f_{IN} = 118 MHz	25°C		83		dBc
f_{IN} = 139.5 MHz	25°C		82		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−98		dBc
f_{IN} = 19.7 MHz	Full		−93	−85	dBc
f_{IN} = 48 MHz	25°C		−94		dBc
f_{IN} = 69.5 MHz	25°C		−92		dBc
f_{IN} = 118 MHz	25°C		−83		dBc
f_{IN} = 139.5 MHz	25°C		−82		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−95		dBc
f_{IN} = 19.7 MHz	Full		−96	−86	dBc
f_{IN} = 48 MHz	25°C		−94		dBc
f_{IN} = 69.5 MHz	25°C		−92		dBc
f_{IN} = 118 MHz	25°C		−90		dBc
f_{IN} = 139.5 MHz	25°C		−90		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS					
f_{IN1} = 30.1 MHz, f_{IN2} = 32.1 MHz	25°C		92		dBc
CROSSTALK, WORST ADJACENT CHANNEL[2]	25°C		−90		dB
Crosstalk, Worst Adjacent Channel Overrange Condition[3]	25°C		−85		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 10 MHz, with −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[3] Overrange condition is defined as 3 dB above input full scale.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 3.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	0.2		3.6	V p-p
Input Voltage Range	Full	GND − 0.2		AVDD + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
LOGIC INPUTS (PDWN, SYNC, SCLK)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUTS (CSB1, CSB2)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (SDIO)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (D±x1, D±x2), ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	281	350	422	mV
Output Offset Voltage (V_{OS})	Full	1.12	1.22	1.38	V
Output Coding (Default)			Twos complement		
DIGITAL OUTPUTS (D±x1, D±x2), LOW POWER, REDUCED SIGNAL OPTION					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	150	201	250	mV
Output Offset Voltage (V_{OS})	Full	1.12	1.22	1.38	V
Output Coding (Default)			Twos complement		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO/DFS pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 4.

Parameter[1, 2]	Symbol	Temp	Min	Typ	Max	Unit
CLOCK[3]						
Input Clock Rate		Full	10		520	MHz
Conversion Rate		Full	10		65	MSPS
Clock Pulse Width High	t_{EH}	Full		7.69		ns
Clock Pulse Width Low	t_{EL}	Full		7.69		ns
OUTPUT PARAMETERS[3]						
Propagation Delay	t_{PD}	Full	1.5	2.3	3.1	ns
Rise Time (20% to 80%)	t_R	Full		300		ps
Fall Time (20% to 80%)	t_F	Full		300		ps
FCO±1, FCO±2 Propagation Delay	t_{FCO}	Full	1.5	2.3	3.1	ns
DCO±1, DCO±2 Propagation Delay[4]	t_{CPD}	Full		t_{FCO} + (t_{SAMPLE}/28)		ns
DCO±1, DCO±2 to Data Delay[4]	t_{DATA}	Full	(t_{SAMPLE}/28) − 300	(t_{SAMPLE}/28)	(t_{SAMPLE}/28) + 300	ps
DCO±1, DCO±2 to FCO±1, FCO±2 Delay[4]	t_{FRAME}	Full	(t_{SAMPLE}/28) − 300	(t_{SAMPLE}/28)	(t_{SAMPLE}/28) + 300	ps
Data to Data Skew	$t_{DATA-MAX} - t_{DATA-MIN}$	Full		±50	±200	ps
Wake-Up Time (Standby)		25°C		35		µs
Wake-Up Time (Power-Down)[5]		25°C		375		µs
Pipeline Latency		Full		16		Clock cycles
APERTURE						
Aperture Delay	t_A	25°C		1		ns
Aperture Uncertainty (Jitter)	t_J	25°C		135		fs rms
Out-of-Range Recovery Time		25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] Adjustable using the SPI.
[4] t_{SAMPLE}/28 is based on the number of bits, divided by 2, because the delays are based on half duty cycles. $t_{SAMPLE} = 1/f_{SAMPLE}$.
[5] Wake-up time is defined as the time required to return to normal operation from power-down mode.

Timing Diagrams

Refer to the Memory Map Register Descriptions section for SPI register setting of output mode.

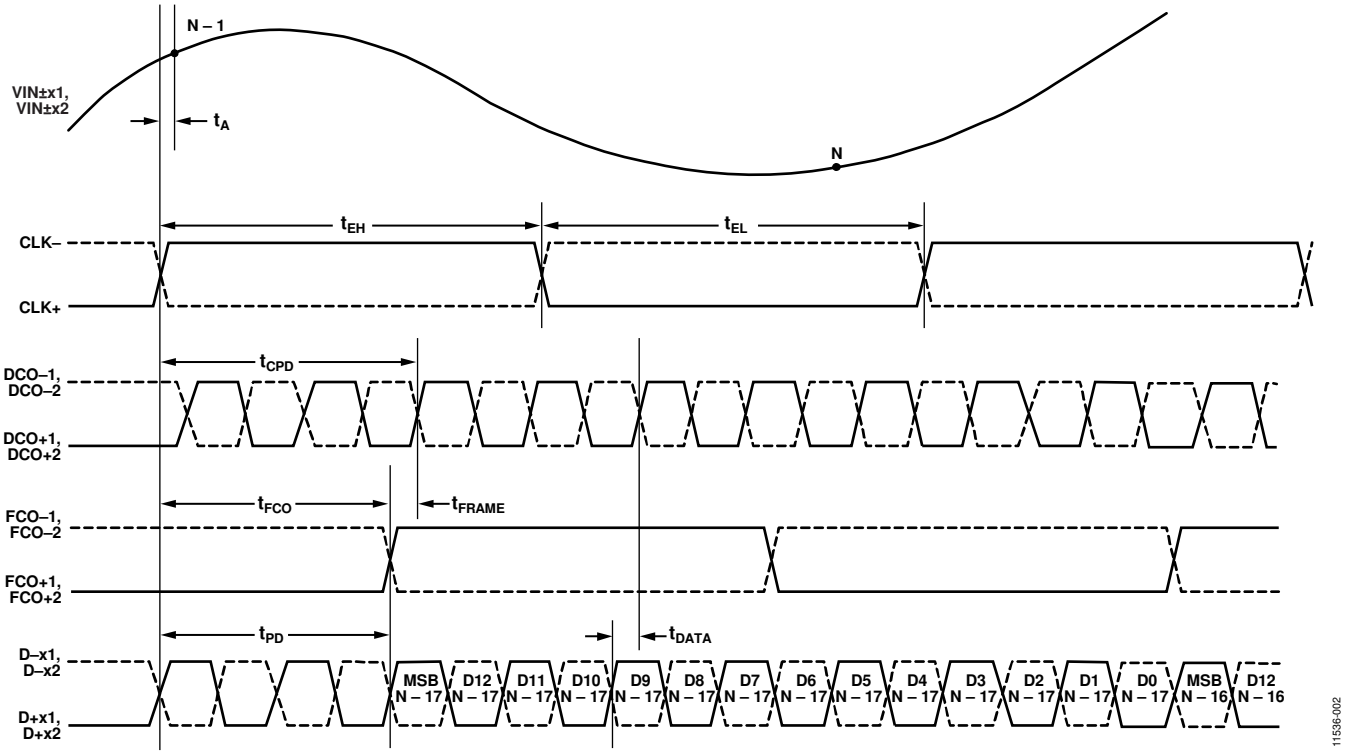

Figure 3. Wordwise DDR, 1× Frame, 14-Bit Output Mode (Default)

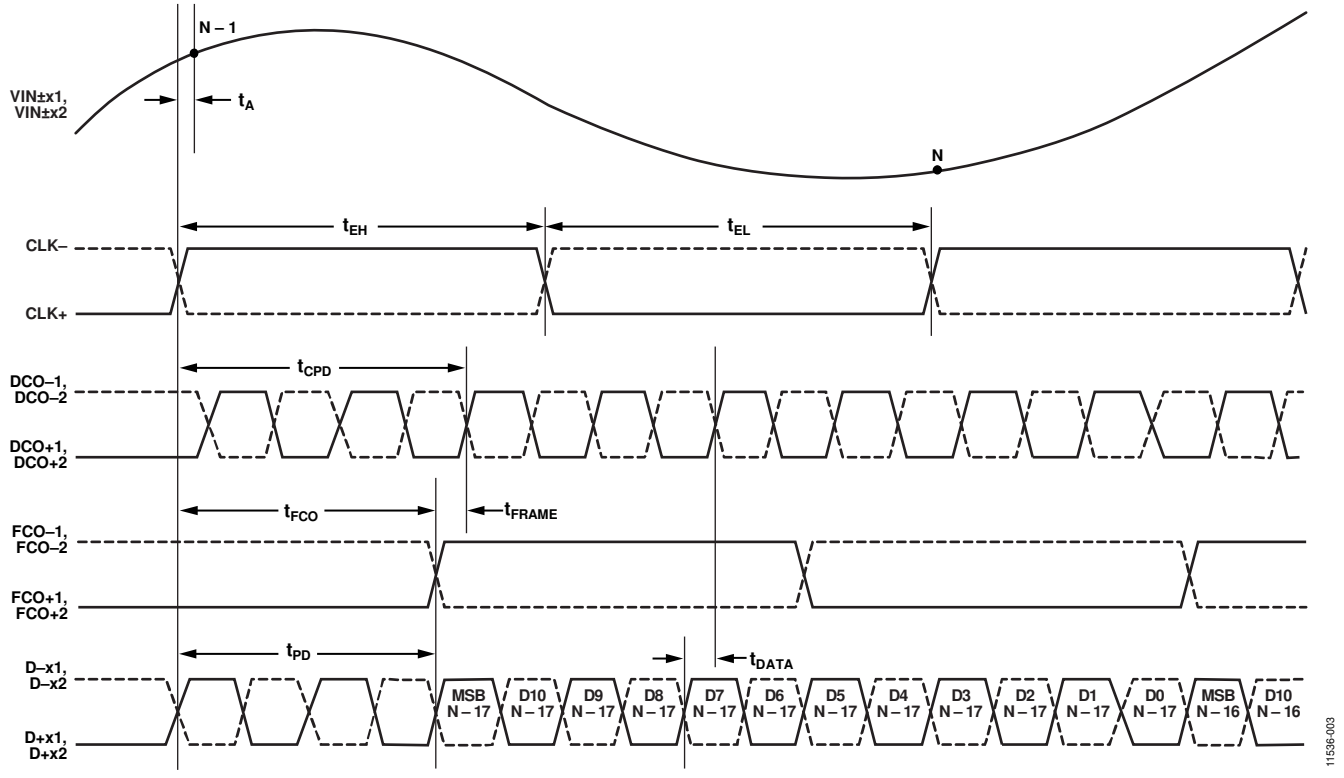

Figure 4. Wordwise DDR, 1× Frame, 12-Bit Output Mode

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Limit	Unit
SYNC TIMING REQUIREMENTS			
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.24	ns typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.40	ns typ
SPI TIMING REQUIREMENTS	See Figure 50		
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB1/CSB2 and SCLK	2	ns min
t_H	Hold time between CSB1/CSB2 and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 50)	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 50)	10	ns min

SYNC Timing Diagram

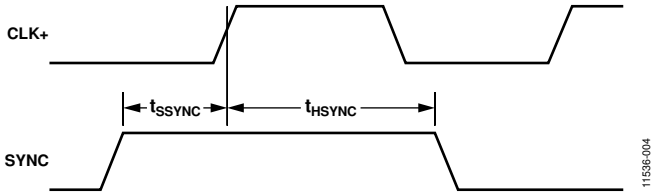

Figure 5. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to GND	−0.3 V to +2.0 V
DRVDD to GND	−0.3 V to +2.0 V
Digital Outputs (D±x1, D±x2, DCO±1, DCO±2, FCO±1, FCO±2) to GND	−0.3 V to +2.0 V
CLK+, CLK− to GND	−0.3 V to +2.0 V
VIN±x1, VIN±x2 to GND	−0.3 V to +2.0 V
SCLK/DTP, SDIO/DFS, CSB1, CSB2 to GND	−0.3 V to +2.0 V
SYNC, PDWN to GND	−0.3 V to +2.0 V
RBIAS1, RBIAS2 to GND	−0.3 V to +2.0 V
VREF, VCM1, VCM2, SENSE to GND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. Airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Table 7. Thermal Resistance (Simulated)

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	Ψ_{JT}[1, 2]	Unit
144-Ball, 10 mm × 10 mm CSP-BGA	0	30.2	0.13	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

AD9249
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VIN–G2	VIN+G2	VIN–G1	VIN–F2	VIN–F1	VIN–E2	VIN–E1	VIN–D2	VIN–D1	VIN–C2	VIN+C1	VIN–C1
B	VIN–H1	VIN+H1	VIN+G1	VIN+F2	VIN+F1	VIN+E2	VIN+E1	VIN+D2	VIN+D1	VIN+C2	VIN+B2	VIN–B2
C	VIN–H2	VIN+H2	SYNC	VCM1	VCM2	VREF	SENSE	RBIAS1	RBIAS2	GND	VIN+B1	VIN–B1
D	GND	GND	GND	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	GND	VIN+A2	VIN–A2
E	CLK–	CLK+	GND	AVDD	GND	GND	GND	GND	AVDD	CSB1	VIN+A1	VIN–A1
F	GND	GND	GND	AVDD	GND	GND	GND	GND	AVDD	CSB2	SDIO/DFS	SCLK/DTP
G	D–H2	D+H2	GND	AVDD	GND	GND	GND	GND	AVDD	PDWN	D+A1	D–A1
H	D–H1	D+H1	GND	AVDD	GND	GND	GND	GND	AVDD	GND	D+A2	D–A2
J	D–G2	D+G2	GND	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	GND	D+B1	D–B1
K	D–G1	D+G1	DRVDD	DRVDD	GND	GND	GND	GND	DRVDD	DRVDD	D+B2	D–B2
L	D–F2	D+F2	D+E2	D+E1	FCO+1	DCO+1	DCO+2	FCO+2	D+D2	D+D1	D+C1	D–C1
M	D–F1	D+F1	D–E2	D–E1	FCO–1	DCO–1	DCO–2	FCO–2	D–D2	D–D1	D+C2	D–C2

11536-005

Figure 6. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
C10, D1 to D3, D10, E3, E5 to E8, F1 to F3, F5 to F8, G3, G5 to G8, H3, H5 to H8, H10, J3, J10, K5 to K8	GND	Ground.
D4 to D9, E4, E9, F4, F9, G4, G9, H4, H9, J4 to J9	AVDD	1.8 V Analog Supply.
K3, K4, K9, K10	DRVDD	1.8 V Digital Output Driver Supply.
E1, E2	CLK–, CLK+	Input Clock Complement, Input Clock True.
G12, G11	D–A1, D+A1	Bank 1 Digital Output Complement, Bank 1 Digital Output True.
H12, H11	D–A2, D+A2	Bank 2 Digital Output Complement, Bank 2 Digital Output True.
J12, J11	D–B1, D+B1	Bank 1 Digital Output Complement, Bank 1 Digital Output True.
K12, K11	D–B2, D+B2	Bank 2 Digital Output Complement, Bank 2 Digital Output True
L12, L11	D–C1, D+C1	Bank 1 Digital Output Complement, Bank 1 Digital Output True.

Pin No.	Mnemonic	Description
M12, M11	D−C2, D+C2	Bank 2 Digital Output Complement, Bank 2 Digital Output True.
M10, L10	D−D1, D+D1	Bank 1 Digital Output Complement, Bank 1 Digital Output True.
M9, L9	D−D2, D+D2	Bank 2 Digital Output Complement, Bank 2 Digital Output True.
M4, L4	D−E1, D+E1	Bank 1 Digital Output Complement, Bank 1 Digital Output True.
M3, L3	D−E2, D+E2	Bank 2 Digital Output Complement, Bank 2 Digital Output True.
M1, M2	D−F1, D+F1	Bank 1 Digital Output Complement, Bank 1 Digital Output True.
L1, L2	D−F2, D+F2	Bank 2 Digital Output Complement, Bank 2 Digital Output True.
K1, K2	D−G1, D+G1	Bank 1 Digital Output Complement, Bank 1 Digital Output True.
J1, J2	D−G2, D+G2	Bank 2 Digital Output Complement, Bank 2 Digital Output True.
H1, H2	D−H1, D+H1	Bank 1 Digital Output Complement, Bank 1 Digital Output True.
G1, G2	D−H2, D+H2	Bank 2 Digital Output Complement, Bank 2 Digital Output True.
M6, L6, M7, L7	DCO−1, DCO+1, DCO−2, DCO+2	Data Clock Digital Output Complement, Data Clock Digital Output True. DCO±1 is used to capture D±x1 digital output data; DCO±2 is used to capture D±x2 digital output data.
M5, L5, M8, L8	FCO−1, FCO+1, FCO−2, FCO+2	Frame Clock Digital Output Complement, Frame Clock Digital Output True. FCO±1 frames D±x1 digital output data; FCO±2 frames D±x2 digital output data.
F12	SCLK/DTP	Serial Clock (SCLK)/Digital Test Pattern (DTP).
F11	SDIO/DFS	Serial Data Input/Output (SDIO)/Data Format Select (DFS).
E10, F10	CSB1, CSB2	Chip Select Bar. CSB1 enables/disables SPI for eight channels in Bank 1; CSB2 enables/disables SPI for eight channels in Bank 2.
G10	PDWN	Power-Down.
E12, E11	VIN−A1, VIN+A1	Analog Input Complement, Analog Input True.
D12, D11	VIN−A2, VIN+A2	Analog Input Complement, Analog Input True.
C12, C11	VIN−B1, VIN+B1	Analog Input Complement, Analog Input True.
B12, B11	VIN−B2, VIN+B2	Analog Input Complement, Analog Input True.
A12, A11	VIN−C1, VIN+C1	Analog Input Complement, Analog Input True.
A10, B10	VIN−C2, VIN+C2	Analog Input Complement, Analog Input True.
A9, B9	VIN−D1, VIN+D1	Analog Input Complement, Analog Input True.
A8, B8	VIN−D2, VIN+D2	Analog Input Complement, Analog Input True.
A7, B7	VIN−E1, VIN+E1	Analog Input Complement, Analog Input True.
A6, B6	VIN−E2, VIN+E2	Analog Input Complement, Analog Input True.
A5, B5	VIN−F1, VIN+F1	Analog Input Complement, Analog Input True.
A4, B4	VIN−F2, VIN+F2	Analog Input Complement, Analog Input True.
A3, B3	VIN−G1, VIN+G1	Analog Input Complement, Analog Input True.
A1, A2	VIN−G2, VIN+G2	Analog Input Complement, Analog Input True.
B1, B2	VIN−H1, VIN+H1	Analog Input Complement, Analog Input True.
C1, C2	VIN−H2, VIN+H2	Analog Input Complement, Analog Input True.
C8, C9	RBIAS1, RBIAS2	Sets analog current bias. Connect each RBIASx pin to a 10 kΩ (1% tolerance) resistor to ground.
C7	SENSE	Reference Mode Selection.
C6	VREF	Voltage Reference Input/Output.
C4, C5	VCM1, VCM2	Analog Output Voltage at Midsupply. Sets the common mode of the analog inputs, external to the ADC, as shown in Figure 35 and Figure 36.
C3	SYNC	Digital Input; Synchronizing Input to Clock Divider. This pin is internally pulled to ground by a 30 kΩ resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

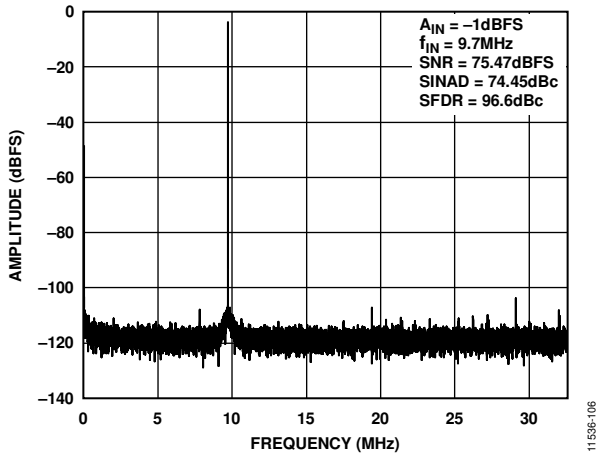

Figure 7. Single-Tone 32k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 65 MSPS

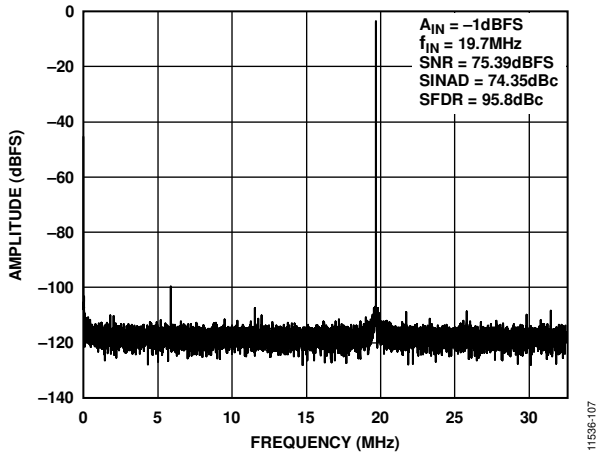

Figure 8. Single-Tone 32k FFT with f_{IN} = 19.7 MHz, f_{SAMPLE} = 65 MSPS

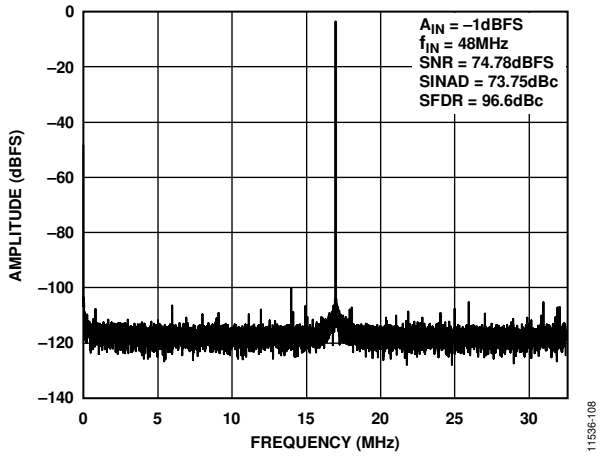

Figure 9. Single-Tone 32k FFT with f_{IN} = 48 MHz, f_{SAMPLE} = 65 MSPS

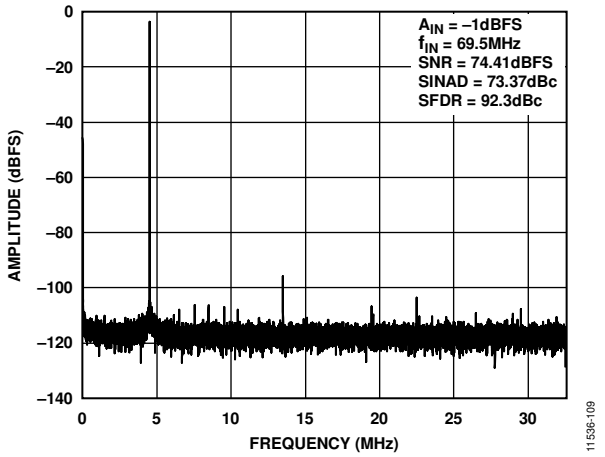

Figure 10. Single-Tone 32k FFT with f_{IN} = 69.5 MHz, f_{SAMPLE} = 65 MSPS

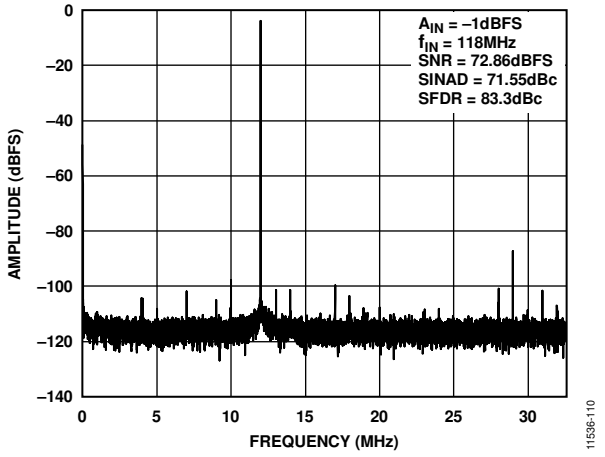

Figure 11. Single-Tone 32k FFT with f_{IN} = 118 MHz, f_{SAMPLE} = 65 MSPS

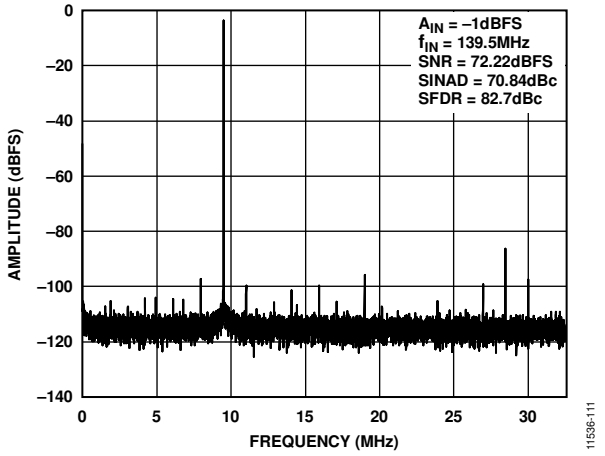

Figure 12. Single-Tone 32k FFT with f_{IN} = 139.5 MHz, f_{SAMPLE} = 65 MSPS

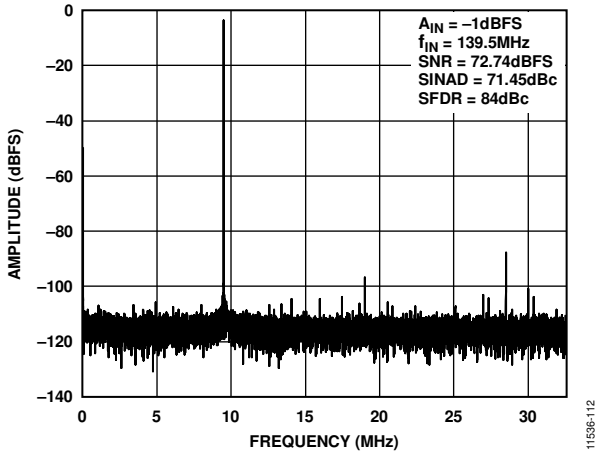

Figure 13. Single-Tone 32k FFT with f_{IN} = 139.5 MHz, f_{SAMPLE} = 65 MSPS, Clock Divider = 4

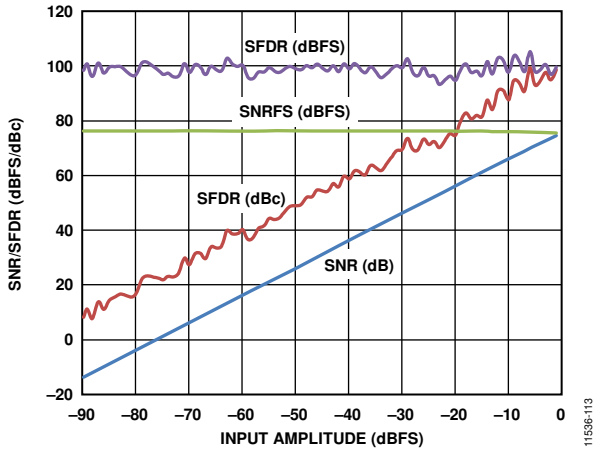

Figure 14. SNR/SFDR vs. Input Amplitude; f_{IN} = 9.7 MHz, f_{SAMPLE} = 65 MSPS

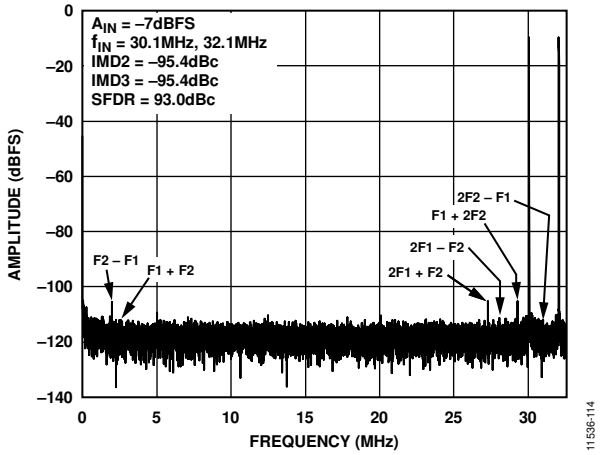

Figure 15. Two Tone FFT, f_{IN} = 30.1 MHz and 32.1 MHz, f_{SAMPLE} = 65 MSPS

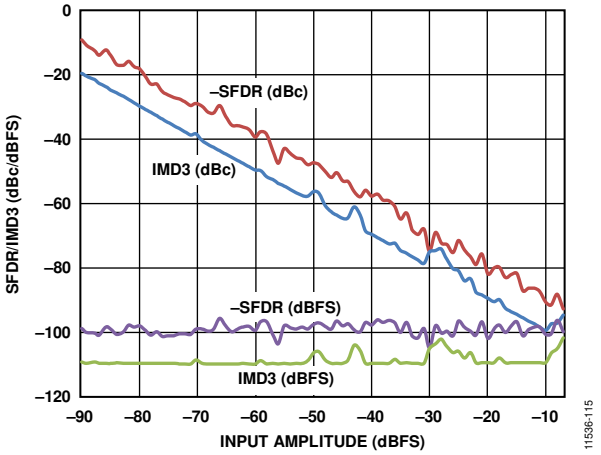

Figure 16. Two-Tone SFDR/IMD3 vs. Input Amplitude; f_{IN1} = 30.1 MHz, f_{IN2} = 32.1 MHz, f_{SAMPLE} = 65 MSPS

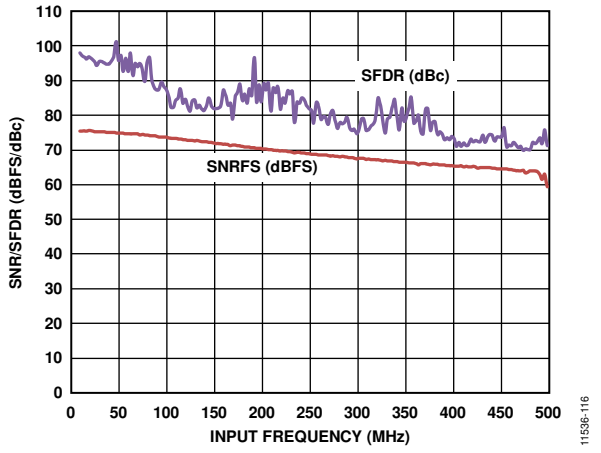

Figure 17. SNR/SFDR vs. f_{IN}; f_{SAMPLE} = 65 MSPS

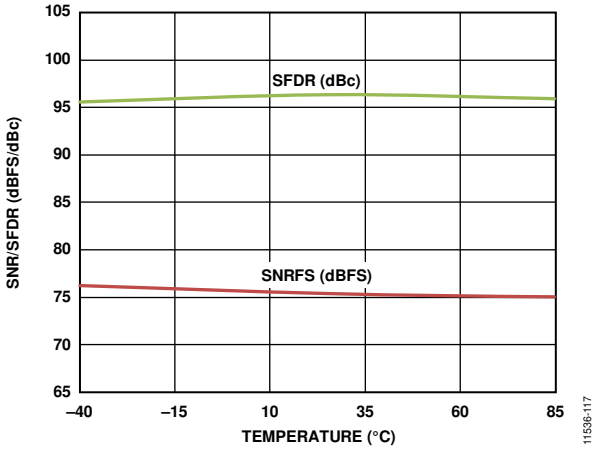

Figure 18. SNR/SFDR vs. Temperature; f_{IN} = 9.7 MHz, f_{SAMPLE} = 65 MSPS

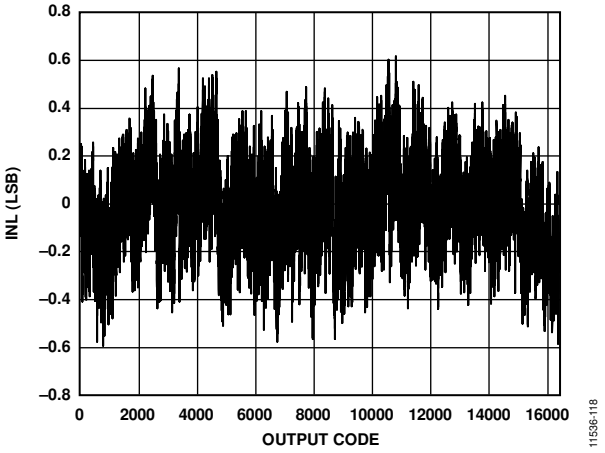

Figure 19. INL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 65 MSPS

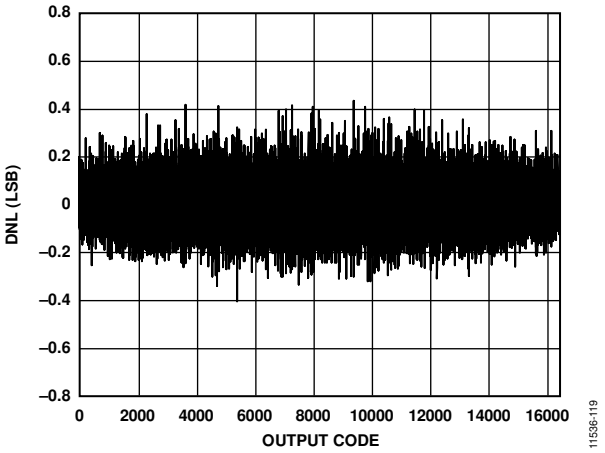

Figure 20. DNL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 65 MSPS

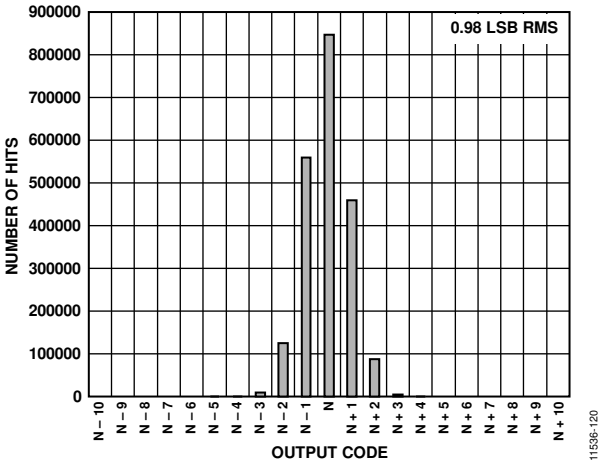

Figure 21. Input Referred Noise Histogram; f_{SAMPLE} = 65 MSPS

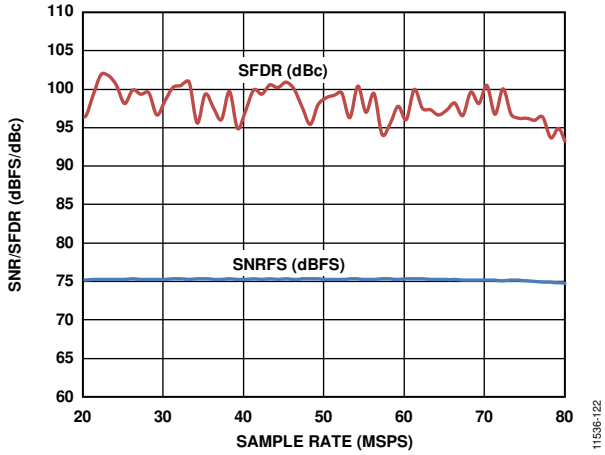

Figure 22. SNR/SFDR vs. Sample Rate; f_{IN} = 9.7 MHz, f_{SAMPLE} = 65 MSPS

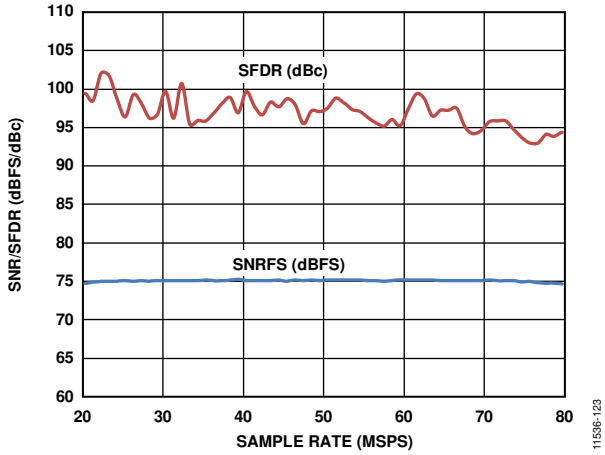

Figure 23. SNR/SFDR vs. Sample Rate; f_{IN} =19.7 MHz, f_{SAMPLE} = 65 MSPS

EQUIVALENT CIRCUITS

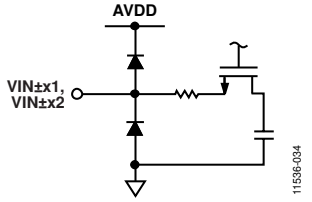

Figure 24. Equivalent Analog Input Circuit

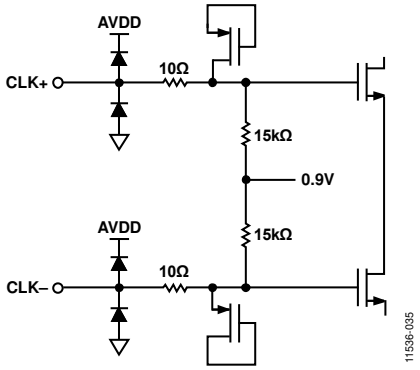

Figure 25. Equivalent Clock Input Circuit

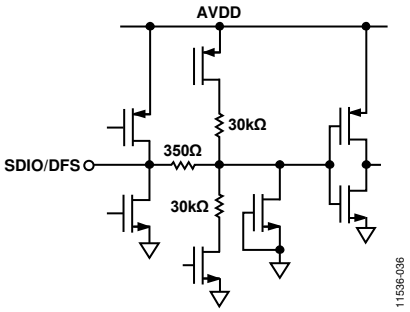

Figure 26. Equivalent SDIO/DFS Input Circuit

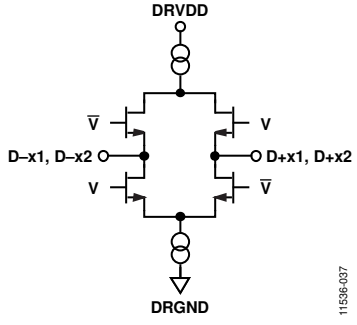

Figure 27. Equivalent Digital Output Circuit

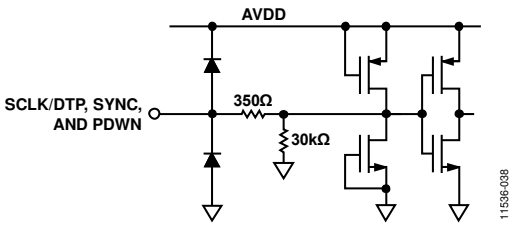

Figure 28. Equivalent SCLK/DTP, SYNC, and PDWN Input Circuit

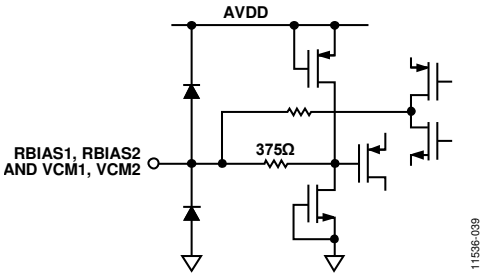

Figure 29. Equivalent RBIASx and VCMx Circuit

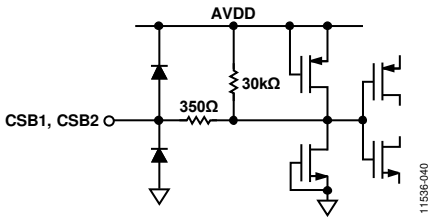

Figure 30. Equivalent CSBx Input Circuit

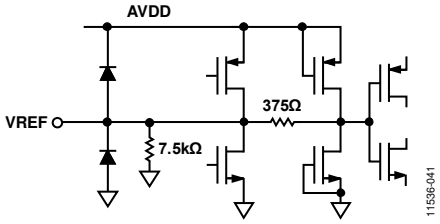

Figure 31. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9249 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The serializer transmits this converted data in a 14-bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9249 is a differential switched capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal dependent errors and achieve optimum performance.

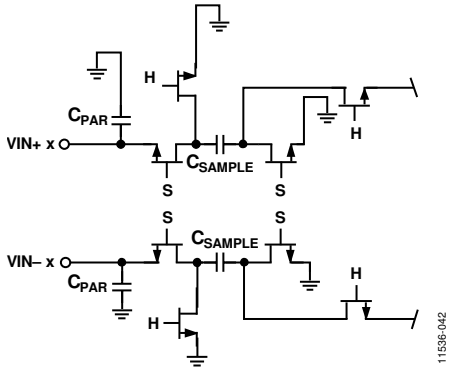

Figure 32. Switched Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 32). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Place either a differential capacitor or two single-ended capacitors on the inputs to provide a matching passive network. This configuration ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values vary, depending on the application.

Input Common Mode

The analog inputs of the AD9249 are not internally dc biased. Therefore, in ac-coupled applications, the user must provide this bias externally. For optimum performance, set the device so that V_{CM} = AVDD/2. However, the device can function over a wider range with reasonable performance, as shown in Figure 33.

An on-chip, common-mode voltage reference is included in the design and is available at the VCMx pin. Decouple the VCMx pin to ground using a 0.1 µF capacitor, as described in the Applications Information section.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9249, the largest available input span is 2 V p-p.

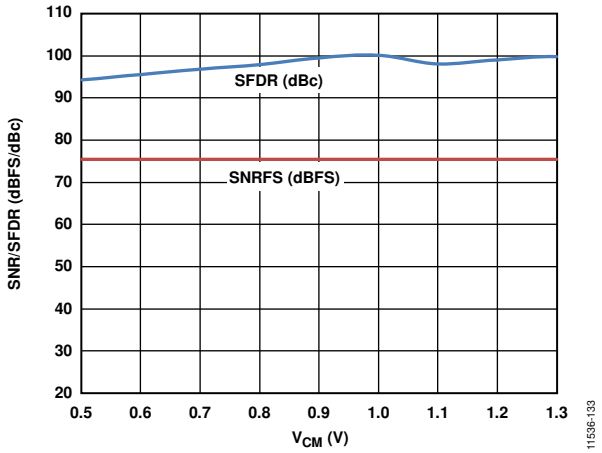

Figure 33. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 9.7 MHz, f_{SAMPLE} = 65 MSPS

Differential Input Configurations

There are several ways to drive the AD9249, either actively or passively. However, optimum performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the AD9249 provides excellent performance and a flexible interface to the ADC (see Figure 35) for baseband applications. Similarly, differential transformer coupling also provides excellent performance (see Figure 36).

Because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9249, use of these passive configurations is recommended wherever possible.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is recommended that the AD9249 inputs not be driven single-ended.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9249. Configure VREF using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the Internal Reference Connection section and the External Reference Operation section. Bypass the VREF pin to ground externally, using a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

Internal Reference Connection

A comparator within the AD9249 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 34), setting VREF to 1.0 V.

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting V_{REF} (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	GND to 0.2	1.0 internal	2.0
Fixed External Reference	AVDD	1.0 applied to external VREF pin	2.0

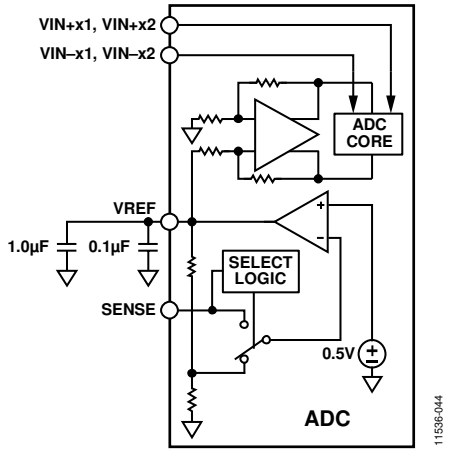

Figure 34. Internal Reference Configuration

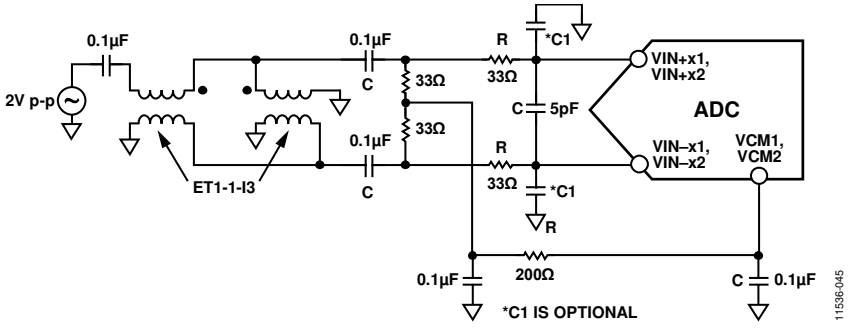

Figure 35. Differential Double Balun Input Configuration for Baseband Applications

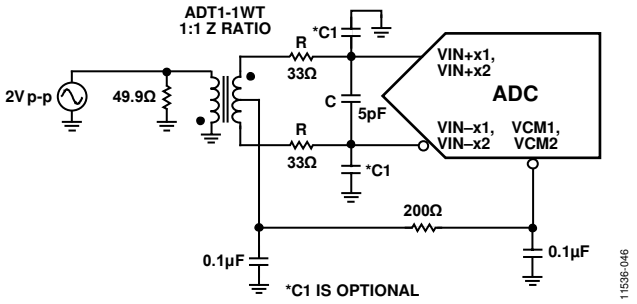

Figure 36. Differential Transformer Coupled Configuration for Baseband Applications

If the internal reference of the AD9249 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 37 shows how the internal reference voltage is affected by loading.

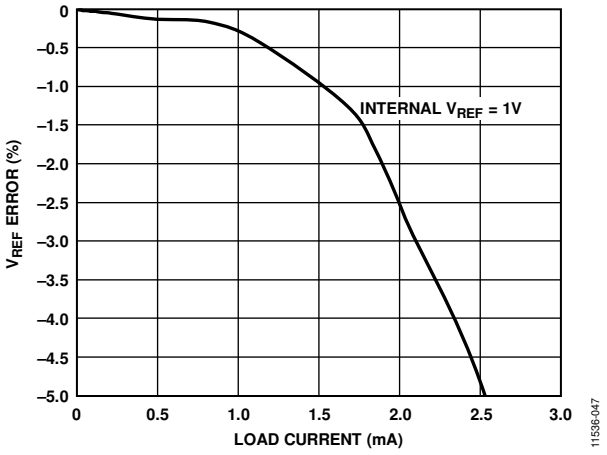

Figure 37. V_{REF} Error vs. Load Current

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 38 shows the typical drift characteristics of the internal reference in 1.0 V mode.

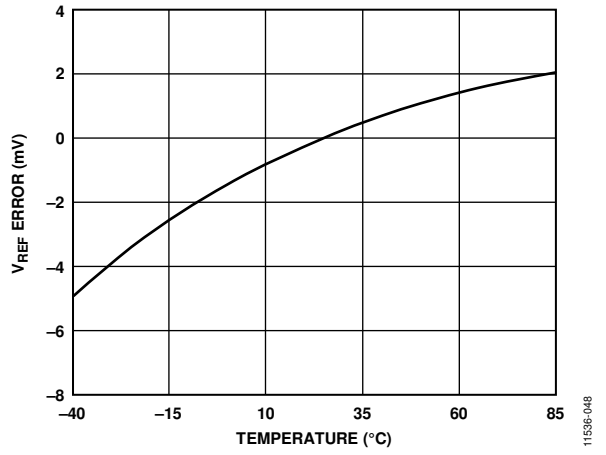

Figure 38. Typical V_{REF} Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load (see Figure 31). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, limit the external reference to a maximum of 1.0 V.

Do not leave the SENSE pin floating.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9249 sample clock inputs, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally (see Figure 25) and require no external bias.

Clock Input Options

The AD9249 has a flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the utmost concern, as described in the Jitter Considerations section.

Figure 39 and Figure 40 show two preferred methods for clocking the AD9249 (at clock rates of up to 520 MHz prior to the internal clock divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

The RF balun configuration is recommended for clock frequencies from 65 MHz to 520 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The antiparallel Schottky diodes across the transformer/balun secondary winding limit clock excursions into the AD9249 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9249 while preserving the fast rise and fall times of the signal that are critical to achieving a low jitter performance. However, the diode capacitance comes into play at frequencies above 500 MHz. Take care when choosing the appropriate signal limiting diode.

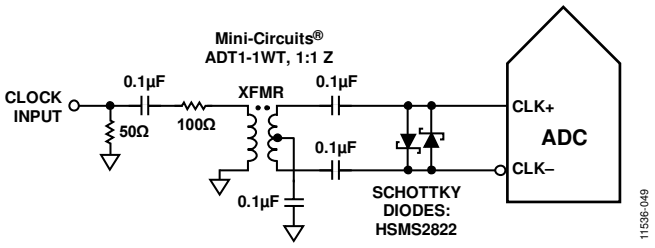

Figure 39. Transformer-Coupled Differential Clock (Up to 200 MHz)

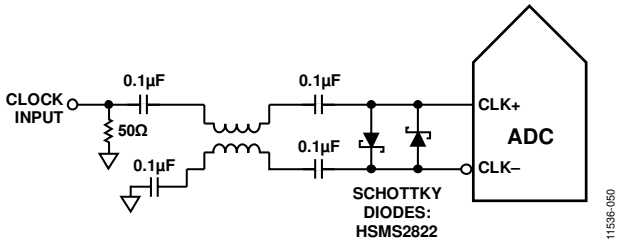

Figure 40. Balun-Coupled Differential Clock (65 MHz to 520 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 41. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515-x/AD9516-x/AD9517-x clock drivers offer excellent jitter performance.

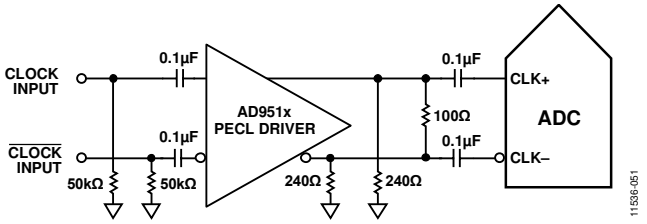

Figure 41. Differential PECL Sample Clock (Up to 520 MHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 42. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515-x/AD9516-x/AD9517-x clock drivers offer excellent jitter performance.

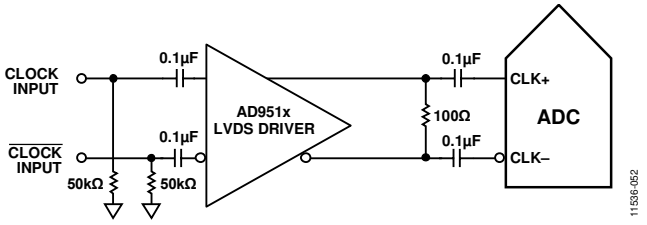

Figure 42. Differential LVDS Sample Clock (Up to 520 MHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK– pin to ground with a 0.1 µF capacitor (see Figure 43).

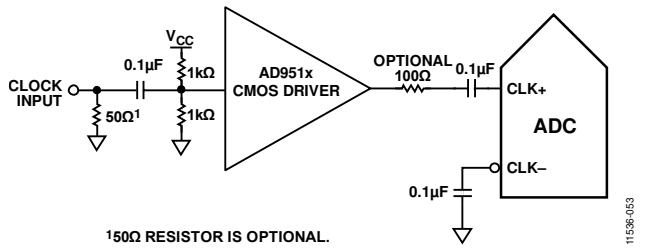

Figure 43. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9249 contains an input clock divider with the ability to divide the input clock by integer values from 1 to 8.

The AD9249 clock divider can be synchronized using the external SYNC input. Bit 0 and Bit 1 of Register 0x109 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows the clock dividers of multiple devices to be aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9249 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9249. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS turned on.

Jitter on the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) that is due only to aperture jitter (t_J) is expressed by

$$SNR\ Degradation = 20 \log_{10}\left(\frac{1}{2\pi \times f_A \times t_J}\right)$$

In this equation, the rms aperture jitter represents the root-sum-square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 44).

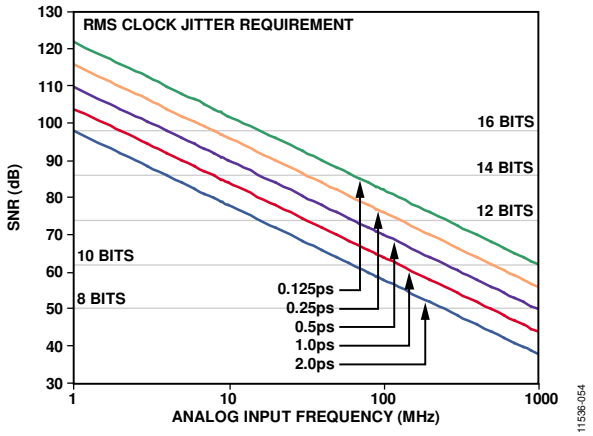

Figure 44. Ideal SNR vs. Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9249. Separate the clock driver power supplies from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators are excellent clock sources. If another type of source generates the clock (by gating, dividing, or another method), ensure that it is retimed by the original clock at the last step.

See the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, for more in depth information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 45, the power dissipated by the AD9249 is proportional to its sample rate and can be set to one of several power saving modes using Register 0x100, Bits[2:0].

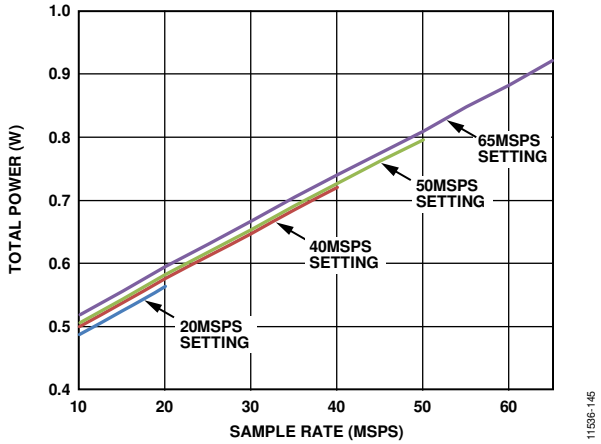

Figure 45. Total Power vs. f_{SAMPLE} for f_{IN} = 9.7 MHz

The AD9249 is placed in power-down mode either by the SPI port or by asserting the PDWN pin high. In this state, the ADC typically dissipates 2 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9249 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. The internal capacitors are discharged when the device enters power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times. When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more details on using these features.

DIGITAL OUTPUTS AND TIMING

The AD9249 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This can be changed to a low power, reduced signal option (similar to the IEEE 1596.3 standard) via the SPI. The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing (or 700 mV p-p differential) at the receiver.

When operating in reduced range mode, the output current reduces to 2 mA. This results in a 200 mV swing (or 400 mV p-p differential) across a 100 Ω termination at the receiver.

The AD9249 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as near to the receiver as possible. If there is no far end receiver termination or there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than 24 inches, with all traces the same length. Place the differential output traces as near to each other as possible. An example of the FCO and data stream with proper trace length and position is shown in Figure 46. Figure 47 shows an LVDS output timing example in reduced range mode.

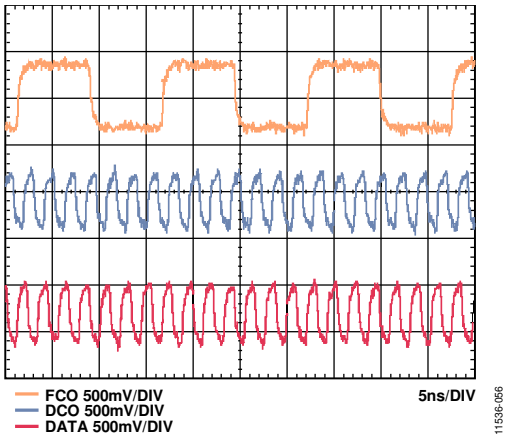

Figure 46. LVDS Output Timing Example in ANSI-644 Mode (Default)

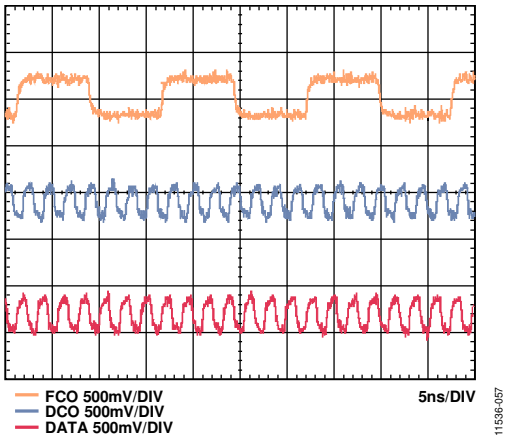

Figure 47. LVDS Output Timing Example in Reduced Range Mode

Figure 48 shows an example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths of less than 24 inches on standard FR-4 material.

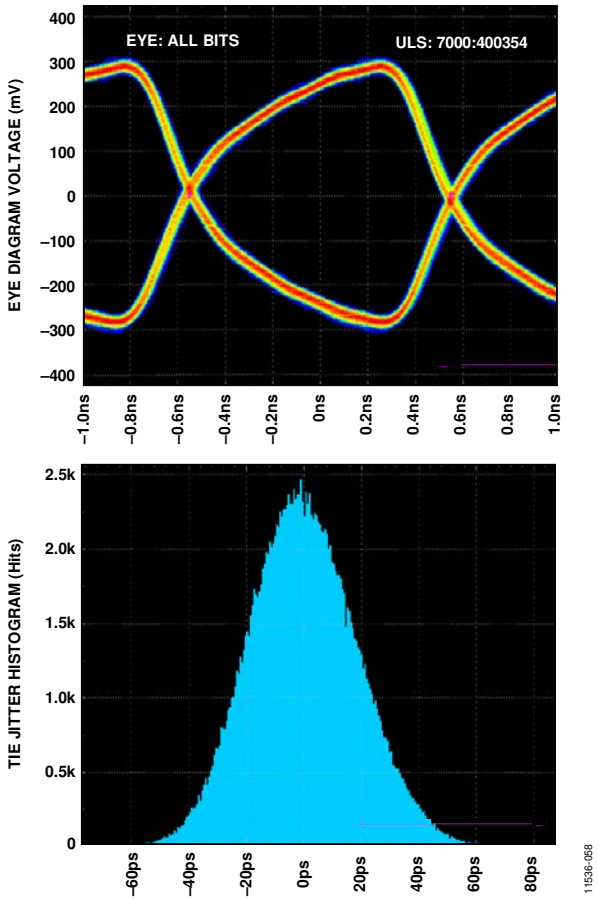

Figure 48. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less Than 24 Inches on Standard FR-4 Material, External 100 Ω Far End Termination Only

Figure 49 shows an example of trace lengths exceeding 24 inches on standard FR-4 material. Note that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position.

It is the responsibility of the user to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches. Additional SPI options allow the user to further increase the internal termination (increasing the current) of all 16 outputs to drive longer trace lengths, which can be achieved by programming Register 0x15. Although this option produces sharper rise and fall times on the data edges and is less prone to bit errors, it also increases the power dissipation of the DRVDD supply.

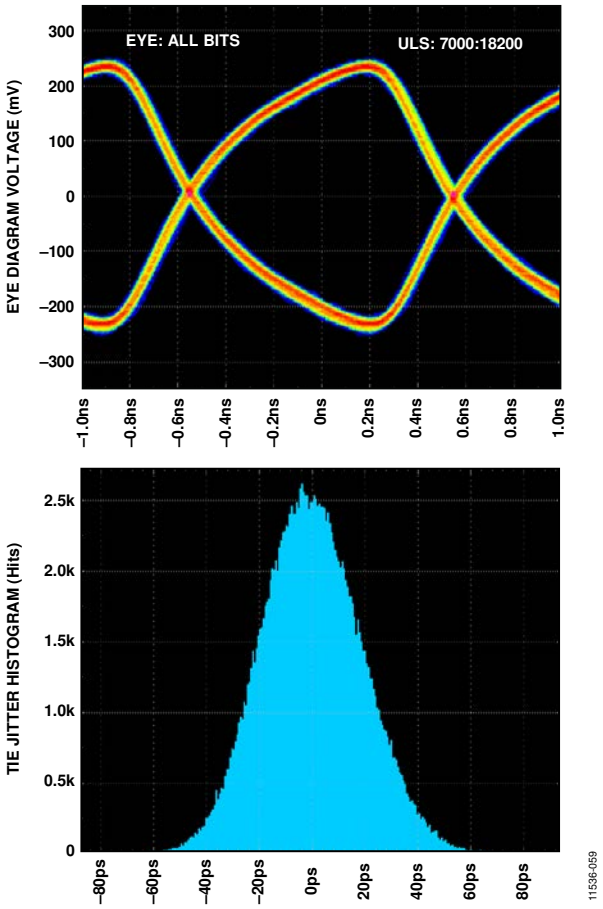

Figure 49. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Greater Than 24 Inches on Standard FR-4 Material, External 100 Ω Far End Termination Only

The default format of the output data is twos complement. Table 10 shows an example of the output coding format. To change the output data format to offset binary, see the Memory Map section.

Data from each ADC is serialized and provided on a separate channel in DDR mode. The data rate for each serial stream is equal to 14 bits times the sample clock rate, quantity divided by 2, with a maximum of 455 Mbps (14 bits × 65 MSPS)/2 = 455 Mbps. The lowest typical conversion rate is 10 MSPS. See the Memory Map section for details on enabling this feature.

Table 10. Digital Output Coding

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode
VIN+ – VIN–	< –VREF – 0.5 LSB	00 0000 0000 0000	10 0000 0000 0000
VIN+ – VIN–	= –VREF	00 0000 0000 0000	10 0000 0000 0000
VIN+ – VIN–	= 0	10 0000 0000 0000	00 0000 0000 0000
VIN+ – VIN–	= +VREF – 1.0 LSB	11 1111 1111 1111	01 1111 1111 1111
VIN+ – VIN–	> +VREF – 0.5 LSB	11 1111 1111 1111	01 1111 1111 1111

Two output clock types are provided to assist in capturing data from the AD9249. DCO±1 and DCO±2 clock the output data, and their frequency is equal to 7× the sample clock (CLK±) rate for the default mode of operation. Data is clocked out of the AD9249 and must be captured on the rising and falling edges of the DCO that supports double data rate (DDR) capturing. DCO±1 is used to capture the D±x1 (Bank 1) data; DCO±2 is used to capture the D±x2 (Bank 2) data. FCO±1 and FCO±2 signal the start of a new output byte, and the frequency is equal to the sample clock rate. FCO±1 frames the D±x1 (Bank 1) data; FCO±2 frames the D±x2 (Bank 2) data (see Figure 3 and Figure 4).

When the SPI is used, the DCO phase can be adjusted in 60° increments relative to one data cycle (30° relative to one DCO cycle). This enables the user to refine system timing margins, if required. The default DCO±1 and DCO±2 to output data edge timing, as shown in Figure 3, is 180° relative to one data cycle (90° relative to one DCO cycle).

A 12-bit serial stream can also be initiated from the SPI. This allows the user to implement and test compatibility to lower resolution systems. When changing the resolution to a 12-bit serial stream, the data stream is shortened. See Figure 4 for the 12-bit example.

In default mode, as shown in Figure 3, the MSB is first in the data output serial stream. This can be inverted so that the LSB is first in the data output serial stream by using the SPI.

There are 12 digital output test pattern options available that can be initiated through the SPI. This is a useful feature when validating receiver capture and timing (see Table 11 for the output bit sequencing options that are available). Some test patterns have two serial sequential words and can alternate in various ways, depending on the test pattern chosen. Note that some patterns do not adhere to the data format select option. In addition, custom user-defined test patterns can be assigned in Register 0x19, Register 0x1A, Register 0x1B, and Register 0x1C.

Table 11. Flexible Output Test Modes

Output Test Mode Bit Sequence (Reg. 0x0D)	Pattern Name	Digital Output Word 1[1]	Digital Output Word 2[1]	Subject to Data Format Select[1]	Notes
0000	Off (default)	N/A	N/A	N/A	
0001	Midscale short	1000 0000 0000 (12-bit) 10 0000 0000 0000 (14-bit)	N/A	Yes	Offset binary code shown
0010	+Full-scale short	1111 1111 1111 (12-bit) 11 1111 1111 1111 (14-bit)	N/A	Yes	Offset binary code shown
0011	−Full-scale short	0000 0000 0000 (12-bit) 00 0000 0000 0000 (14-bit)	N/A	Yes	Offset binary code shown
0100	Checkerboard	1010 1010 1010 (12-bit) 10 1010 1010 1010 (14-bit)	0101 0101 0101 (12-bit) 01 0101 0101 0101 (14-bit)	No	
0101	PN sequence long[2]	N/A	N/A	Yes	PN23 ITU 0.150 $X^{23} + X^{18} + 1$
0110	PN sequence short[2]	N/A	N/A	Yes	PN9 ITU 0.150 $X^{9} + X^{5} + 1$
0111	One-/zero-word toggle	1111 1111 1111 (12-bit) 11 1111 1111 1111 (14-bit)	0000 0000 0000 (12-bit) 00 0000 0000 0000 (14-bit)	No	
1000	User input	Register 0x19 to Register 0x1A	Register 0x1B to Register 0x1C	No	
1001	1-/0-bit toggle	1010 1010 1010 (12-bit) 10 1010 1010 1010 (14-bit)	N/A	No	
1010	1× sync	0000 0011 1111 (12-bit) 00 0000 0111 1111 (14-bit)	N/A	No	
1011	One bit high	1000 0000 0000 (12-bit) 10 0000 0000 0000 (14-bit)	N/A	No	Pattern associated with the external pin
1100	Mixed frequency	1010 0011 0011 (12-bit) 10 1000 0110 0111 (14-bit)	N/A	No	

[1] N/A means not applicable.
[2] All test mode options except PN sequence short and PN sequence long can support 12-bit to 14-bit word lengths to verify data capture to the receiver.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ or 511 bits. Refer to Section 5.1 of the ITU-T 0.150 (05/96) standard for a description of the PN sequence and how it is generated. The seed value is all 1s (see Table 12 for the initial values). The output is a parallel representation of the serial PN9 sequence in MSB-first format. The first output word is the first 14 bits of the PN9 sequence in MSB aligned form.

Table 12. PN Sequence

Sequence	Initial Value	Next Three Output Samples (MSB First) Twos Complement
PN Sequence Short	0x1FE0	0x1DF1, 0x3CC8, 0x294E
PN Sequence Long	0x1FFF	0x1FE0, 0x2001, 0x1C00

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ or 8,388,607 bits. Refer to Section 5.6 of the ITU-T 0.150 (05/96) standard for a description of the PN sequence and how it is generated. The seed value is all 1s (see Table 12 for the initial values) and the AD9249 inverts the bit stream with relation to the ITU standard. The output is a parallel representation of the serial PN23 sequence in MSB-first format. The first output word is the first 14 bits of the PN23 sequence in MSB aligned format.

Consult the Memory Map section for information on how to change these additional digital output timing features through the SPI.

SDIO/DFS Pin

For applications that do not require SPI mode operation, the CSB1 and CSB2 pins are tied to AVDD, and the SDIO/DFS pin controls the output data format select as described in Table 13.

Table 13. Output Data Format Select Pin Settings

DFS Pin Voltage	Output Mode
AVDD	Twos complement
GND (Default)	Offset binary

SCLK/DTP Pin

The SCLK/DTP pin can enable a single digital test pattern if it and the CSB1 and CSB2 pins are held high during device power-up. When SCLK/DTP is tied to AVDD, the ADC channel outputs shift out the following pattern: 10 0000 0000 0000. The FCO±1, FCO±2, DCO±1, and DCO±2 pins function normally while all channels shift out the repeatable test pattern. This pattern allows the user to perform timing alignment adjustments among the FCO±1, FCO±2, DCO±1, DCO±2, and output data. The SCLK/DTP pin has an internal 30 kΩ resistor to GND. It can be left unconnected for normal operation.

Table 14. Digital Test Pattern Pin Settings

Selected DTP	DTP Voltage	Resulting D±xx
Normal Operation	No connect	Normal operation
DTP	AVDD	10 0000 0000 0000

Additional and custom test patterns can also be observed when commanded from the SPI port. Consult the Memory Map section for information about the options that are available.

CSB1 and CSB2 Pins

The CSB1 and CSB2 pins are tied to AVDD for applications that do not require SPI mode operation. Tying CSB1 and CSB2 high causes all SCLK and SDIO SPI communication information to be ignored.

CSB1 selects/deselects SPI circuitry affecting outputs D±A1 to D±H1 (Bank 1). CSB2 selects/deselects SPI circuitry affecting outputs D±A2 to D±H2 (Bank 2).

It is recommended that CSB1 and CSB2 be controlled with the same signal; that is, tie them together. In this way, whether tying them to AVDD or selecting SPI functionality, both banks of ADCs are controlled identically and are always in the same state.

RBIAS1 and RBIAS2 Pins

To set the internal core bias current of the ADC, place a 10.0 kΩ, 1% tolerance resistor to ground at each of the RBIAS1 and RBIAS2 pins.