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ANALOG DEVICES

Evaluation Board User Guide
UG-003

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the AD9650/AD9268/AD9258/AD9251/AD9231/AD9204/AD9269/AD6659 Analog-to-Digital Converters

FEATURES

Full featured evaluation board for the AD9650/AD9268/AD9258/AD9251/AD9231/AD9204/AD9269/AD6659
SPI interface for setup and control
External, on-board oscillator, or AD9517 clocking options
Balun/transformer or amplifier input drive options
LDO regulator or switching power supply options
VisualAnalog® and SPI controller software interfaces

EQUIPMENT NEEDED

Analog signal source and antialiasing filter
Sample clock source (if not using the on-board oscillator)
2 switching power supplies (6.0 V, 2.5 A), CUI EPS060250UH-PHP-SZ, provided
PC running Windows® 98 (2nd ed.), Windows 2000, Windows ME, or Windows XP
USB 2.0 port, recommended (USB 1.1 compatible)
AD9650, AD9268, AD9258, AD9251, AD9231, AD9204, AD9269, or AD6659 board
HSC-ADC-EVALCZ FPGA-based data capture kit

SOFTWARE NEEDED

VisualAnalog
SPI controller

DOCUMENTS NEEDED

AD9650, AD9268, AD9258, AD9251, AD9231, AD9204, AD9269, or AD6659 data sheet
HSC-ADC-EVALCZ data sheet
AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*
AN-878 Application Note, *High Speed ADC SPI Control Software*
AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*
AN-835 Application Note, *Understanding ADC Testing and Evaluation*

GENERAL DESCRIPTION

This document describes the AD9650, AD9268, AD9258, AD9251, AD9231, AD9204, AD9269, and AD6659 evaluation board, which provides all of the support circuitry required to operate these parts in their various modes and configurations. The application software used to interface with the devices is also described.

The AD9650, AD9268, AD9258, AD9251, AD9231, AD9204, AD9269, and AD6659 data sheets provide additional information and should be consulted when using the evaluation board. All documents and software tools are available at www.analog.com/fifo. For additional information or questions, send an email to highspeed.converters@analog.com.

TYPICAL MEASUREMENT SETUP

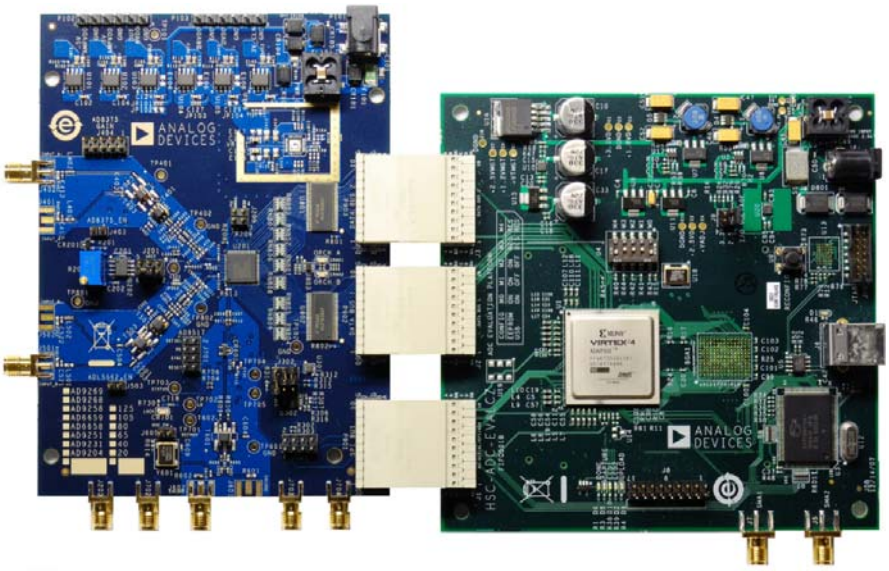

Figure 1. AD9268 and AD9269 Family Evaluation Board and HSC-ADC-EVALCZ Data Capture Board

TABLE OF CONTENTS

REVISION HISTORY

9/10—Rev. 0 to Rev. A

Changes to Title, Features Section, Documents Needed Section, and General Description Section 1
Changes to Evaluation Board Hardware Section 3
Added Table 1; Renumbered Sequentially 3
Added Figure 3; Renumbered Sequentially 5
Changes to Default Operation and Jumper Selection Settings Section 5
Added AD9650 Family Section, AD9268 Family Section, and AD9269 Family Section 5
Changes to VREF Section, Clock Circuitry for the AD9269 Family Section, and Clock Circuitry for the AD9650 and the AD9268 Family Section 6
Added Table 2 6
Changes to Evaluation Board Software Quick Start Procedures Section and Configuring the Board Section 8
Added Table 3; Renumbered Sequentially 27

11/09—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The evaluation board provides all of the support circuitry required to operate these parts in their various modes and configurations. Figure 2 shows the typical bench characterization setup used to evaluate the ac performance. It is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the signal chain. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is necessary to achieve the specified noise performance.

The evaluation board covers multiple families of ADCs and is populated slightly differently between the families. Table 1 shows the three main families and the ADCs that fall within each family. When a reference is made to the AD9269, for example, this applies to all the ADCs within that family, that is, the AD9251, the AD9231, and the AD9204, the AD9269, and the AD6659.

Table 1.

Family Name	ADCs within Each Family
AD9650	AD9650
AD9268	AD9268, AD9258
AD9269	AD9251, AD9231, AD9204, AD9269, AD6659

See the Evaluation Board Software Quick Start Procedures section to get started, and see Figure 17 to Figure 31 for the complete schematics and layout diagrams. These diagrams demonstrate the routing and grounding techniques that should be applied at the system level when designing application boards using these converters.

POWER SUPPLIES

This evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to the rated 100 V ac to the 240 V ac wall outlet at 47 Hz to 63 Hz. The output from the supply is provided through a 2.1 mm inner diameter jack that connects to the printed circuit board (PCB) at P101. The 6 V supply is fused and conditioned on the PCB before connecting to the low dropout linear regulators (default configuration) that supply the proper bias to each of the various sections on the board.

The evaluation board can be powered in a nondefault condition using external bench power supplies. To do this, the E101, E102, E114, E103, E105, and E107 ferrite beads can be removed to disconnect the outputs from the on-board LDOs. This enables the user to bias each section of the board individually. Use P102 and P103 to connect a different supply for each section. A 1.8 V supply is needed with a 1 A current capability for DUT_AVDD and DRVDD; however, it is recommended that separate supplies be used for both analog and digital domains. An additional supply is also required to supply 1.8 V for digital support circuitry on the board, DVDD. This should also have a 1 A current capability and can be combined with DRVDD with little or no degradation in performance. To operate the evaluation board using the SPI and alternate clock options, a separate 3.3 V analog supply is needed in addition to the other supplies. This 3.3 V supply, or 3V_CLK, should have a 1 A current capability.

Two additional supplies, 5V_AMPVDD and 3V_AMPVDD, are used to bias the optional input path amplifiers and optional VREF buffer. If used, these supplies should each have 1 A current capability.

A second optional power supply configuration allows replacing the LDOs that supply the AVDD and DRVDD rails of the ADC with the ADP2114 step-down dc-to-dc regulator. Using this switching controller in place of the LDO regulators to power the AVDD and DRVDD supplies of the ADC allows customers to evaluate the performance of the ADC when powered by a more efficient regulator.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise, such as the Rohde & Schwarz SMA, or HP 8644B signal generators or an equivalent. Use a 1 m shielded, RG-58, 50 Ω coaxial cable for connecting to the evaluation board. Enter the desired frequency and amplitude (see the Specifications section in the data sheet of the respective part). When connecting the analog input source, use of a multipole, narrow-band band-pass filter with 50 Ω terminations is recommended. Analog Devices, Inc., uses TTE and K&L Microwave, Inc., band-pass filters. The filters should be connected directly to the evaluation board.

If an external clock source is used, it should also be supplied with a clean signal generator as previously specified. Typically, most Analog Devices evaluation boards can accept ~2.8 V p-p or 13 dBm sine wave input for the clock.

OUTPUT SIGNALS

The default setup uses the Analog Devices high speed converter evaluation platform (HSC-ADC-EVALCZ) for data capture. The CMOS output signals from Channel A and Channel B are buffered through U801 and U802 and are routed through P903 and P902, respectively, to the FPGA on the data capture board.

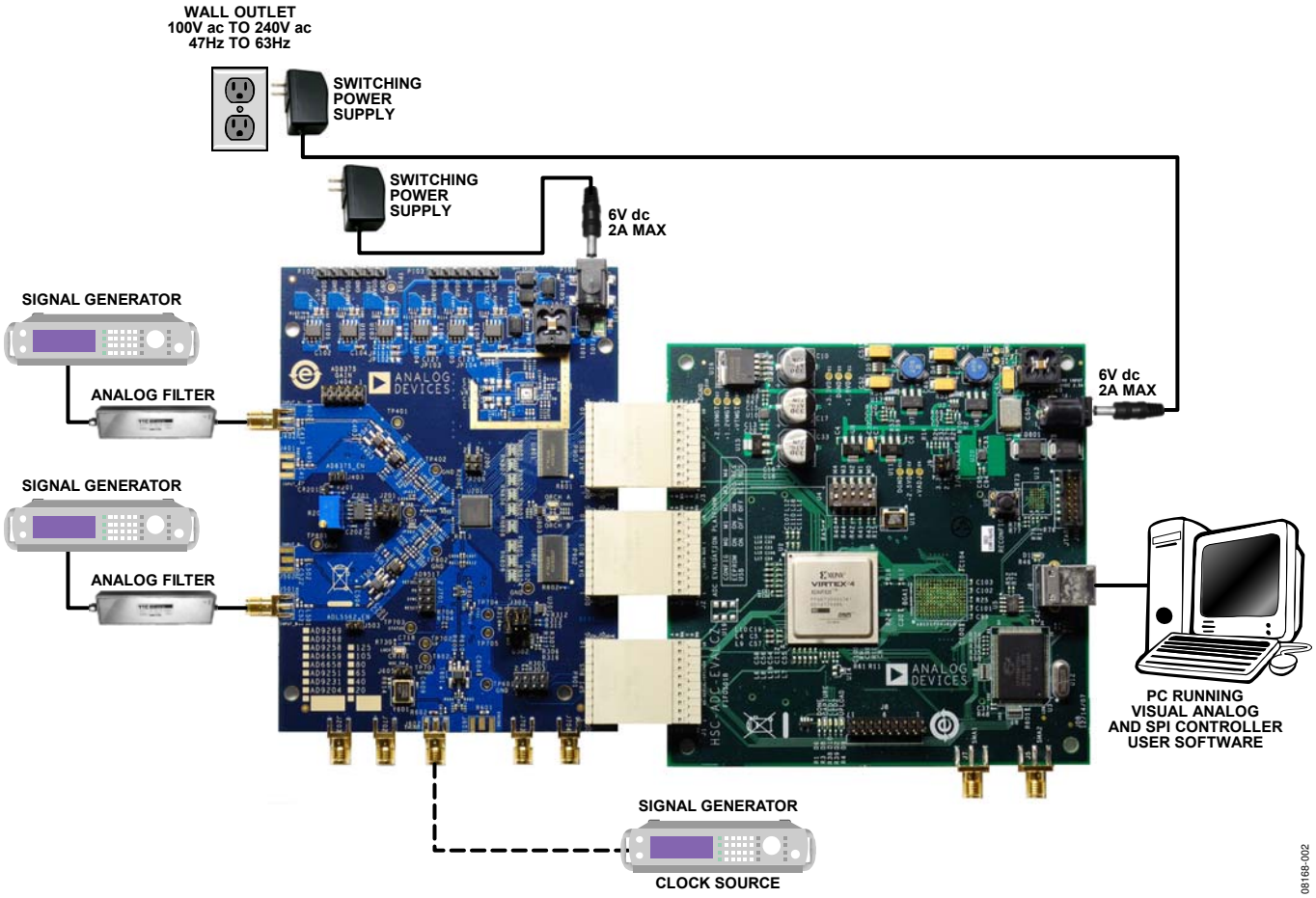

Figure 2. Evaluation Board Connection

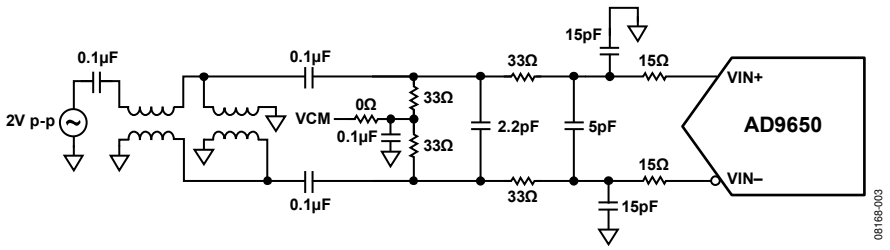

Figure 3. Default Analog Input Configuration of the AD9650 Family

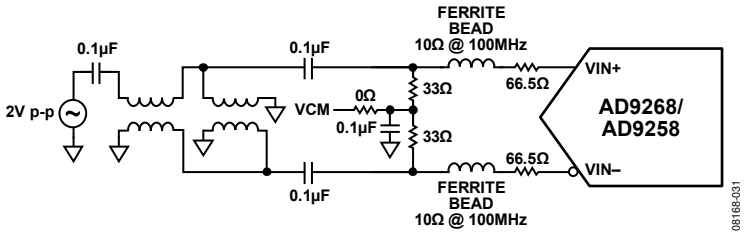

Figure 4. Default Analog Input Configuration of the AD9268 Family

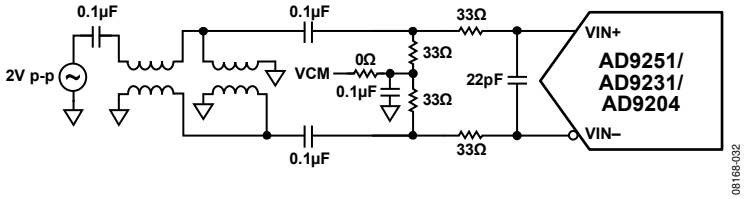

Figure 5. Default Analog Input Configuration of the AD9269 Family

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

This section explains the default and optional settings or modes allowed on the AD9650/AD9268/AD9258/AD9251/AD9231/AD9204/AD9269/AD6659 Rev. C evaluation board.

Power Circuitry

Connect the switching power supply that is supplied in the evaluation kit between a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz and P101.

Analog Input

The A and B channel inputs on the evaluation board are set up for a double balun-coupled analog input with a 50 Ω impedance.

AD9650 Family

The default input network, as configured on the AD9650 evaluation board, is shown in Figure 3

AD9268 Family

For the AD9268 family, the default analog input configuration supports analog input frequencies of up to ~250 MHz (see Figure 4). This input network is optimized to support a wide frequency band. See the AD9258 and AD9268 data sheets for additional information on the recommended networks for different input frequency ranges.

AD9269 Family

For the AD9269 family, the default analog input configuration supports analog input frequencies of up to ~150 MHz (see Figure 5). The nominal input drive level is 10 dBm to achieve 2 V p-p full scale into 50 Ω. At higher input frequencies, slightly higher input drive levels are required due to losses in the front-end network.

Optionally, the Channel A input on the board can be configured to use the AD8375 digitally variable gain amplifier (DVGA). The AD8375 component is included on the evaluation board at U401. However, the path into and out of the AD8375 can be configured in many different ways depending on the application; therefore, the parts in the input and output path are left unpopulated. Users should see the AD8375 data sheet for additional information on this part and for configuring the inputs and outputs. The AD8375 by default is held in power-down mode but can be enabled by adding a jumper on J403.

The Channel B input is also set up with an optional input path through the ADL5562 ultralow distortion RF/IF differential amplifier. Similar to Channel A, the amplifier is included on the board at U501; however, the input-/output-related components are not included. Users should see the ADL5562 data sheet for additional information on this part and for configuring the inputs and outputs. The ADL5562 is also normally held in power-down mode and can be enabled by adding a jumper on J503. The ADL5562 on the Channel B input can also be substituted with the ADA4937 or the ADA4938 to allow evaluation of these parts with the ADC.

VREF

The default VREF configuration is to connect the SENSE pin to AGND for internal VREF operation. This is done by connecting Pin 4 and Pin 6 on Header J201. Table 2 summarizes the internal VREF voltage for the different families of ADCs.

Table 2. Default VREF Configuration

Family Name	Internal VREF (V)	Full-Scale Range (V p-p)
AD9650	1.35	2.7
AD9268	1	2
AD9269	1	2

The AD9650 and AD9269 families operate with a fixed reference. For the AD9268 family, the reference voltage can be changed to 0.5 V for a 1.0 V p-p full-scale range by moving the SENSE pin jumper connection on J201 from Pin 4 through Pin 6 to Pin 3 through Pin 4 (this connects the SENSE pin to the VREF pin).

To use the programmable reference mode for the AD9268 family, a resistor divider can be set up by installing R204 and R205. The jumper on J201 should be removed for this mode of operation. See the data sheet of the specific part for the additional information on using the programmable reference mode.

A separate unpopulated external reference option using the AD1580 reference and the AD822 amplifier is also included on the evaluation board. To enable the external reference populate CR201, U202, R202, R201, C201, and C202 with the values shown in the Evaluation Board Schematics and Artwork section and Bill of Materials section. The J201 jumper should be placed between Pin 4 and Pin 2 to set the reference input to the external reference mode.

RBIAS

RBIAS has a default setting of 10 kΩ (R206) to ground and is used to set the ADC core bias current. Note that using a resistor value other than a 10 kΩ, 1% resistor for RBIAS may degrade the performance of the device.

Clock Circuitry for the AD9269 Family

The default clock input circuit on the AD9269 evaluation board family uses a simple transformer-coupled circuit using a high bandwidth 1:1 impedance ratio transformer (T601) that adds a low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The transformer converts the single-ended input to a differential signal that is clipped by CR601 before entering the ADC clock inputs.

The AD9269 evaluation board family is by default set up to be clocked through the transformer-coupled input network from the crystal oscillator, Y601. This oscillator is a low phase noise oscillator from Valpey Fisher (VFAC3-BHL-40MHz/VFAC3-BHL-65MHz/VFAC3-BHL-80MHz). If a different clock source is desired, remove J605 to disable the oscillator from running and connect the external clock source to the SMA connector, J602 (labeled ENCODE+).

Clock Circuitry for the AD9650 and the AD9268 Family

The default clock input circuit on the AD9650 and AD9268 family evaluation boards uses a similar circuit to the AD9269 family but uses a higher bandwidth 1:1 impedance ratio balun (T602) that adds a low amount of jitter to the clock path. The clock input is again 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The balun converts the single-ended input to a differential signal that is clipped before entering the ADC clock inputs.

The board is set by default to use an external clock generator. An external clock source capable of driving a 50 Ω terminated input should be connected to J602. This family is shipped from Valpey Fisher with a low phase noise oscillator installed. The oscillator frequency is set to match the rated speed of the part: 125 MHz, 105 MHz, or 80 MHz for the AD9268 family and 105 MHz, 80 MHz, 65 MHz, or 25 MHz for the AD9650 family. To enable the oscillator, install J605, and to connect it into the clock path, add a 0 Ω resistor at C610. R602 should also be removed to remove the 50 Ω termination from the output of the oscillator.

A differential LVPECL clock driver output can also be used to clock the ADC input using the AD9517 (U701). To place the AD9517 into the clock path, populate R607 and R608 with 0 Ω resistors and remove R609 and R610 to disconnect the default clock path inputs. In addition, populate R731 and R732 with 0 Ω resistors and remove R611 and R612 to disconnect the default clock path outputs and insert the AD9517 LVPECL Output 3. The AD9517 must be configured through the SPI controller software to set up the PLL and other operation modes. Consult the AD9517 data sheet for more information about these and other options.

PDWN

To enable the power-down feature, add a shorting jumper across J205 at Pin 1 and Pin 2 to connect the PDWN pin to DRVDD.

$\overline{OE}$

To disable the outputs using the $\overline{OE}$ pin, add a shorting jumper across J205 at Pin 3 and Pin 4 to connect the $\overline{OE}$ pin to DRVDD.

Non-SPI Mode

For users who want to operate the DUT without using SPI, remove the shorting jumpers on J302. This disconnects the $\overline{CS}$, SCLK/DFS, and SDIO/DCS pins from the SPI control bus, allowing the DUT to operate in non-SPI mode. In this mode, the SCLK/DFS and SDIO/DCS pins take on their alternate functions to select the data format and enable/disable the DCS. With the jumpers removed, DCS is disabled; to enable DCS, add a shorting jumper on J302 between Pin 2 to Pin 3. With the jumper removed, the data format is set to offset binary. To set the data format to twos complement, a jumper should be added on J302 between Pin 5 and Pin 6.

Switching Power Supply

Optionally, the ADC on the board can be configured to use the ADP2114 dual switching power supply to provide power to the DRVDD and AVDD rails of the ADC. To configure the board to operate from the ADP2114, the following changes must be incorporated (see the Evaluation Board Schematics and Artwork and Bill of Materials sections for specific recommendations for part values):

1. Install R120 and R122 to enable the ADP2114.
2. Install R107 and R109.
3. Install R110, R111, C108, and C109.
4. Install R108, R118, C110, C111, C112, and C113.
5. Install L101, L102, E116, and E117.
6. Install R125 and R127.
7. Remove JP101 and JP103 and install JP102 and JP104.
8. Remove E103, E105, and E107 and install E104, E106, and E108.

Making these changes enables the switching converter to power the ADC. Using the switching converter as the ADC power source is more efficient than using the default LDOs.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

This section provides quick start procedures for using the AD9650, AD9268, AD9258, AD9251, AD9231, AD9204, AD9269, and AD6659 evaluation board. Both the default and optional settings are described.

CONFIGURING THE BOARD

Before using the software for testing, configure the evaluation board as follows:

1. Connect the evaluation board to the data capture board, as shown in Figure 1 and Figure 2.
2. Connect one 6 V, 2.5 A switching power supply (such as the CUI, Inc., EPS060250UH-PHP-SZ supplied) to the AD9650, AD9268, AD9258, AD9251, AD9231, AD9204, AD9269, or AD6659 board.
3. Connect one 6 V, 2.5 A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the HSC-ADC-EVALCZ board.
4. Connect the HSC-ADC-EVALCZ board (J6) to the PC with a USB cable.
5. On the ADC evaluation board, confirm that three jumpers are installed on J302, one between Pin 1and Pin 2, one between Pin 4 and Pin 5, and one between Pin 8 and Pin 9, to connect the SPI bus to the DUT.
6. If using an AD9269 family board, ensure that J605 (OSC_EN) has a jumper installed to use the on-board 50 MHz/65 MHz/ 80 MHz Valpey Fisher VFAC3 oscillator. If using an AD9650 or AD9268 family board, make sure a low jitter sample clock is applied at J602.
7. On the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal to the desired A and/or B channel(s). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results, use a narrow-band, band-pass filter with 50 Ω terminations and an appropriate center frequency. (Analog Devices uses TTE, Allen Avionics, and K&L band-pass filters.)

USING THE SOFTWARE FOR TESTING

Setting Up the ADC Data Capture

After configuring the board, set up the ADC data capture using the following steps:

1. Open VisualAnalog on the connected PC. The appropriate part type should be listed in the status bar of the **VisualAnalog – New Canvas** window. Select the template that corresponds to the type of testing to be performed (see Figure 6 where the AD9268 is shown as an example).

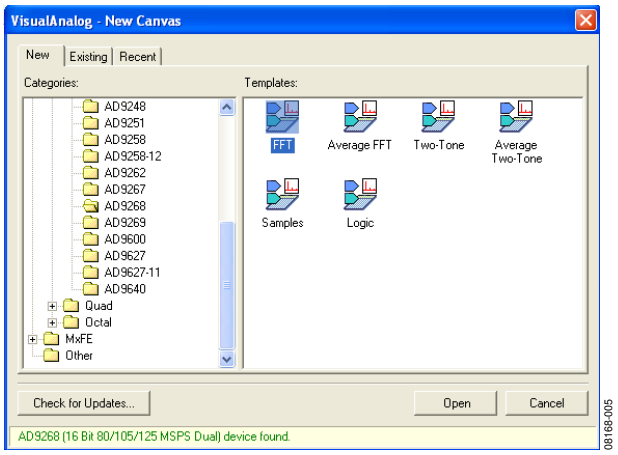

Figure 6. VisualAnalog, New Canvas Window

2. After the template is selected, a message appears asking if the default configuration can be used to program the FPGA (see Figure 7). Click **Yes** and the window closes.

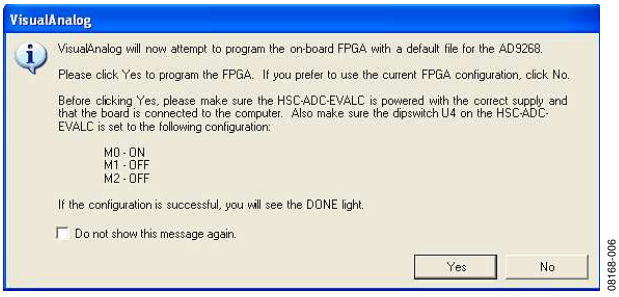

Figure 7. VisualAnalog Default Configuration Message

3. To change features to settings other than the default settings, click the **Expand Display** button, located on the bottom right corner of the window, to see what is shown in Figure 9. Detailed instructions for changing the features and capture settings can be found in the AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*. After the changes are made to the capture settings, click **Collapse Display** (see Figure 8).

Figure 8. VisualAnalog Window Toolbar, Collapsed Display

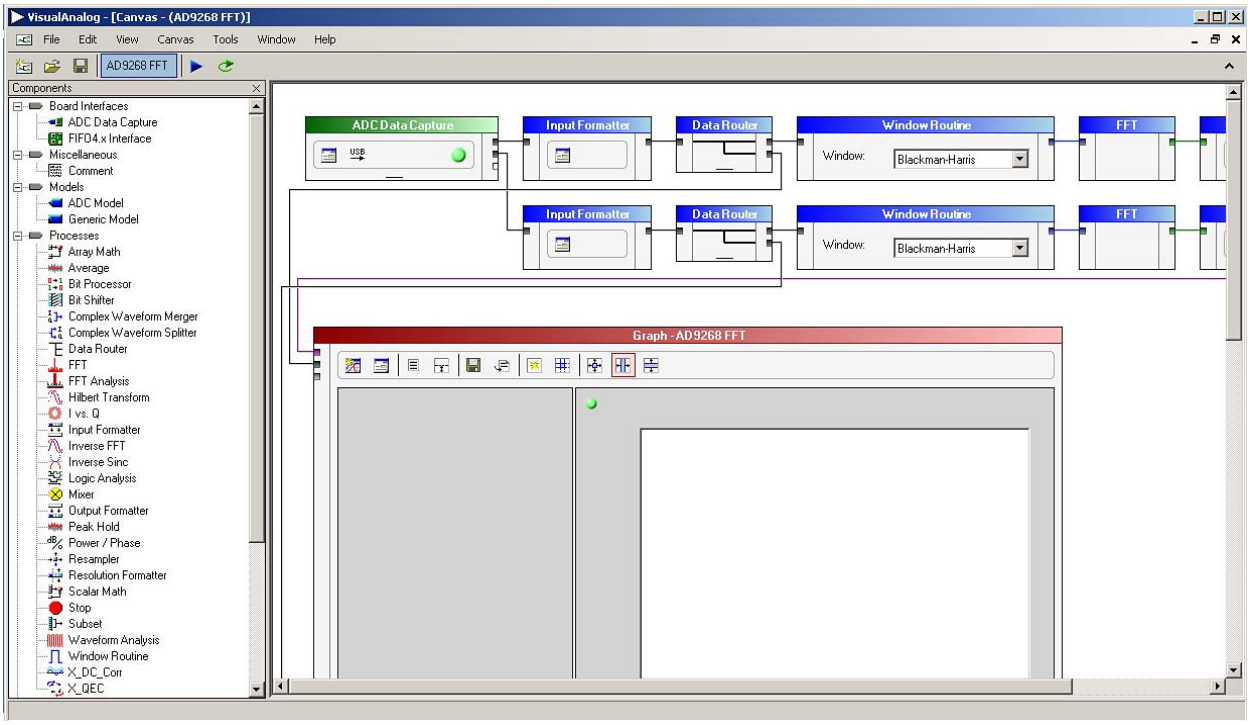

Figure 9. VisualAnalog, Main Window

Setting Up the SPI Controller Software

After the ADC data capture board setup is complete, set up the SPI controller software using the following procedure:

1. Open the SPI controller software by going to the **Start** menu or by double-clicking the **SPIController** software desktop icon. If prompted for a configuration file, select the appropriate one. If not, check the title bar of the window to determine which configuration is loaded. If necessary, choose **Cfg Open** from the **File** menu and select the appropriate file based on your part type. Note that the **CHIP ID(1)** field should be filled to indicate whether the correct SPI controller configuration file is loaded (see Figure 10).

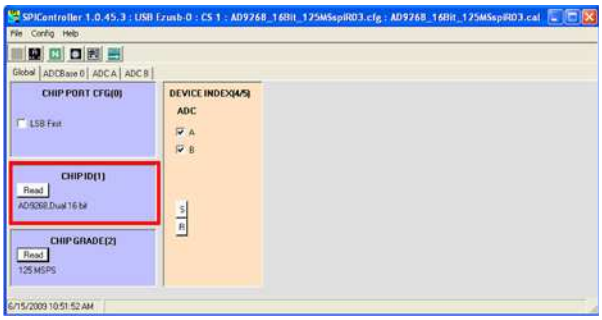

Figure 10. SPI Controller, CHIP ID(1) Box

2. Click the **New DUT** button in the **SPIController** window (see Figure 11).

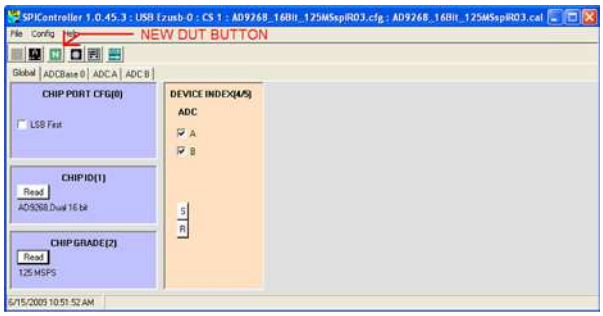

Figure 11. SPI Controller, New DUT Button

3. In the **ADCBase 0** tab of the **SPIController** window, find the **CLOCK DIVIDE(B)** box (see Figure 12). If using the clock divider, use the drop-down box to select the correct clock divide ratio, if necessary. See the appropriate part data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information.

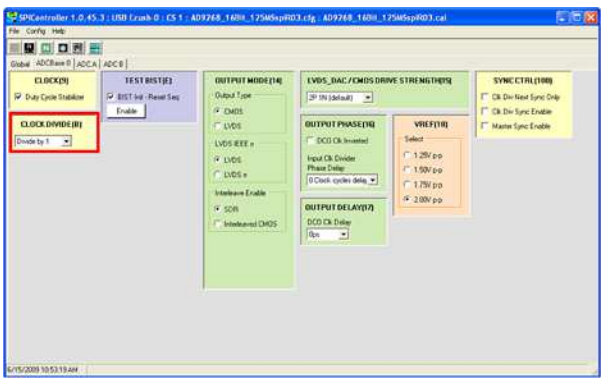

Figure 12. SPI Controller, CLOCK DIVIDE(B) Box

4. Note that other settings can be changed on the **ADCBase 0** page (see Figure 12) and the **ADC A** and **ADC B** pages (see Figure 13) to set up the part in the desired mode. The **ADCBase 0** page settings affect the entire part, whereas the settings on the **ADC A** and **ADC B** pages affect the selected channel only. See the appropriate part data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information on the available settings.

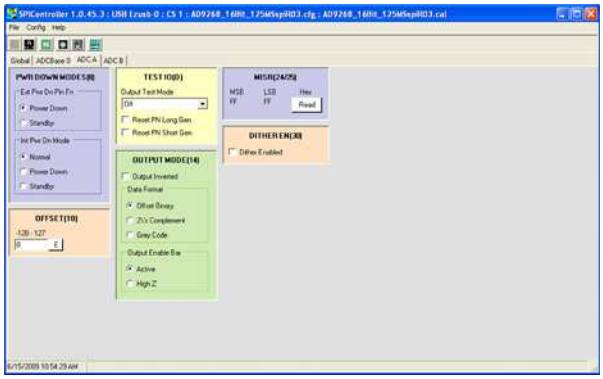

Figure 13. SPI Controller, Example ADC A Page

5. Click the **Run** button in the **VisualAnalog** toolbar (see Figure 14).

Figure 14. Run Button (Encircled in Red) in VisualAnalog Toolbar, Collapsed Display

Adjusting the Amplitude of the Input Signal

The next step is to adjust the amplitude of the input signal for each channel as follows:

1. Adjust the amplitude of the input signal so that the fundamental is at the desired level. Examine the **Fund Power** reading in the left panel of the **VisualAnalog Graph - AD9268 Average FFT** window (see Figure 15).

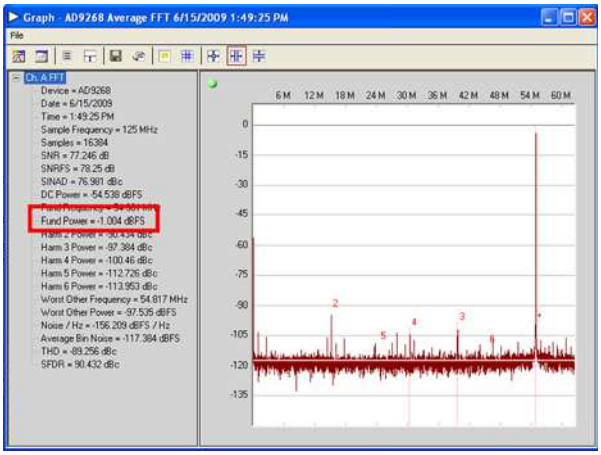

Figure 15. Graph Window of VisualAnalog

2. Repeat this procedure for Channel B.
3. Click the disk icon within the **Graph** window to save the performance plot data as a .csv formatted file. See Figure 16 for an example.

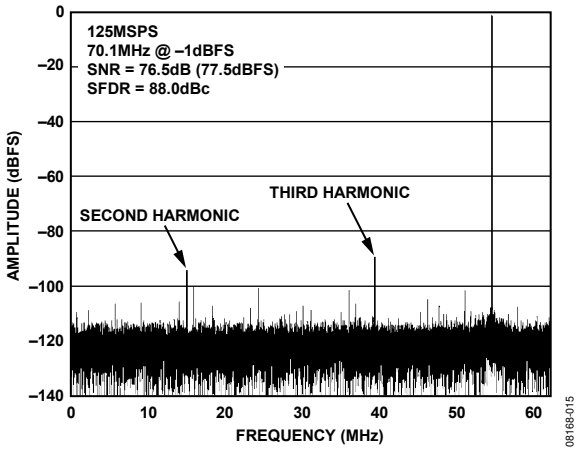

Figure 16. Typical FFT, AD9268/AD9258

Troubleshooting Tips

If the FFT plot appears abnormal, do the following:

- If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce the input level, if necessary.
- In **VisualAnalog**, click the **Settings** button in the **Input Formatter** block. Check that **Number Format** is set to the correct encoding (offset binary by default). Repeat for the other channel.

If the FFT appears normal but the performance is poor, check the following:

- Make sure an appropriate filter is used on the analog input.
- Make sure the signal generators for the clock and the analog input are clean (low phase noise).
- Change the analog input frequency slightly if noncoherent sampling is being used.
- Make sure the SPI config file matches the product being evaluated.

If the FFT window remains blank after **Run** is clicked, do the following:

- Make sure the evaluation board is securely connected to the HSC-ADC-EVALCZ board.
- Make sure the FPGA has been programmed by verifying that the **DONE** LED is illuminated on the HSC-ADC-EVALCZ board. If this LED is not illuminated, make sure the U4 switch on the board is in the correct position for USB CONFIG.
- Make sure the correct FPGA program was installed by selecting the **Settings** button in the **ADC Data Capture** block in **VisualAnalog**. Then select the **FPGA** tab and verify that the proper FPGA bin file is selected for the part.

If **VisualAnalog** indicates that the **FIFO Capture timed out**, do the following:

- Make sure all power and USB connections are secure.
- Probe the DCOA signal at RN801 (Pin 2) on the evaluation board and confirm that a clock signal is present at the ADC sampling rate.

EVALUATION BOARD SCHEMATICS AND ARTWORK

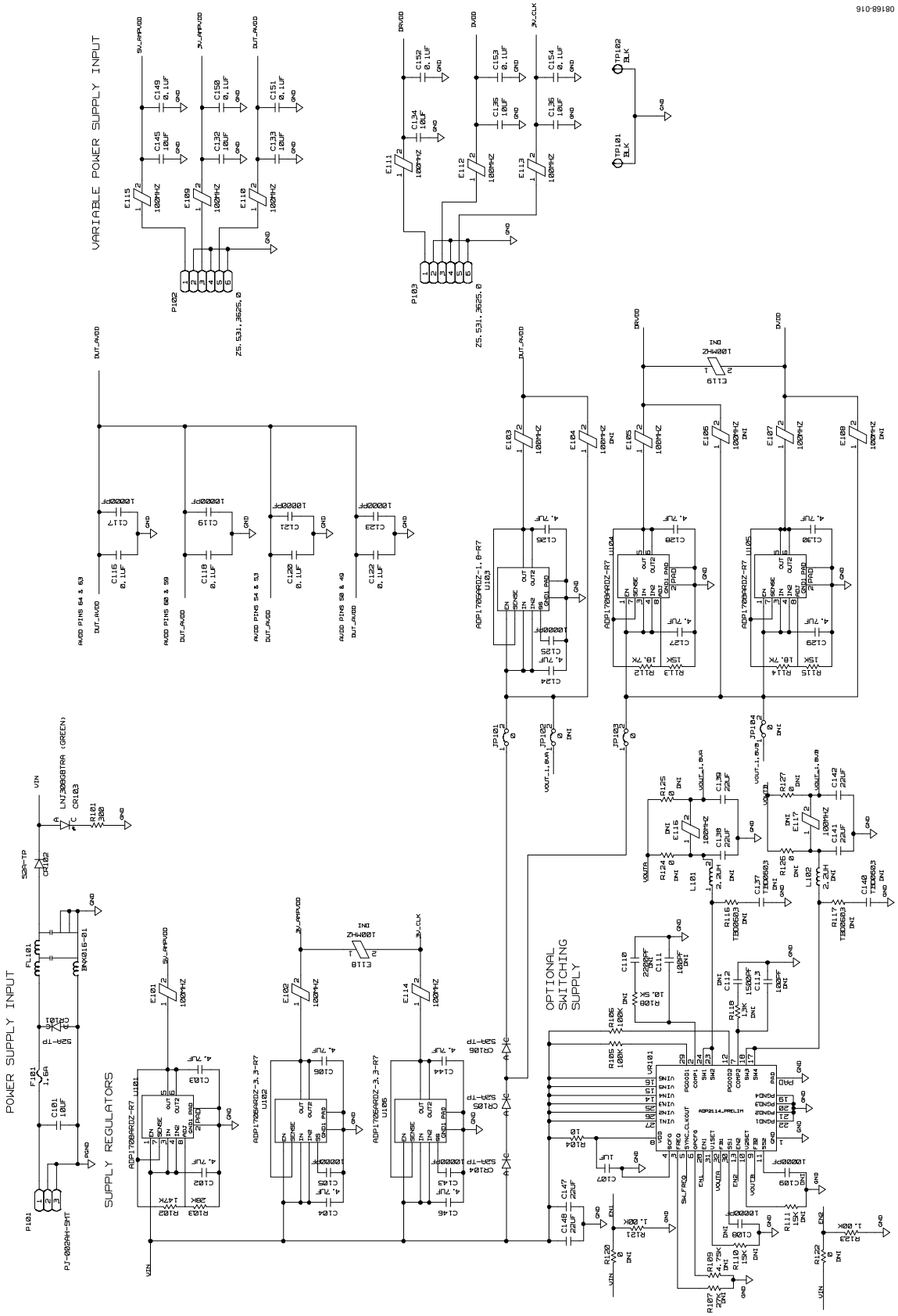

Figure 17. Board Power Input and Supply Circuits

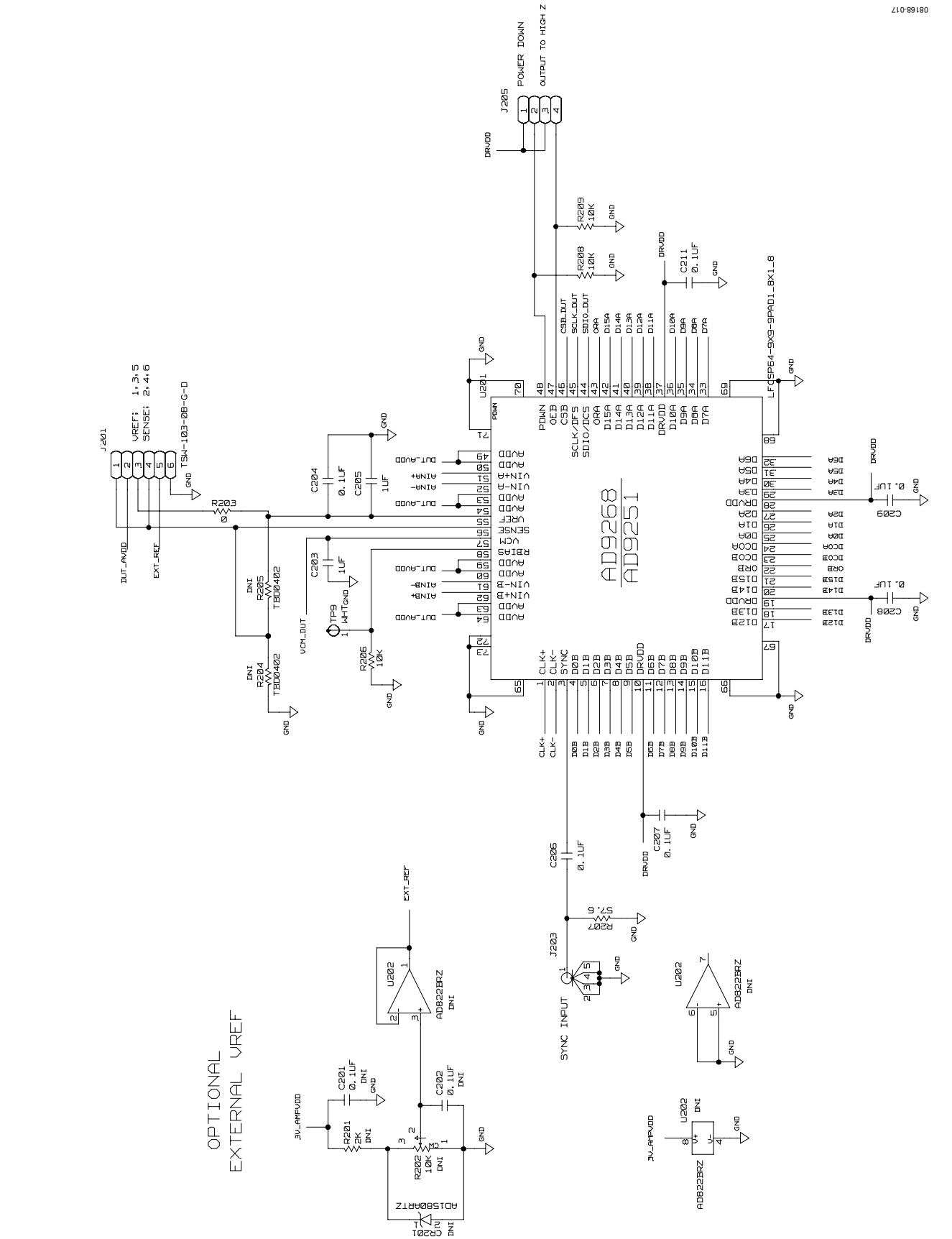

Figure 18. DUT and Related Circuits

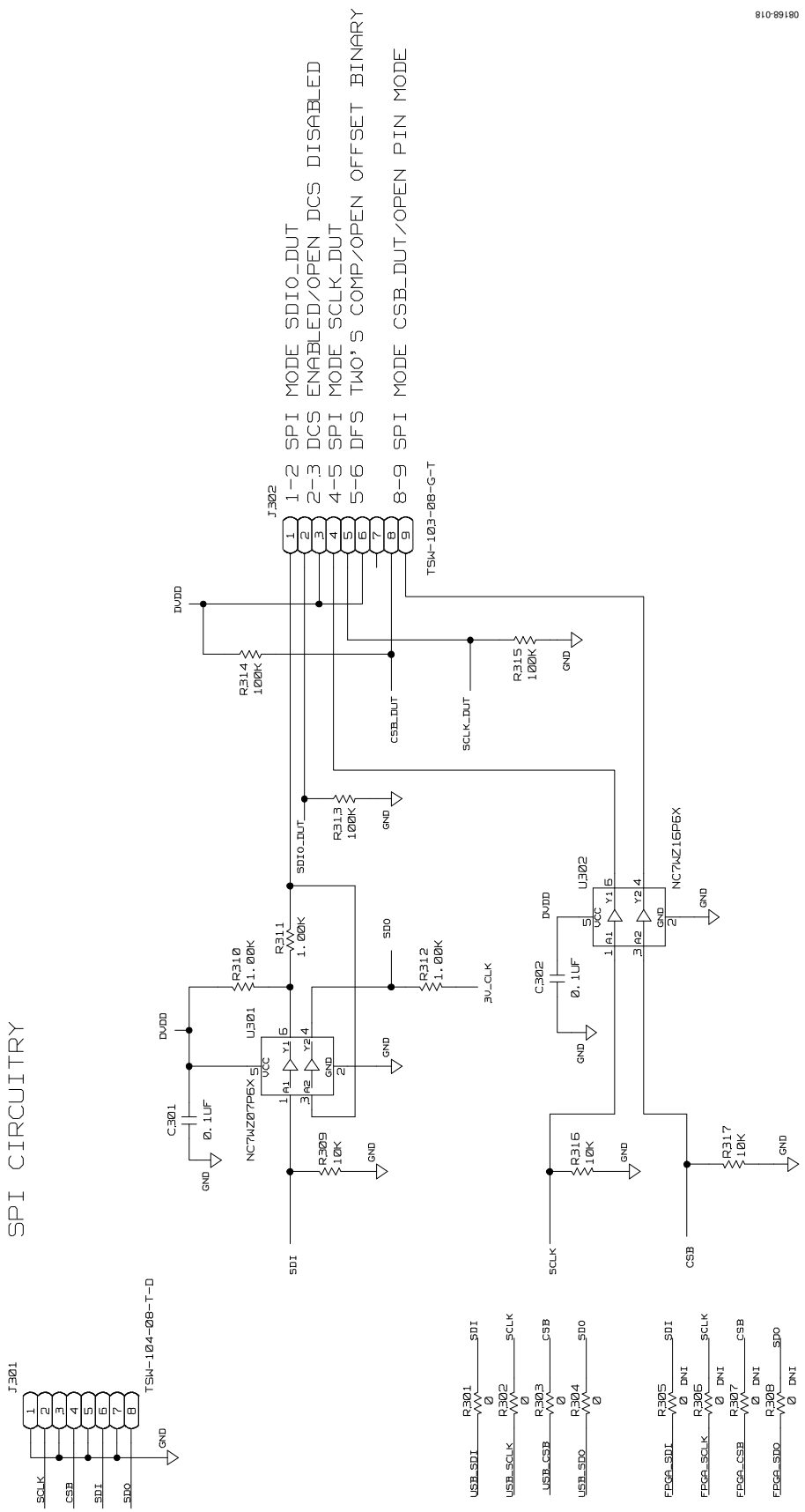

Figure 19. SPI Interface Circuit

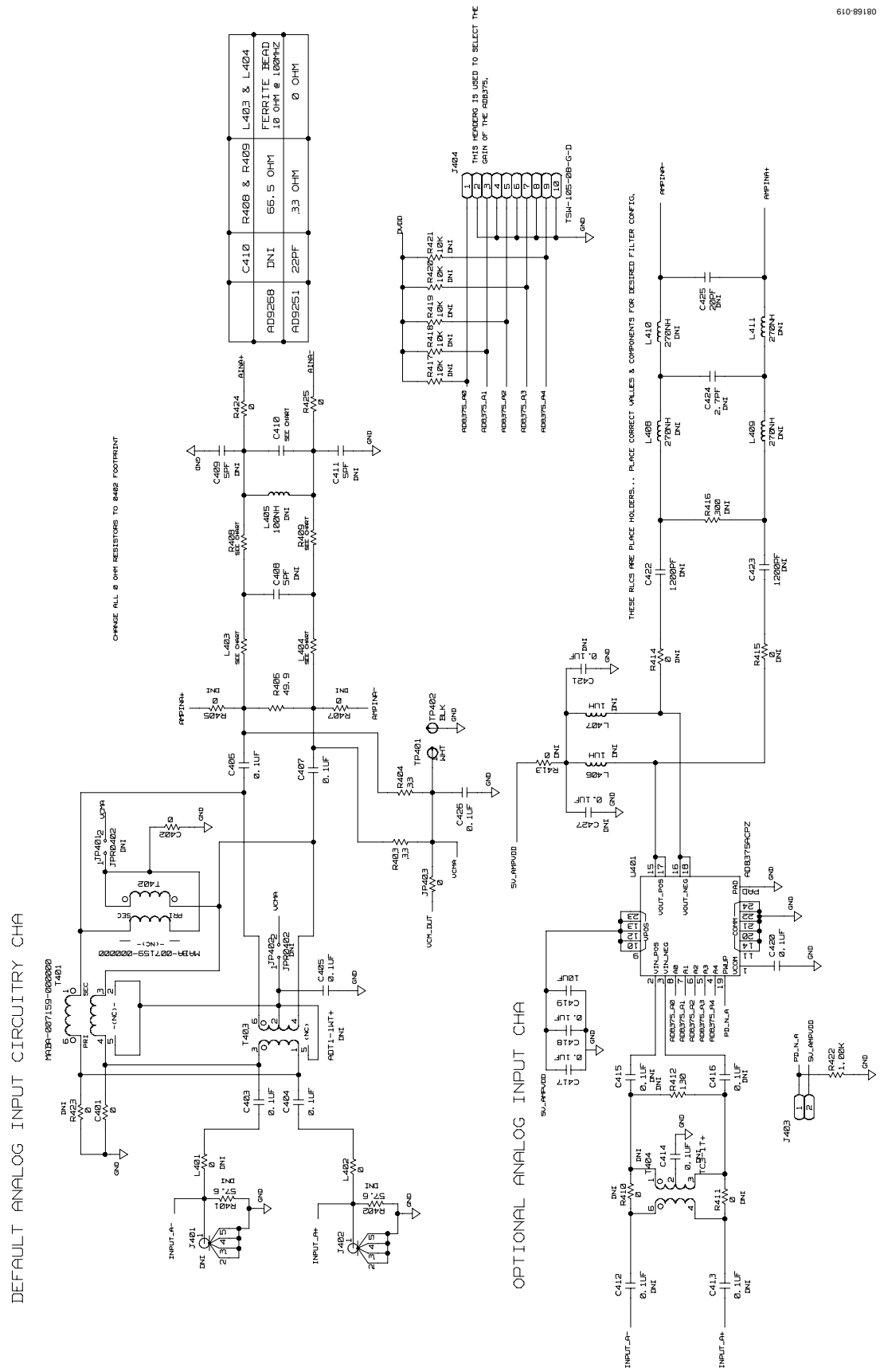

Figure 20. Channel A Input Circuits

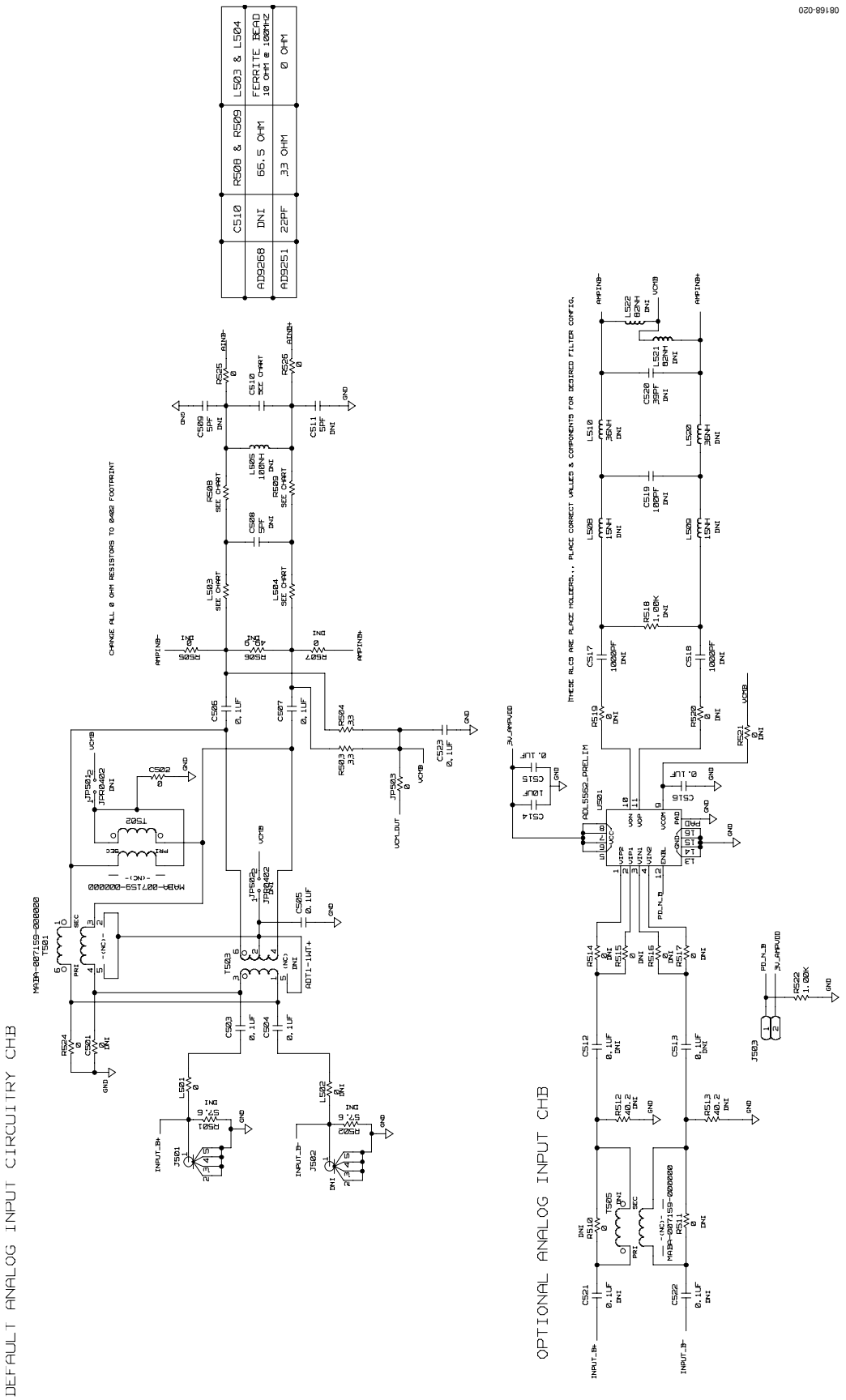

Figure 21. Channel B Analog Input Circuits

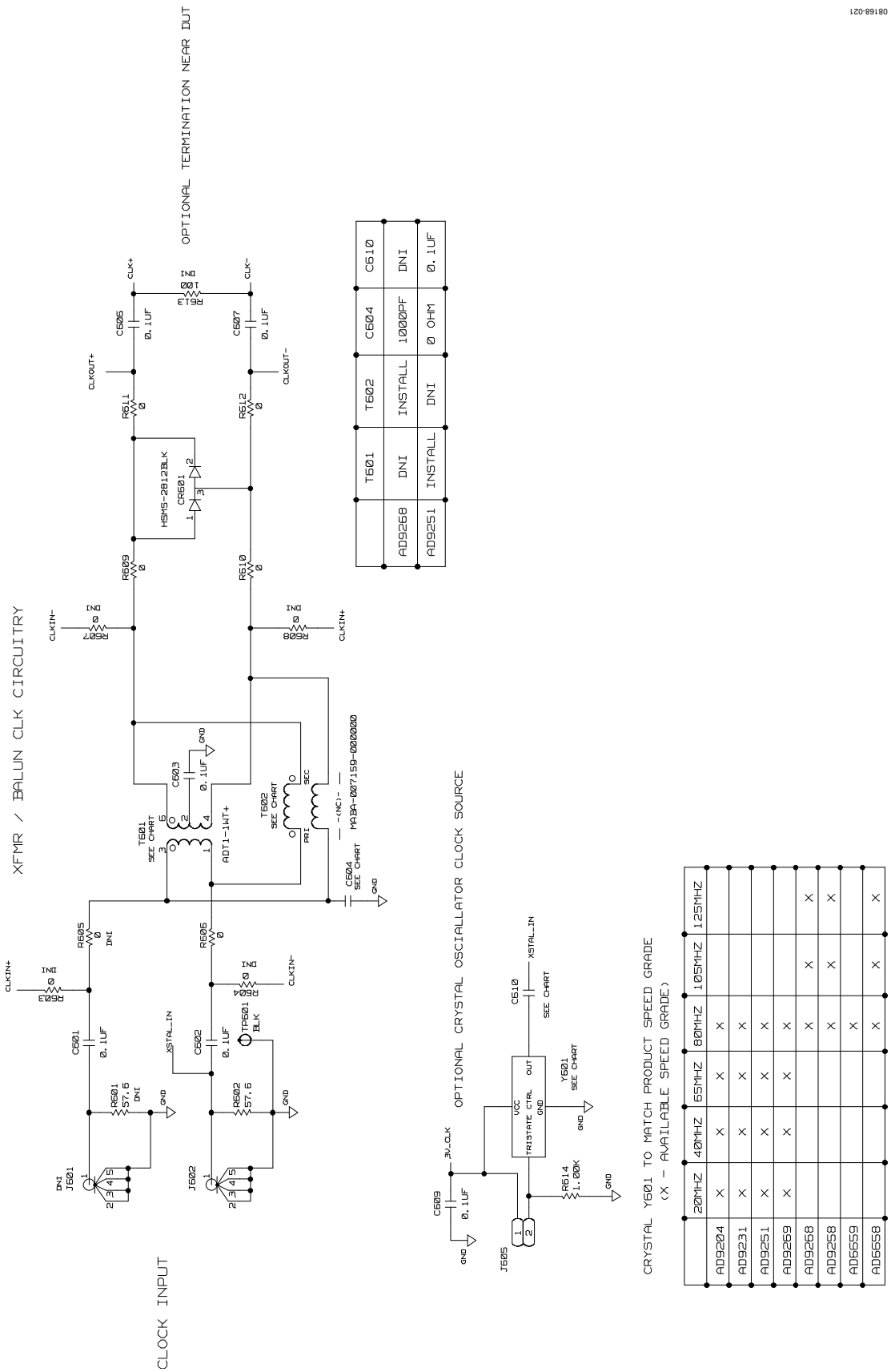

Figure 22. Default Clock Path Input Circuits

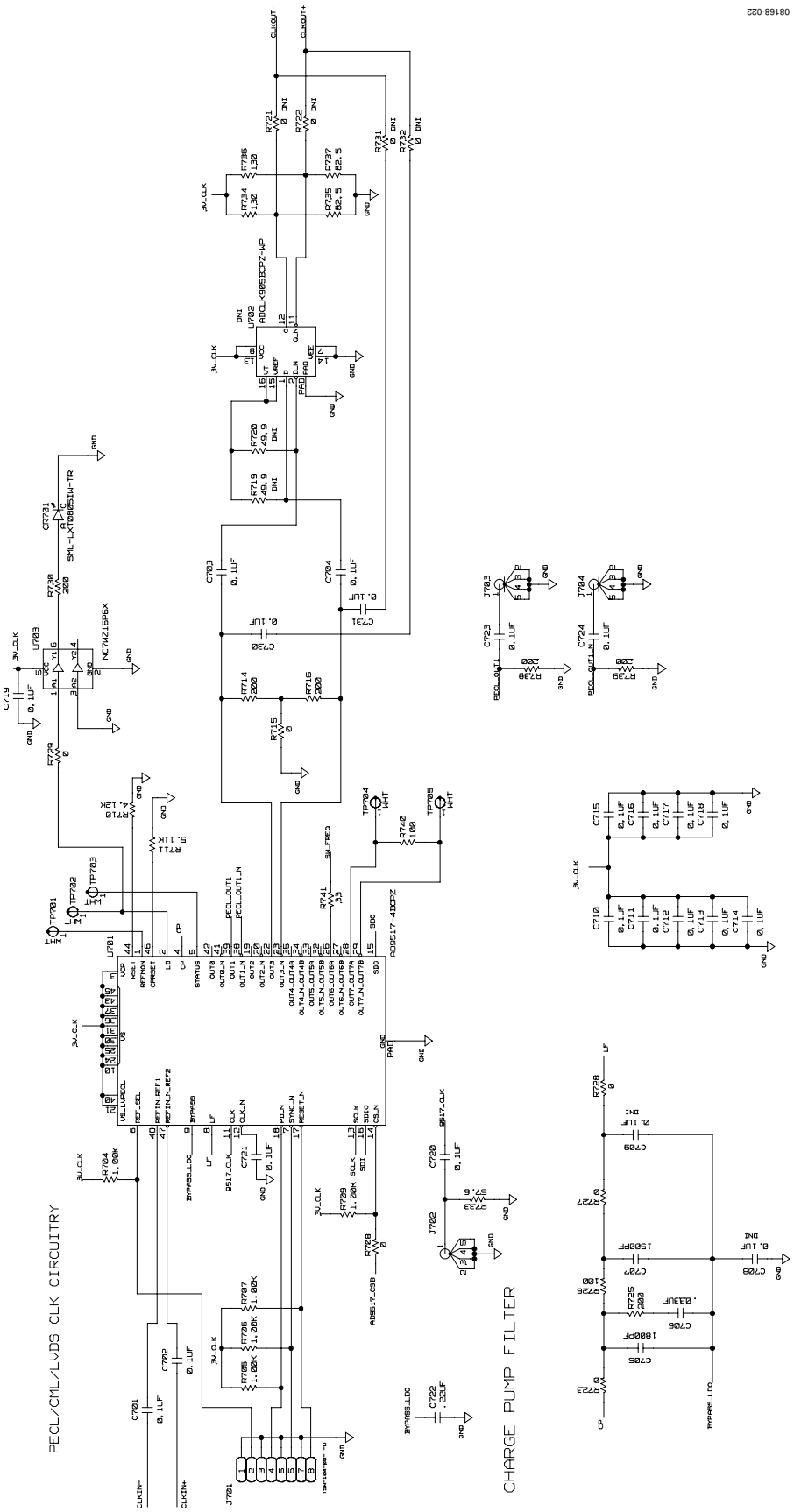

Figure 23. Optional AD9517 Clock Input Circuit

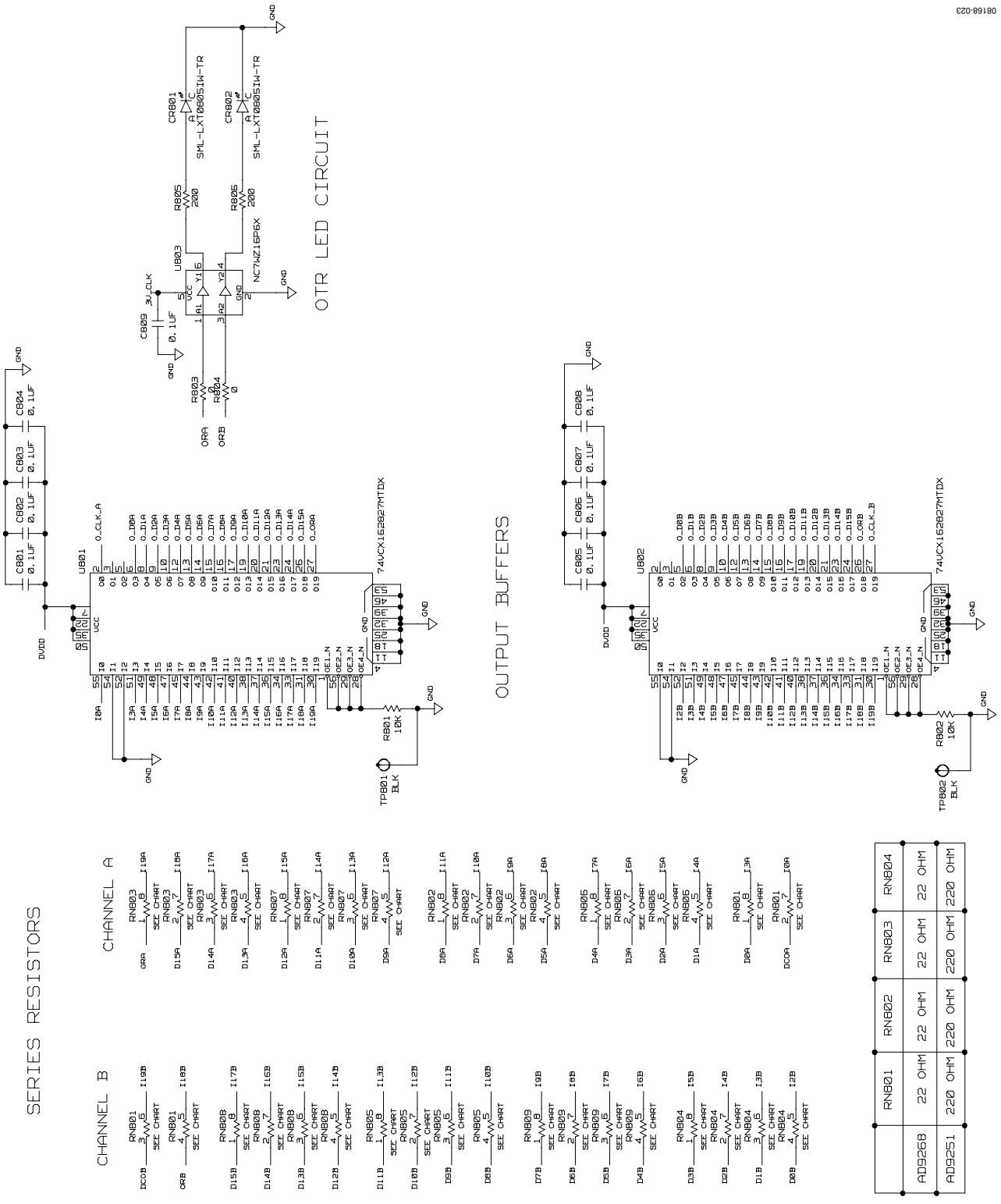

Figure 24. Output Buffer Circuits

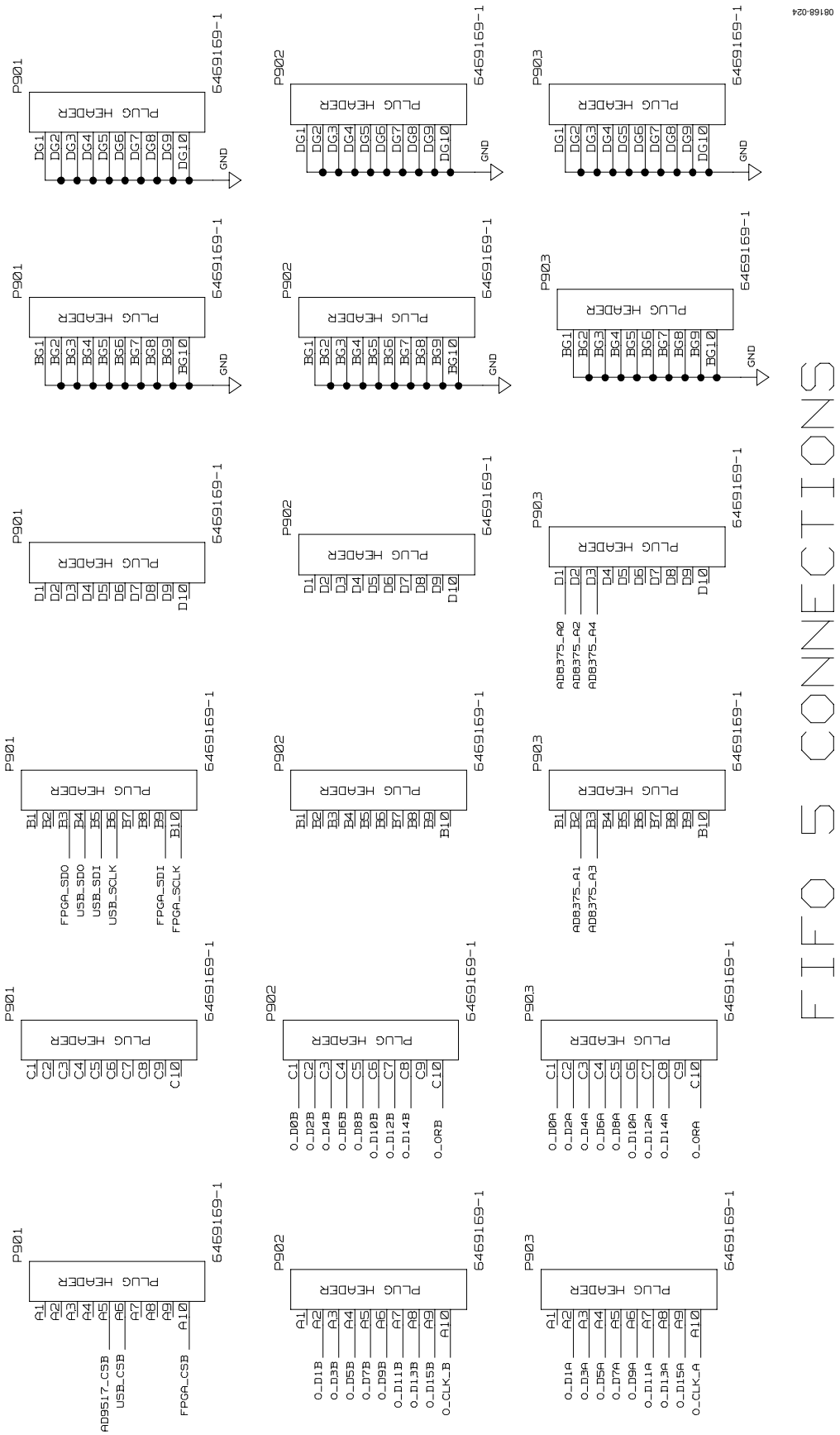

Figure 25. FIFO Board Connector

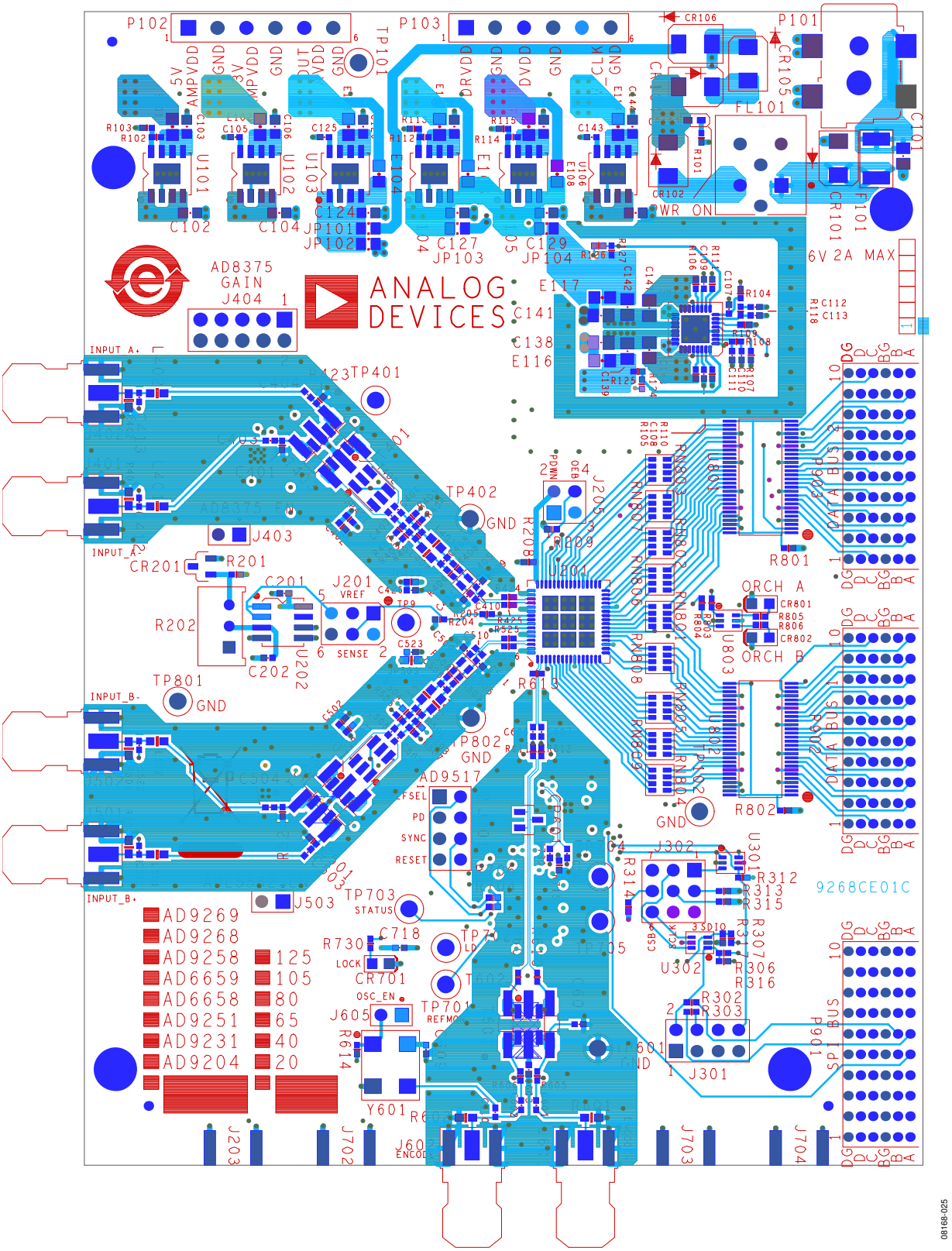

Figure 26. Top Side

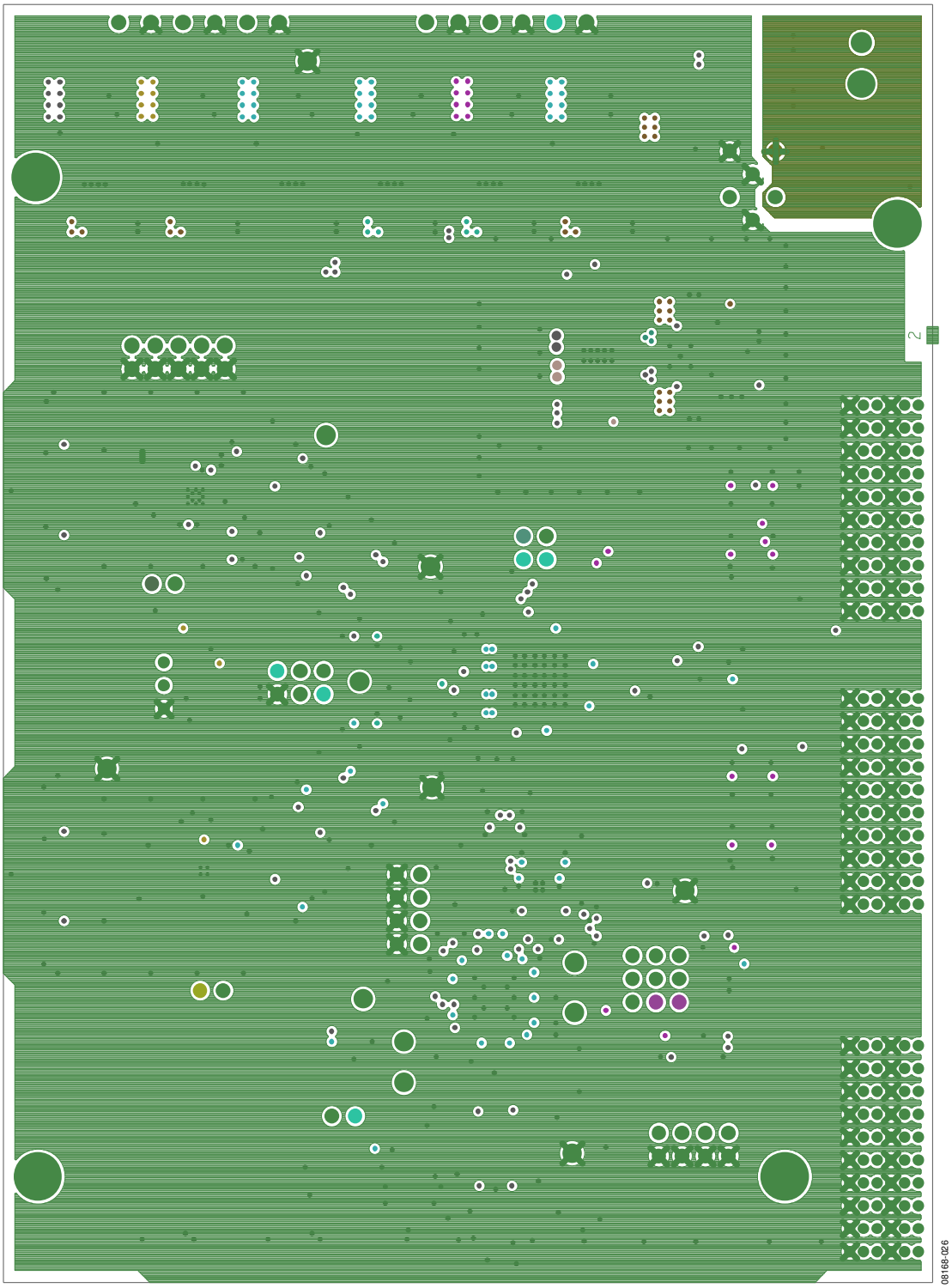

Figure 27. Ground Plane (Layer 2)

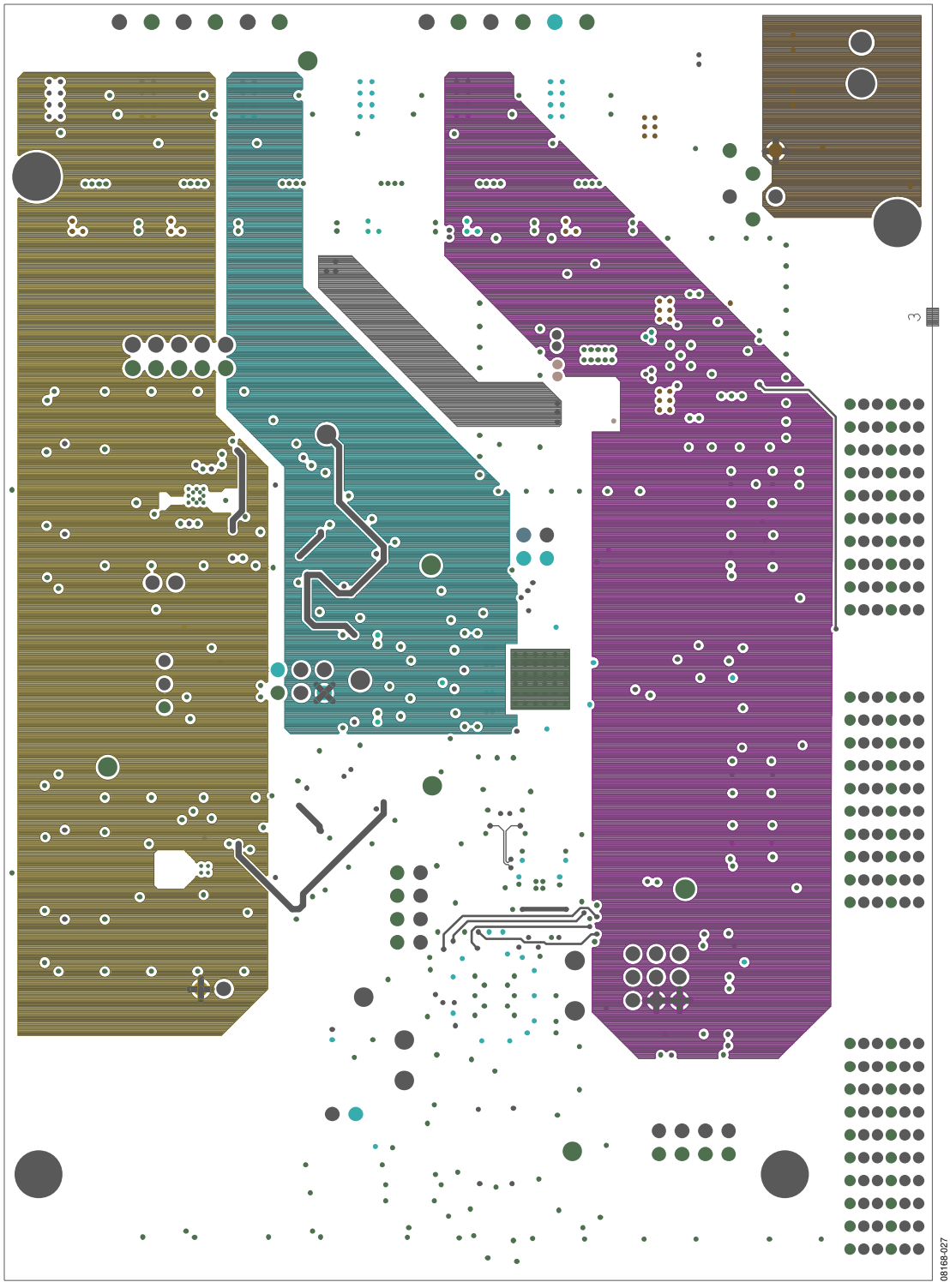

Figure 28. Power Plane (Layer 3)

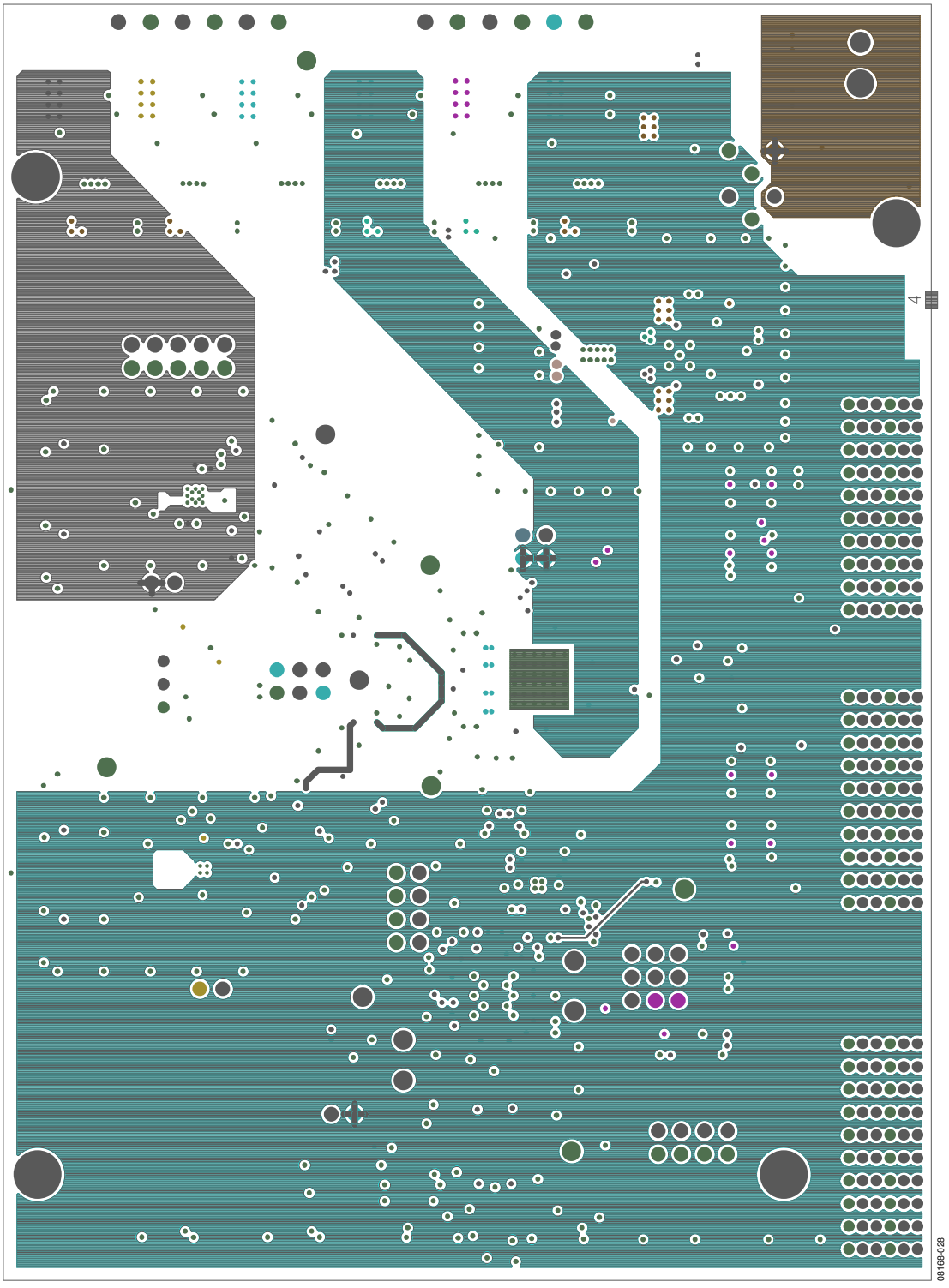

Figure 29. Power Plane (Layer 4)

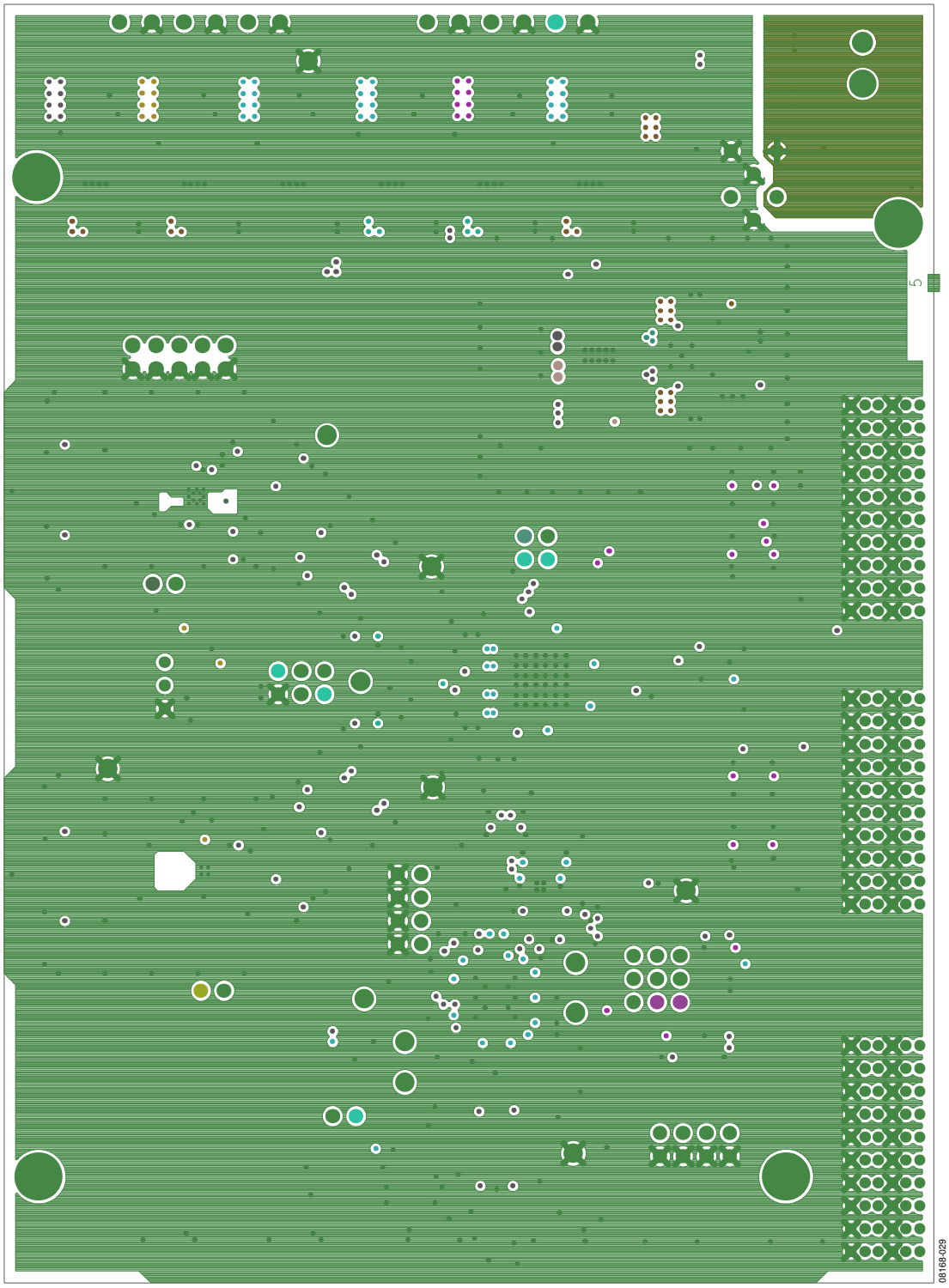

Figure 30. Ground Plane (Layer 5)