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Octal, 14-Bit, 50 MSPS, Serial LVDS, 1.8 V ADC

Data Sheet **AD9252**

FEATURES

- 8 analog-to-digital converters (ADCs) integrated into 1 package
- 93.5 mW ADC power per channel at 50 MSPS
- SNR = 73 dB (to Nyquist)
- ENOB = 12 bits
- SFDR = 84 dBc (to Nyquist)
- Excellent linearity
  - DNL = ±0.4 LSB (typical); INL = ±1.5 LSB (typical)
- Serial LVDS (ANSI-644, default)
  - Low power, reduced signal option (similar to IEEE 1596.3)
- Data and frame clock outputs
- 325 MHz, full-power analog bandwidth
- 2 V p-p input voltage range
- 1.8 V supply operation
- Serial port control
  - Full-chip and individual-channel power-down modes
  - Flexible bit orientation
  - Built-in and custom digital test pattern generation
  - Programmable clock and data alignment
  - Programmable output resolution
  - Standby mode

APPLICATIONS

- Medical imaging and nondestructive ultrasound
- Portable ultrasound and digital beam-forming systems
- Quadrature radio receivers
- Diversity radio receivers
- Tape drives
- Optical networking
- Test equipment

GENERAL DESCRIPTION

The AD9252 is an octal, 14-bit, 50 MSPS ADC with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. Operating at a conversion rate of up to 50 MSPS, it is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock (DCO) for capturing data on the output and a frame clock (FCO) for signaling a new output byte are provided. Individual channel power-down is supported and typically consumes less than 2 mW when all channels are disabled.

FUNCTIONAL BLOCK DIAGRAM

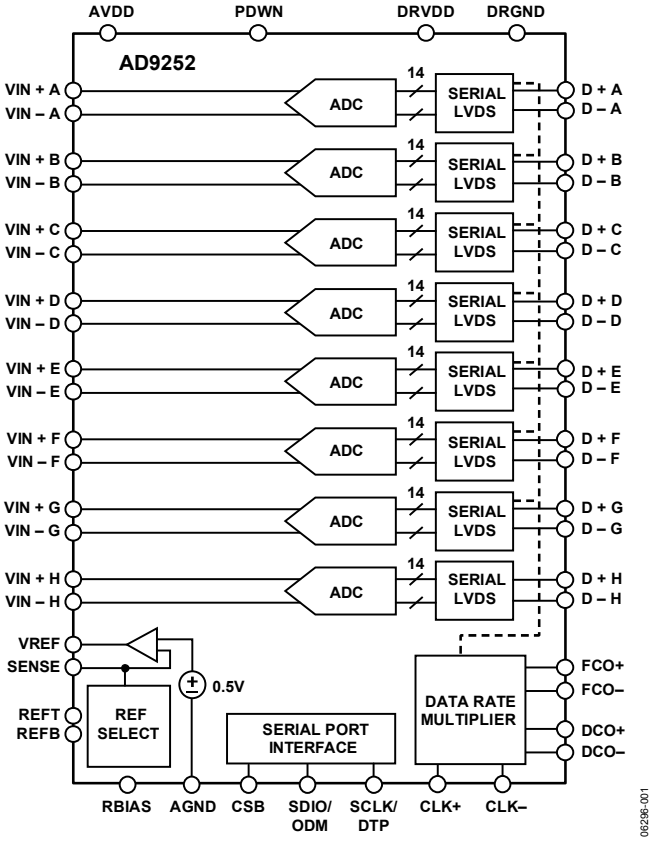

Figure 1.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9252 is available in an RoHS compliant, 64-lead LFCSP. It is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Small Footprint. Eight ADCs are contained in a small package.
2. Low Power of 93.5 mW per Channel at 50 MSPS.
3. Ease of Use. A data clock output (DCO) operates up to 350 MHz and supports double data rate (DDR) operation.
4. User Flexibility. SPI control offers a wide range of flexible features to meet specific system requirements.
5. Pin-Compatible Family. This includes the AD9212 (10-bit) and AD9222 (12-bit).

Rev. E

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Fax: 781.461.3113

AD9252* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9252 Evaluation Board

DOCUMENTATION

Application Notes

- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9252: Octal, 14-Bit, 50 MSPS, Serial LVDS, 1.8 V ADC Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog
- AD9252 IBIS Models

REFERENCE MATERIALS

Customer Case Studies

- National Instruments Case Study

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9252 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9252 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

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Submit feedback for this data sheet.

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SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 1.

		AD9252-50			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full		±1	±8	mV
Offset Matching	Full		±3	±8	mV
Gain Error	Full		±1.5	±2.5	% FS
Gain Matching	Full		±0.3	±0.7	% FS
Differential Nonlinearity (DNL)	Full		±0.4	±1	LSB
Integral Nonlinearity (INL)	Full		±1.5	±4	LSB
TEMPERATURE DRIFT					
Offset Error	Full		±2		ppm/°C
Gain Error	Full		±17		ppm/°C
Reference Voltage (1 V Mode)	Full		±21		ppm/°C
REFERENCE					
Output Voltage Error (VREF = 1 V)	Full		±2	±30	mV
Load Regulation @ 1.0 mA (VREF = 1 V)	Full		3		mV
Input Resistance	Full		6		kΩ
ANALOG INPUTS					
Differential Input Voltage Range (VREF = 1 V)	Full		2		V p-p
Common-Mode Voltage	Full		AVDD/2		V
Differential Input Capacitance	Full		7		pF
Analog Bandwidth, Full Power	Full		325		MHz
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
IAVDD	Full		360	373.4	mA
IDRVDD	Full		55.5	58	mA
Total Power Dissipation (Including Output Drivers)	Full		748	773	mW
Power-Down Dissipation	Full		2	11	mW
Standby Dissipation[2]	Full		89		mW
CROSSTALK					
AIN = −0.5 dBFS	Full		−90		dB
Overrange[3]	Full		−90		dB

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Can be controlled via the SPI.
[3] Overrange condition is specific with 6 dB of the full-scale input range.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 2.

		AD9252-50			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 2.4 MHz	Full		73.2		dB
f_{IN} = 19.7 MHz	Full	71	73		dB
f_{IN} = 35 MHz	Full		72.7		dB
f_{IN} = 70 MHz	Full		71		dB
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)					
f_{IN} = 2.4 MHz	Full		72.5		dB
f_{IN} = 19.7 MHz	Full	70.2	72.2		dB
f_{IN} = 35 MHz	Full		72		dB
f_{IN} = 70 MHz	Full		70.5		dB
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 2.4 MHz	Full		11.87		Bits
f_{IN} = 19.7 MHz	Full	11.5	11.84		Bits
f_{IN} = 35 MHz	Full		11.79		Bits
f_{IN} = 70 MHz	Full		11.5		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 2.4 MHz	Full		85		dBc
f_{IN} = 19.7 MHz	Full	73	84		dBc
f_{IN} = 35 MHz	Full		83		dBc
f_{IN} = 70 MHz	Full		79		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 2.4 MHz	Full		−85		dBc
f_{IN} = 19.7 MHz	Full		−84	−73	dBc
f_{IN} = 35 MHz	Full		−83		dBc
f_{IN} = 70 MHz	Full		−79		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD)					
f_{IN} = 2.4 MHz	Full		−90		dBc
f_{IN} = 19.7 MHz	Full		−90	−80	dBc
f_{IN} = 35 MHz	Full		−90		dBc
f_{IN} = 70 MHz	Full		−89		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS					
f_{IN1} = 15 MHz, f_{IN2} = 16 MHz	25°C		80.0		dBc
f_{IN1} = 70 MHz, f_{IN2} = 71 MHz	25°C		80.0		dBc

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 3.

		AD9252-50			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
LOGIC INPUTS (PDWN, SCLK/DTP)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		70		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (SDIO/ODM)					
Logic 1 Voltage	Full	1.2		DRVDD + 0.3	V
Logic 0 Voltage	Full	0		0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC OUTPUT (SDIO/ODM)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (D + x, D − x), (ANSI-644)					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V
Output Coding (Default)			Offset binary		
DIGITAL OUTPUTS (D + x, D − x), (LOW POWER, REDUCED SIGNAL OPTION)					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	V
Output Coding (Default)			Offset binary		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] This is specified for LVDS and LVPECL only.
[3] This is specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, unless otherwise noted.

Table 4.

		AD9252-50			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Unit**
CLOCK[2]					
Maximum Clock Rate	Full	50			MSPS
Minimum Clock Rate	Full			10	MSPS
Clock Pulse Width High (t_{EH})	Full		10.0		ns
Clock Pulse Width Low (t_{EL})	Full		10.0		ns
OUTPUT PARAMETERS[2, 3]					
Propagation Delay (t_{PD})	Full	1.5	2.3	3.1	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO Propagation Delay (t_{FCO})	Full	1.5	2.3	3.1	ns
DCO Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/28)		ns
DCO to Data Delay (t_{DATA})[4]	Full	(t_{SAMPLE}/28) − 300	(t_{SAMPLE}/28)	(t_{SAMPLE}/28) + 300	ps
DCO to FCO Delay (t_{FRAME})[4]	Full	(t_{SAMPLE}/28) − 300	(t_{SAMPLE}/28)	(t_{SAMPLE}/28) + 300	ps
Data-to-Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±50	±200	ps
Wake-Up Time (Standby)	25°C		600		ns
Wake-Up Time (Power-Down)	25°C		375		µs
Pipeline Latency	Full		8		CLK cycles
APERTURE					
Aperture Delay (t_A)	25°C		750		ps
Aperture Uncertainty (Jitter)	25°C		<1		ps rms
Out-of-Range Recovery Time	25°C		1		CLK cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Can be adjusted via the SPI.
[3] Measurements were made using a part soldered to FR-4 material.
[4] t_{SAMPLE}/28 is based on the number of bits divided by 2 because the delays are based on half duty cycles.

TIMING DIAGRAMS

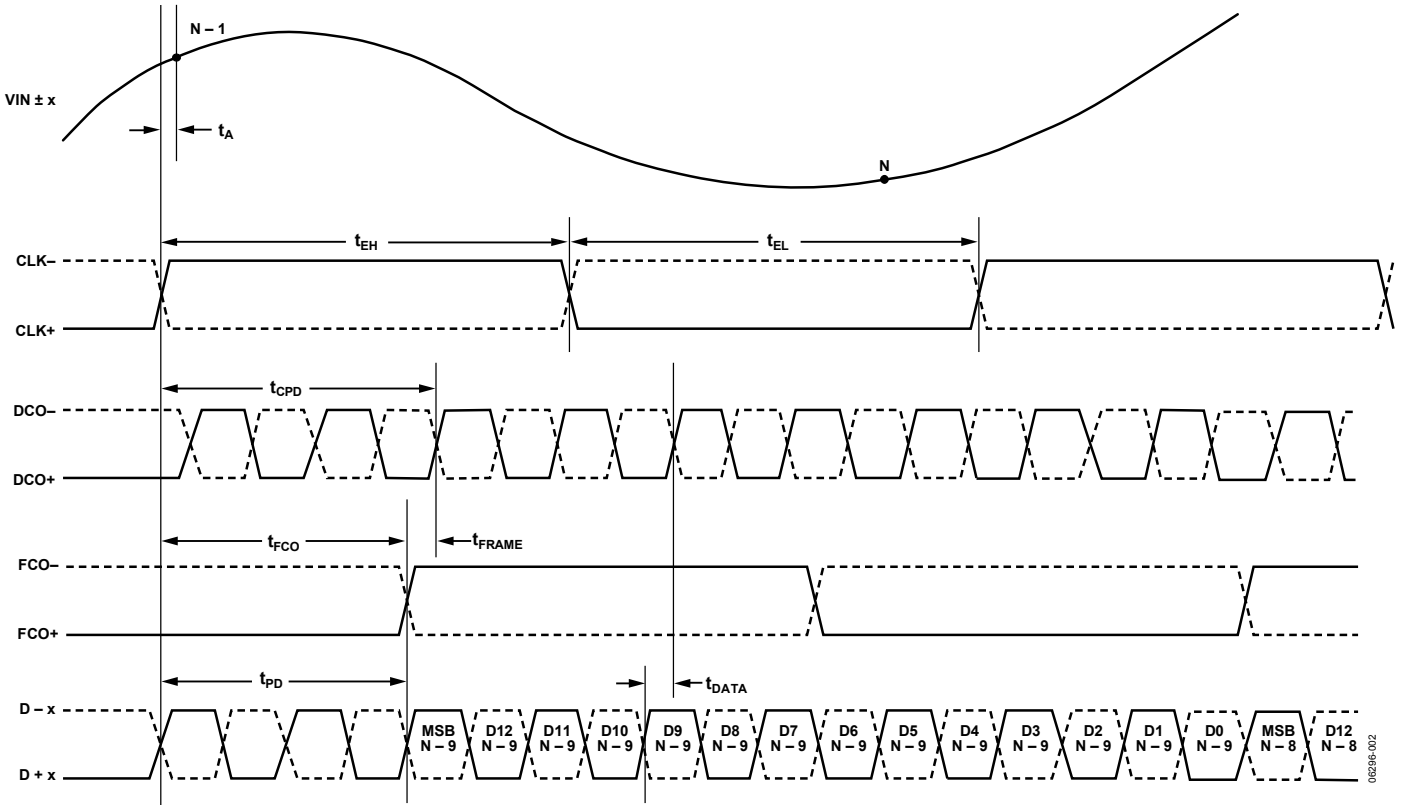

Figure 2. 14-Bit Data Serial Stream (Default), MSB First

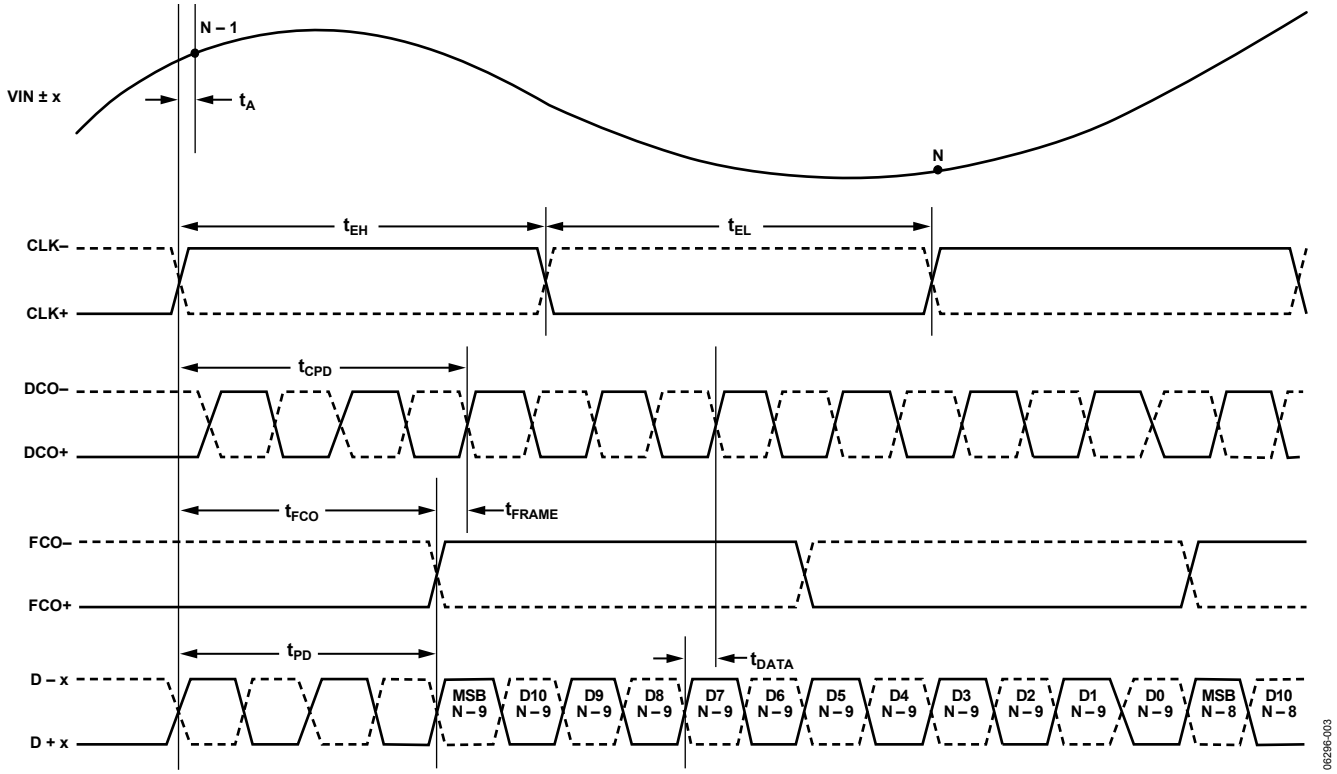

Figure 3. 12-Bit Data Serial Stream, MSB First

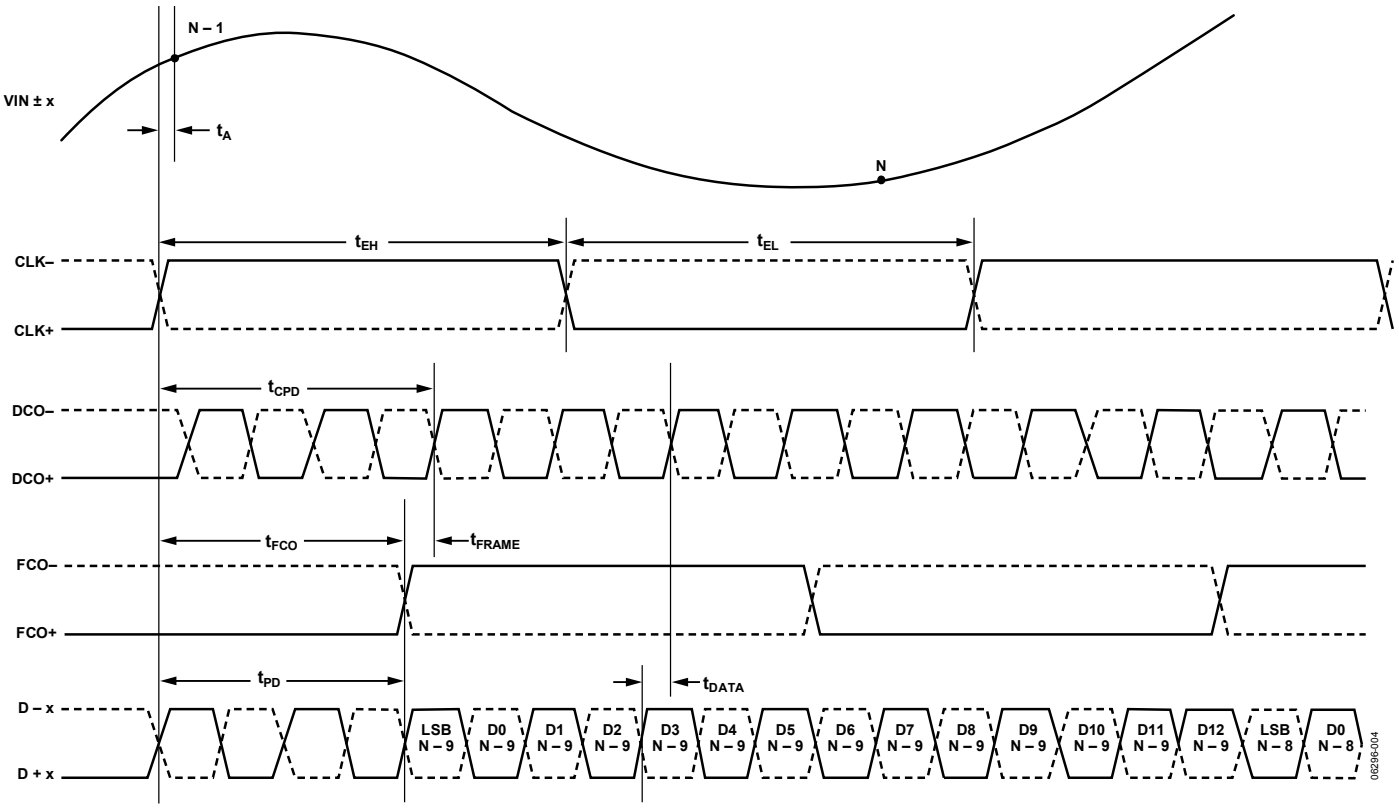

Figure 4. 14-Bit Data Serial Stream, LSB First

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
ELECTRICAL		
AVDD	AGND	−0.3 V to +2.0 V
DRVDD	DRGND	−0.3 V to +2.0 V
AGND	DRGND	−0.3 V to +0.3 V
AVDD	DRVDD	−2.0 V to +2.0 V
Digital Outputs (D + x, D − x, DCO+, DCO−, FCO+, FCO−)	DRGND	−0.3 V to +2.0 V
CLK+, CLK−	AGND	−0.3 V to +3.9 V
VIN + x, VIN − x	AGND	−0.3 V to +2.0 V
SDIO/ODM	AGND	−0.3 V to +2.0 V
PDWN, SCLK/DTP, CSB	AGND	−0.3 V to +3.9 V
REFT, REFB, RBIAS	AGND	−0.3 V to +2.0 V
VREF, SENSE	AGND	−0.3 V to +2.0 V
ENVIRONMENTAL		
Operating Temperature Range (Ambient)		−40°C to +85°C
Storage Temperature Range (Ambient)		−65°C to +150°C
Maximum Junction Temperature		150°C
Lead Temperature (Soldering, 10 sec)		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE

Table 6.

Air Flow Velocity (m/s)	θ_{JA}[1]	θ_{JB}	θ_{JC}	Unit
0.0	17.7			°C/W
1.0	15.5	8.7	0.6	°C/W
2.5	13.9			°C/W

[1] θ_{JA} for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

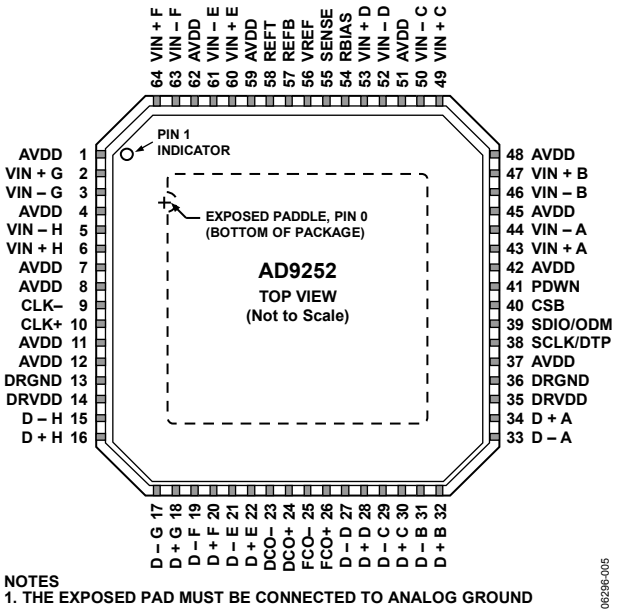

Figure 5. 64-Lead LFCSP Pin Configuration, Top View

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND	Analog Ground (Exposed Paddle)
1, 4, 7, 8, 11, 12, 37, 42, 45, 48, 51, 59, 62	AVDD	1.8 V Analog Supply
13, 36	DRGND	Digital Output Driver Ground
14, 35	DRVDD	1.8 V Digital Output Driver Supply
2	VIN + G	ADC G Analog Input True
3	VIN – G	ADC G Analog Input Complement
5	VIN – H	ADC H Analog Input Complement
6	VIN + H	ADC H Analog Input True
9	CLK–	Input Clock Complement
10	CLK+	Input Clock True
15	D – H	ADC H Digital Output Complement
16	D + H	ADC H Digital Output True
17	D – G	ADC G Digital Output Complement
18	D + G	ADC G Digital Output True
19	D – F	ADC F Digital Output Complement
20	D + F	ADC F Digital Output True
21	D – E	ADC E Digital Output Complement
22	D + E	ADC E Digital Output True
23	DCO–	Data Clock Digital Output Complement
24	DCO+	Data Clock Digital Output True
25	FCO–	Frame Clock Digital Output Complement
26	FCO+	Frame Clock Digital Output True
27	D – D	ADC D Digital Output Complement
28	D + D	ADC D Digital Output True
29	D – C	ADC C Digital Output Complement
30	D + C	ADC C Digital Output True
31	D – B	ADC B Digital Output Complement

Pin No.	Mnemonic	Description
32	D + B	ADC B Digital Output True
33	D − A	ADC A Digital Output Complement
34	D + A	ADC A Digital Output True
38	SCLK/DTP	Serial Clock/Digital Test Pattern
39	SDIO/ODM	Serial Data Input-Output/Output Driver Mode
40	CSB	Chip Select Bar
41	PDWN	Power-Down
43	VIN + A	ADC A Analog Input True
44	VIN − A	ADC A Analog Input Complement
46	VIN − B	ADC B Analog Input Complement
47	VIN + B	ADC B Analog Input True
49	VIN + C	ADC C Analog Input True
50	VIN − C	ADC C Analog Input Complement
52	VIN − D	ADC D Analog Input Complement
53	VIN + D	ADC D Analog Input True
54	RBIAS	External Resistor to Set the Internal ADC Core Bias Current
55	SENSE	Reference Mode Selection
56	VREF	Voltage Reference Input/Output
57	REFB	Negative Differential Reference
58	REFT	Positive Differential Reference
60	VIN + E	ADC E Analog Input True
61	VIN − E	ADC E Analog Input Complement
63	VIN − F	ADC F Analog Input Complement
64	VIN + F	ADC F Analog Input True

EQUIVALENT CIRCUITS

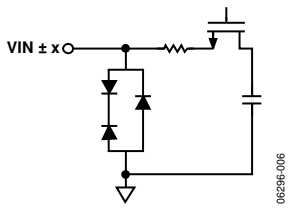

Figure 6. Equivalent Analog Input Circuit

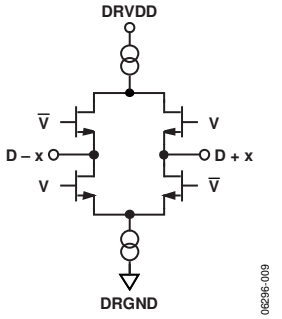

Figure 9. Equivalent Digital Output Circuit

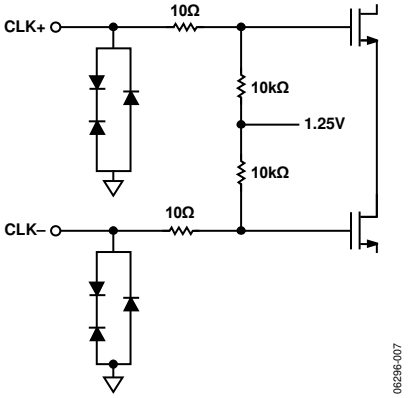

Figure 7. Equivalent Clock Input Circuit

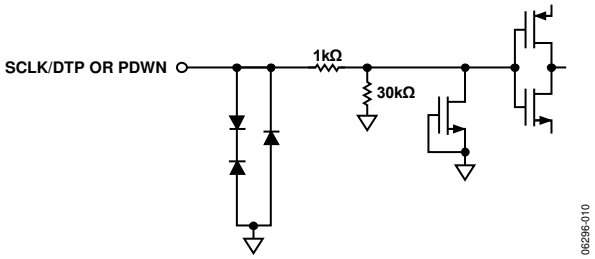

Figure 10. Equivalent SCLK/DTP or PDWN Input Circuit

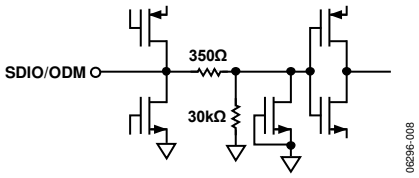

Figure 8. Equivalent SDIO/ODM Input Circuit

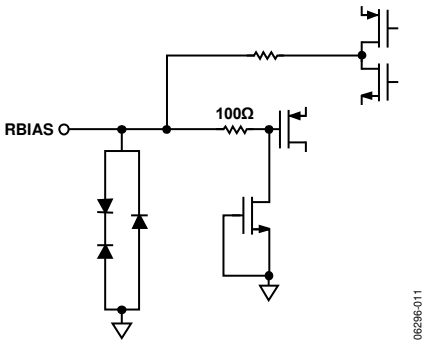

Figure 11. Equivalent RBIAS Circuit

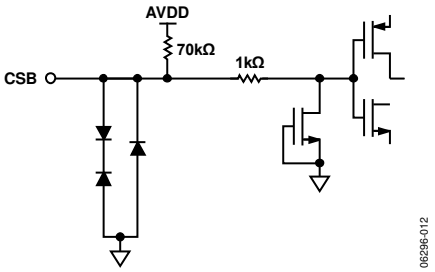

Figure 12. Equivalent CSB Input Circuit

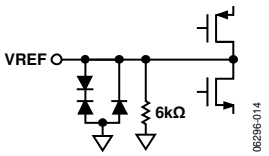

Figure 14. Equivalent VREF Circuit

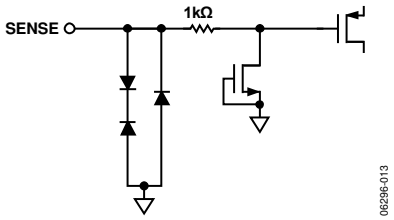

Figure 13. Equivalent SENSE Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

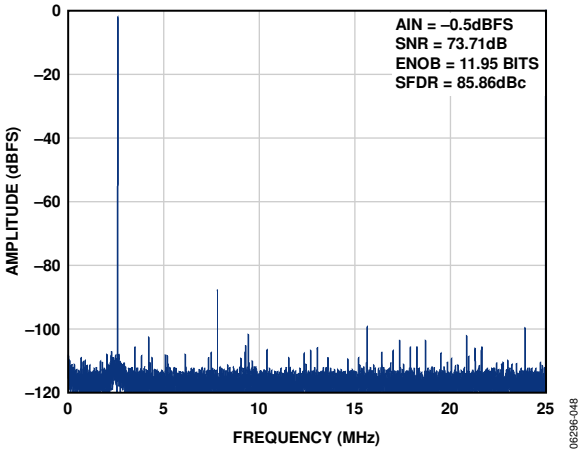

Figure 15. Single-Tone 32k FFT with f_{IN} = 2.3 MHz, f_{SAMPLE} = 50 MSPS

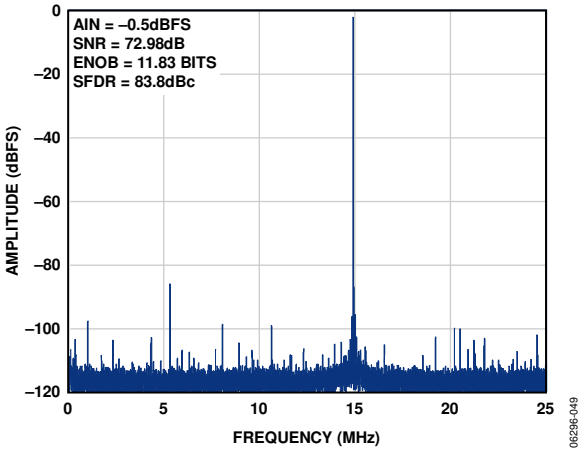

Figure 16. Single-Tone 32k FFT with f_{IN} = 35 MHz, f_{SAMPLE} = 50 MSPS

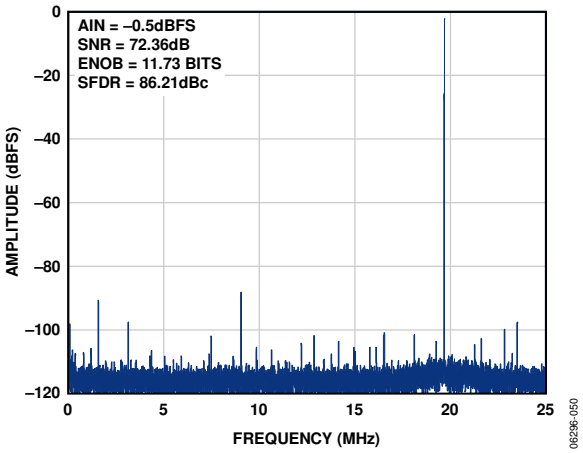

Figure 17. Single-Tone 32k FFT with f_{IN} = 70 MHz, f_{SAMPLE} = 50 MSPS

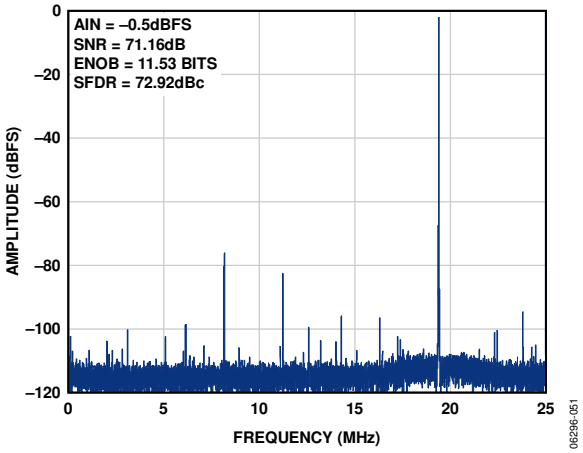

Figure 18. Single-Tone 32k FFT with f_{IN} = 120 MHz, f_{SAMPLE} = 50 MSPS

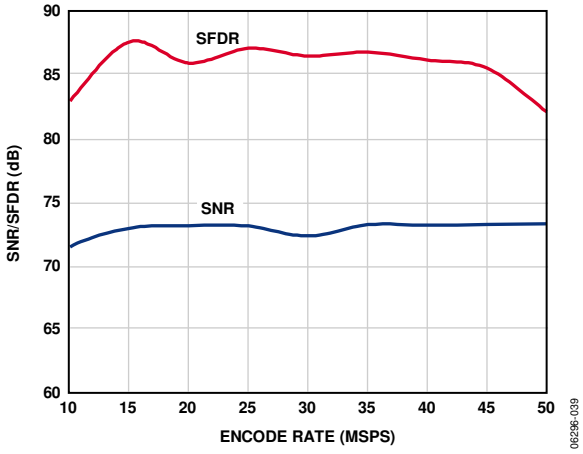

Figure 19. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 10.3 MHz, AD9252-50

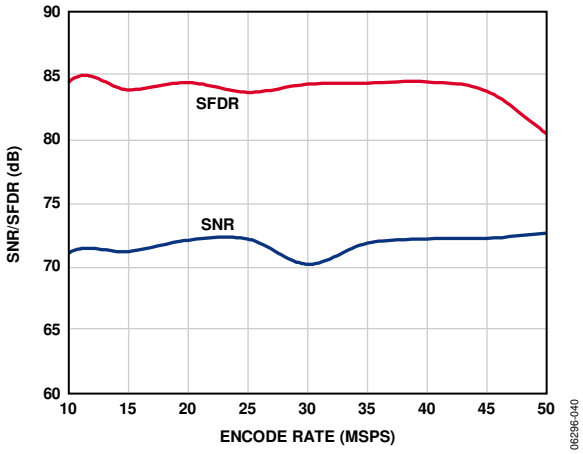

Figure 20. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 19.7 MHz, AD9252-50

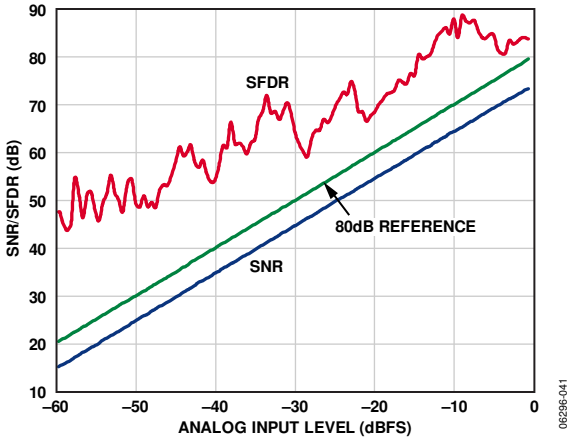

Figure 21. SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz, f_{SAMPLE} = 50 MSPS

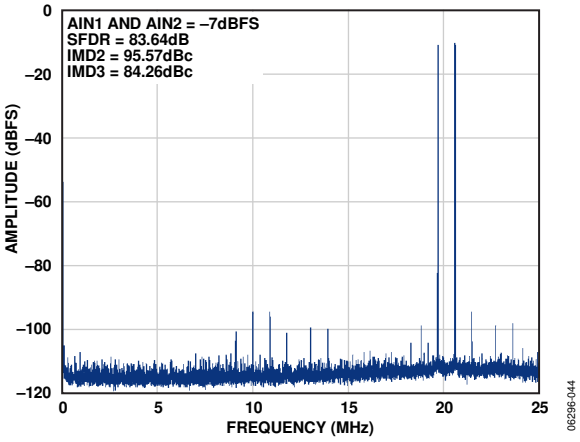

Figure 24. Two-Tone 32k FFT with f_{IN1} = 70 MHz and f_{IN2} = 71 MHz, f_{SAMPLE} = 50 MSPS

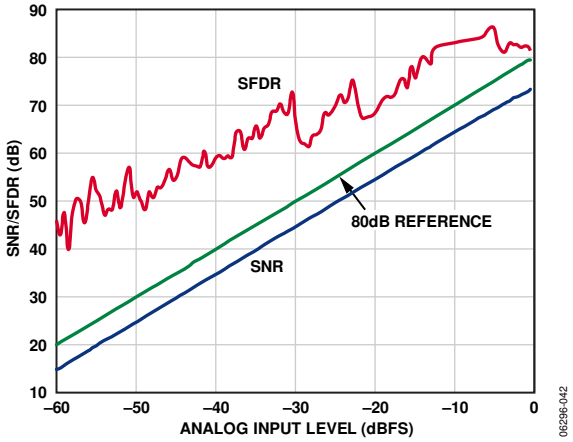

Figure 22. SNR/SFDR vs. Analog Input Level, f_{IN} = 19.7 MHz, f_{SAMPLE} = 50 MSPS

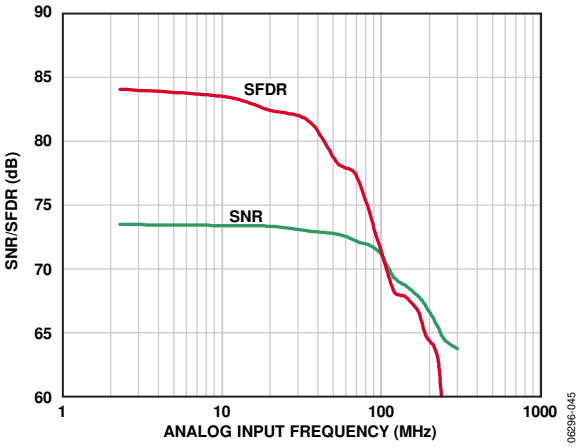

Figure 25. SNR/SFDR vs. f_{IN}, f_{SAMPLE} = 50 MSPS

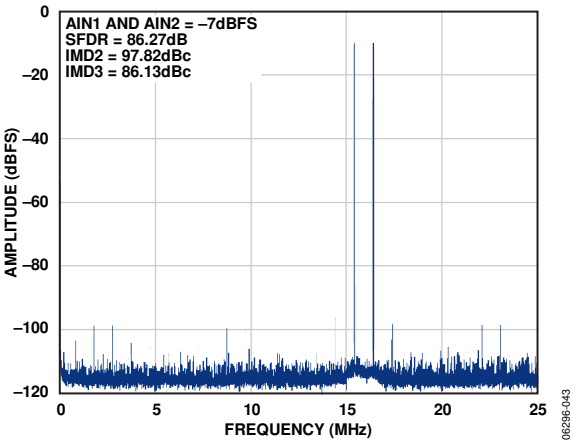

Figure 23. Two-Tone 32k FFT with f_{IN1} = 15 MHz and f_{IN2} = 16 MHz, f_{SAMPLE} = 50 MSPS

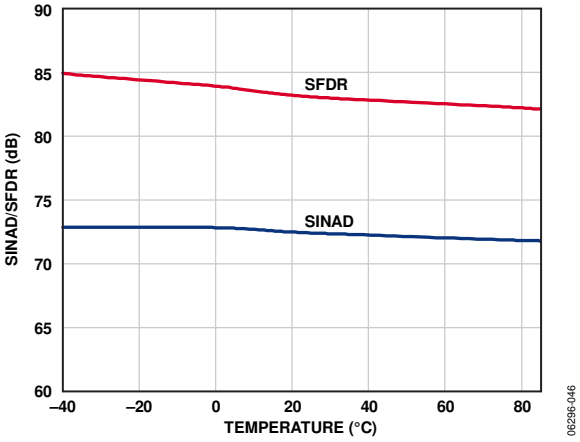

Figure 26. SINAD/SFDR vs. Temperature, f_{IN} = 19.7 MHz, f_{SAMPLE} = 50 MSPS

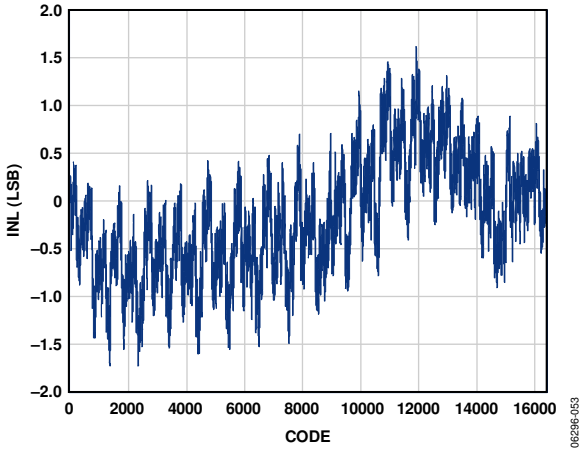

Figure 27. INL, f_{IN} = 2.3 MHz, f_{SAMPLE} = 50 MSPS

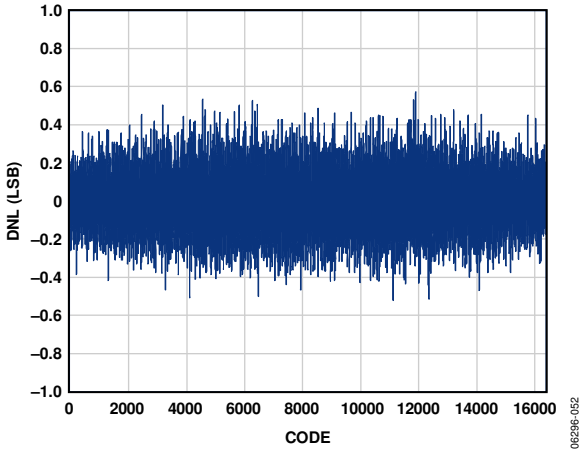

Figure 28. DNL, f_{IN} = 2.3 MHz, f_{SAMPLE} = 50 MSPS

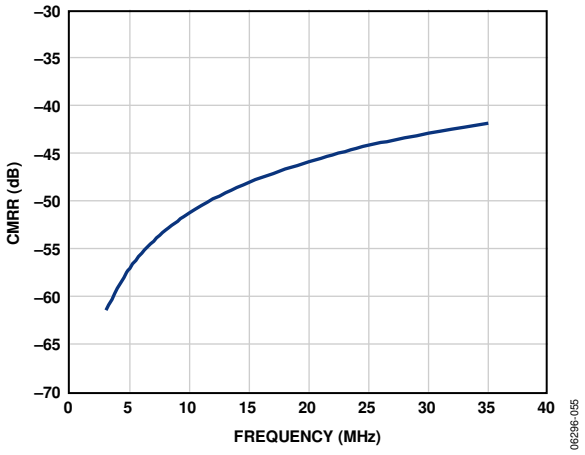

Figure 29. CMRR vs. Frequency, f_{SAMPLE} = 50 MSPS

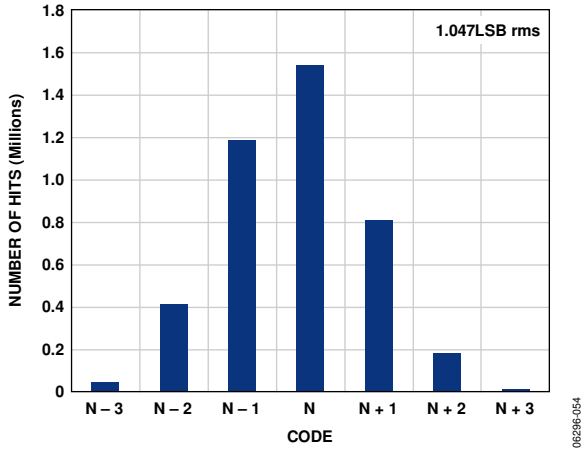

Figure 30. Input-Referred Noise Histogram, f_{SAMPLE} = 50 MSPS

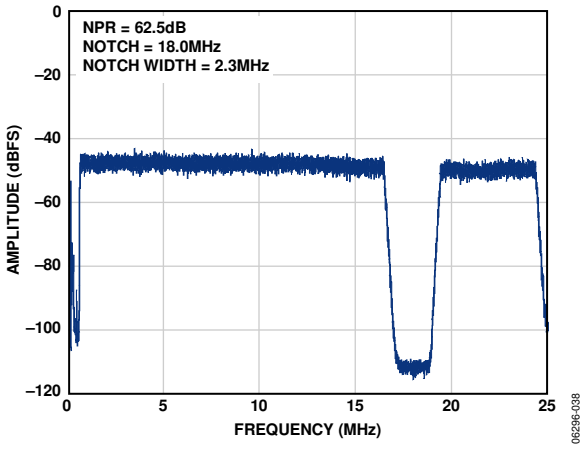

Figure 31. Noise Power Ratio (NPR), f_{SAMPLE} = 50 MSPS

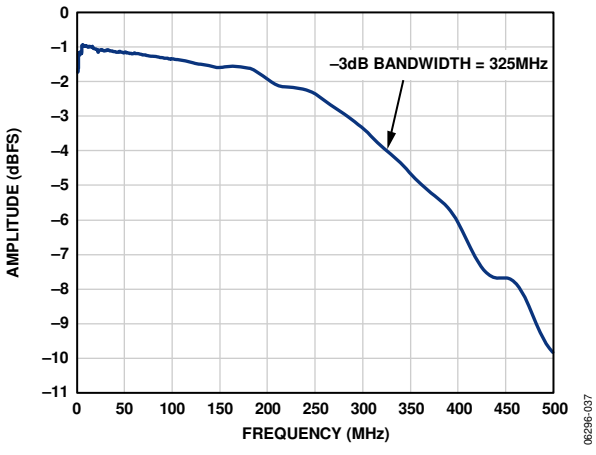

Figure 32. Full-Power Bandwidth vs. Frequency, f_{SAMPLE} = 50 MSPS

THEORY OF OPERATION

The AD9252 architecture consists of a pipelined ADC divided into three sections: a 4-bit first stage followed by eight 1.5-bit stages and a 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9252 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. An input common-mode voltage of midsupply minimizes signal-dependent errors and provides optimum performance.

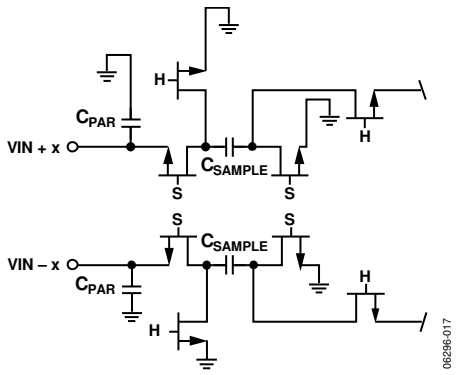

Figure 33. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 33). When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low-Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and therefore achieve the maximum bandwidth of the ADC. Such use of low-Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

The analog inputs of the AD9252 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 34 and Figure 35.

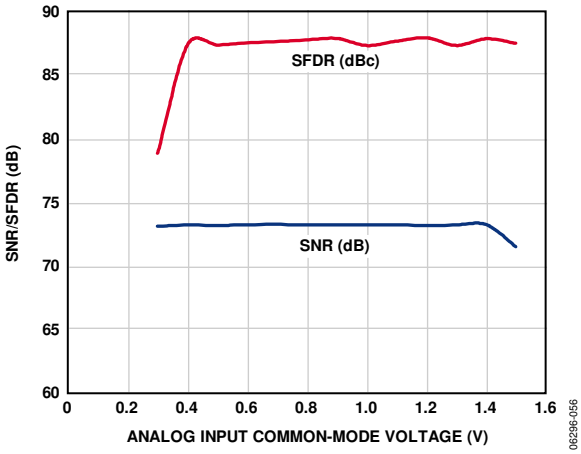

Figure 34. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 2.3 MHz, f_{SAMPLE} = 50 MSPS

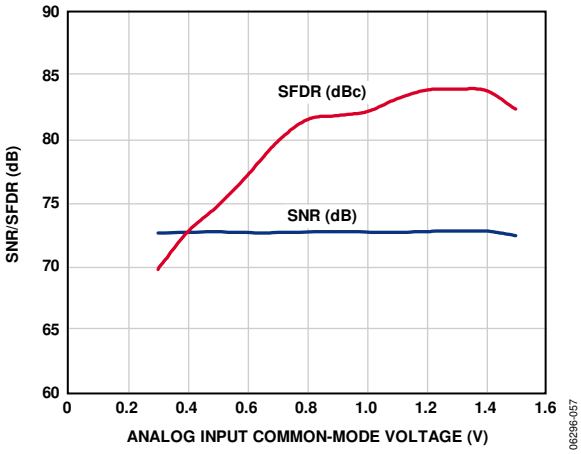

Figure 35. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 35 MHz, f_{SAMPLE} = 50 MSPS

For best dynamic performance, the source impedances driving VIN + x and VIN − x should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates the positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as

$$REFT = 1/2\ (AVDD + VREF)$$
$$REFB = 1/2\ (AVDD - VREF)$$
$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from these equations that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9252, the largest input span available is 2 V p-p.

Differential Input Configurations

There are several ways to drive the AD9252 either actively or passively; however, optimum performance is achieved by driving the analog input differentially. For example, using the AD8334 differential driver to drive the AD9252 provides excellent performance and a flexible interface to the ADC (see Figure 39) for baseband applications. This configuration is commonly used for medical ultrasound systems.

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 36 and Figure 37), because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9252.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

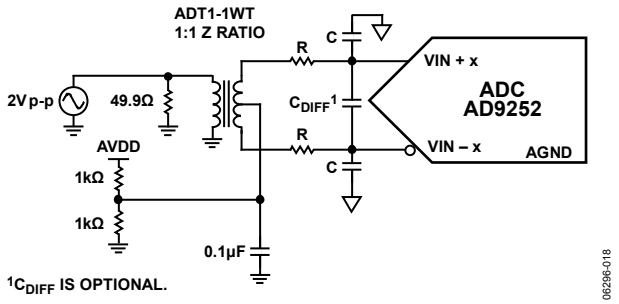

Figure 36. Differential Transformer-Coupled Configuration for Baseband Applications

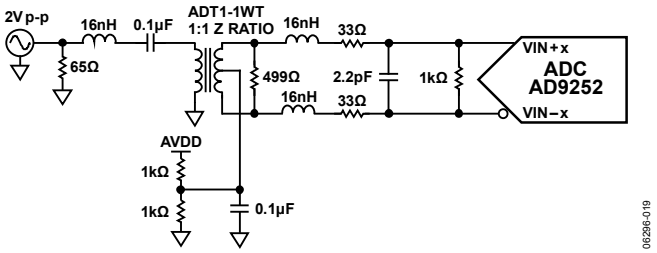

Figure 37. Differential Transformer-Coupled Configuration for IF Applications

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the application requires a single-ended input configuration, ensure that the source impedances on each input are well matched in order to achieve the best possible performance. A full-scale input of 2 V p-p can still be applied to the ADC's VIN + x pin while the VIN − x pin is terminated. Figure 38 details a typical single-ended input configuration.

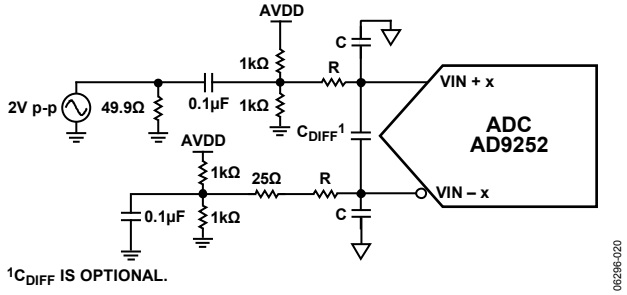

Figure 38. Single-Ended Input Configuration

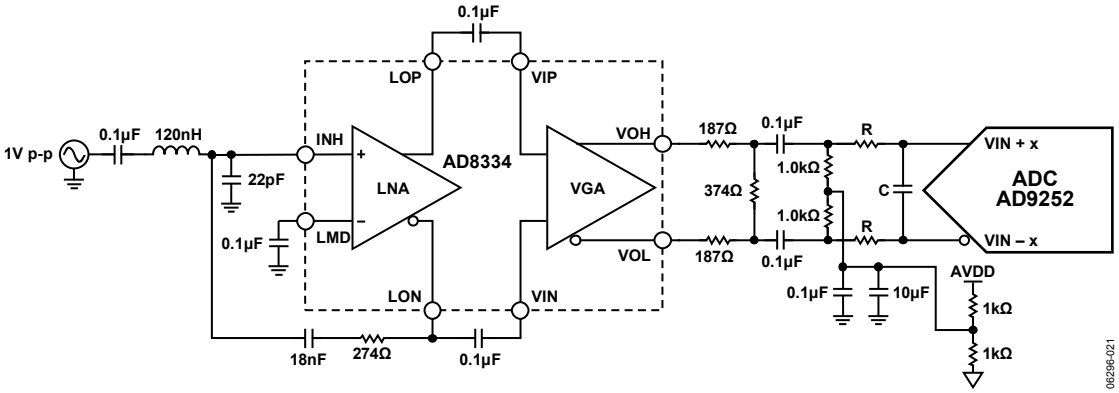

Figure 39. Differential Input Configuration Using the AD8334

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9252 sample clock inputs (CLK+ and CLK–) should be clocked with a differential signal. This signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally and require no additional biasing.

Figure 40 shows the preferred method for clocking the AD9252. The low jitter clock source is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9252 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9252, and it preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

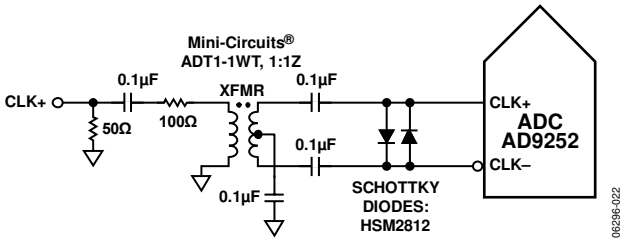

Figure 40. Transformer-Coupled Differential Clock

Another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 41. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

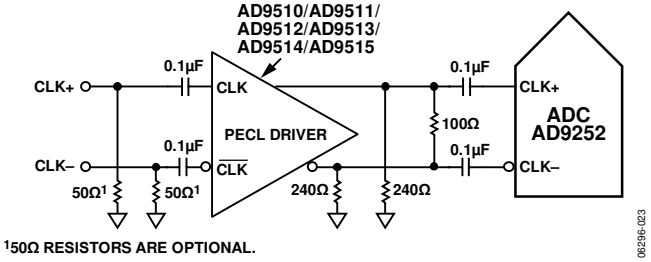

Figure 41. Differential PECL Sample Clock

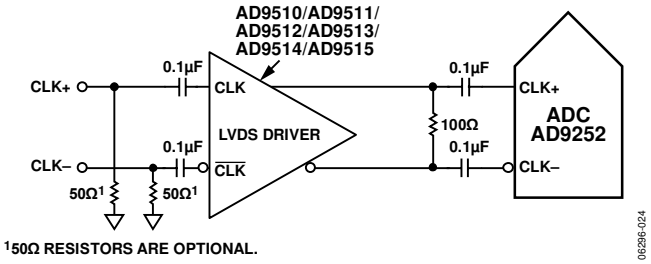

Figure 42. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be driven directly from a CMOS gate, and the CLK– pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 43). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages of up to 3.3 V, making the selection of the drive logic voltage very flexible.

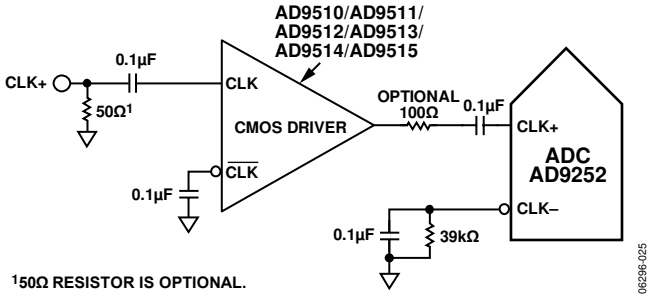

Figure 43. Single-Ended 1.8 V CMOS Sample Clock

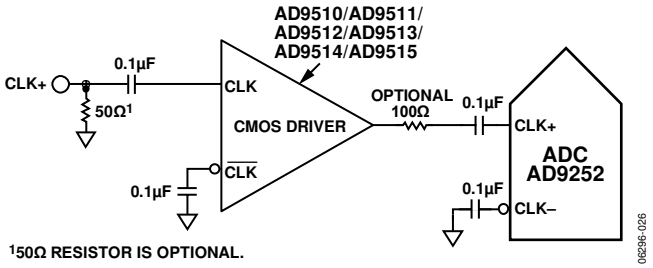

Figure 44. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9252 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9252. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See the Memory Map section for more details on using this feature.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20 \times \log 10(1/2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 45).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9252. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

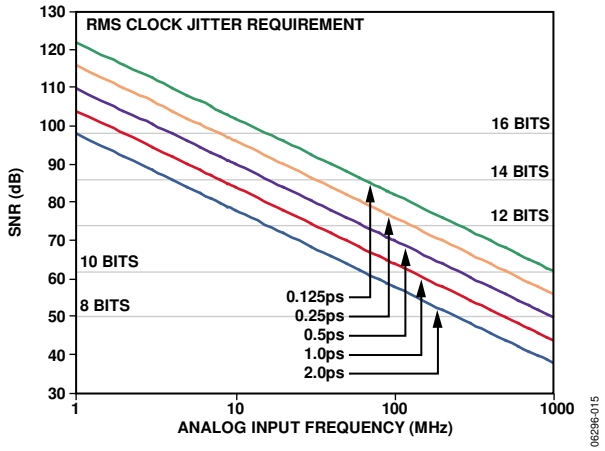

Figure 45. Ideal SNR vs. Input Frequency and Jitter

Power Dissipation and Power-Down Mode

As shown in Figure 46, the power dissipated by the AD9252 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

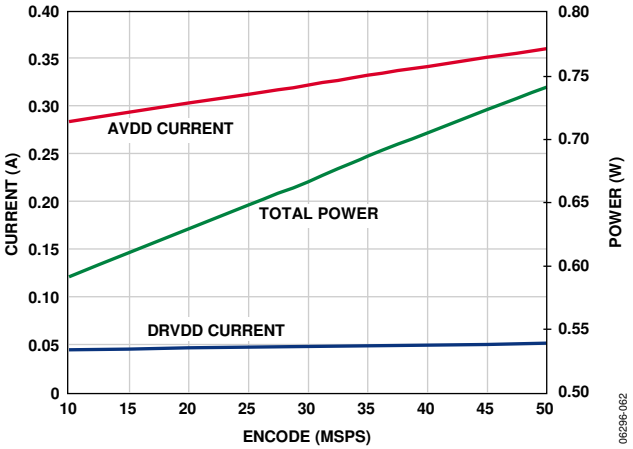

Figure 46. Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz, f_{SAMPLE} = 50 MSPS

By asserting the PDWN pin high, the AD9252 is placed into power-down mode. In this state, the ADC typically dissipates 11 mW. During power-down, the LVDS output drivers are placed into a high impedance state. The AD9252 returns to normal operating mode when the PDWN pin is pulled low. This pin is both 1.8 V and 3.3 V tolerant.

In power-down mode, low power dissipation is achieved by shutting down the reference, reference buffer, PLL, and biasing networks. The decoupling capacitors on REFT and REFB are discharged when entering power-down mode and must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in the power-down mode: shorter cycles result in proportionally shorter wake-up times. With the recommended 0.1 µF and 4.7 µF decoupling capacitors on REFT and REFB, approximately 1 sec is required to fully discharge the reference buffer decoupling capacitors and approximately 375 µs is required to restore full operation.

There are several other power-down options available when using the SPI. The user can individually power down each channel or put the entire device into standby mode. The latter option allows the user to keep the internal PLL powered when fast wake-up times (~600 ns) are required. See the Memory Map section for more details on using these features.

Digital Outputs and Timing

The AD9252 differential outputs conform to the ANSI-644 LVDS standard by default upon power-up. This can be changed to a low power, reduced signal option (similar to the IEEE 1596.3 standard) via the SDIO/ODM pin or the SPI. This LVDS standard can further reduce the overall power dissipation of the device by approximately 36 mW. See the SDIO/ODM Pin section or Table 16 in the Memory Map section for more information. The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver.

The AD9252 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. If there is no far-end receiver termination or there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be no longer than 24 inches and that the differential output traces be kept close together and at equal lengths. An example of the FCO and data stream when the AD9252 is used with traces of proper length and position is shown in Figure 47.

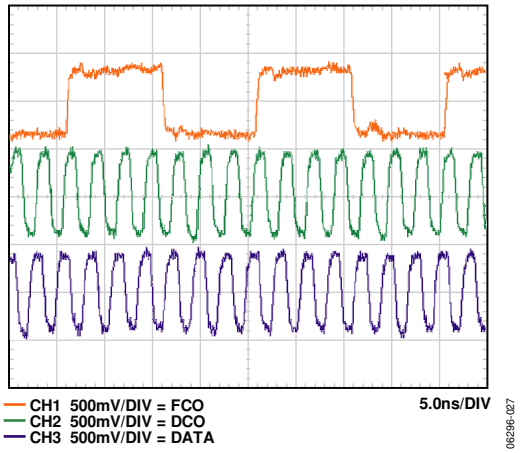

Figure 47. LVDS Output Timing Example in ANSI-644 Mode (Default)

An example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths less than 24 inches on standard FR-4 material is shown in Figure 48. Figure 49 shows an example of the trace length exceeding 24 inches on standard FR-4 material. Notice that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position. It is the user's responsibility to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches. Additional SPI options allow the user to further increase the internal termination (increasing the current) of all eight outputs in order to drive longer trace lengths (see Figure 50). Even though this produces sharper rise and fall times on the data edges and is less prone to bit errors, the power dissipation of the DRVDD supply increases when this option is used. In addition, notice in Figure 50 that the histogram has improved.

In cases that require increased driver strength to the DCO± and FCO± outputs because of load mismatch, Register 0x15 allows the user to increase the drive strength by 2×. To do this, first set the appropriate bit in Register 0x05. Note that this feature cannot be used with Bit 4 and Bit 5 in Register 0x15. Bit 4 and Bit 5 take precedence over this feature. See the Memory Map section for more details.

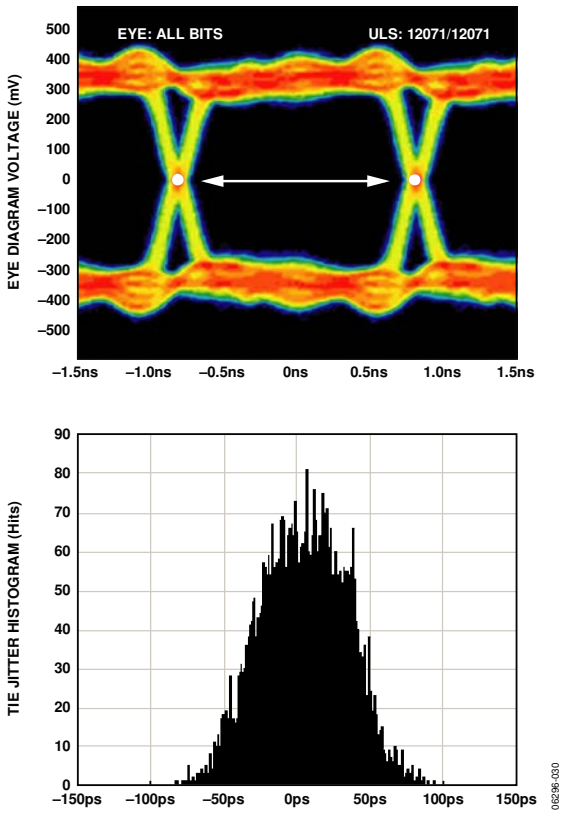

Figure 48. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths Less Than 24 Inches on Standard FR-4

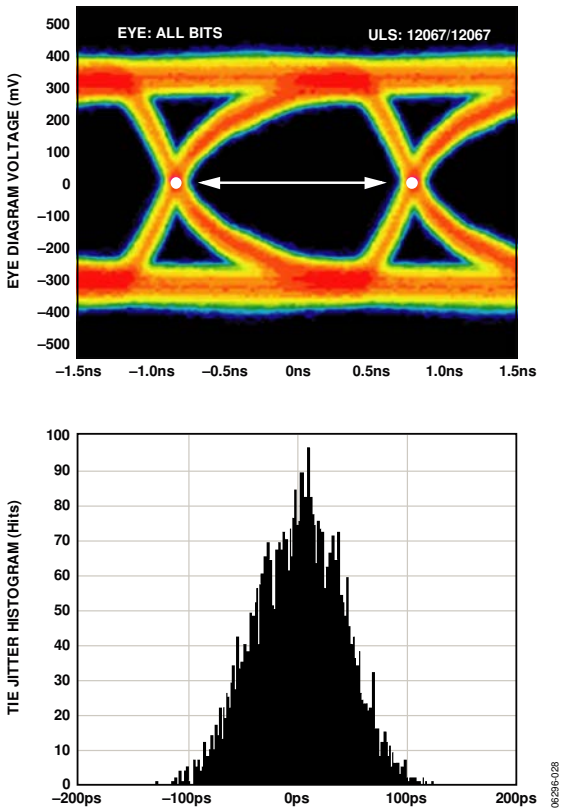

Figure 49. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths Greater Than 24 Inches on Standard FR-4

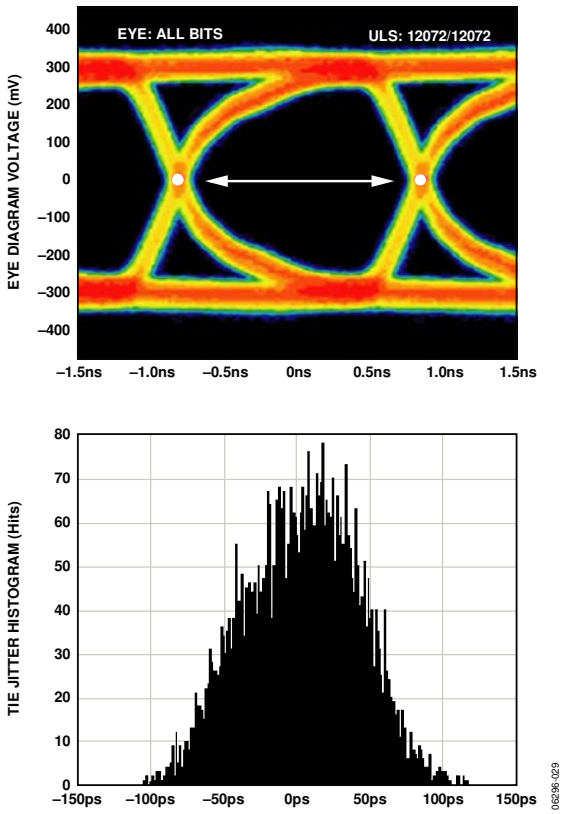

Figure 50. Data Eye for LVDS Outputs in ANSI-644 Mode with 100 Ω Termination On and Trace Lengths Greater Than 24 Inches on Standard FR-4

The format of the output data is offset binary by default. An example of the output coding format can be found in Table 8. To change the output data format to twos complement, see the Memory Map section.

Table 8. Digital Output Coding

Code	(VIN + x) − (VIN − x), Input Span = 2 V p-p (V)	Digital Output Offset Binary (D13 ... D0)
16383	+1.00	11 1111 1111 1111
8192	0.00	10 0000 0000 0000
8191	−0.000122	01 1111 1111 1111
0	−1.00	00 0000 0000 0000

Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to 14 bits times the sample clock rate, with a maximum of 700 Mbps (14 bits × 50 MSPS = 700 Mbps). The lowest typical conversion rate is 10 MSPS. However, if lower sample rates are required for a specific application, the PLL can be set up via the SPI to allow encode rates as low as 5 MSPS. See the Memory Map section for information about enabling this feature.

Two output clocks are provided to assist in capturing data from the AD9252. The DCO is used to clock the output data and is equal to seven times the sample clock (CLK) rate. Data is clocked out of the AD9252 and must be captured on the rising and falling edges of the DCO that supports double data rate (DDR) capturing. The FCO is used to signal the start of a new output byte and is equal to the sample clock rate. See the timing diagram shown in Figure 2 for more information.

Table 9. Flexible Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select
0000	Off (default)	N/A	N/A	N/A
0001	Midscale short	1000 0000 (8-bit) 10 0000 0000 (10-bit) 1000 0000 0000 (12-bit) 10 0000 0000 0000 (14-bit)	Same	Yes
0010	+Full-scale short	1111 1111 (8-bit) 11 1111 1111 (10-bit) 1111 1111 1111 (12-bit) 11 1111 1111 1111 (14-bit)	Same	Yes
0011	−Full-scale short	0000 0000 (8-bit) 00 0000 0000 (10-bit) 0000 0000 0000 (12-bit) 00 0000 0000 0000 (14-bit)	Same	Yes
0100	Checkerboard	1010 1010 (8-bit) 10 1010 1010 (10-bit) 1010 1010 1010 (12-bit) 10 1010 1010 1010 (14-bit)	0101 0101 (8-bit) 01 0101 0101 (10-bit) 0101 0101 0101 (12-bit) 01 0101 0101 0101 (14-bit)	No
0101	PN sequence long[1]	N/A	N/A	Yes
0110	PN sequence short[1]	N/A	N/A	Yes
0111	One-/zero-word toggle	1111 1111 (8-bit) 11 1111 1111 (10-bit) 1111 1111 1111 (12-bit) 11 1111 1111 1111 (14-bit)	0000 0000 (8-bit) 00 0000 0000 (10-bit) 0000 0000 0000 (12-bit) 00 0000 0000 0000 (14-bit)	No
1000	User input	Register 0x19 and Register 0x1A	Register 0x1B and Register 0x1C	No
1001	1-/0-bit toggle	1010 1010 (8-bit) 10 1010 1010 (10-bit) 1010 1010 1010 (12-bit) 10 1010 1010 1010 (14-bit)	N/A	No
1010	1× sync	0000 1111 (8-bit) 00 0001 1111 (10-bit) 0000 0011 1111 (12-bit) 00 0000 0111 1111 (14-bit)	N/A	No
1011	One bit high	1000 0000 (8-bit) 10 0000 0000 (10-bit) 1000 0000 0000 (12-bit) 10 0000 0000 0000 (14-bit)	N/A	No
1100	Mixed frequency	1010 0011 (8-bit) 10 0110 0011 (10-bit) 1010 0011 0011 (12-bit) 10 1000 0110 0111 (14-bit)	N/A	No

[1] All test mode options except PN sequence short and PN sequence long can support 8- to 14-bit word lengths in order to verify data capture to the receiver.

When the SPI is used, the DCO phase can be adjusted in 60° increments relative to the data edge. This enables the user to refine system timing margins if required. The default DCO+ and DCO– timing, as shown in Figure 2, is 90° relative to the output data edge.

An 8-, 10-, and 12-bit serial stream can also be initiated from the SPI. This allows the user to implement different serial stream to test the device's compatibility with lower and higher resolution systems. When changing the resolution to an 8-, 10-, or 12-bit serial stream, the data stream is shortened. See Figure 3 for a 12-bit example.

When the SPI is used, the data outputs can be inverted from their nominal state. This is not to be confused with inverting the serial stream to an LSB-first mode. In default mode, as shown in Figure 2, the MSB is first in the data output serial stream. However, this can be inverted so that the LSB is first in the data output serial stream (see Figure 4).

There are 12 digital output test pattern options available that can be initiated through the SPI. This feature is useful when validating receiver capture and timing. Refer to Table 9 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern chosen. Note that some patterns do not adhere to the data format select option. In addition, customer user-defined test patterns can be assigned in the 0x19, 0x1A, 0x1B, and 0x1C register addresses. All test mode options except PN sequence short and PN sequence long can support 8- to 14-bit word lengths in order to verify data capture to the receiver.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ or 511 bits. A description of the PN sequence and how it is generated can be found in Section 5.1 of the ITU-T 0.150 (05/96) standard. The only difference is that the starting value must be a specific value instead of all 1s (see Table 10 for the initial values).

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ or 8,388,607 bits. A description of the PN sequence and how it is generated can be found in Section 5.6 of the ITU-T 0.150 (05/96) standard. The only differences are that the starting value must be a specific value instead of all 1s (see Table 10 for the initial values) and the AD9252 inverts the bit stream with relation to the ITU standard.

Table 10. PN Sequence

Sequence	Initial Value	First Three Output Samples (MSB First)
PN Sequence Short	0x0df	0x37e4, 0x3533, 0x0063
PN Sequence Long	0x26e028	0x191f, 0x35c2, 0x2359

SDIO/ODM Pin

The SDIO/ODM pin is for use in applications that do not require SPI mode operation. This pin can enable a low power, reduced signal option (similar to the IEEE 1596.3 reduced range link output standard) if it and the CSB pin are tied to AVDD during device power-up. This option should only be used when the digital output trace lengths are less than 2 inches from the LVDS receiver. When this option is used, the FCO, DCO, and outputs function normally, but the LVDS signal swing of all channels is reduced from 350 mV p-p to 200 mV p-p, allowing the user to further reduce the power on the DRVDD supply.

For applications where this pin is not used, it should be tied low. In this case, the device pin can be left open, and the 30 kΩ internal pull-down resistor pulls this pin low. This pin is only 1.8 V tolerant. If applications require this pin to be driven from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

Table 11. Output Driver Mode Pin Settings

Selected ODM	ODM Voltage	Resulting Output Standard	Resulting FCO and DCO
Normal Operation	AGND (10 kΩ pull-down resistor)	ANSI-644 (default)	ANSI-644 (default)
ODM	AVDD	Low power, reduced signal option	Low power, reduced signal option

SCLK/DTP Pin

The SCLK/DTP pin is for use in applications that do not require SPI mode operation. This pin can enable a single digital test pattern if it and the CSB pin are held high during device power-up. When the SCLK/DTP is tied to AVDD, the ADC channel outputs shift out the following pattern: 10 0000 0000 0000. The FCO and DCO function normally while all channels shift out the repeatable test pattern. This pattern allows the user to perform timing alignment adjustments among the FCO, DCO, and output data. For normal operation, this pin should be tied to AGND through a 10 kΩ resistor. This pin is both 1.8 V and 3.3 V tolerant.

Table 12. Digital Test Pattern Pin Settings

Selected DTP	DTP Voltage	Resulting D + x and D – x	Resulting FCO and DCO
Normal Operation	AGND (10 kΩ pull-down resistor)	Normal operation	Normal operation
DTP	AVDD	10 0000 0000 0000	Normal operation

Additional and custom test patterns can also be observed when commanded from the SPI port. Consult the Memory Map section for information about the options available.