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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Quad, 14-Bit, 80 MSPS/105 MSPS/125 MSPS Serial LVDS 1.8 V Analog-to-Digital Converter

Data Sheet **AD9253**

## FEATURES

- 1.8 V supply operation
- Low power: 110 mW per channel at 125 MSPS with scalable power options
- SNR = 74 dB (to Nyquist)
- SFDR = 90 dBc (to Nyquist)
- DNL = ±0.75 LSB (typical); INL = ±2.0 LSB (typical)
- Serial LVDS (ANSI-644, default) and low power, reduced signal option (similar to IEEE 1596.3)
- 650 MHz full power analog bandwidth
- 2 V p-p input voltage range
- Serial port control
  - Full chip and individual channel power-down modes
  - Flexible bit orientation
  - Built-in and custom digital test pattern generation
  - Multichip sync and clock divider
  - Programmable output clock and data alignment
  - Programmable output resolution
  - Standby mode

## APPLICATIONS

- Medical ultrasound
- High speed imaging
- Quadrature radio receivers
- Diversity radio receivers
- Test equipment

## GENERAL DESCRIPTION

The AD9253 is a quad, 14-bit, 80 MSPS/105 MSPS/125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual-channel power-down is supported and typically consumes less than 2 mW when all channels are disabled. The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable output clock and data alignment and digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9253 is available in a RoHS-compliant, 48-lead LFCSP. It is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

## FUNCTIONAL BLOCK DIAGRAM

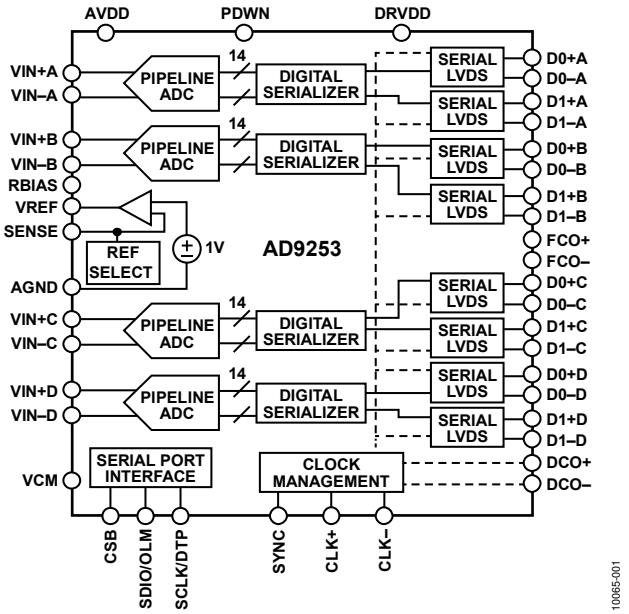


*Figure 1.*

## PRODUCT HIGHLIGHTS

1. Small Footprint. Four ADCs are contained in a small, space-saving package.
2. Low power of 110 mW/channel at 125 MSPS with scalable power options.
3. Pin compatible to the AD9633 12-bit quad ADC.
4. Ease of Use. A data clock output (DCO) operates at frequencies of up to 500 MHz and supports double data rate (DDR) operation.
5. User Flexibility. The SPI control offers a wide range of flexible features to meet specific system requirements.

Rev. B Document Feedback


One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 
Technical Support www.analog.com

# AD9253* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD9253 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-737: How ADIsimADC Models an ADC
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

### Data Sheet

- AD9253-DSCC: Military Data Sheet
- AD9253-EP: Enhanced Product Data Sheet
- AD9253: Quad, 14-Bit, 80 MSPS/105 MSPS/125 MSPS Serial LVDS 1.8 V Analog-to-Digital Converter

### User Guides

- Evaluating the AD9253/AD9633/AD9653 Analog-to-Digital Converters

## TOOLS AND SIMULATIONS

- Visual Analog
- AD9253 IBIS Model

## REFERENCE DESIGNS

- CN0249

## REFERENCE MATERIALS

### Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

### Tutorials

- MT-230: Noise Considerations in High Speed Converter Signal Chains

## DESIGN RESOURCES

- AD9253 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD9253 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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# SPECIFICATIONS

## DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

**Table 1.**

| | | AD9253-80 | | | AD9253-105 | | | AD9253-125 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter[1]** | **Temp** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| RESOLUTION | | 14 | | | 14 | | | 14 | | | Bits |
| ACCURACY | | | | | | | | | | | |
| No Missing Codes | Full | Guaranteed | | | Guaranteed | | | Guaranteed | | | |
| Offset Error | Full | −0.7 | −0.3 | +0.1 | −0.7 | −0.3 | +0.1 | −0.7 | −0.3 | +0.1 | % FSR |
| Offset Matching | Full | −0.6 | +0.2 | +0.6 | −0.6 | +0.2 | +0.6 | −0.6 | +0.2 | +0.6 | % FSR |
| Gain Error | Full | −10 | −5 | 0 | −10 | −5 | 0 | −10 | −5 | 0 | % FSR |
| Gain Matching | Full | | 1 | 1.6 | | 1 | 1.6 | | 1.1 | 1.6 | % FSR |
| Differential Nonlinearity (DNL) | Full | −1 | | +1.6 | −0.8 | | +1.5 | −0.8 | | +1.5 | LSB |
| | 25°C | | ±0.8 | | | ±0.75 | | | ±0.75 | | LSB |
| Integral Nonlinearity (INL) | Full | −4.0 | | +4.0 | −4.0 | | 4.0 | −4.0 | | +4.0 | LSB |
| | 25°C | | ±1.5 | | | ±2.0 | | | ±2.0 | | LSB |
| TEMPERATURE DRIFT | | | | | | | | | | | |
| Offset Error | Full | | ±2 | | | ±2 | | | ±2 | | ppm/°C |
| INTERNAL VOLTAGE REFERENCE | | | | | | | | | | | |
| Output Voltage (1 V Mode) | Full | 0.98 | 1.0 | 1.02 | 0.98 | 1.0 | 1.02 | 0.98 | 1.0 | 1.02 | V |
| Load Regulation at 1.0 mA ($V_{REF}$ = 1 V) | Full | | 2 | | | 2 | | | 2 | | mV |
| Input Resistance | Full | | 7.5 | | | 7.5 | | | 7.5 | | kΩ |
| INPUT-REFERRED NOISE | | | | | | | | | | | |
| $V_{REF}$ = 1.0 V | 25°C | | 0.94 | | | 0.94 | | | 0.94 | | LSB rms |
| ANALOG INPUTS | | | | | | | | | | | |
| Differential Input Voltage ($V_{REF}$ = 1 V) | Full | | 2 | | | 2 | | | 2 | | V p-p |
| Common-Mode Voltage | Full | | 0.9 | | | 0.9 | | | 0.9 | | V |
| Differential Input Resistance | | | 5.2 | | | 5.2 | | | 5.2 | | kΩ |
| Differential Input Capacitance | Full | | 3.5 | | | 3.5 | | | 3.5 | | pF |
| POWER SUPPLY | | | | | | | | | | | |
| AVDD | Full | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| DRVDD | Full | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| $I_{AVDD}$[2] | Full | | 131 | 144 | | 158 | 172 | | 183 | 200 | mA |
| $I_{DRVDD}$ (ANSI-644 Mode)[2] | Full | | 63 | 81 | | 67 | 95 | | 71 | 100 | mA |
| $I_{DRVDD}$ (Reduced Range Mode)[2] | 25°C | | 42 | | | 48 | | | 53 | | mA |
| TOTAL POWER CONSUMPTION | | | | | | | | | | | |
| DC Input | Full | | 326 | | | 375 | | | 423 | | mW |
| Sine Wave Input (Four Channels Including Output Drivers ANSI-644 Mode) | Full | | 349 | 405 | | 405 | 481 | | 457 | 540 | mW |
| Sine Wave Input (Four Channels Including Output Drivers Reduced Range Mode) | 25°C | | 311 | | | 371 | | | 425 | | mW |
| Power-Down | Full | | 2 | | | 2 | | | 2 | | mW |
| Standby[3] | Full | | 178 | | | 209 | | | 236 | | mW |

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave on all four channels.
[3] Can be controlled via the SPI.

## AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

**Table 2.**

| | | AD9253-80 | | | AD9253-105 | | | AD9253-125 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter[1]** | **Temp** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| SIGNAL-TO-NOISE RATIO (SNR) | | | | | | | | | | | |
| $f_{IN}$ = 9.7 MHz | 25°C | | 75.4 | | | 75.1 | | | 75.3 | | dBFS |
| $f_{IN}$ = 30.5 MHz | 25°C | | 74.9 | | | 75.0 | | | 75.2 | | dBFS |
| $f_{IN}$ = 70 MHz | Full | 72.2 | 74.7 | | 72.2 | 74.4 | | 73 | 74.2 | | dBFS |
| $f_{IN}$ = 140 MHz | 25°C | | 72.3 | | | 73.1 | | | 72.2 | | dBFS |
| $f_{IN}$ = 200 MHz | 25°C | | 70.7 | | | 71.2 | | | 70.7 | | dBFS |
| SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD) | | | | | | | | | | | |
| $f_{IN}$ = 9.7 MHz | 25°C | | 75.3 | | | 75.0 | | | 75.2 | | dBFS |
| $f_{IN}$ = 30.5 MHz | 25°C | | 74.8 | | | 74.9 | | | 75.1 | | dBFS |
| $f_{IN}$ = 70 MHz | Full | 71.8 | 74.6 | | 70.8 | 74.2 | | 72.6 | 74.1 | | dBFS |
| $f_{IN}$ = 140 MHz | 25°C | | 72.1 | | | 72.8 | | | 71.9 | | dBFS |
| $f_{IN}$ = 200 MHz | 25°C | | 70.5 | | | 70.8 | | | 70.4 | | dBFS |
| EFFECTIVE NUMBER OF BITS (ENOB) | | | | | | | | | | | |
| $f_{IN}$ = 9.7 MHz | 25°C | | 12.2 | | | 12.1 | | | 12.2 | | Bits |
| $f_{IN}$ = 30.5 MHz | 25°C | | 12.1 | | | 12.1 | | | 12.1 | | Bits |
| $f_{IN}$ = 70 MHz | Full | 11.6 | 11.9 | | 11.5 | 12.0 | | 11.8 | 12.0 | | Bits |
| $f_{IN}$ = 140 MHz | 25°C | | 11.6 | | | 11.8 | | | 11.6 | | Bits |
| $f_{IN}$ = 200 MHz | 25°C | | 11.5 | | | 11.5 | | | 11.4 | | Bits |
| SPURIOUS-FREE DYNAMIC RANGE (SFDR) | | | | | | | | | | | |
| $f_{IN}$ = 9.7 MHz | 25°C | | 98 | | | 98 | | | 98 | | dBc |
| $f_{IN}$ = 30.5 MHz | 25°C | | 93 | | | 92 | | | 92 | | dBc |
| $f_{IN}$ = 70 MHz | Full | 77 | 94 | | 75 | 89 | | 77 | 90 | | dBc |
| $f_{IN}$ = 140 MHz | 25°C | | 85 | | | 85 | | | 85 | | dBc |
| $f_{IN}$ = 200 MHz | 25°C | | 84 | | | 82 | | | 83 | | dBc |
| WORST HARMONIC (SECOND OR THIRD) | | | | | | | | | | | |
| $f_{IN}$ = 9.7 MHz | 25°C | | −98 | | | −98 | | | −98 | | dBc |
| $f_{IN}$ = 30.5 MHz | 25°C | | −93 | | | −92 | | | −92 | | dBc |
| $f_{IN}$ = 70 MHz | Full | | −94 | −77 | | −89 | −75 | | −90 | −77 | dBc |
| $f_{IN}$ = 140 MHz | 25°C | | −85 | | | −85 | | | −85 | | dBc |
| $f_{IN}$ = 200 MHz | 25°C | | −84 | | | −82 | | | −83 | | dBc |
| WORST OTHER (EXCLUDING SECOND OR THIRD) | | | | | | | | | | | |
| $f_{IN}$ = 9.7 MHz | 25°C | | −99 | | | −98 | | | −100 | | dBc |
| $f_{IN}$ = 30.5 MHz | 25°C | | −98 | | | −98 | | | −99 | | dBc |
| $f_{IN}$ = 70 MHz | Full | | −97 | −77 | | −94 | −77 | | −94 | −84 | dBc |
| $f_{IN}$ = 140 MHz | 25°C | | −97 | | | −97 | | | −95 | | dBc |
| $f_{IN}$ = 200 MHz | 25°C | | −94 | | | −91 | | | −91 | | dBc |
| TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS | | | | | | | | | | | |
| $f_{IN1}$ = 70.5 MHz, $f_{IN2}$ = 72.5 MHz | 25°C | | 90 | | | 88 | | | 86 | | dBc |
| CROSSTALK[2] | Full | | −95 | | | −95 | | | −95 | | dB |
| CROSSTALK (OVERRANGE CONDITION)[3] | 25°C | | −89 | | | −89 | | | −89 | | dB |
| POWER SUPPLY REJECTION RATIO (PSRR)[1, 4] | | | | | | | | | | | |
| AVDD | 25°C | | 48 | | | 48 | | | 48 | | dB |
| DRVDD | 25°C | | 75 | | | 75 | | | 75 | | dB |
| ANALOG INPUT BANDWIDTH, FULL POWER | 25°C | | 650 | | | 650 | | | 650 | | MHz |

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 70 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[3] Overrange condition is specified as being 3 dB above the full-scale input range.
[4] PSRR is measured by injecting a sinusoidal signal at 10 MHz to the power supply pin and measuring the output spur on the FFT. PSRR is calculated as the ratio of the amplitudes of the spur voltage over the pin voltage, expressed in decibels.

## DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

**Table 3.**

| Parameter[1] | Temp | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CLOCK INPUTS (CLK+, CLK−) | | | | | |
| Logic Compliance | | | CMOS/LVDS/LVPECL | | |
| Differential Input Voltage[2] | Full | 0.2 | | 3.6 | V p-p |
| Input Voltage Range | Full | AGND − 0.2 | | AVDD + 0.2 | V |
| Input Common-Mode Voltage | Full | | 0.9 | | V |
| Input Resistance (Differential) | 25°C | | 15 | | kΩ |
| Input Capacitance | 25°C | | 4 | | pF |
| LOGIC INPUTS (PDWN, SYNC, SCLK) | | | | | |
| Logic 1 Voltage | Full | 1.2 | | AVDD + 0.2 | V |
| Logic 0 Voltage | Full | 0 | | 0.8 | V |
| Input Resistance | 25°C | | 30 | | kΩ |
| Input Capacitance | 25°C | | 2 | | pF |
| LOGIC INPUT (CSB) | | | | | |
| Logic 1 Voltage | Full | 1.2 | | AVDD + 0.2 | V |
| Logic 0 Voltage | Full | 0 | | 0.8 | V |
| Input Resistance | 25°C | | 26 | | kΩ |
| Input Capacitance | 25°C | | 2 | | pF |
| LOGIC INPUT (SDIO) | | | | | |
| Logic 1 Voltage | Full | 1.2 | | AVDD + 0.2 | V |
| Logic 0 Voltage | Full | 0 | | 0.8 | V |
| Input Resistance | 25°C | | 26 | | kΩ |
| Input Capacitance | 25°C | | 5 | | pF |
| LOGIC OUTPUT (SDIO)[3] | | | | | |
| Logic 1 Voltage ($I_{OH}$ = 800 µA) | Full | | 1.79 | | V |
| Logic 0 Voltage ($I_{OL}$ = 50 µA) | Full | | | 0.05 | V |
| DIGITAL OUTPUTS (D0±x, D1±x), ANSI-644 | | | | | |
| Logic Compliance | | | LVDS | | |
| Differential Output Voltage ($V_{OD}$) | Full | 290 | 345 | 400 | mV |
| Output Offset Voltage ($V_{OS}$) | Full | 1.15 | 1.25 | 1.35 | V |
| Output Coding (Default) | | | Twos complement | | |
| DIGITAL OUTPUTS (D0±x, D1±x), LOW POWER, REDUCED SIGNAL OPTION | | | | | |
| Logic Compliance | | | LVDS | | |
| Differential Output Voltage ($V_{OD}$) | Full | 160 | 200 | 230 | mV |
| Output Offset Voltage ($V_{OS}$) | Full | 1.15 | 1.25 | 1.35 | V |
| Output Coding (Default) | | | Twos complement | | |

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] This is specified for LVDS and LVPECL only.
[3] This is specified for 13 SDIO/OLM pins sharing the same connection.

## SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

**Table 4.**

| Parameter[1, 2] | Temp | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CLOCK[3] | | | | | |
| Input Clock Rate | Full | 10 | | 1000 | MHz |
| Conversion Rate[4] | Full | 10 | | 80/105/125 | MSPS |
| Clock Pulse Width High ($t_{EH}$) | Full | | 6.25/4.76/4.00 | | ns |
| Clock Pulse Width Low ($t_{EL}$) | Full | | 6.25/4.76/4.00 | | ns |
| OUTPUT PARAMETERS[3] | | | | | |
| Propagation Delay ($t_{PD}$) | Full | 1.5 | 2.3 | 3.1 | ns |
| Rise Time ($t_R$) (20% to 80%) | Full | | 300 | | ps |
| Fall Time ($t_F$) (20% to 80%) | Full | | 300 | | ps |
| FCO Propagation Delay ($t_{FCO}$) | Full | 1.5 | 2.3 | 3.1 | ns |
| DCO Propagation Delay ($t_{CPD}$)[5] | Full | | $t_{FCO}$ + ($t_{SAMPLE}$/16) | | ns |
| DCO to Data Delay ($t_{DATA}$)[5] | Full | ($t_{SAMPLE}$/16) − 300 | ($t_{SAMPLE}$/16) | ($t_{SAMPLE}$/16) + 300 | ps |
| DCO to FCO Delay ($t_{FRAME}$)[5] | Full | ($t_{SAMPLE}$/16) − 300 | ($t_{SAMPLE}$/16) | ($t_{SAMPLE}$/16) + 300 | ps |
| Lane Delay ($t_{LD}$) | | | 90 | | ps |
| Data to Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$) | Full | | ±50 | ±200 | ps |
| Wake-Up Time (Standby) | 25°C | | 250 | | ns |
| Wake-Up Time (Power-Down)[6] | 25°C | | 375 | | µs |
| Pipeline Latency | Full | | 16 | | Clock cycles |
| APERTURE | | | | | |
| Aperture Delay ($t_A$) | 25°C | | 1 | | ns |
| Aperture Uncertainty (Jitter, $t_J$) | 25°C | | 135 | | fs rms |
| Out-of-Range Recovery Time | 25°C | | 1 | | Clock cycles |

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] Can be adjusted via the SPI. The conversion rate is the clock rate after the divider.
[4] The maximum conversion rate is based on two-lane output mode. See the Digital Outputs and Timing section for the maximum conversion rate in one-lane output mode.
[5] $t_{SAMPLE}$/16 is based on the number of bits in two LVDS data lanes. $t_{SAMPLE} = 1/f_S$.
[6] Wake-up time is defined as the time required to return to normal operation from power-down mode.

## TIMING SPECIFICATIONS

**Table 5.**

| Parameter | Description | Limit | Unit |
|---|---|---|---|
| SYNC TIMING REQUIREMENTS | | | |
| $t_{SSYNC}$ | SYNC to rising edge of CLK+ setup time | 1.2 | ns min |
| $t_{HSYNC}$ | SYNC to rising edge of CLK+ hold time | −0.2 | ns min |
| SPI TIMING REQUIREMENTS | See Figure 74 | | |
| $t_{DS}$ | Setup time between the data and the rising edge of SCLK | 2 | ns min |
| $t_{DH}$ | Hold time between the data and the rising edge of SCLK | 2 | ns min |
| $t_{CLK}$ | Period of the SCLK | 40 | ns min |
| $t_S$ | Setup time between CSB and SCLK | 2 | ns min |
| $t_H$ | Hold time between CSB and SCLK | 2 | ns min |
| $t_{HIGH}$ | SCLK pulse width high | 10 | ns min |
| $t_{LOW}$ | SCLK pulse width low | 10 | ns min |
| $t_{EN\_SDIO}$ | Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 74) | 10 | ns min |
| $t_{DIS\_SDIO}$ | Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 74) | 10 | ns min |

### *Timing Diagrams*

Refer to the Memory Map Register Descriptions section and Table 21 for SPI register settings.

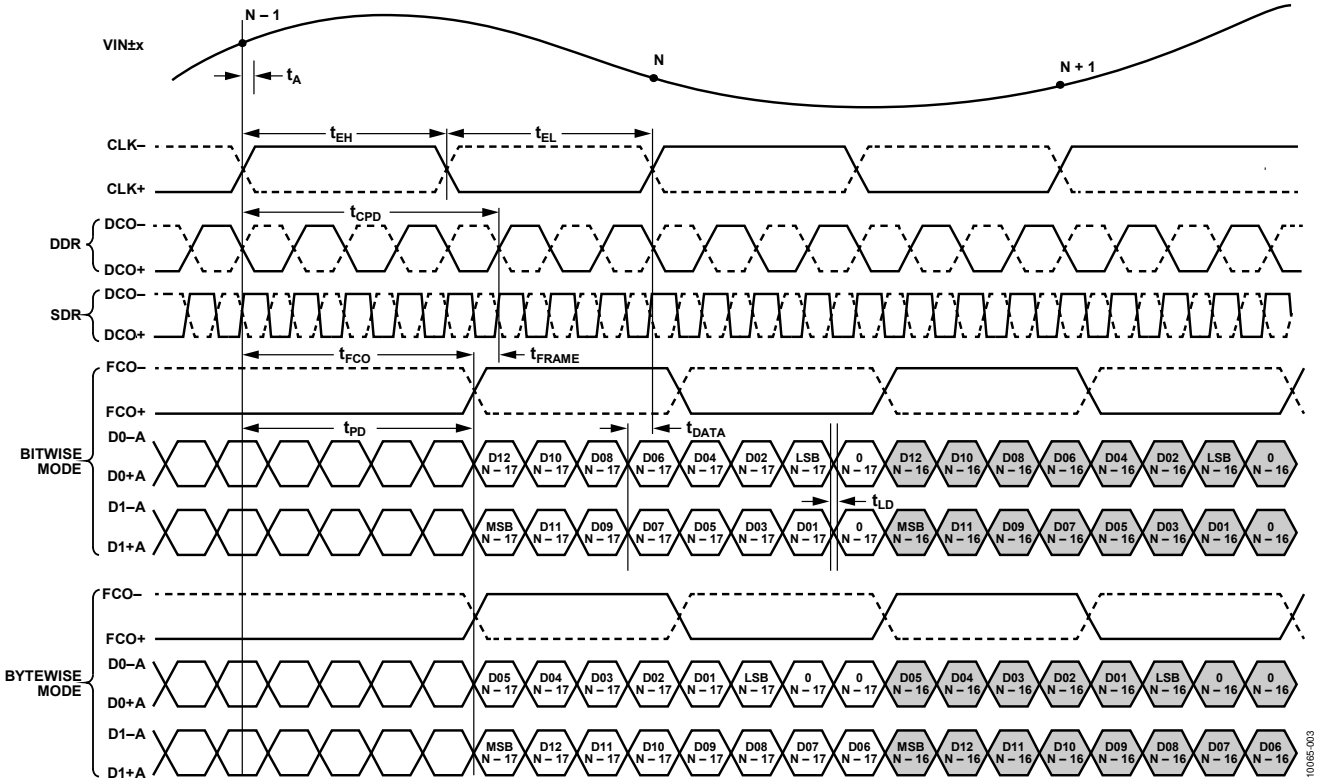


*Figure 2. 16-Bit DDR/SDR, Two-Lane, 1× Frame Mode (Default)*

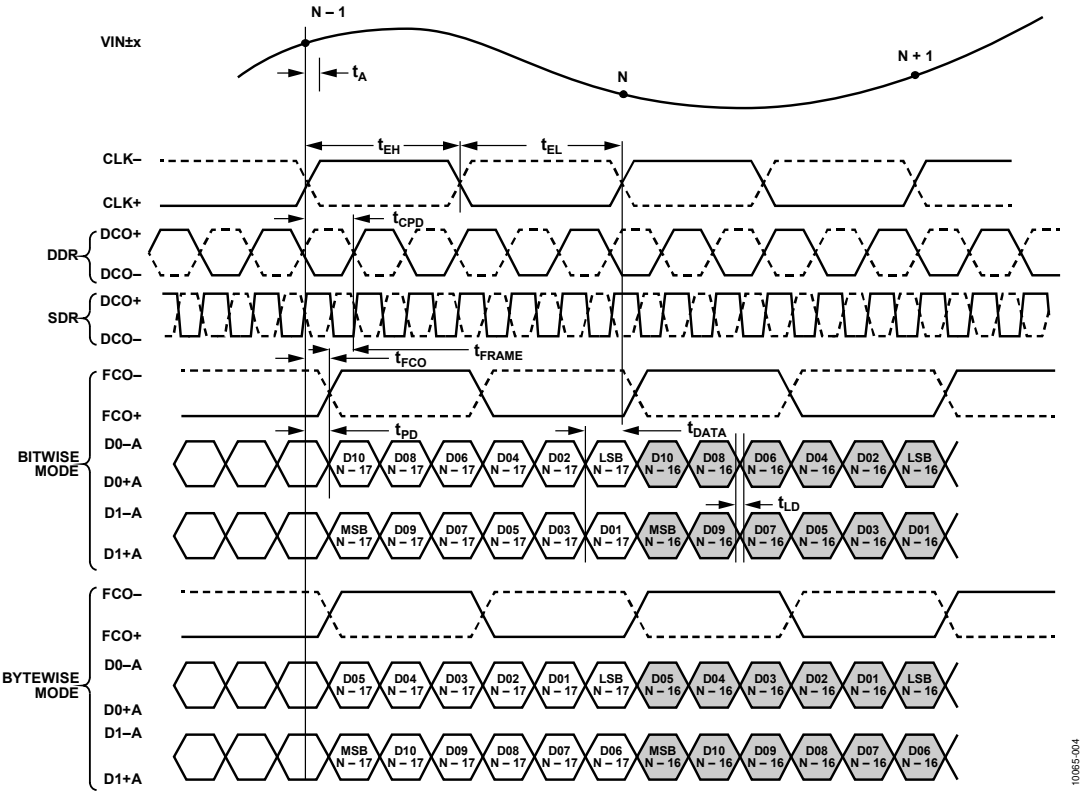


*Figure 3. 12-Bit DDR/SDR, Two-Lane, 1× Frame Mode*

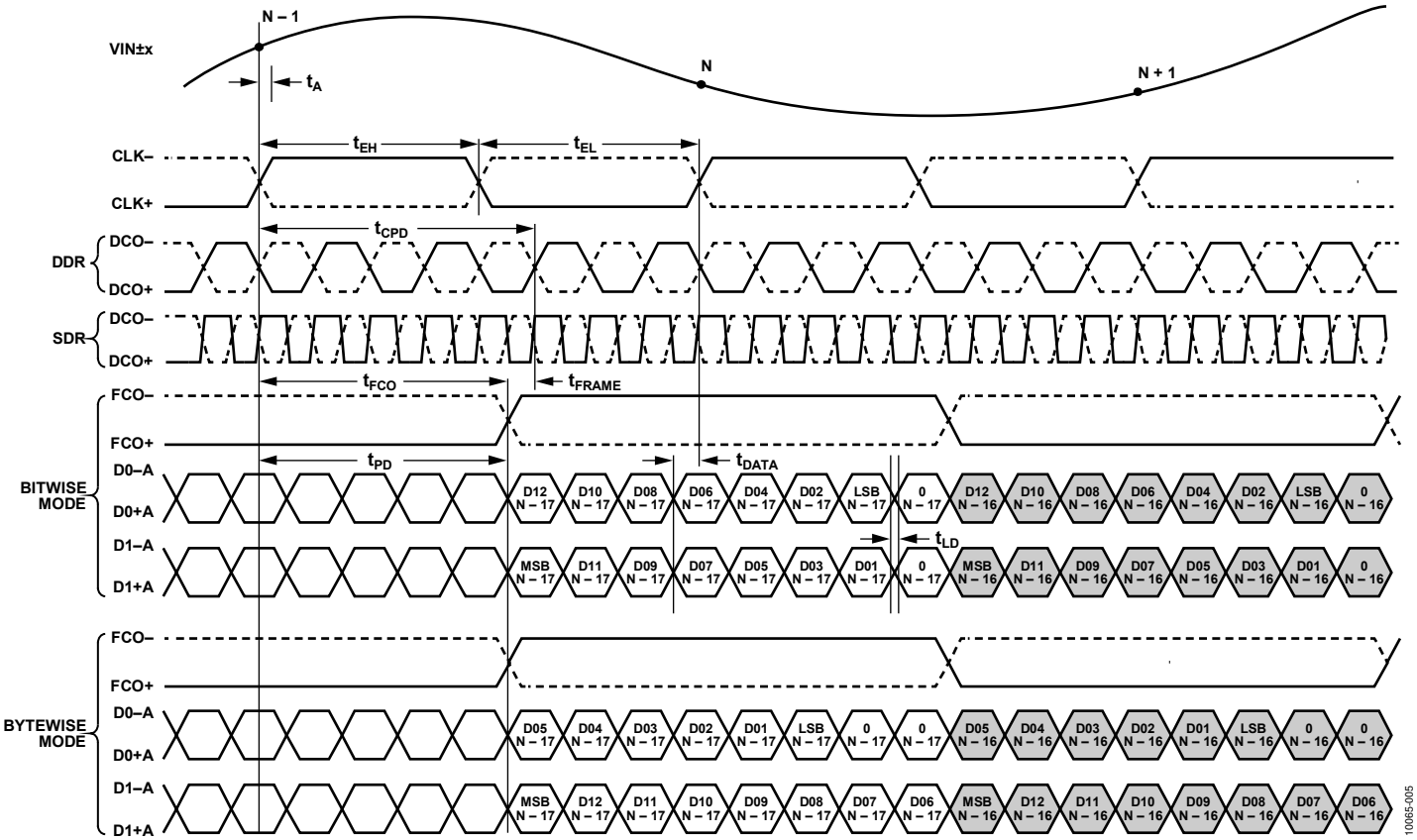


*Figure 4. 16-Bit DDR/SDR, Two-Lane, 2× Frame Mode*

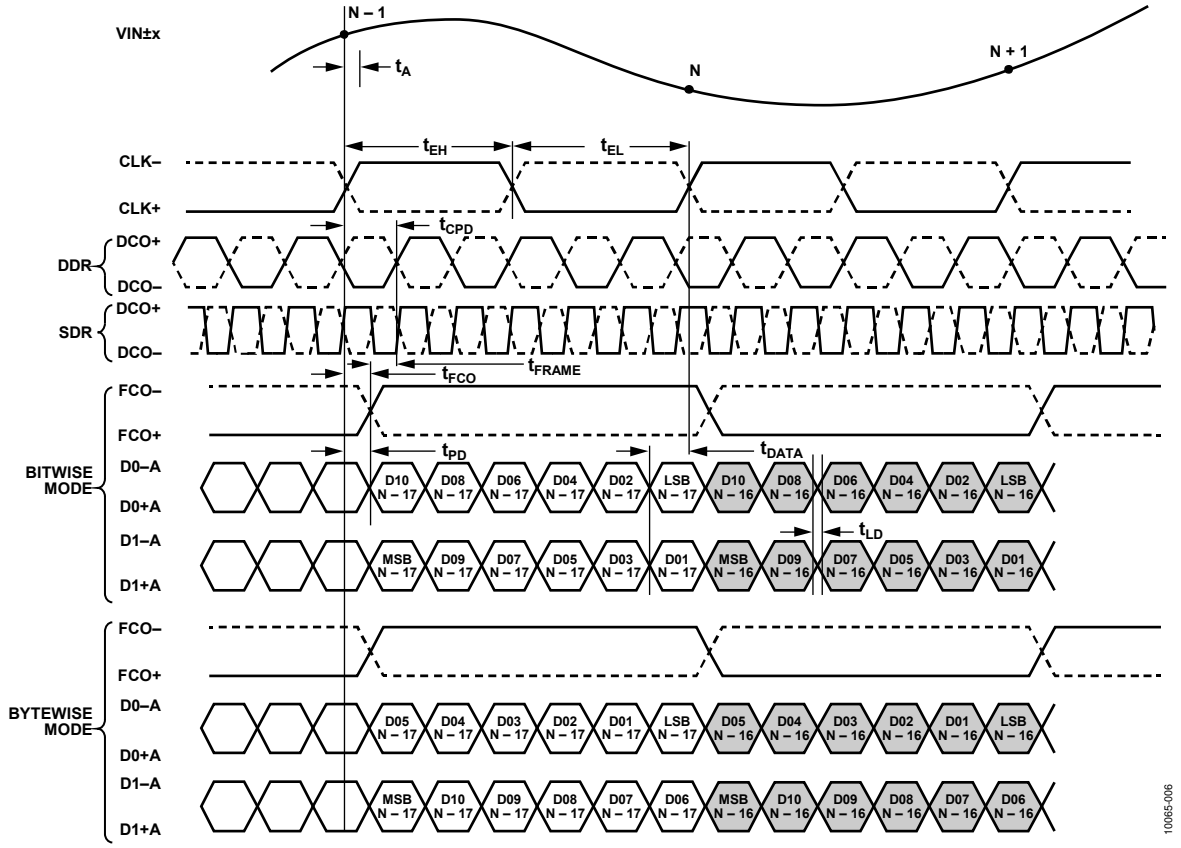


*Figure 5. 12-Bit DDR/SDR, Two-Lane, 2× Frame Mode*

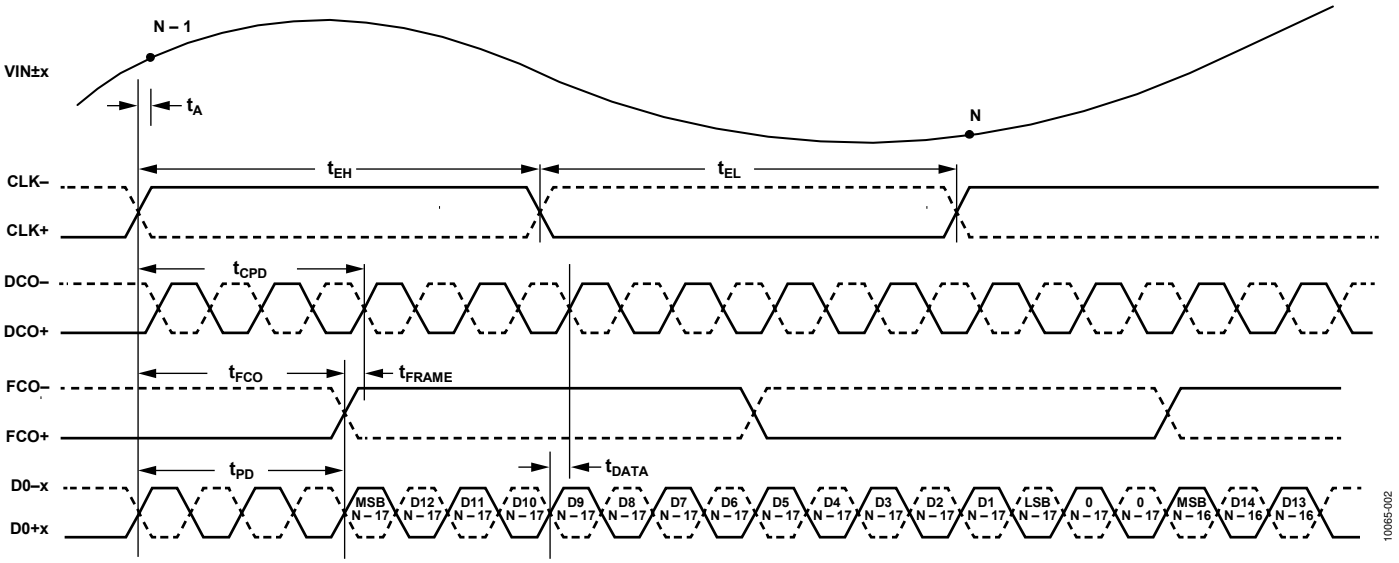


*Figure 6. Wordwise DDR, One-Lane, 1× Frame, 16-Bit Output Mode*

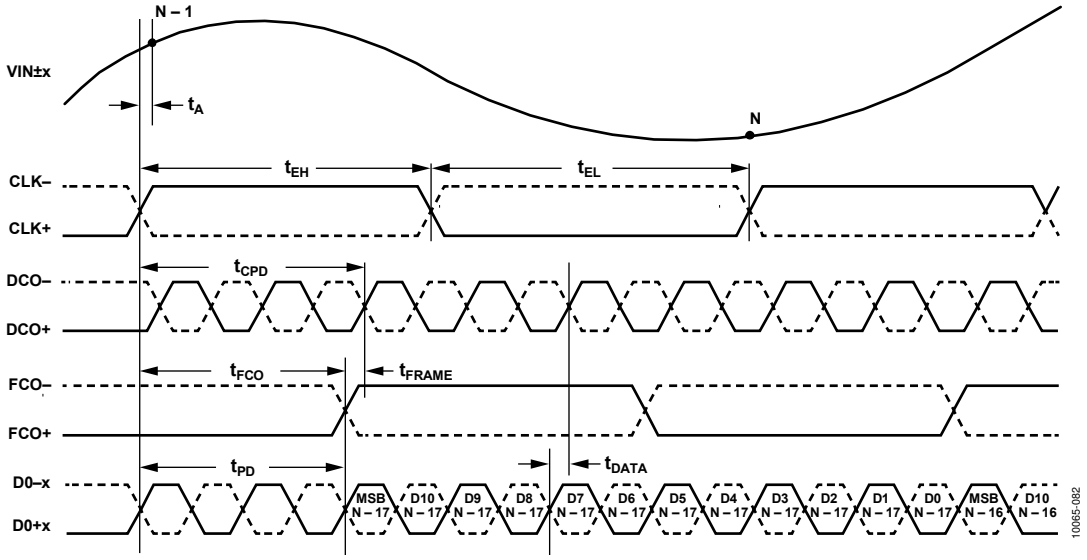


*Figure 7. Wordwise DDR, One-Lane, 1× Frame, 12-Bit Output Mode*

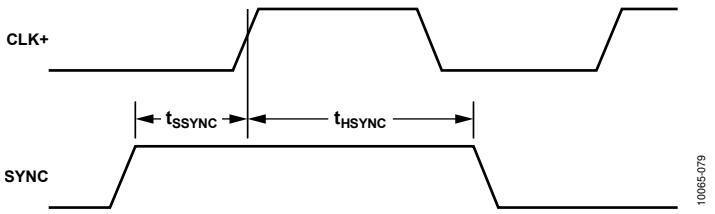


*Figure 8. SYNC Input Timing Requirements*

# ABSOLUTE MAXIMUM RATINGS

**Table 6.**

| Parameter | Rating |
|---|---|
| Electrical | |
| AVDD to AGND | −0.3 V to +2.0 V |
| DRVDD to AGND | −0.3 V to +2.0 V |
| Digital Outputs (D0±x, D1±x, DCO+, DCO−, FCO+, FCO−) to AGND | −0.3 V to +2.0 V |
| CLK+, CLK− to AGND | −0.3 V to +2.0 V |
| VIN+x, VIN−x to AGND | −0.3 V to +2.0 V |
| SCLK/DTP, SDIO/OLM, CSB to AGND | −0.3 V to +2.0 V |
| SYNC, PDWN to AGND | −0.3 V to +2.0 V |
| RBIAS to AGND | −0.3 V to +2.0 V |
| VREF, SENSE to AGND | −0.3 V to +2.0 V |
| Environmental | |
| Operating Temperature Range (Ambient) | −40°C to +85°C |
| Maximum Junction Temperature | 150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Storage Temperature Range (Ambient) | −65°C to +150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

**Table 7. Thermal Resistance**

| Package Type | Air Flow Velocity (m/sec) | $\theta_{JA}$[1] | $\theta_{JB}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|---|---|
| 48-Lead LFCSP | 0.0 | 23.7 | 7.8 | 7.1 | °C/W |
| 7 mm × 7 mm | 1.0 | 20.0 | N/A | N/A | °C/W |
| (CP-48-13) | 2.5 | 18.7 | N/A | N/A | °C/W |

[1] $\theta_{JA}$ for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

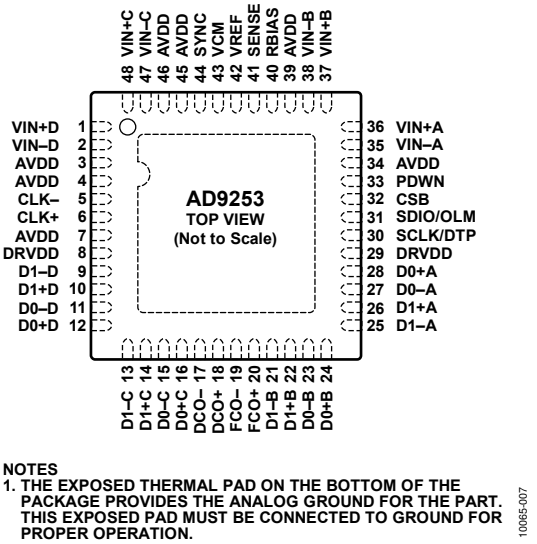


*Figure 9. 48-Lead LFCSP Pin Configuration, Top View*

**Table 8. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 0 | AGND, Exposed Pad | Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation. |
| 1 | VIN+D | ADC D Analog Input True. |
| 2 | VIN−D | ADC D Analog Input Complement. |
| 3, 4, 7, 34, 39, 45, 46 | AVDD | 1.8 V Analog Supply Pins. |
| 5, 6 | CLK−, CLK+ | Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs. |
| 8, 29 | DRVDD | Digital Output Driver Supply. |
| 9, 10 | D1−D, D1+D | Channel D Digital Outputs, (Disabled in One-Lane Mode[1]). |
| 11, 12 | D0−D, D0+D | Channel D Digital Outputs, (Disabled in One-Lane Mode[1]). |
| 13, 14 | D1−C, D1+C | Channel C Digital Outputs, (Channel D Digital Outputs in One-Lane Mode[1]). |
| 15, 16 | D0−C, D0+C | Channel C Digital Outputs. |
| 17, 18 | DCO−, DCO+ | Data Clock Outputs. |
| 19, 20 | FCO−, FCO+ | Frame Clock Outputs. |
| 21, 22 | D1−B, D1+B | Channel B Digital Outputs. |
| 23, 24 | D0−B, D0+B | Channel B Digital Outputs, (Channel A Digital Outputs in One-Lane Mode[1]). |
| 25, 26 | D1−A, D1+A | Channel A Digital Outputs, (Disabled in One-Lane Mode[1]). |
| 27, 28 | D0−A, D0+A | Channel A Digital Outputs, (Disabled in One-Lane Mode[1]). |
| 30 | SCLK/DTP | SPI Clock Input/Digital Test Pattern. |
| 31 | SDIO/OLM | SPI Data Input and Output Bidirectional SPI Data/Output Lane Mode. |
| 32 | CSB | SPI Chip Select Bar. Active low enable; 30 kΩ internal pull-up. |
| 33 | PDWN | Digital Input, 30 kΩ Internal Pull-Down.<br>PDWN high = power-down device.<br>PDWN low = run device, normal operation. |
| 35 | VIN−A | ADC A Analog Input Complement. |
| 36 | VIN+A | ADC A Analog Input True. |
| 37 | VIN+B | ADC B Analog Input True. |
| 38 | VIN−B | ADC B Analog Input Complement. |
| 40 | RBIAS | Sets Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground. |
| 41 | SENSE | Reference Mode Selection. |
| 42 | VREF | Voltage Reference Input and Output. |
| 43 | VCM | Analog Input Common-Mode Voltage. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 44 | SYNC | Digital Input. SYNC input to clock divider. |
| 47 | VIN−C | ADC C Analog Input Complement. |
| 48 | VIN+C | ADC C Analog Input True. |

[1] Output channel assignments are shown first for default two-lane mode. If one-lane mode is used, output channel assignments change as indicated in parenthesis. Register 0x21 Bits[6:4] invoke one-lane mode.

# TYPICAL PERFORMANCE CHARACTERISTICS

## AD9253-80

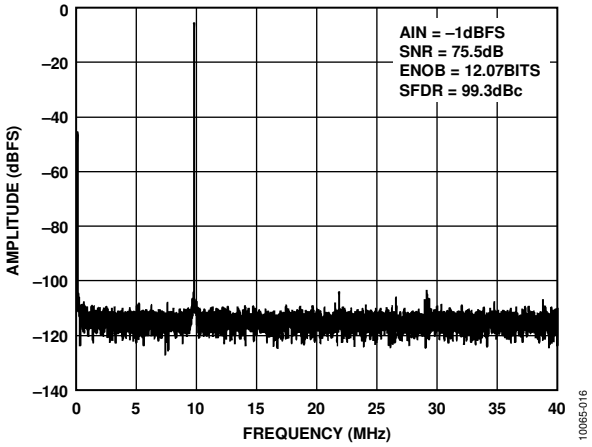


Figure 10. Single-Tone 16k FFT with $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 80 MSPS

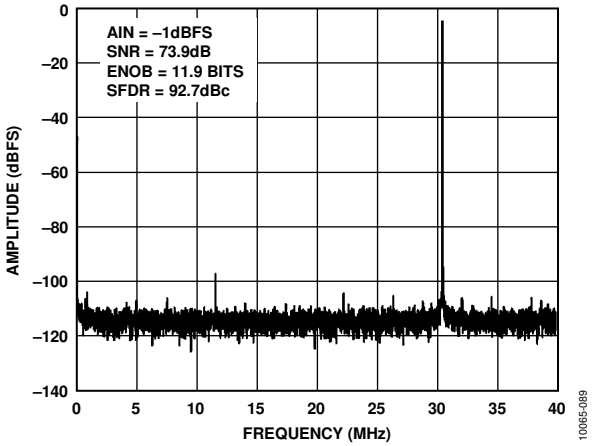


Figure 11. Single-Tone 16k FFT with $f_{IN}$ = 30.5 MHZ, $f_{SAMPLE}$ = 80 MSPS

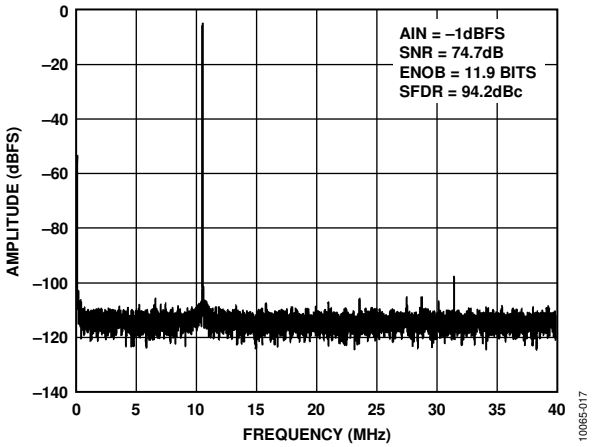


Figure 12. Single-Tone 16k FFT with $f_{IN}$ = 70 MHz, $f_{SAMPLE}$ = 80 MSPS

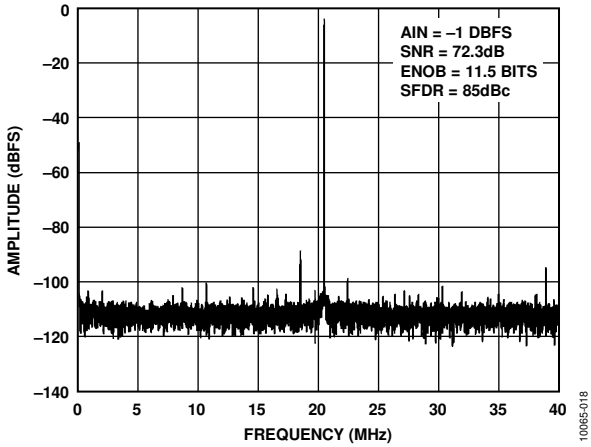


Figure 13. Single-Tone 16k FFT with $f_{IN}$ = 140 MHz, $f_{SAMPLE}$ = 80 MSPS

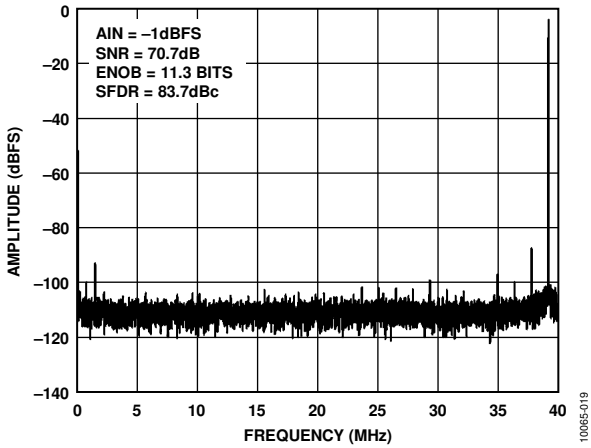


Figure 14. Single-Tone 16k FFT with $f_{IN}$ = 200 MHz, $f_{SAMPLE}$ = 80 MSPS

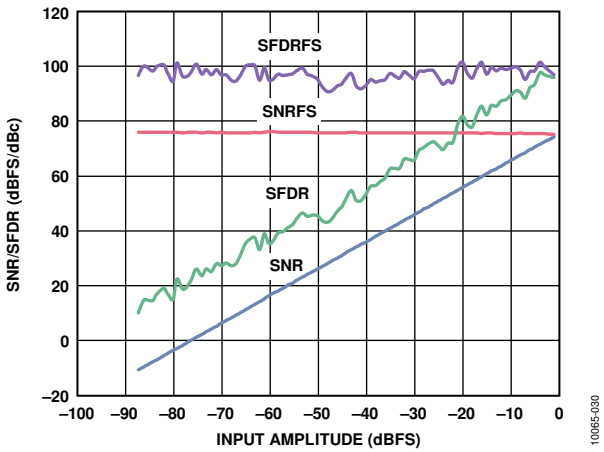


Figure 15. SNR/SFDR vs. Analog Input Level, $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 80 MSPS

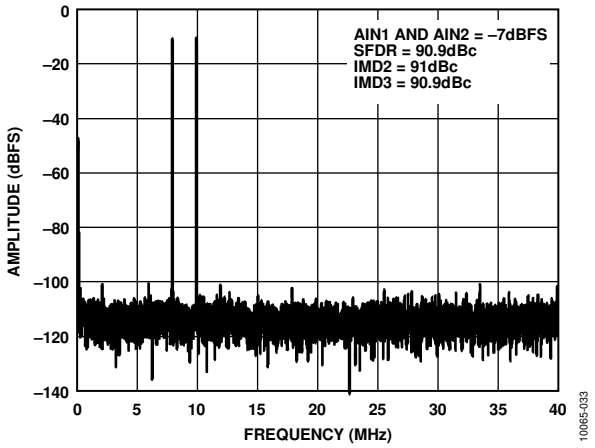


Figure 16. Two-Tone 16k FFT with $f_{IN1}$ = 70.5 MHz and $f_{IN2}$ = 72.5 MHz, $f_{SAMPLE}$ = 80 MSPS

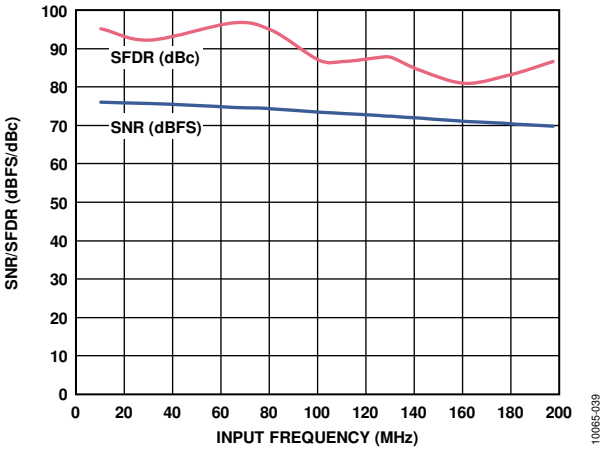


Figure 18. SNR/SFDR vs. $f_{IN}$, $f_{SAMPLE}$ = 80 MSPS

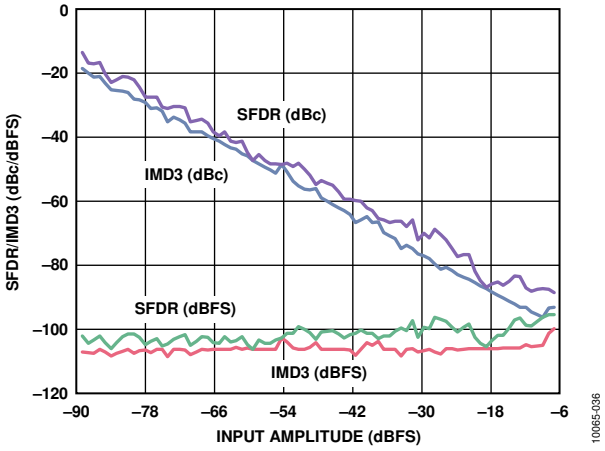


Figure 17. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with $f_{IN1}$ = 70.5 MHz and $f_{IN2}$ = 72.5 MHz, $f_{SAMPLE}$ = 80 MSPS

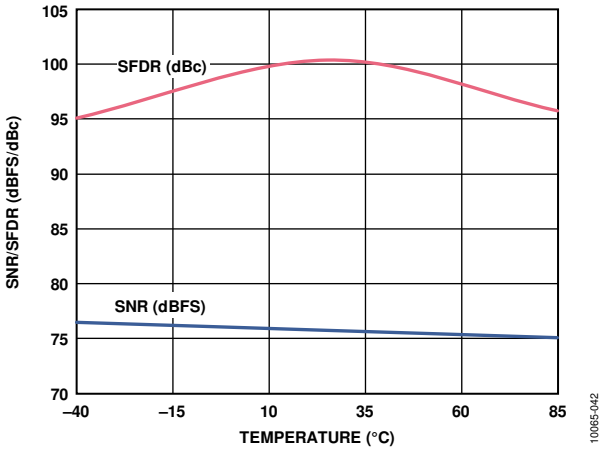


Figure 19. SNR/SFDR vs. Temperature, $f_{IN}$ = 10.3 MHz, $f_{SAMPLE}$ = 80 MSPS

## AD9253-105

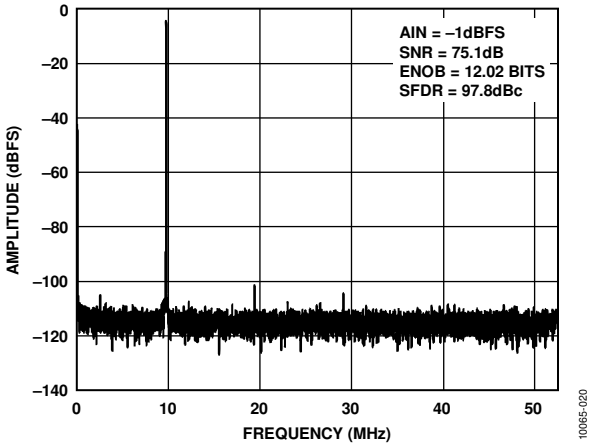


Figure 20. Single-Tone 16k FFT with $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 105 MSPS

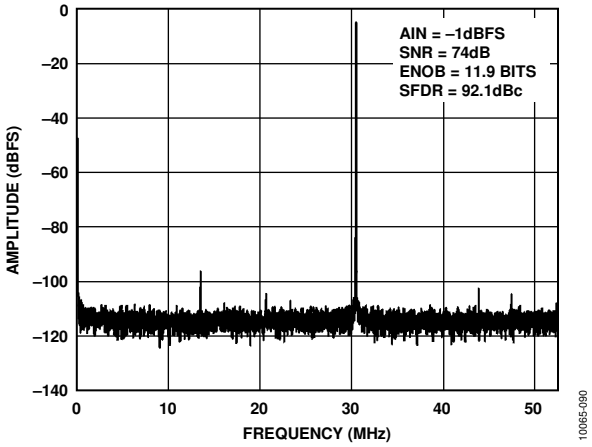


Figure 21. Single-Tone 16k FFT with $f_{IN}$ = 30.5 MHZ, $f_{SAMPLE}$ = 105 MSPS

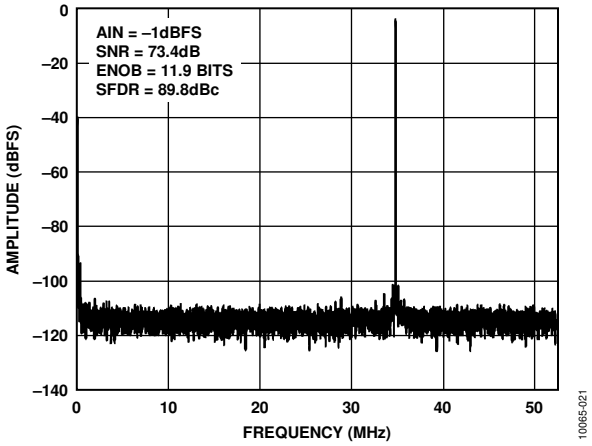


Figure 22. Single-Tone 16k FFT with $f_{IN}$ = 70 MHz, $f_{SAMPLE}$ = 105 MSPS

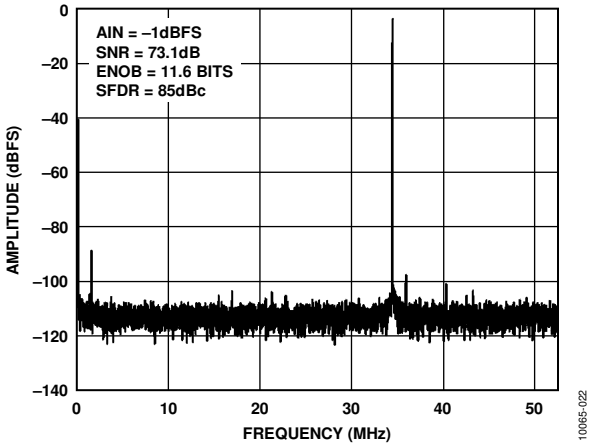


Figure 23. Single-Tone 16k FFT with $f_{IN}$ = 140 MHz, $f_{SAMPLE}$ = 105 MSPS

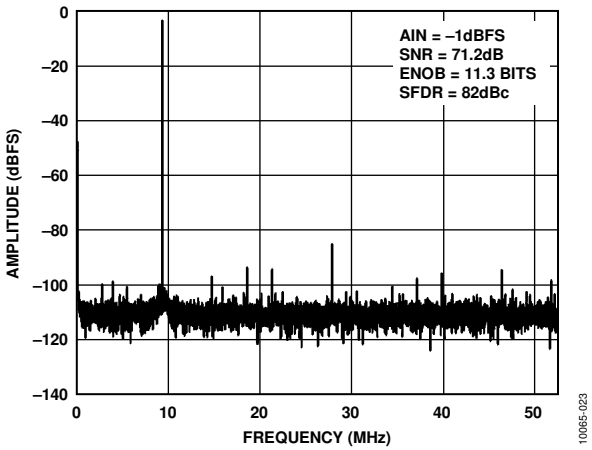


Figure 24. Single-Tone 16k FFT with $f_{IN}$ = 200 MHz, $f_{SAMPLE}$ = 105 MSPS

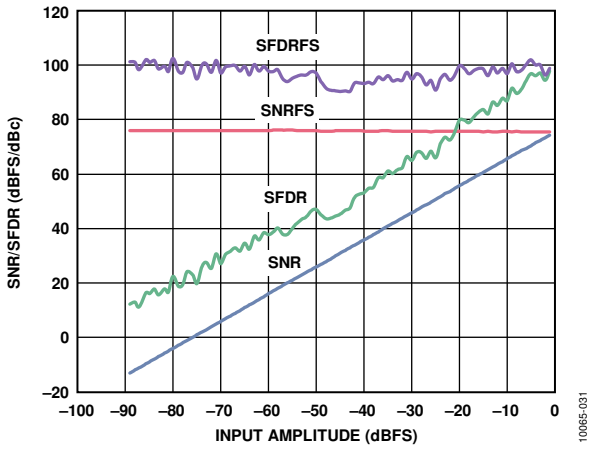


Figure 25. SNR/SFDR vs. Analog Input Level, $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 105 MSPS

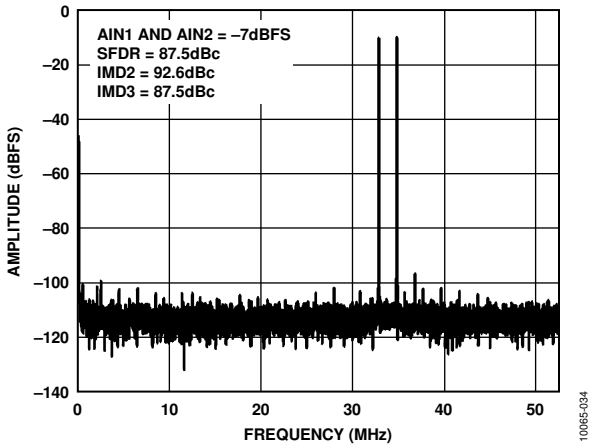


Figure 26. Two-Tone 16k FFT with $f_{IN1}$ = 70.5 MHz and $f_{IN2}$ = 72.5 MHz, $f_{SAMPLE}$ = 105 MSPS

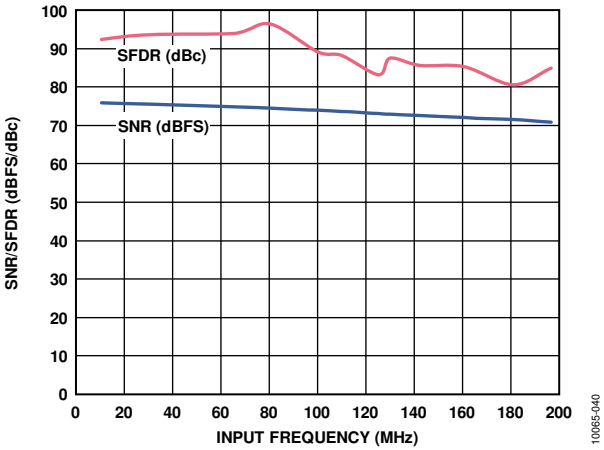


Figure 28. SNR/SFDR vs. $f_{IN}$, $f_{SAMPLE}$ = 105 MSPS

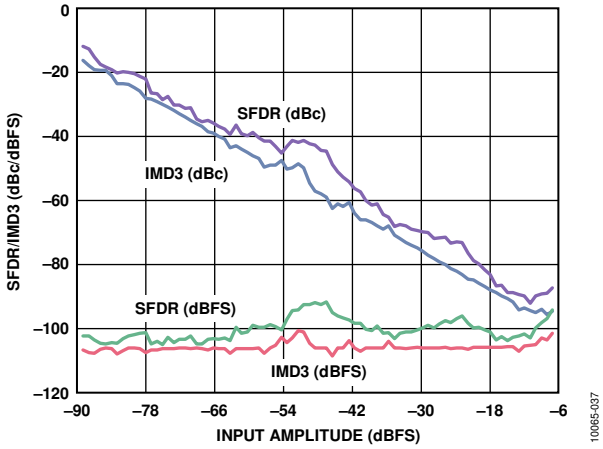


Figure 27. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with $f_{IN1}$ = 70.5 MHz and $f_{IN2}$ = 72.5 MHz, $f_{SAMPLE}$ = 105 MSPS

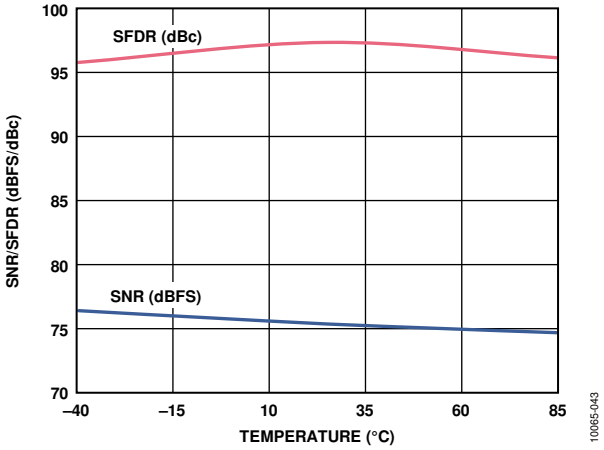


Figure 29. SNR/SFDR vs. Temperature, $f_{IN}$ = 10.3 MHz, $f_{SAMPLE}$ = 105 MSPS

## AD9253-125

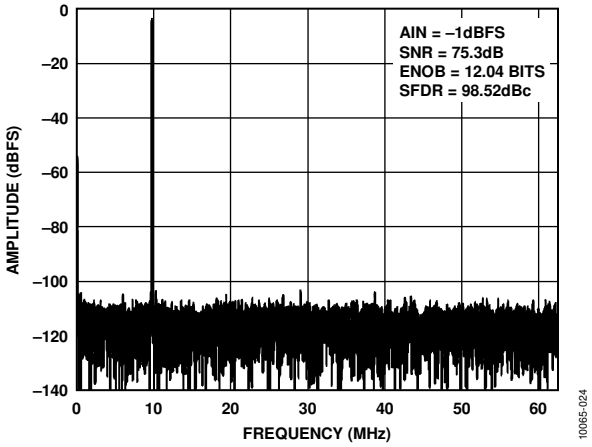


Figure 30. Single-Tone 16k FFT with $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 125 MSPS

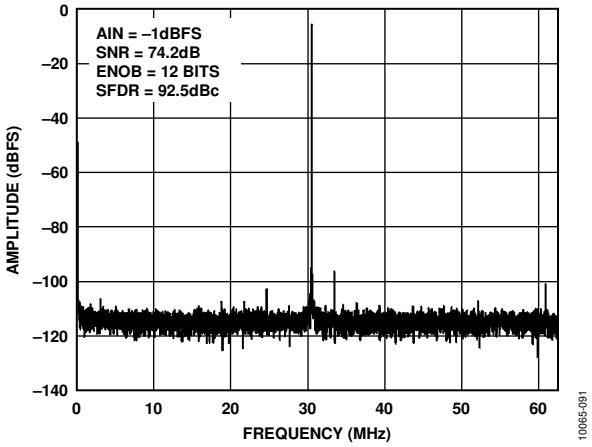


Figure 31. Single-Tone 16k FFT with $f_{IN}$ = 30.5 MHZ, $f_{SAMPLE}$ = 125 MSPS

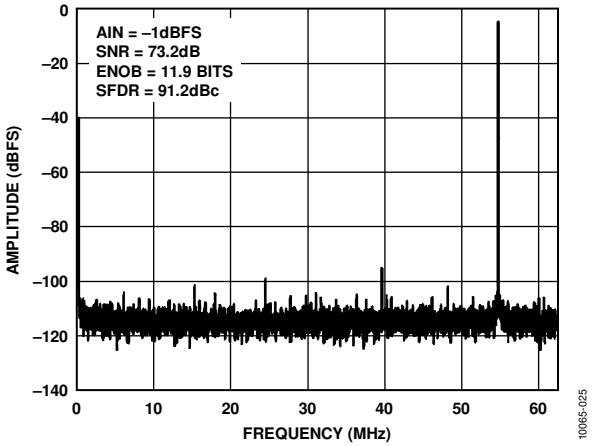


Figure 32. Single-Tone 16k FFT with $f_{IN}$ = 70 MHz, $f_{SAMPLE}$ = 125 MSPS

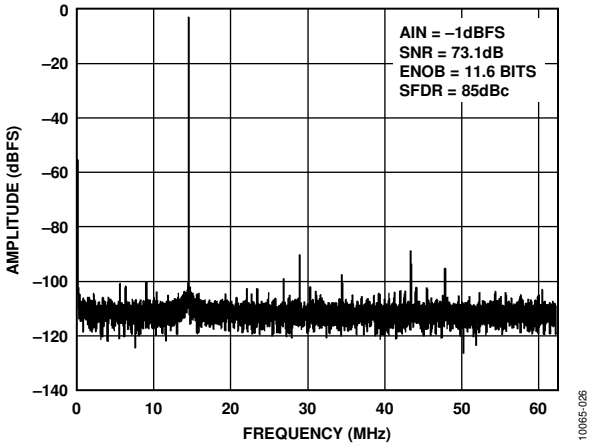


Figure 33. Single-Tone 16k FFT with $f_{IN}$ = 140 MHz, $f_{SAMPLE}$ = 125 MSPS

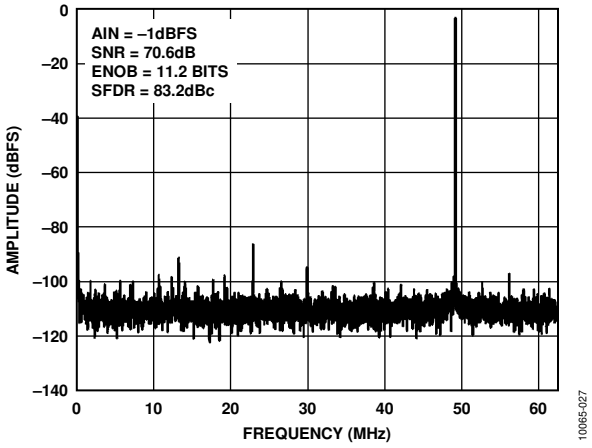


Figure 34. Single-Tone 16k FFT with $f_{IN}$ = 200 MHz, $f_{SAMPLE}$ = 125 MSPS

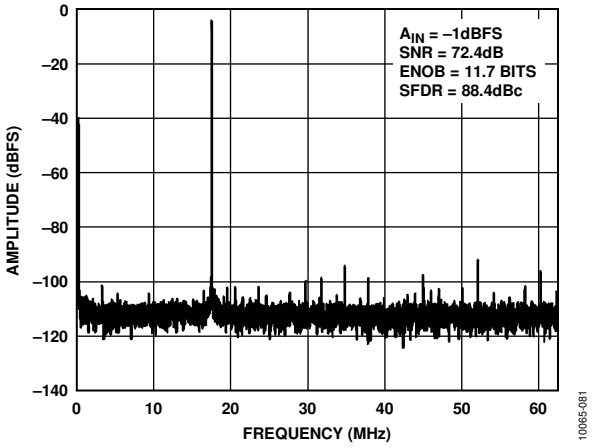


Figure 35. Single-Tone 16k FFT with $f_{IN}$ = 140 MHz at $f_{SAMPLE}$ = 122.88 MSPS

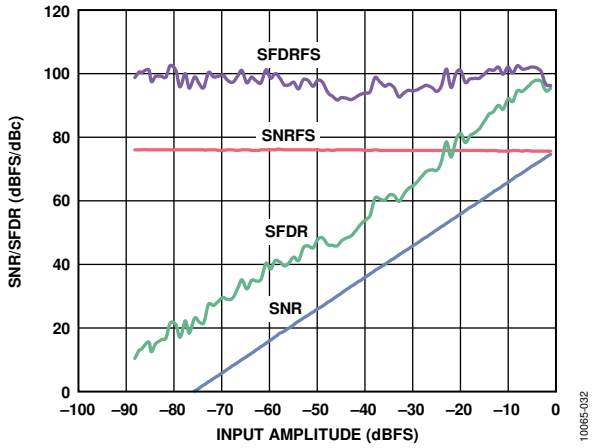


Figure 36. SNR/SFDR vs. Analog Input Level, $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 125 MSPS

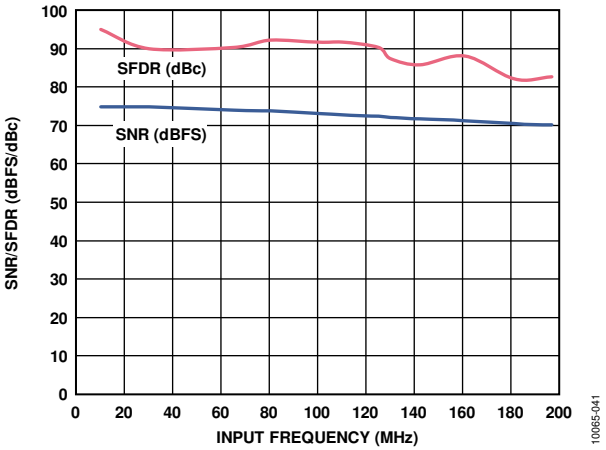


Figure 39. SNR/SFDR vs. $f_{IN}$, $f_{SAMPLE}$ = 125 MSPS

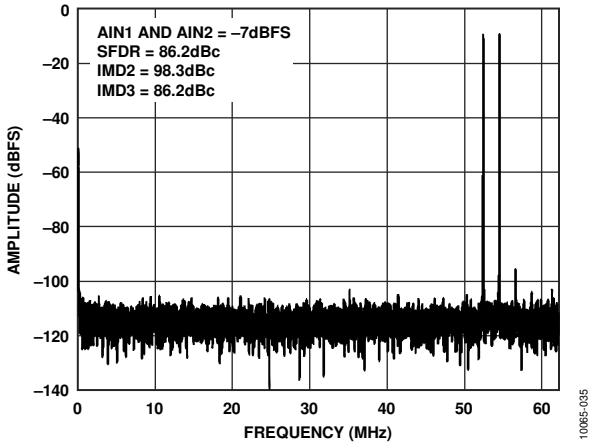


Figure 37. Two-Tone 16k FFT with $f_{IN1}$ = 70.5 MHz and $f_{IN2}$ = 72.5 MHz, $f_{SAMPLE}$ = 125 MSPS

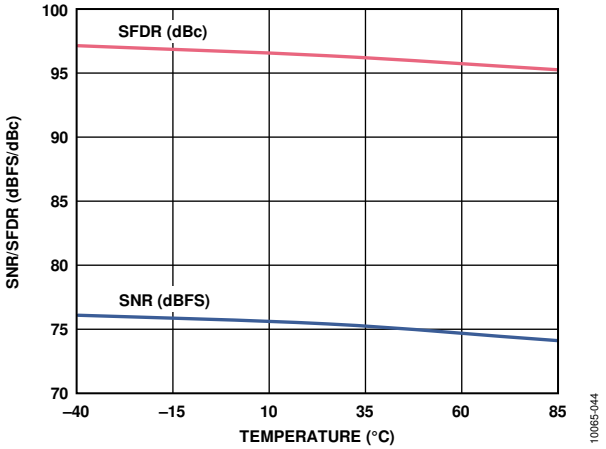


Figure 40. SNR/SFDR vs. Temperature, $f_{IN}$ = 10.3 MHz, $f_{SAMPLE}$ = 125 MSPS

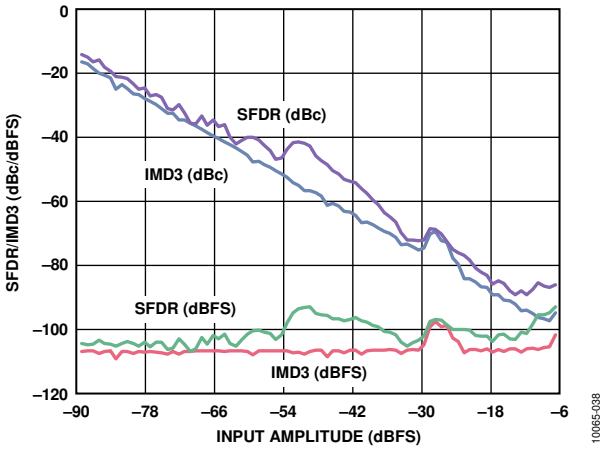


Figure 38. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with $f_{IN1}$ = 70.5 MHz and $f_{IN2}$ = 72.5 MHz, $f_{SAMPLE}$ = 125 MSPS

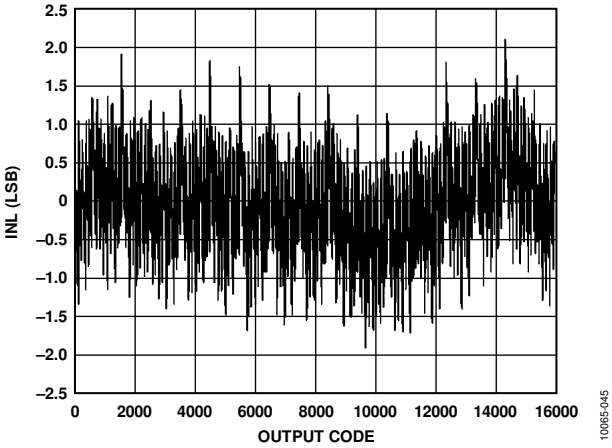


Figure 41. INL, $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 125 MSPS

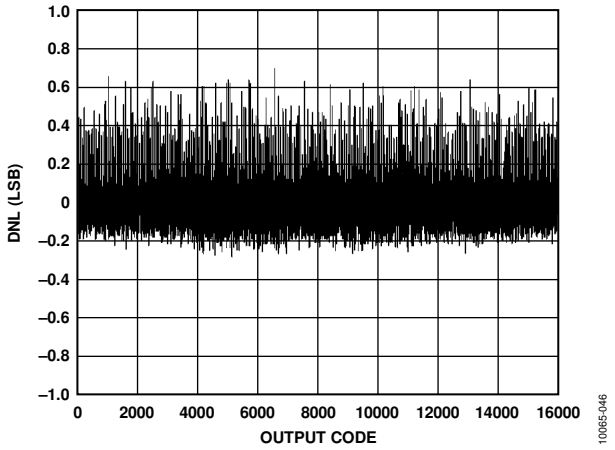


Figure 42. DNL, $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 125 MSPS

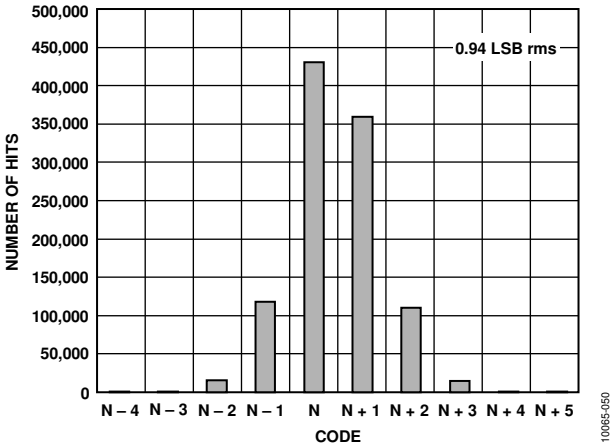


Figure 43. Input-Referred Noise Histogram, $f_{SAMPLE}$ = 125 MSPS

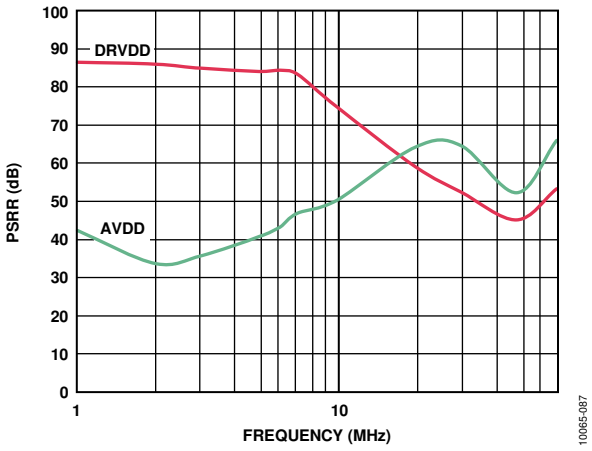


Figure 44. PSRR vs. Frequency, $f_{CLK}$ = 125 MHz, $f_{SAMPLE}$ = 125 MSPS

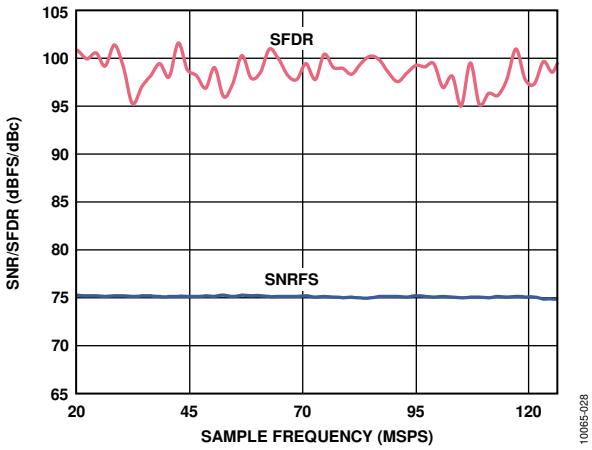


Figure 45. SNR/SFDR vs. Encode, $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 125 MSPS

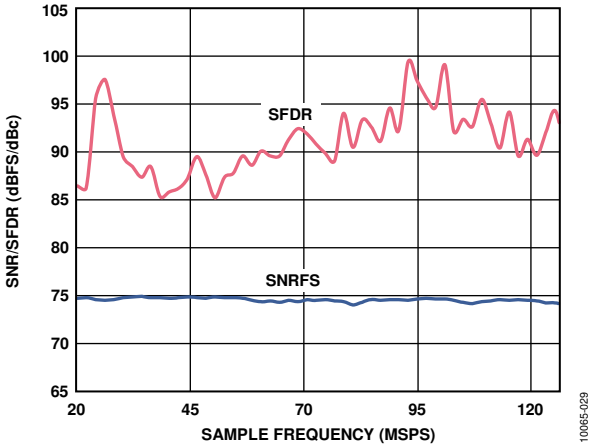


Figure 46. SNR/SFDR vs. Encode, $f_{IN}$ = 70 MHz, $f_{SAMPLE}$ = 125 MSPS

# EQUIVALENT CIRCUITS

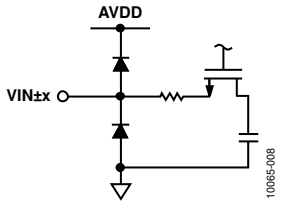


Figure 47. Equivalent Analog Input Circuit

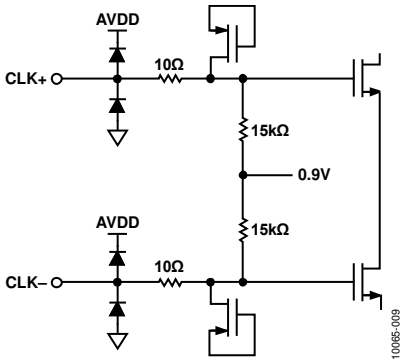


Figure 48. Equivalent Clock Input Circuit

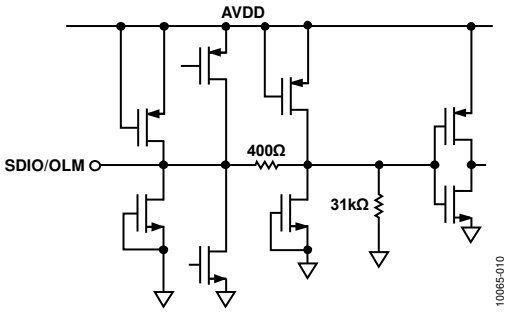


Figure 49. Equivalent SDIO/OLM Input Circuit

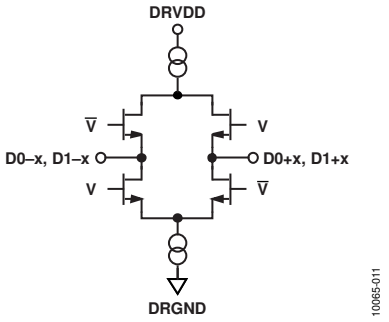


Figure 50. Equivalent Digital Output Circuit

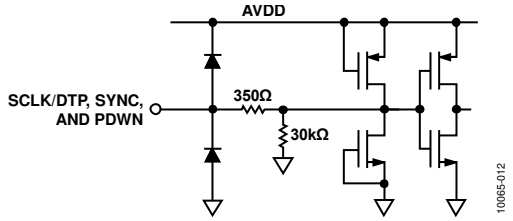


Figure 51. Equivalent SCLK/DTP, SYNC, and PDWN Input Circuit

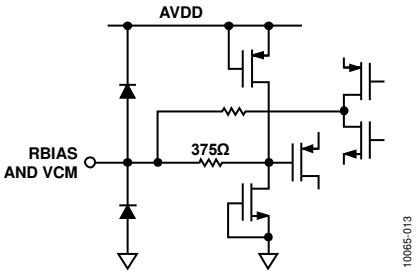


Figure 52. Equivalent RBIAS and VCM Circuit

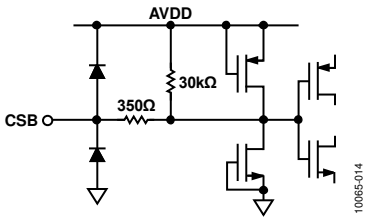


Figure 53. Equivalent CSB Input Circuit

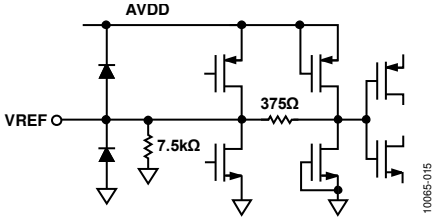


Figure 54. Equivalent VREF Circuit

# THEORY OF OPERATION

The AD9253 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The serializer transmits this converted data in a 16-bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

## ANALOG INPUT CONSIDERATIONS

The analog input to the AD9253 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

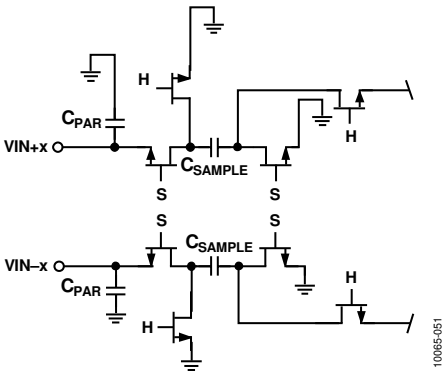


*Figure 55. Switched-Capacitor Input Circuit*

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 55). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and therefore achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

### *Input Common Mode*

The analog inputs of the AD9253 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM}$ = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 56.

An on-chip, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9253, the largest input span available is 2 V p-p.

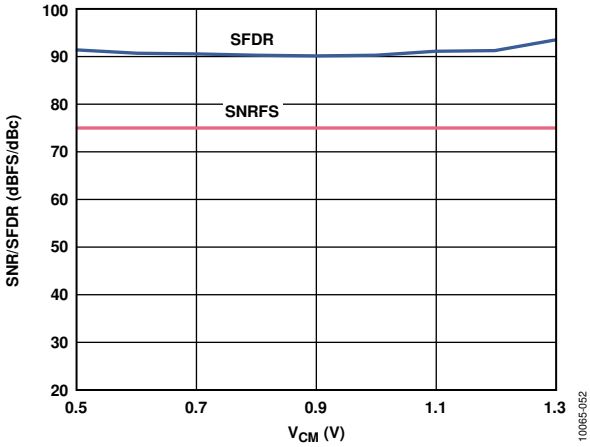


*Figure 56. SNR/SFDR vs. Common-Mode Voltage, $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 125 MSPS*

### *Differential Input Configurations*

There are several ways to drive the AD9253 either actively or passively. However, optimum performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the AD9253 provides excellent performance and a flexible interface to the ADC (see Figure 58) for baseband applications.

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 59), because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9253.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is not recommended to drive the AD9253 inputs single-ended.

## VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9253. VREF can be configured using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the Internal Reference Connection section and the External Reference Operation section. The VREF pin should be externally decoupled to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

### *Internal Reference Connection*

A comparator within the AD9253 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 57), setting VREF to 1.0 V.

**Table 9. Reference Configuration Summary**

| Selected Mode | SENSE Voltage (V) | Resulting VREF (V) | Resulting Differential Span (V p-p) |
|---|---|---|---|
| Fixed Internal Reference | AGND to 0.2 | 1.0 internal | 2.0 |
| Fixed External Reference | AVDD | 1.0 applied to external VREF pin | 2.0 |

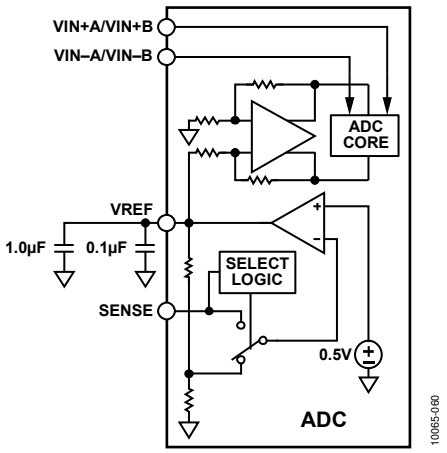


*Figure 57. Internal Reference Configuration*

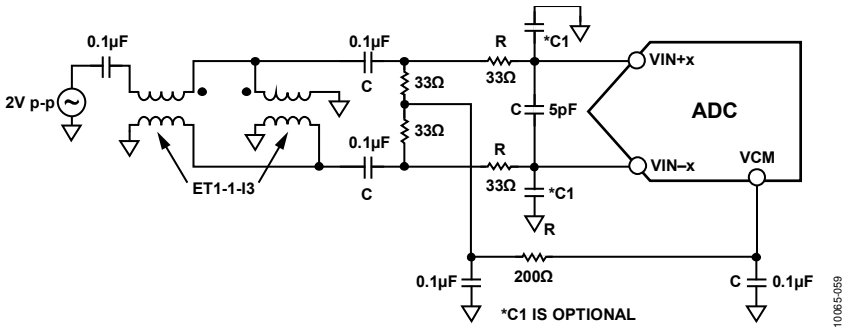


*Figure 58. Differential Double Balun Input Configuration for Baseband Applications*

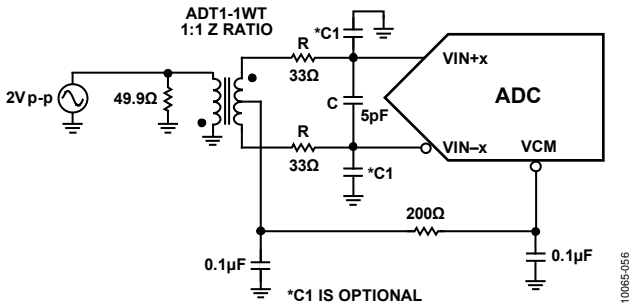


*Figure 59. Differential Transformer-Coupled Configuration for Baseband Applications*

If the internal reference of the AD9253 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 60 shows how the internal reference voltage is affected by loading.

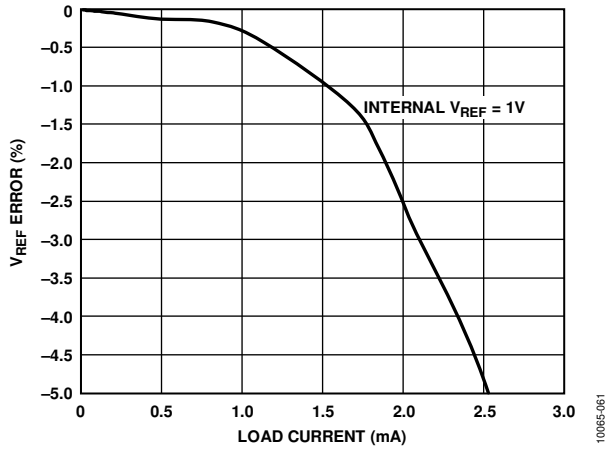


*Figure 60. $V_{REF}$ Error vs. Load Current*

### External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 61 shows the typical drift characteristics of the internal reference in 1.0 V mode.

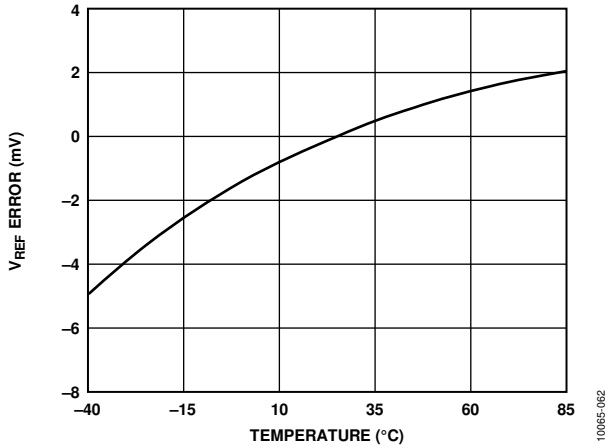


*Figure 61. Typical $V_{REF}$ Drift*

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load (see Figure 54). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.0 V.

It is not recommended to leave the SENSE pin floating.

## CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9253 sample clock inputs, CLK+ and CLK–, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally (see Figure 48) and require no external bias.

### Clock Input Options

The AD9253 has a flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 62 and Figure 63 show two preferred methods for clocking the AD9253 (at clock rates up to 1 GHz prior to internal CLK divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 1 GHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The antiparallel Schottky diodes across the transformer/balun secondary winding limit clock excursions into the AD9253 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9253 while preserving the fast rise and fall times of the signal that are critical to achieving low jitter performance. However, the diode capacitance comes into play at frequencies above 500 MHz. Care must be taken in choosing the appropriate signal limiting diode.

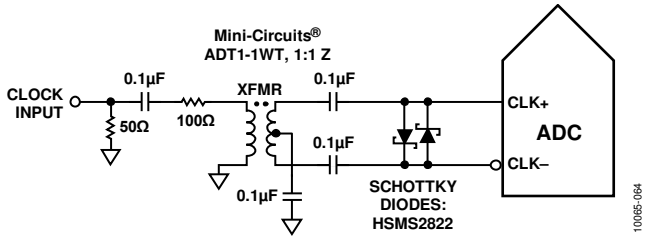


*Figure 62. Transformer-Coupled Differential Clock (Up to 200 MHz)*

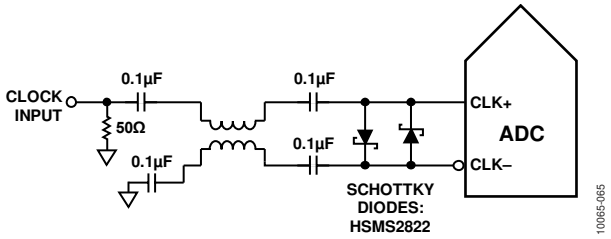


*Figure 63. Balun-Coupled Differential Clock (Up to 1 GHz)*

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 65. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 clock drivers offer excellent jitter performance.

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 66. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 clock drivers offer excellent jitter performance.

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK– pin to ground with a 0.1 µF capacitor (see Figure 67).

### *Input Clock Divider*

The AD9253 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8.

The AD9253 clock divider can be synchronized using the external SYNC input. Bit 0 and Bit 1 of Register 0x109 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

### *Clock Duty Cycle*

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9253 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9253. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS on, as shown in Figure 64.

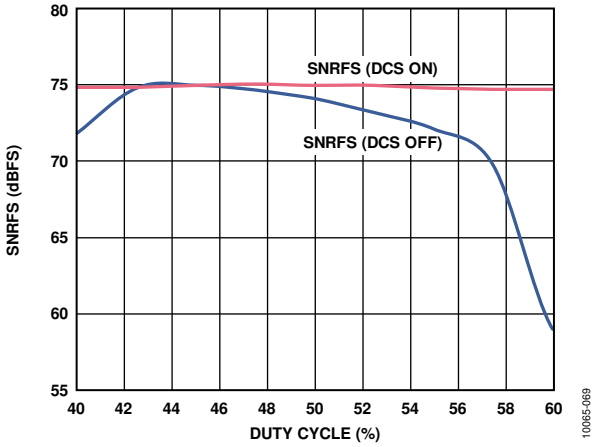


*Figure 64. SNR vs. DCS On/Off*

Jitter in the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

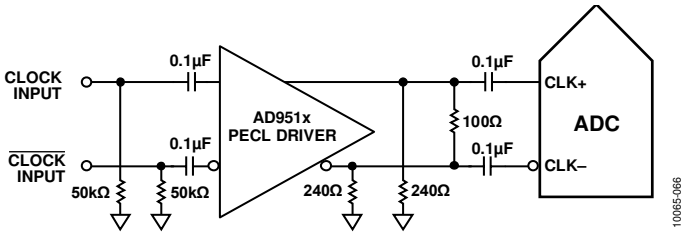


*Figure 65. Differential PECL Sample Clock (Up to 1 GHz)*

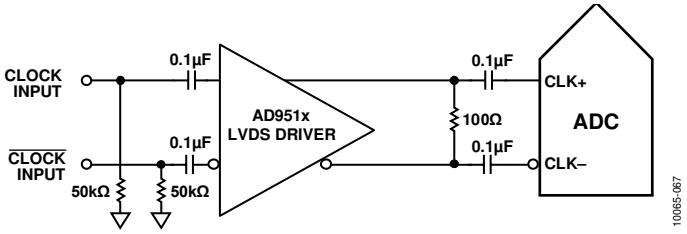


*Figure 66. Differential LVDS Sample Clock (Up to 1 GHz)*

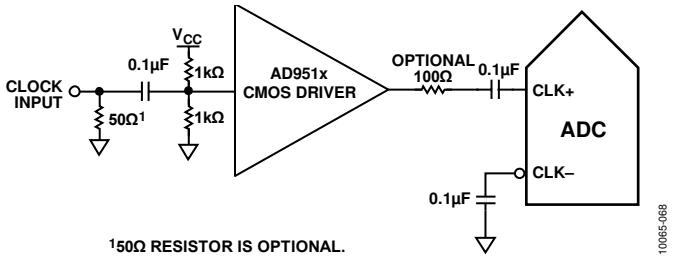


*Figure 67. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)*