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FEATURES

- Monolithic 16-bit, oversampled A/D converter**
- 8× oversampling mode, 20 MSPS clock**
- 2.5 MHz output word rate**
- 1.01 MHz signal passband with 0.004 dB ripple**
- Signal-to-noise ratio: 88.5 dB**
- Total harmonic distortion: -96 dB**
- Spurious-free dynamic range: 100 dB**
- Input referred noise: 0.6 LSB**
- Selectable oversampling ratio: 1×, 2×, 4×, 8×**
- Selectable power dissipation: 150 mW to 585 mW**
- 85 dB stop-band attenuation**
- 0.004 dB pass-band ripple**
- Linear phase**
- Single 5 V analog supply, 5 V/3 V digital supply**
- Synchronize capability for parallel ADC interface**
- Twos complement output data**
- 44-lead MQFP**

PRODUCT DESCRIPTION

The AD9260 is a 16-bit, high-speed oversampled analog-to-digital converter (ADC) that offers exceptional dynamic range over a wide bandwidth. The AD9260 is manufactured on an advanced CMOS process. High dynamic range is achieved with an oversampling ratio of 8× through the use of a proprietary technique that combines the advantages of sigma-delta and pipeline converter technologies. The AD9260 is a switched-capacitor ADC with a nominal full-scale input range of 4 V. It offers a differential input with 60 dB of common-mode rejection of common-mode signals. The signal range of each differential input is ±1 V centered on a 2.0 V common-mode level.

The on-chip decimation filter is configured for maximum performance and flexibility. A series of three half-band FIR filter stages provide 8× decimation filtering with 85 dB of stop-band attenuation and 0.004 dB of pass-band ripple. An onboard digital multiplexer allows the user to access data from the various stages of the decimation filter. The on-chip programmable reference and reference buffer amplifier are configured for maximum accuracy and flexibility. An external reference can also be chosen to suit the user's specific dc accuracy and drift requirements.

The AD9260 operates on a single +5 V supply, typically consuming 585 mW of power. A power scaling circuit is provided allowing the AD9260 to operate at power consump-

Rev. C

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FUNCTIONAL BLOCK DIAGRAM

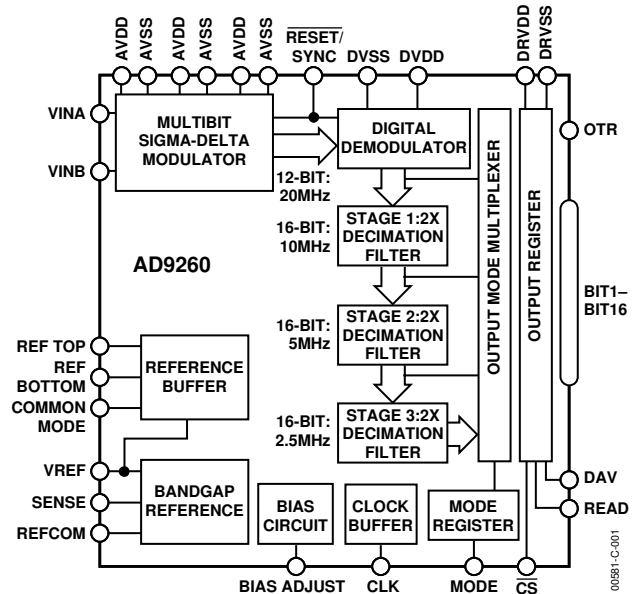


Figure 1.

tion levels as low as 150 mW at reduced clock and data rates. The AD9260 is available in a 44-lead MQFP package and is specified to operate over the industrial temperature range.

PRODUCT HIGHLIGHTS

The AD9260 is fabricated on a very cost effective CMOS process. High speed, precision, mixed-signal analog circuits are combined with high density digital filter circuits. The AD9260 offers a complete single-chip 16-bit sampling ADC with a 2.5 MHz output data rate in a 44-lead MQFP.

Selectable Internal Decimation Filtering—The AD9260 provides a high performance decimation filter with 0.004 dB pass-band ripple and 85 dB of stop-band attenuation. The filter is configurable with options for 1×, 2×, 4×, and 8× decimation.

Power Scaling—The AD9260 consumes a low 585 mW of power at 16-bit resolution and 2.5 MHz output data rate. Its power can be scaled down to as low as 150 mW at reduced clock rates.

Single Supply—Both the analog and digital portions of the AD9260 can operate off of a single +5 V supply, simplifying system power supply design. The digital logic will also accommodate a single +3 V supply for reduced power.

AD9260* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-202: An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change
- AN-282: Fundamentals of Sampled Data Systems
- AN-311: How to Reliably Protect CMOS Circuits Against Power Supply Overvoltage
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-397: Electrically Induced Damage to Standard Linear Integrated Circuits:
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9260: High Speed Oversampling CMOS ADC with 16-Bit Resolution at a 2.5 MHz Output Word Rate Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC
- Understanding Continuous-Time, Discrete-Time Sigma-Delta ADCs And Nyquist ADCs

DESIGN RESOURCES

- AD9260 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9260 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

7/04—Changed from Rev. B to Rev. C

Changed “trimpot” to “variable resistor”	Universal
Updated Format	Universal
Updated Outline Dimensions	43
Changes to Ordering Guide	43

5/00—Changed from Rev. A to Rev. B.

1/98—Changed from Rev. 0 to Rev. A.

SPECIFICATIONS

CLOCK INPUT FREQUENCY RANGE

Table 1.

Parameter—Decimation Factor (N)	AD9260 (8)	AD9260 (4)	AD9260 (2)	AD9260 (1)	Unit
CLOCK INPUT (Modulator Sample Rate, f_{CLOCK})	1	1	1	1	kHz min
	20	20	20	20	MHz max
OUTPUT WORD RATE ($FS = f_{\text{CLOCK}}/N$)	0.125	0.250	0.500	1	kHz min
	2.5	5	10	20	MHz max

DC SPECIFICATIONS

AVDD = +5 V, DVDD = +3 V, DRVDD = +3 V, $f_{\text{CLOCK}} = 20$ MSPS, $V_{\text{REF}} = +2.5$ V, Input CML = 2.0 V T_{MIN} to T_{MAX} unless otherwise noted, $R_{\text{BIAS}} = 2$ k Ω .

Table 2.

Parameter—Decimation Factor (N)	AD9260 (8)	AD9260 (4)	AD9260 (2)	AD9260 (1)	Unit
RESOLUTION	16	16	16	12	Bits min
INPUT REFERRED NOISE (TYP)					
1.0 V Reference	1.40	2.4	6.0	1.3	LSB rms typ
2.5 V Reference ¹	0.68 (90.6)	1.2 (86)	3.7 (76)	1.0 (63.2)	LSB rms typ (dB typ)
ACCURACY					
Integral Nonlinearity (INL)	± 0.75	± 0.75	± 0.75	± 0.3	LSB typ
Differential Nonlinearity (DNL)	± 0.50	± 0.50	± 0.50	± 0.25	LSB typ
No Missing Codes	16	16	16	12	Bits Guaranteed
Offset Error	0.9 (0.5)	(0.5)	(0.5)	(0.5)	% FSR max (typ @ +25°C)
Gain Error ²	2.75 (0.66)	(0.66)	(0.66)	(0.66)	% FSR max (typ @ +25°C)
Gain Error ³	1.35 (0.7)	(0.7)	(0.7)	(0.7)	% FSR max (typ @ +25°C)
TEMPERATURE DRIFT					
Offset Error	2.5	2.5	2.5	2.5	ppm/°C typ
Gain Error ²	22	22	22	22	ppm/°C typ
Gain Error ³	7.0	7.0	7.0	7.0	ppm/°C typ
POWER SUPPLY REJECTION					
AVDD, DVDD, DRVDD (+5 V ± 0.25 V)	0.06	0.06	0.06	0.06	% FSR max
ANALOG INPUT					
Input Span					
$V_{\text{REF}} = 1.0$ V	1.6	1.6	1.6	1.6	V p p Diff. max
$V_{\text{REF}} = 2.5$ V	4.0	4.0	4.0	4.0	V p p Diff. max
Input (VINA or VINB) Range	+0.5	+0.5	+0.5	+0.5	V min
	+AVDD -0.5	+AVDD -0.5	+AVDD -0.5	+AVDD -0.5	V max
Input Capacitance	10.2	10.2	10.2	10.2	pF typ
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	1	1	1	1	V typ
Output Voltage Error (1 V Mode)	± 14	± 14	± 14	± 14	mV max
Output Voltage (2.5 V Mode)	2.5	2.5	2.5	2.5	V typ
Output Voltage Error (2.5 V Mode)	± 35	± 35	± 35	± 35	mV max
Load Regulation ⁴					
1 V REF	0.5	0.5	0.5	0.5	mV max
2.5 V REF	2.0	2.0	2.0	2.0	mV max
REFERENCE INPUT RESISTANCE	8	8	8	8	k Ω
POWER SUPPLIES					
Supply Voltages					
AVDD	+5	+5	+5	+5	V ($\pm 5\%$)

AD9260

Parameter—Decimation Factor (N)	AD9260 (8)	AD9260 (4)	AD9260 (2)	AD9260 (1)	Unit
DVDD and DRVDD	+5.5 +2.7	+5.5 +2.7	+5.5 +2.7	+5.5 +2.7	V max V min
Supply Current					
IAVDD	115	115	115	115	mA typ
IDVDD	12.5	10.3	6.5	134	mA max
IDRVDD	0.450	0.850	1.7	2.4	mA typ
				3.5	mA max
				2.6	mA typ
POWER CONSUMPTION	613	608	600	585	mW typ
				630	mW max

¹ VINA and VINB connect to DUT CML.

² Including Internal 2.5 V reference.

³ Excluding Internal 2.5 V reference.

⁴ Load regulation with 1 mA load current (in addition to that required by AD9260).

AC SPECIFICATIONS

AVDD = +5 V, DVDD = +3 V, DRVDD = +3 V, f_{CLOCK} = 20 MSPS, V_{REF} = +2.5 V, Input CML = 2.0 V T_{MIN} to T_{MAX} unless otherwise noted, R_{BIAS} = 2 kΩ.

Table 3.

Parameter—Decimation Factor (N)	AD9260(8)	AD9260(4)	AD9260(2)	AD9260(1)	Unit
DYNAMIC PERFORMANCE					
INPUT TEST FREQUENCY: 100 kHz (typ)					
Signal-to-Noise Ratio (SNR)					
Input Amplitude = −0.5 dBFS	88.5	82	74	63	dB typ
Input Amplitude = −6.0 dBFS	82.5	78	68	58	dB typ
SNR and Distortion (SINAD)					
Input Amplitude = −0.5 dBFS	87.5	82	74	63	dB typ
Input Amplitude = −6.0 dBFS	82	77.5	69	58	dB typ
Total Harmonic Distortion (THD)					
Input Amplitude = −0.5 dBFS	−96	−96	−97	−98	dB typ
Input Amplitude = −6.0 dBFS	−93	−98	−96	−98	dB typ
Spurious-Free Dynamic Range (SFDR)					
Input Amplitude = −0.5 dBFS	100	98	98	88	dB typ
Input Amplitude = −6.0 dBFS	94	100	94	84	dB typ
INPUT TEST FREQUENCY: 500 kHz					
Signal to Noise Ratio (SNR)					
Input Amplitude = −0.5 dBFS	86.5	82	74	63	dB typ
	80.5				dB min
Input Amplitude = −6.0 dBFS	82.5	77	68	58	dB typ
SNR and Distortion (SINAD)					
Input Amplitude = −0.5 dBFS	86.0	81	74	63	dB typ
	80.0				dB min
Input Amplitude = −6.0 dBFS	82.0	77	68	58	dB typ
Total Harmonic Distortion (THD)					
Input Amplitude = −0.5 dBFS	−97.0	−92	−89	−86	dB typ
	−90.0				dB max
Input Amplitude = −6.0 dBFS	−95.5	−96	−89	−86	dB typ
Spurious-Free Dynamic Range (SFDR)					
Input Amplitude = −0.5 dBFS	99.0	92	91	88	dB typ
	90.0				dB max

Parameter—Decimation Factor (N)	AD9260(8)	AD9260(4)	AD9260(2)	AD9260(1)	Unit
Input Amplitude = -6.0 dBFS	98	100	91	82	dB typ
INPUT TEST FREQUENCY: 1.0 MHz (typ)					
Signal-to-Noise Ratio (SNR)					
Input Amplitude = -0.5 dBFS	85	82	74	63	dB typ
Input Amplitude = -6.0 dBFS	80	76	68	58	dB typ
SNR and Distortion (SINAD)					
Input Amplitude = -0.5 dBFS	84.5	81	74	63	dB typ
Input Amplitude = -6.0 dBFS	80	76	69	58	dB typ
Total Harmonic Distortion (THD)					
Input Amplitude = -0.5 dBFS	-102	-96	-82	-79	dB typ
Input Amplitude = -6.0 dBFS	-96	-94	-84	-77	dB typ
Spurious-Free Dynamic Range (SFDR)					
Input Amplitude = -0.5 dBFS	105	98	83	80	dB typ
Input Amplitude = -6.0 dBFS	98	96	87	80	dB typ
INPUT TEST FREQUENCY: 2.0 MHz (typ)					
Signal-to-Noise Ratio (SNR)					
Input Amplitude = -0.5 dBFS		82	74	63	dB typ
Input Amplitude = -6.0 dBFS		76	68	58	dB typ
SNR and Distortion (SINAD)					
Input Amplitude = -0.5 dBFS		81	73	62	dB typ
Input Amplitude = -6.0 dBFS		76	69	58	dB typ
Total Harmonic Distortion (THD)					
Input Amplitude = -0.5 dBFS		-101	-80	-75	dB typ
Input Amplitude = -6.0 dBFS		-95	-80	-76	dB typ
Spurious-Free Dynamic Range (SFDR)					
Input Amplitude = -0.5 dBFS		104	80	78	dB typ
Input Amplitude = -6.0 dBFS		100	83	79	dB typ
INPUT TEST FREQUENCY: 5.0 MHz (typ)					
Signal-to-Noise Ratio (SNR)					
Input Amplitude = -0.5 dBFS				59	dB typ
Input Amplitude = -6.0 dBFS				57	dB typ
SNR and Distortion (SINAD)					
Input Amplitude = -0.5 dBFS				58	dB typ
Input Amplitude = -6.0 dBFS				57	dB typ
Total Harmonic Distortion (THD)					
Input Amplitude = -0.5 dBFS				-58	dB typ
Input Amplitude = -6.0 dBFS				-67	dB typ
Spurious-Free Dynamic Range (SFDR)					
Input Amplitude = -0.5 dBFS				59	dB typ
Input Amplitude = -6.0 dBFS				70	dB typ
INTERMODULATION DISTORTION					
$f_{IN1} = 475 \text{ kHz}, f_{IN2} = 525 \text{ kHz}$	-93	-91	-91	-83	dBFS typ
$f_{IN1} = 950 \text{ kHz}, f_{IN2} = 1.050 \text{ MHz}$	-95	-86	-85	-83	dBFS typ
DYNAMIC CHARACTERISTICS					
Full Power Bandwidth	75	75	75	75	MHz typ
Small Signal Bandwidth ($A_{IN} = -20 \text{ dBFS}$)	75	75	75	75	MHz typ
Aperture Jitter	2	2	2	2	ps rms typ

AD9260

DIGITAL FILTER CHARACTERISTICS

Table 4.

Parameter	AD9260	Unit
8× DECIMATION (N = 8)		
Pass-Band Ripple	0.00125	dB max
Stop-Band Attenuation	82.5	dB min
Pass-Band	0	MHz min
	$0.605 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
Stop-Band	$1.870 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz min
	$18.130 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
Pass-Band/Transition Band Frequency		
(–0.1 dB Point)	$0.807 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
(–3.0 dB Point)	$1.136 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
Absolute Group Delay ¹	$13.55 \times (20 \text{ MHz}/f_{\text{CLOCK}})$	μs max
Group Delay Variation	0	μs max
Settling Time (to ± 0.0007%) ¹	$24.2 \times (20 \text{ MHz}/f_{\text{CLOCK}})$	μs max
4× DECIMATION (N = 4)		
Pass-Band Ripple	0.001	dB max
Stop-Band Attenuation	82.5	dB min
Pass-Band	0	MHz min
	$1.24 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
Stop-Band	$3.75 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz min
	$16.25 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
Pass-Band/Transition Band Frequency		
(–0.1 dB Point)	$1.61 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
(–3.0 dB Point)	$2.272 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
Absolute Group Delay ¹	$2.90 \times (20 \text{ MHz}/f_{\text{CLOCK}})$	μs max
Group Delay Variation	0	μs max
Settling Time (to ± 0.0007%) ¹	$5.05 \times (20 \text{ MHz}/f_{\text{CLOCK}})$	μs max
2× DECIMATION (N = 2)		
Pass-Band Ripple	0.0005	dB max
Stop-Band Attenuation	85.5	dB min
Pass-Band	0	MHz min
	$2.491 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
Stop-Band	$7.519 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz min
	$12.481 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
Pass-Band/Transition Band Frequency		
(–0.1 dB Point)	$3.231 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
(–3.0 dB Point)	$4.535 \times (f_{\text{CLOCK}}/20 \text{ MHz})$	MHz max
Absolute Group Delay ¹	$0.80 \times (20 \text{ MHz}/f_{\text{CLOCK}})$	μs max
Group Delay Variation	0	μs max
Settling Time (to ± 0.0007%) ¹	$1.40 \times (20 \text{ MHz}/f_{\text{CLOCK}})$	μs max
1× DECIMATION (N = 1)		
Propagation Delay: t_{PROP}	13	ns max
Absolute Group Delay	$(225 \times (20 \text{ MHz}/f_{\text{CLOCK}})) + t_{\text{PROP}}$	ns max

¹ To determine overall Absolute Group Delay and/or Settling Time inclusive of delay from the sigma-delta modulator, add Absolute Group Delay and/or Settling Time pertaining to specific decimation mode to the Absolute Group Delay specified in 1 × decimation.

DIGITAL FILTER CHARACTERISTICS

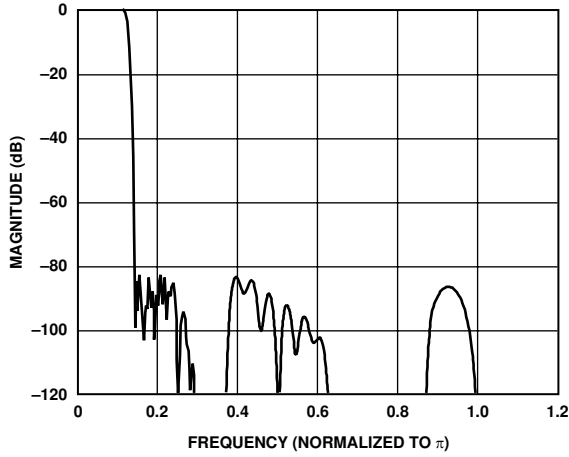


Figure 2. 8x FIR Filter Frequency Response

00581-C-002

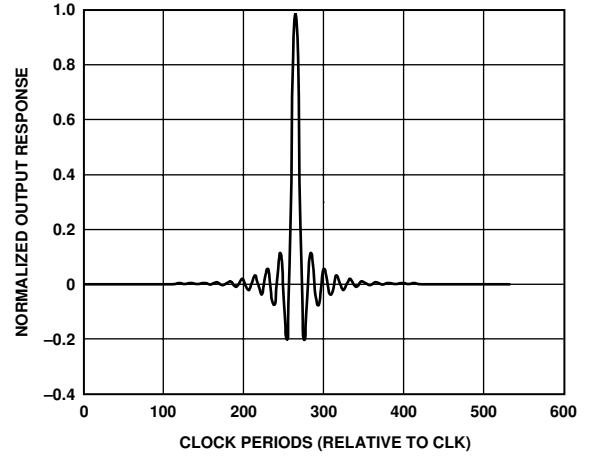


Figure 5. 8x FIR Filter Impulse Response

00581-C-005

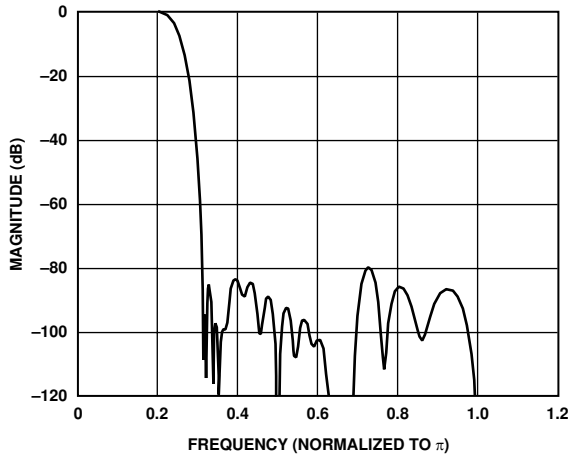


Figure 3. 4x FIR Filter Frequency Response

00581-C-003

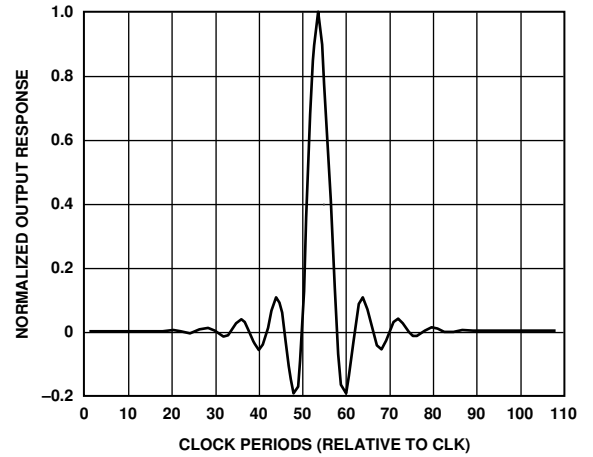


Figure 6. 4x FIR Filter Impulse Response

00581-C-006

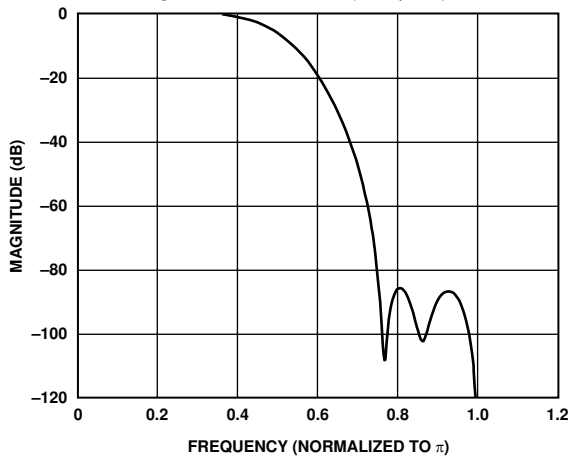


Figure 4. 2x FIR Filter Frequency Response

00581-C-004

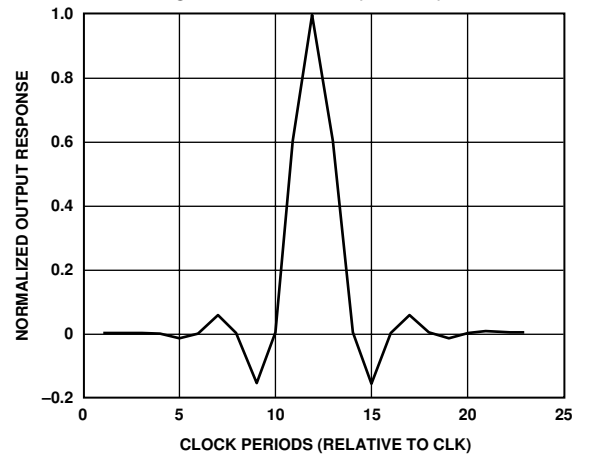


Figure 7. 2x FIR Filter Impulse Response

00581-C-007

AD9260

Table 5. Integer Filter Coefficients for First Stage Decimation Filter (23-Tap Half-Band FIR Filter)

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(23)	-1
H(2)	H(22)	0
H(3)	H(21)	13
H(4)	H(20)	0
H(5)	H(19)	-66
H(6)	H(18)	0
H(7)	H(17)	224
H(8)	H(16)	0
H(9)	H(15)	-642
H(10)	H(14)	0
H(11)	H(13)	2496
H(12)		4048

Table 6. Integer Filter Coefficients for Second Stage Decimation Filter (43-Tap Half-Band FIR Filter)

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(43)	3
H(2)	H(42)	0
H(3)	H(41)	-12
H(4)	H(40)	0
H(5)	H(39)	35
H(6)	H(38)	0
H(7)	H(37)	-83
H(8)	H(36)	0
H(9)	H(35)	172
H(10)	H(34)	0
H(11)	H(33)	-324
H(12)	H(32)	0
H(13)	H(31)	572
H(14)	H(30)	0
H(15)	H(29)	-976
H(16)	H(28)	0
H(17)	H(27)	1680
H(18)	H(26)	0
H(19)	H(25)	-3204
H(20)	H(24)	0
H(21)	H(23)	10274
H(22)		16274

NOTE: The composite filter undecimated coefficients (i.e., impulse response) in the 4× decimation mode can be determined by convolving the first stage filter taps with a “zero stuffed” version of the second stage filter taps (i.e., insert one zero between samples). Similarly, the composite filter coefficients in the 8× decimation mode can be determined by convolving the taps of the composite 4× decimation mode (as previously determined) with a “zero stuffed” version of the third stage filter taps (i.e., insert three zeros between samples).

Table 7. Integer Filter Coefficients for Third Stage Decimation Filter (107-Tap Half-Band FIR Filter)

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(107)	-1
H(2)	H(106)	0
H(3)	H(105)	2
H(4)	H(104)	0
H(5)	H(103)	-2
H(6)	H(102)	0
H(7)	H(101)	3
H(8)	H(100)	0
H(9)	H(99)	-3
H(10)	H(98)	0
H(11)	H(97)	1
H(12)	H(96)	0
H(13)	H(95)	3
H(14)	H(94)	0
H(15)	H(93)	-12
H(16)	H(92)	0
H(17)	H(91)	27
H(18)	H(90)	0
H(19)	H(89)	-50
H(20)	H(88)	0
H(21)	H(87)	85
H(22)	H(86)	0
H(23)	H(85)	-135
H(24)	H(84)	0
H(25)	H(83)	204
H(26)	H(82)	0
H(27)	H(81)	-297
H(28)	H(80)	0
H(29)	H(79)	420
H(30)	H(78)	0
H(31)	H(77)	-579
H(32)	H(76)	0
H(33)	H(75)	784
H(34)	H(74)	0
H(35)	H(73)	-1044
H(36)	H(72)	0
H(37)	H(71)	1376
H(38)	H(70)	0
H(39)	H(69)	-1797
H(40)	H(68)	0
H(41)	H(67)	2344
H(42)	H(66)	0
H(43)	H(65)	-3072
H(44)	H(64)	0
H(45)	H(63)	4089
H(46)	H(62)	0
H(47)	H(61)	-5624
H(48)	H(60)	0
H(49)	H(59)	8280
H(50)	H(58)	0
H(51)	H(57)	-14268
H(52)	H(56)	0
H(53)	H(55)	43520
H(54)		68508

DIGITAL SPECIFICATIONS

AVDD = +5 V, DVDD = +5 V, T_{MIN} to T_{MAX} unless otherwise noted.

Table 8.

Parameter	AD9260	Unit
CLOCK¹ AND LOGIC INPUTS		
High Level Input Voltage (DVDD = +5 V)	+3.5	V min
(DVDD = +3 V)	+2.1	V max
Low Level Input Voltage (DVDD = +5 V)	+1.0	V min
(DVDD = +3 V)	+0.9	V max
High Level Input Current (V _{IN} = DVDD)	± 10	µA max
Low Level Input Current (V _{IN} = 0 V)	± 10	µA max
Input Capacitance	5	pF typ
LOGIC OUTPUTS (with DRVDD = 5 V)		
High Level Output Voltage (I _{OH} = 50 µA)	+4.5	V min
High Level Output Voltage (I _{OH} = 0.5 mA)	+2.4	V min
Low Level Output Voltage ² (I _{OL} = 0.3 mA)	+0.4	V max
Low Level Output Voltage (I _{OL} = 50 µA)	+0.1	V max
Output Capacitance	5	pF typ
LOGIC OUTPUTS (with DRVDD = 3 V)		
High Level Output Voltage (I _{OH} = 50 µA)	+2.4	V min
Low Level Output Voltage (I _{OL} = 50 µA)	+0.7	V max

¹ Since CLK is referenced to AVDD, +5 V logic input levels only apply.

² The AD9260 is not guaranteed to meet V_{OL} = 0.4 V max for standard TTL load of I_{OL} = 1.6 mA.

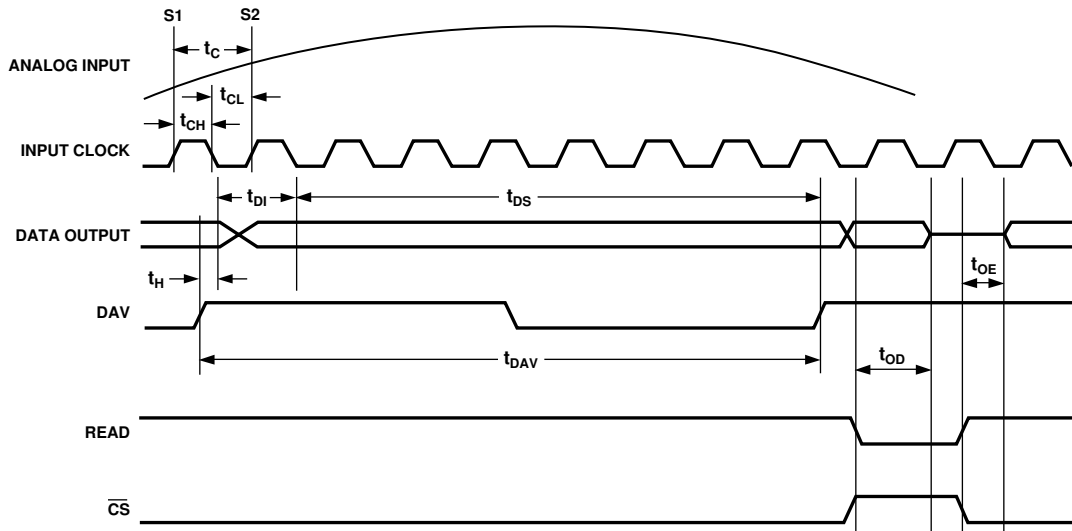


Figure 8. Timing Diagram

00581-C-008

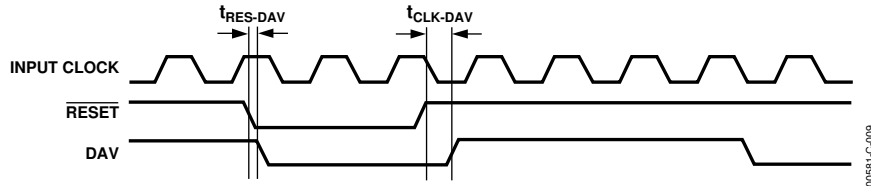


Figure 9. \overline{RESET} Timing Diagram

00891-C-009

SWITCHING SPECIFICATIONS

AVDD = +5 V, DVDD = +5 V, $C_L = 20$ pF, T_{MIN} to T_{MAX} unless otherwise noted.

Table 9.

Parameters	Symbol	AD9260	Unit
Clock Period	t_c	50	ns min
Data Available (DAV) Period	t_{DAV}	$t_c \times Mode$	ns min
Data Invalid	t_{DI}	40% t_{DAV}	ns max
Data Set-Up Time	t_{DS}	$t_{DAV} - t_H - t_{DI}$	ns min
Clock Pulse-Width High	t_{CH}	22.5	ns min
Clock Pulse-Width Low	t_{CL}	22.5	ns min
Data Hold Time	t_H	3.5	ns min
\overline{RESET} to DAV Delay	$t_{RES-DAV}$	10	ns typ
CLOCK to DAV Delay	$t_{CLK-DAV}$	15	ns typ
Three-State Output Disable Time	t_{OD}	8	ns typ
Three-State Output Enable Time	t_{OE}	45	ns typ

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
AVDD to AVSS	-0.3 V to +6.5 V
DVDD to DVSS	-0.3 V to +6.5 V
AVSS to DVSS	-0.3 V to +0.3 V
AVDD to DVDD	-6.5 V to +6.5 V
DRVDD to DRVSS	-0.3 V to +6.5 V
DRVSS to AVSS	-0.3 V to +0.3 V
REFCOM to AVSS	-0.3 V to +0.3 V
CLK, MODE, READ, \overline{CS} , and \overline{RESET} to DVSS	-0.3 V to DVDD + 0.3 V
Digital Outputs to DRVSS	-0.3 V to DRVDD + 0.3 V
VINA, VINB, CML, and BIAS to AVSS	-0.3 V to AVDD + 0.3 V
VREF to AVSS	-0.3 V to AVDD + 0.3 V
SENSE to AVSS	-0.3 V to AVDD + 0.3 V
CAPB and CAPT to AVSS	-0.3 V to AVDD + 0.3 V
Junction Temperature	150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (10 s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

44-Lead MQFP

$\theta_{JA} = 53.2^{\circ}\text{C}/\text{W}$

$\theta_{JC} = 19^{\circ}\text{C}/\text{W}$

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TERMINOLOGY

Integral Nonlinearity (INL)

INL refers to the deviation of each individual code from a line drawn from “negative full scale” through “positive full scale.” The point used as “negative full scale” occurs 1/2 LSB before the first code transition. “Positive full scale” is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 14-bit resolution indicates that all 16384 codes, respectively, must be present over all operating ranges.

NOTE: Conventional INL and DNL measurements don't really apply to $\Sigma\Delta$ converters: the DNL looks continually better if longer data records are taken. For the AD9260, INL and DNL numbers are given as representative.

Zero Error

The major carry transition should occur for an analog value 1/2 LSB below $V_{INA} = V_{INB}$. Zero error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference and the ideal difference between first and last code transitions.

Temperature Drift

The temperature drift for zero error and gain error specifies the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX} .

Power Supply Rejection

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Aperture Jitter

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

Signal-to-Noise and Distortion (S/N+D, SINAD) Ratio

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, it is possible to get a measure of performance expressed as N , the effective number of bits:

$$N = (SINAD - 1.76)/6.02$$

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

Two-Tone SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

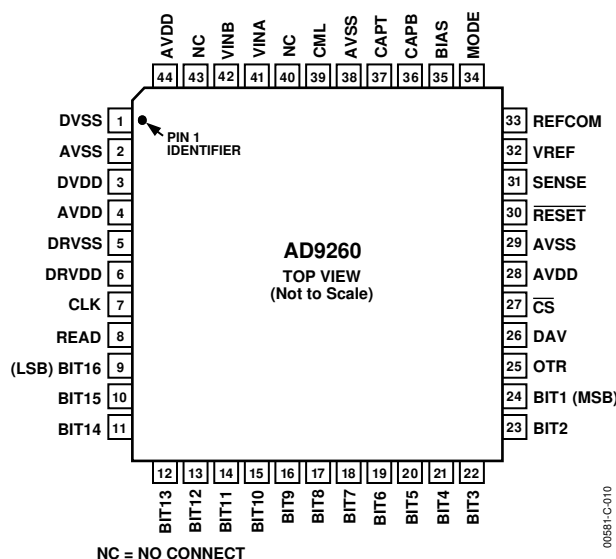


Figure 10. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DVSS	Digital Ground.
2, 29, 38	AVSS	Analog Ground.
3	DVDD	+3 V to +5 V Digital Supply.
4, 28, 44	AVDD	+5 V Analog Supply.
5	DRVSS	Digital Output Driver Ground.
6	DRVDD	+3 V to +5 V Digital Output Driver Supply.
7	CLK	Clock Input.
8	READ	Part of DSP Interface—Pull Low to Disable Output Bits.
9	BIT16	Least Significant Data Bit (LSB).
10–23	BIT15–BIT2	Data Output Bit.
24	BIT1	Most Significant Data Bit (MSB).
25	OTR	Out of Range—Set When Converter or Filter Overflows.
26	DAV	Data Available.
27	\overline{CS}	Chip Select (CS): Active LOW.
30	\overline{RESET}	\overline{RESET} : Active LOW.
31	SENSE	Reference Amplifier SENSE: Selects REF Level.
32	VREF	Input Span Select Reference I/O.
33	REFCOM	Reference Common.
34	MODE	Mode Select—Selects Decimation Mode.
35	BIAS	Power Bias.
36	CAPB	Noise Reduction Pin—Decouples Reference Level.
37	CAPT	Noise Reduction Pin—Decouples Reference Level.
39	CML	Common-Mode Level (AVDD/2.5).
40, 43	NC	No Connect (Ground for Shielding Purposes).
41	VINA	Analog Input Pin (+).
42	VINB	Analog Input Pin (-).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = DVDD = DRVDD = +5.0 V, 4 V Input Span, Differential DC Coupled Input with CML = 2.0 V, $f_{\text{CLOCK}} = 20 \text{ MSPS}$, Full Bias.

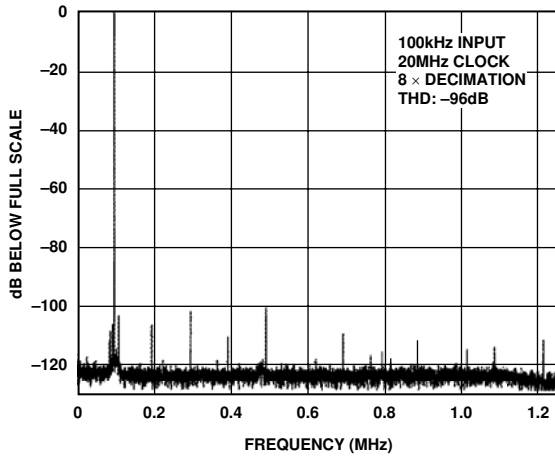


Figure 11. Spectral Plot of the AD9260 at 100 kHz Input, 20 MHz Clock, 8x OSR (2.5 MHz Output Data Rate)

00581-C-011

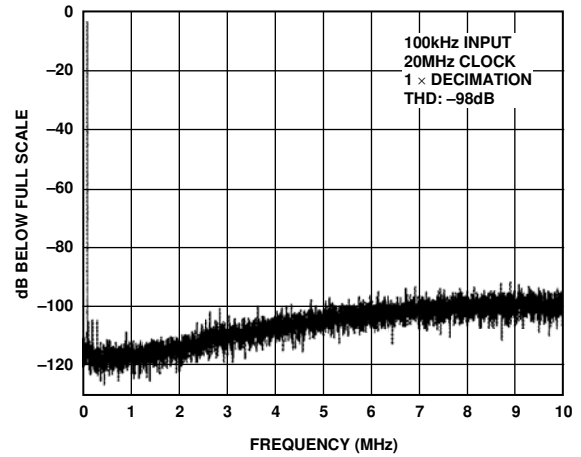


Figure 14. Spectral Plot of the AD9260 at 100 kHz Input, 20 MHz Clock, Undecimated (20 MHz Output Data Rate)

00581-C-014

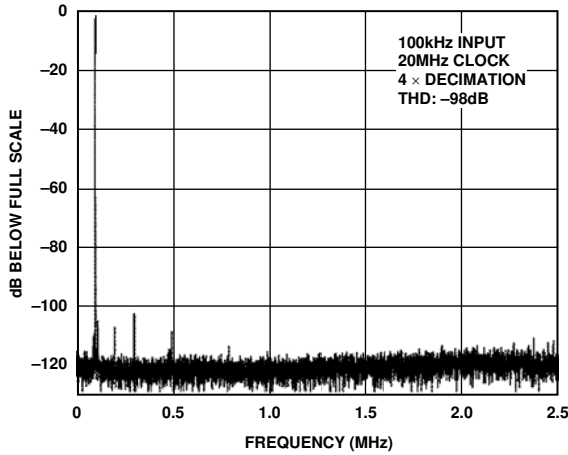


Figure 12. Spectral Plot of the AD9260 at 100 kHz Input, 20 MHz Clock, 4x OSR (5 MHz Output Data Rate)

00581-C-012

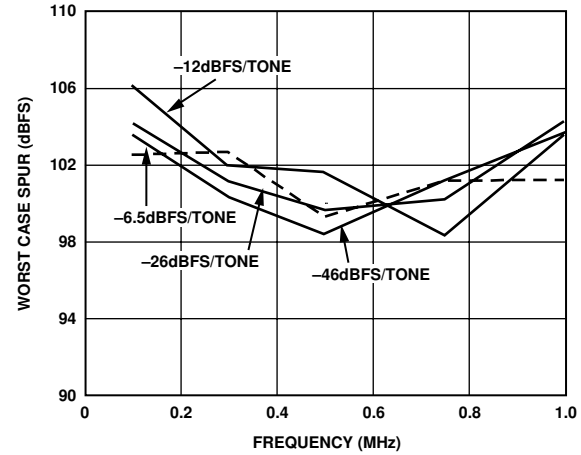


Figure 15. Dual-Tone SFDR vs. Input Frequency ($F_1 = F_2$, Span = 10% Center Frequency, Mode = 8x)

00581-C-015

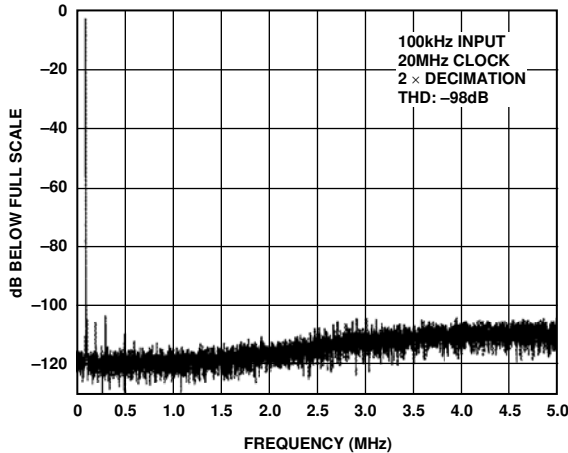


Figure 13. Spectral Plot of the AD9260 at 100 kHz Input, 20 MHz Clock, 2x OSR (10 MHz Output Data Rate)

00581-C-013

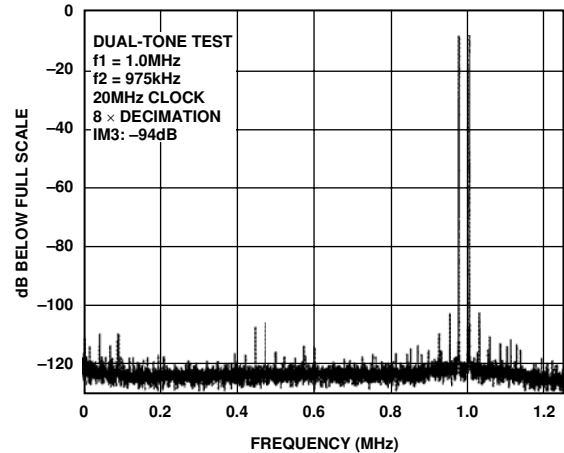


Figure 16. Two-Tone Spectral Performance of the AD9260 Given Inputs at 975 kHz and 1.0 MHz, 20 MHz Clock, 8x Decimation

00581-C-016

TYPICAL AC CHARACTERIZATION CURVES VS. DECIMATION MODE

AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, Differential DC Coupled Input with CML = 2 V, A_{IN} = 0.5 dBFS Full Bias.

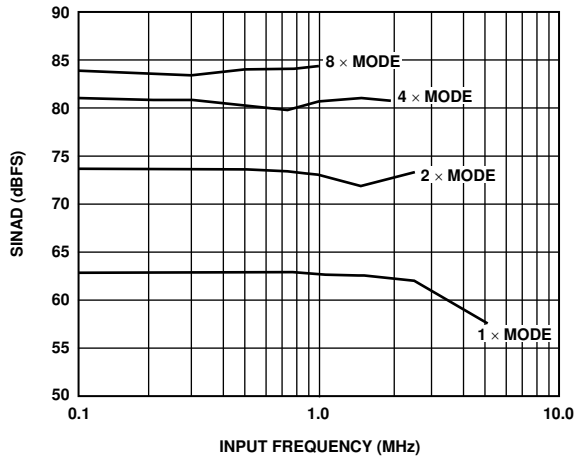


Figure 17. SINAD vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$) 8x SINAD performance limited by noise contribution of input differential op amp driver

00581-C-017

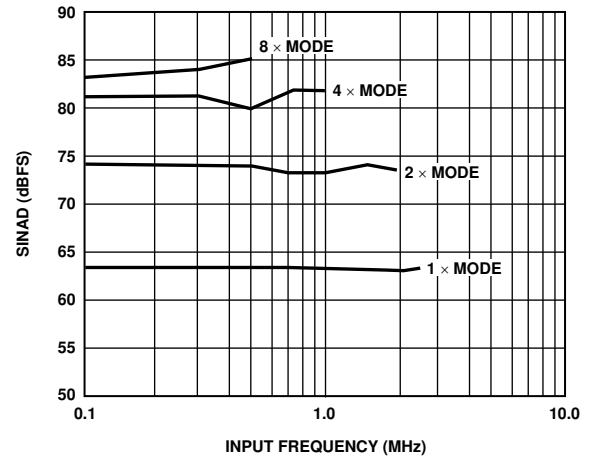


Figure 20. SINAD vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-020

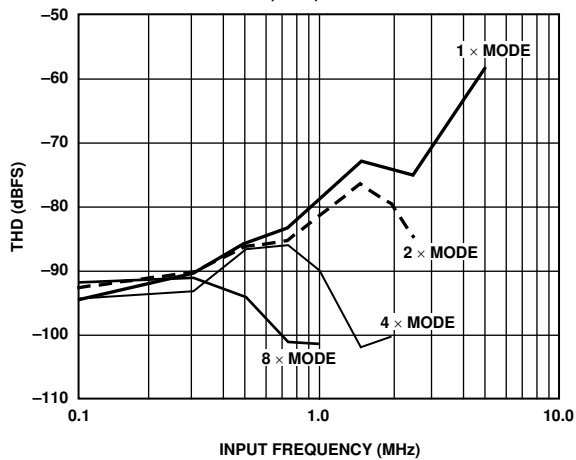


Figure 18. THD vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$)

00581-C-018

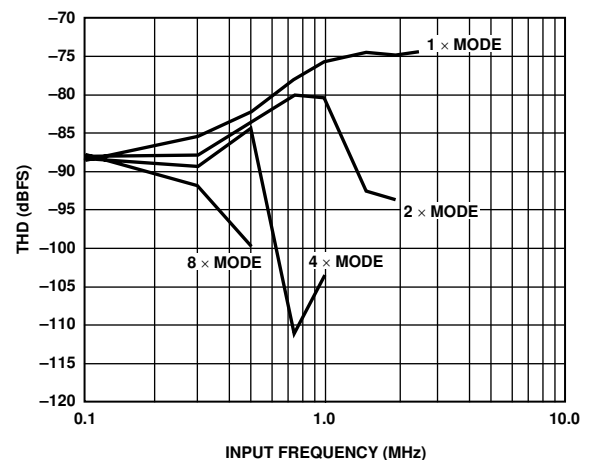


Figure 21. THD vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-021

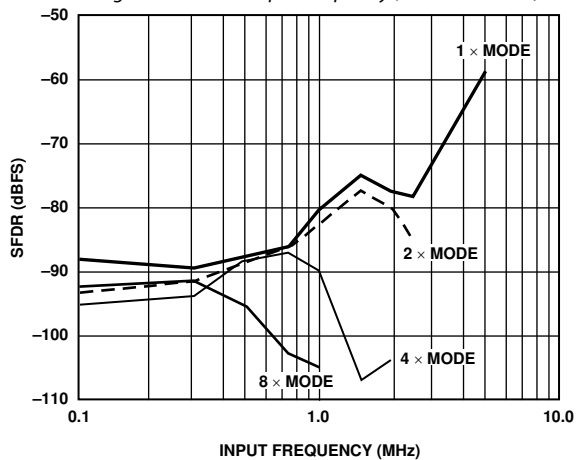


Figure 19. SFDR vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$)

00581-C-019

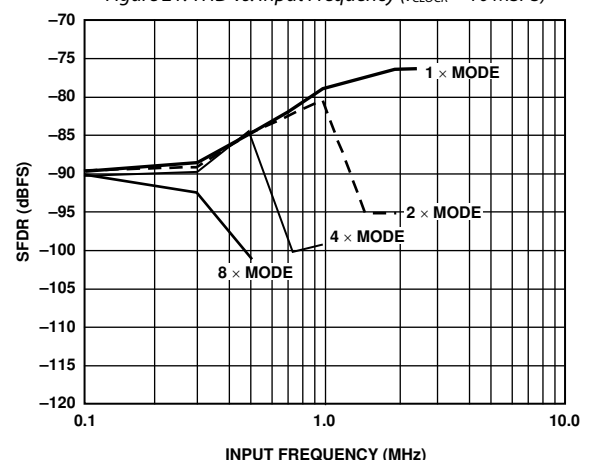


Figure 22. SFDR vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-022

TYPICAL AC CHARACTERIZATION CURVES FOR 8x MODE

AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, Differential DC Coupled Input with CML = 2 V, Full Bias.

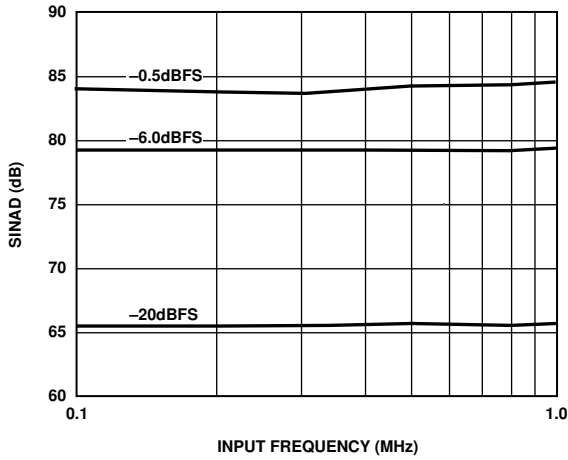


Figure 23. SINAD vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$) SINAD performance limited by noise contribution of input differential op amp driver.

00581-C-023

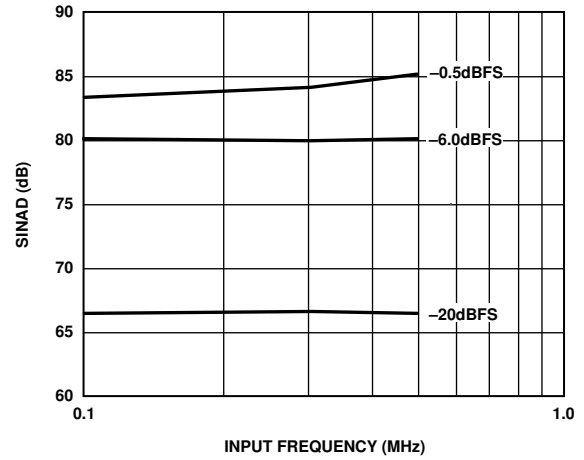


Figure 26. SINAD vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-026

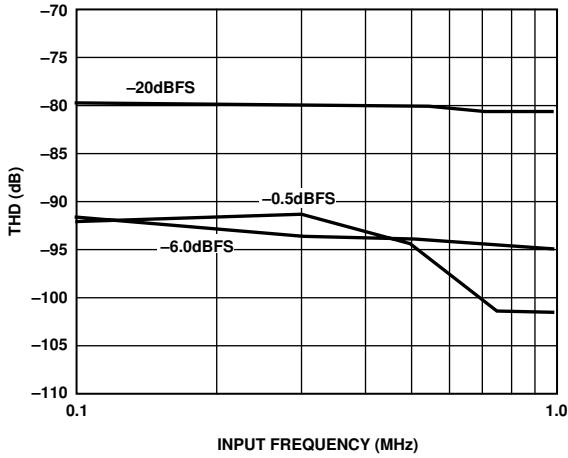


Figure 24. THD vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$)

00581-C-024

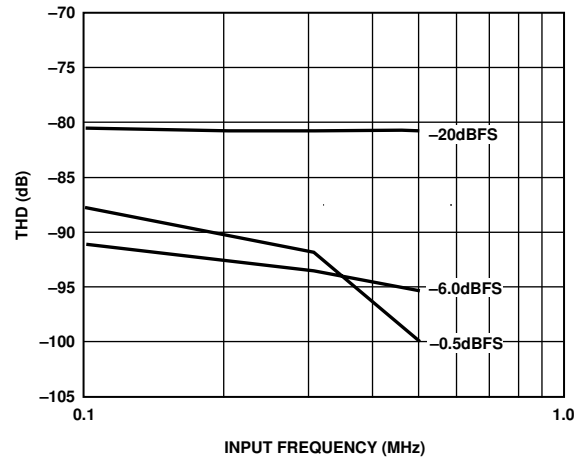


Figure 27. THD vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-027

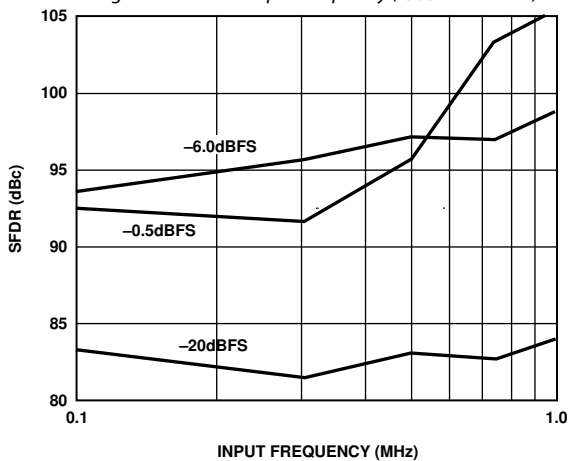


Figure 25. SFDR vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$)

00581-C-025

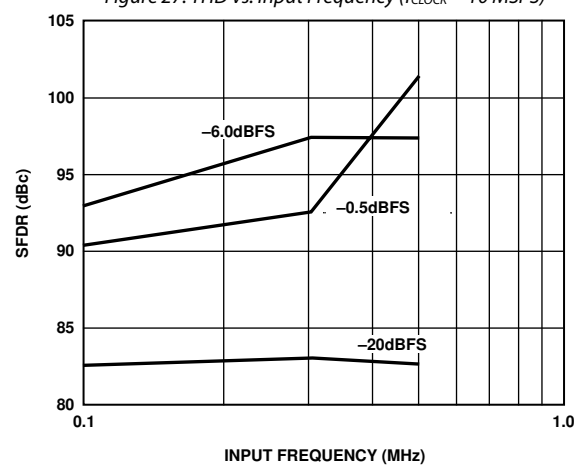


Figure 28. SFDR vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-028

TYPICAL AC CHARACTERIZATION CURVES FOR 4x MODE

AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, Differential DC Coupled Input with CML = 2 V, Full Bias.

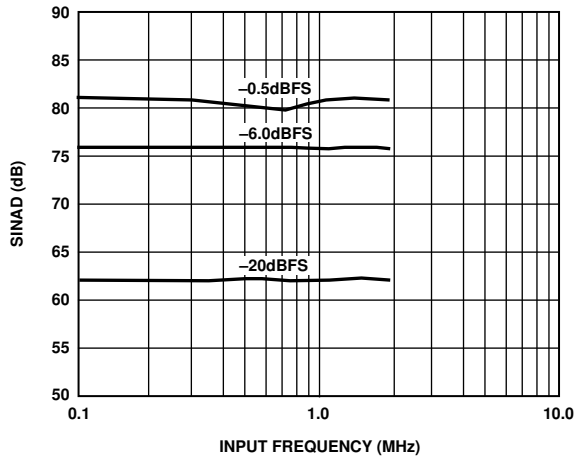


Figure 29. SINAD vs. Input Frequency ($f_{CLOCK} = 20$ MSPS)

00581-C-029

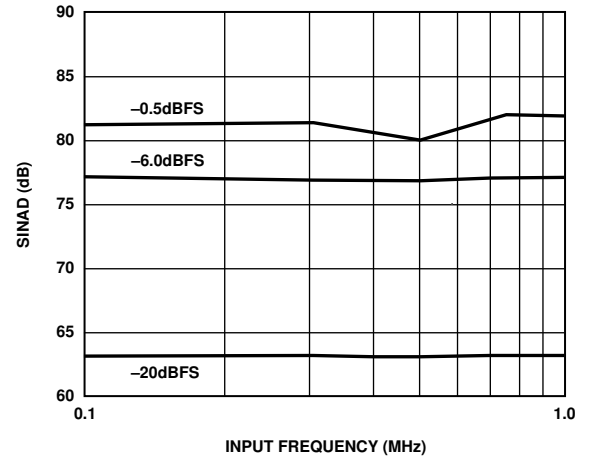


Figure 32. SINAD vs. Input Frequency ($f_{CLOCK} = 10$ MSPS)

00581-C-032

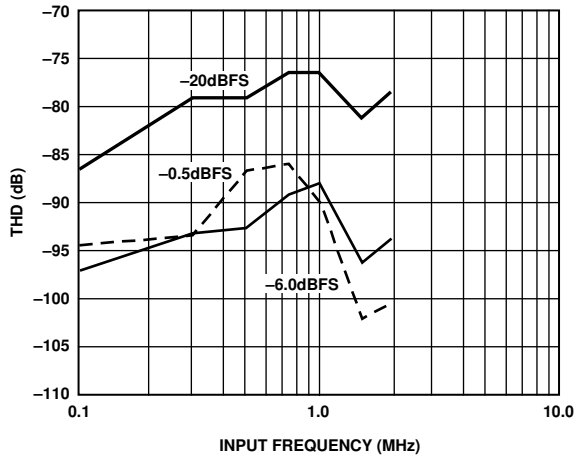


Figure 30. THD vs. Input Frequency ($f_{CLOCK} = 20$ MSPS)

00581-C-030

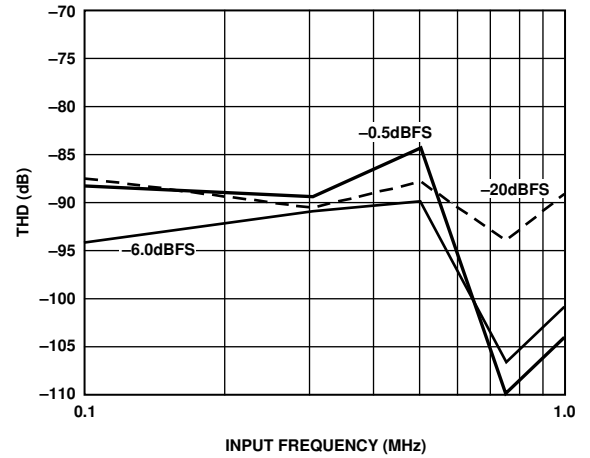


Figure 33. THD vs. Input Frequency ($f_{CLOCK} = 10$ MSPS)

00581-C-033

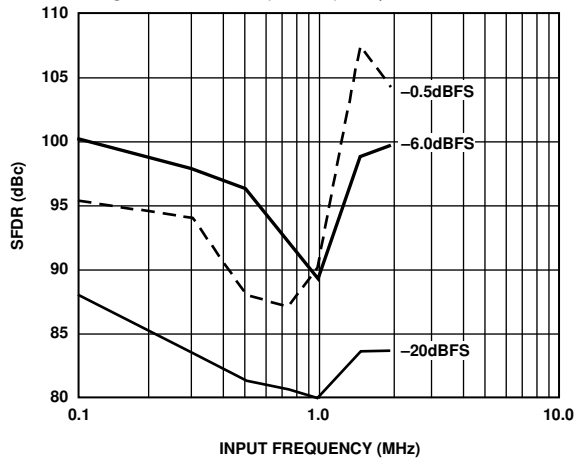


Figure 31. SFDR vs. Input Frequency ($f_{CLOCK} = 20$ MSPS)

00581-C-031

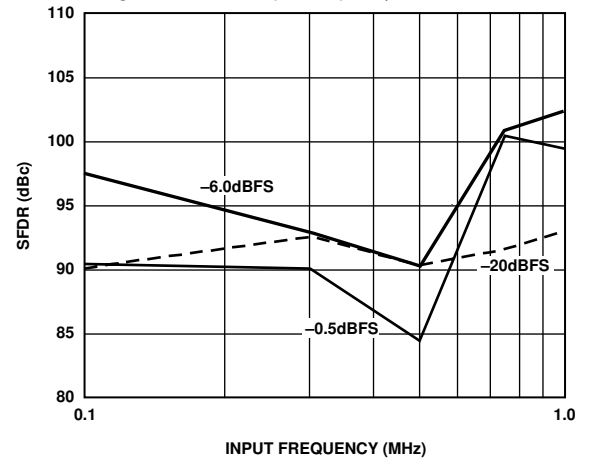


Figure 34. SFDR vs. Input Frequency ($f_{CLOCK} = 10$ MSPS)

00581-C-034

TYPICAL AC CHARACTERIZATION CURVES FOR 2x MODE

AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, Differential DC Coupled Input with CML = 2 V, Full Bias.

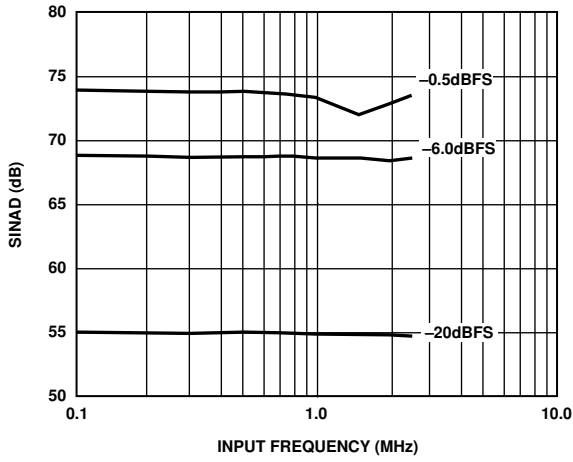


Figure 35. SINAD vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$)

00581-C-035

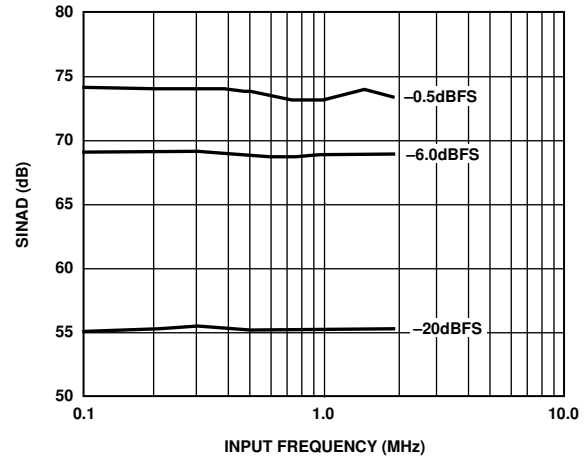


Figure 38. SINAD vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-038

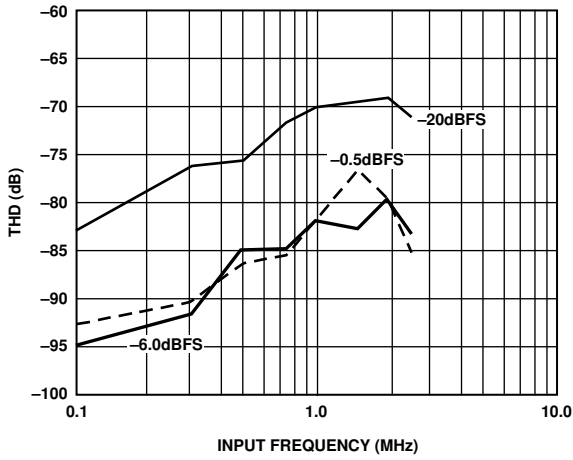


Figure 36. THD vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$)

00581-C-036

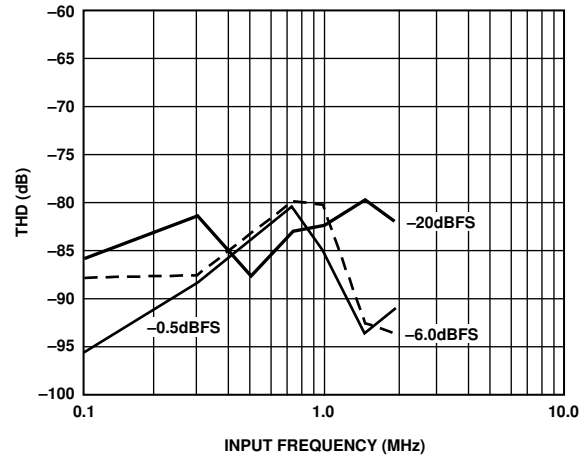


Figure 39. THD vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-039

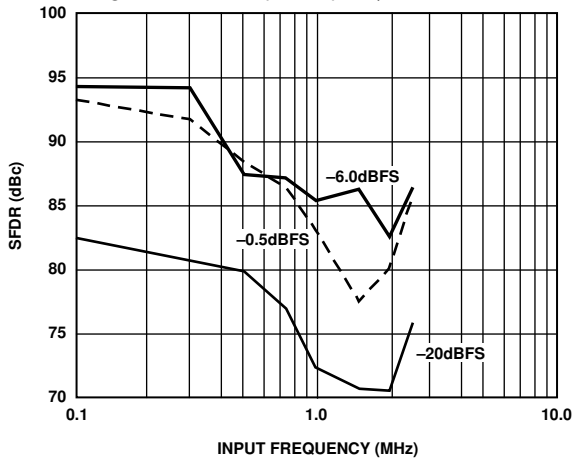


Figure 37. SFDR vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$)

00581-C-037

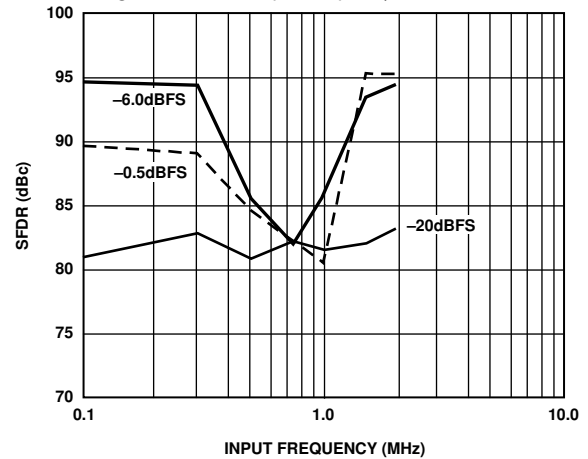


Figure 40. SFDR vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-040

TYPICAL AC CHARACTERIZATION CURVES FOR 1x MODE

AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, Differential DC Coupled Input with CML = 2 V, Full Bias.

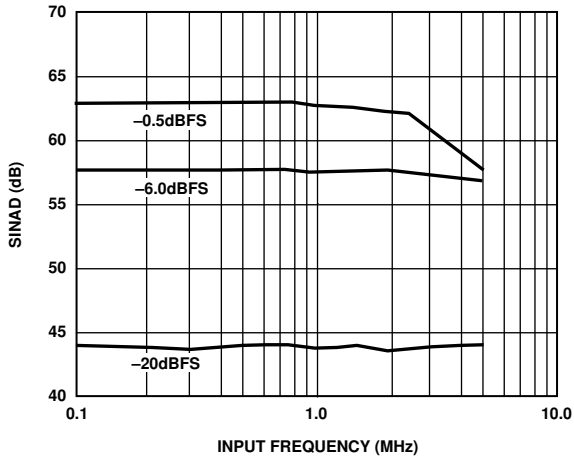


Figure 41. SINAD vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$)

00581-C-041

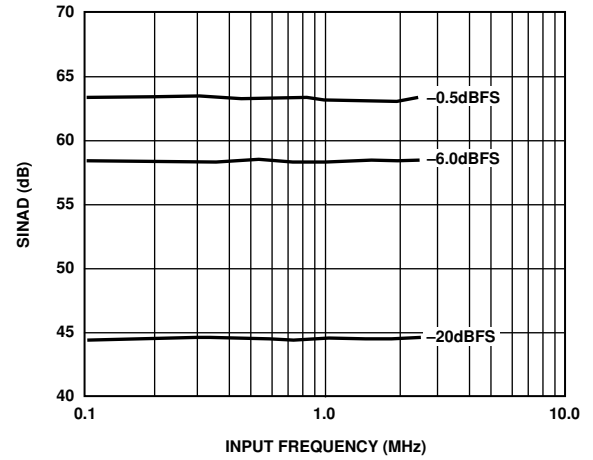


Figure 44. SINAD vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-044

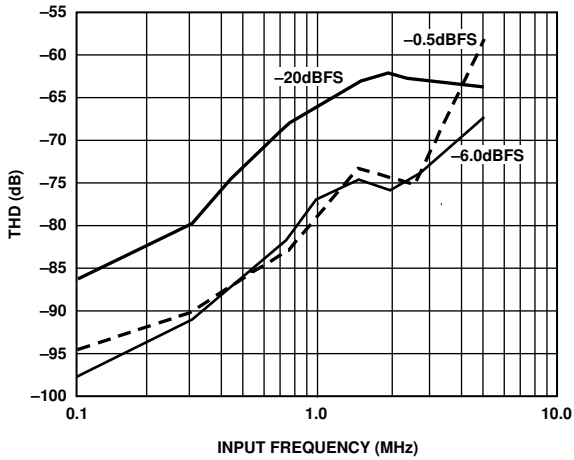


Figure 42. THD vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$)

00581-C-042

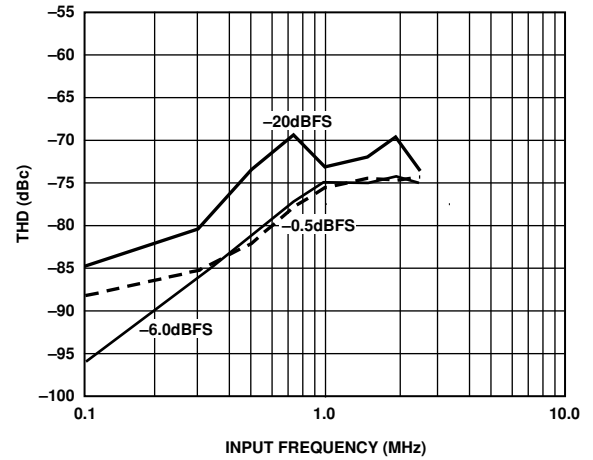


Figure 45. THD vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-045

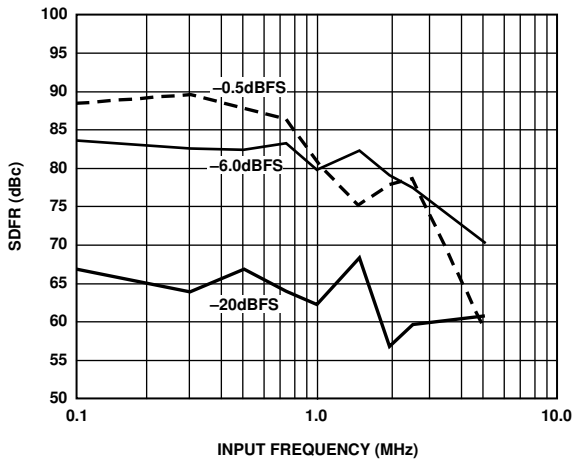


Figure 43. SFDR vs. Input Frequency ($f_{\text{CLOCK}} = 20 \text{ MSPS}$)

00581-C-043

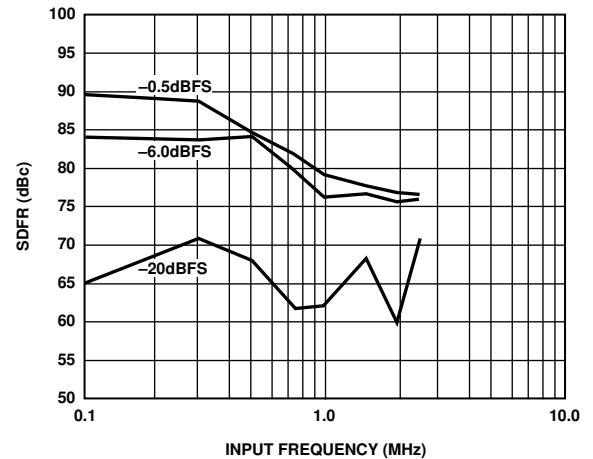


Figure 46. SFDR vs. Input Frequency ($f_{\text{CLOCK}} = 10 \text{ MSPS}$)

00581-C-046

TYPICAL AC CHARACTERIZATION CURVES

AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, $A_{IN} = -0.5$ dBFS, Differential DC Coupled Input with CML = 2 V.

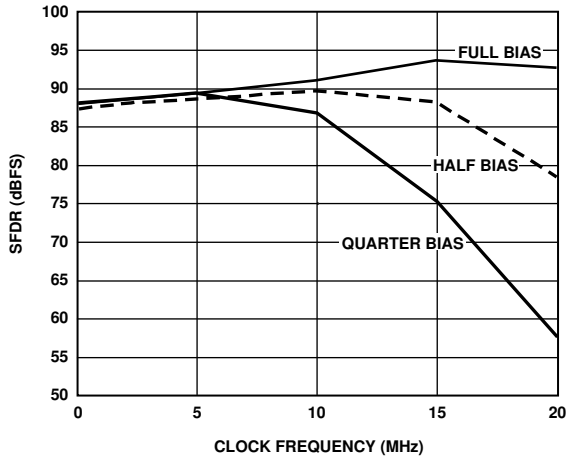


Figure 47. SFDR vs. Clock Rate ($f_{IN} = 100$ kHz in 8x Mode)

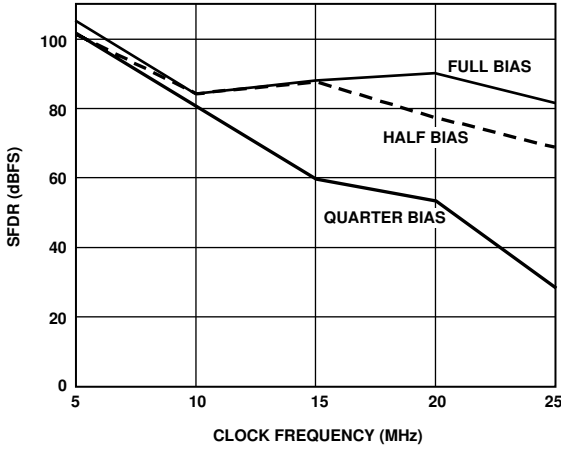


Figure 48. SFDR vs. Clock Rate ($f_{IN} = 500$ kHz in 4x Mode)

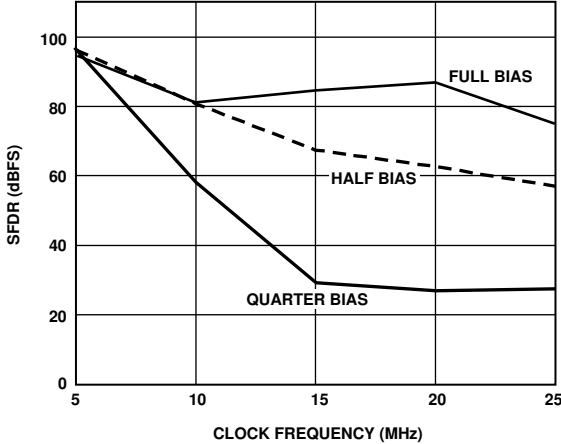


Figure 49. SFDR vs. Clock Rate ($f_{IN} = 1.0$ MHz in 2x Mode)

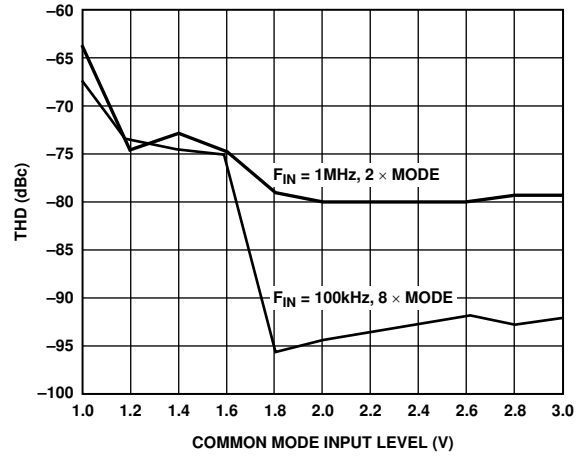


Figure 50. THD vs. Common-Mode Input Level (CML)

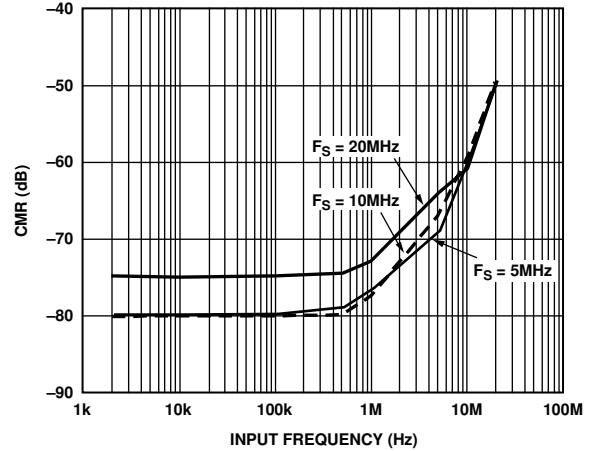


Figure 51. CMR vs. Input Frequency ($V_{CML} = 2$ V p-p, 1x Mode)

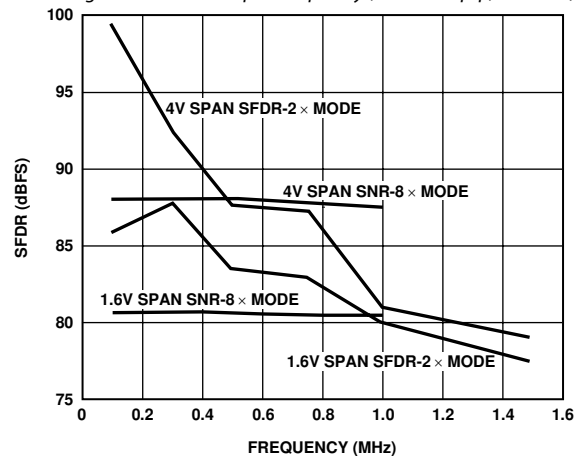


Figure 52. 4 V vs. 1.6 V Span SNR/SFDR ($f_{CLOCK} = 20$ MSPS)

ADDITIONAL AC CHARACTERIZATION CURVES

AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, $A_{IN} = -0.5$ dBFS, Differential DC Coupled Input with CML = 2 V, Full Bias, unless otherwise noted.

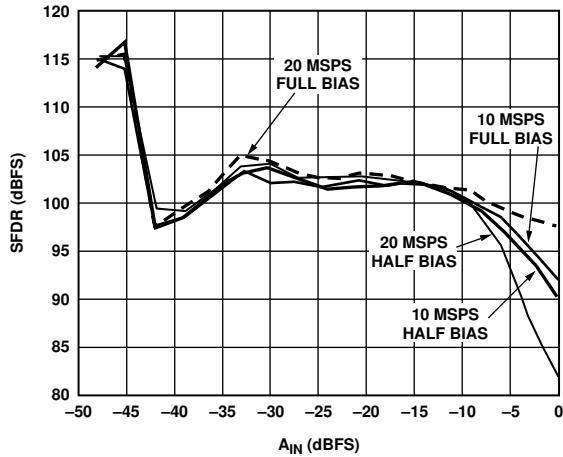


Figure 53. Single-Tone SFDR vs. Amplitude ($f_{IN} = 100$ kHz, 8x Mode)

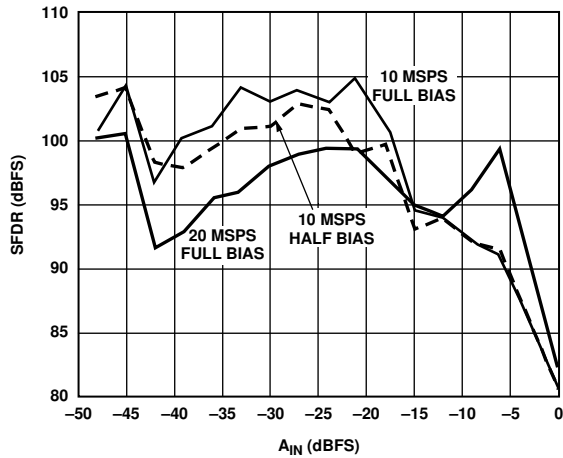


Figure 54. Single-Tone SFDR vs. Amplitude ($f_{IN} = 1.0$ MHz)

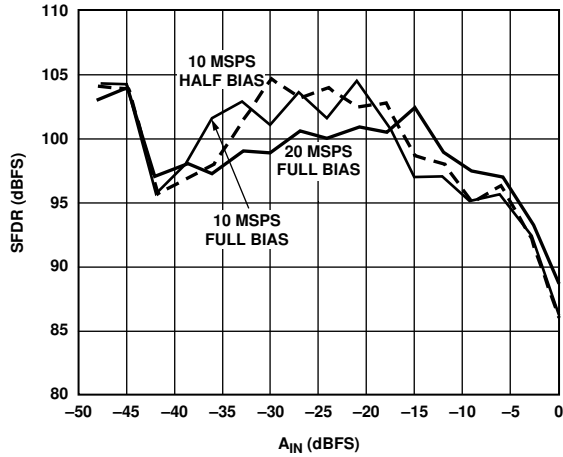


Figure 55. Single-Tone SFDR vs. Amplitude ($f_{IN} = 500$ kHz, 2x Mode)

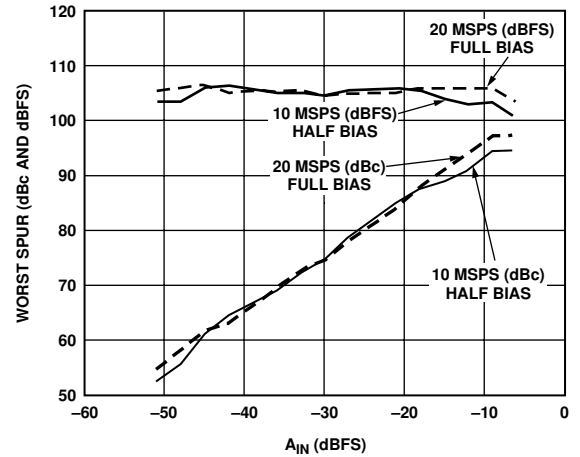


Figure 56. Two-Tone SFDR ($F_1 = 475$ kHz, $F_2 = 525$ MHz, 8x Mode)

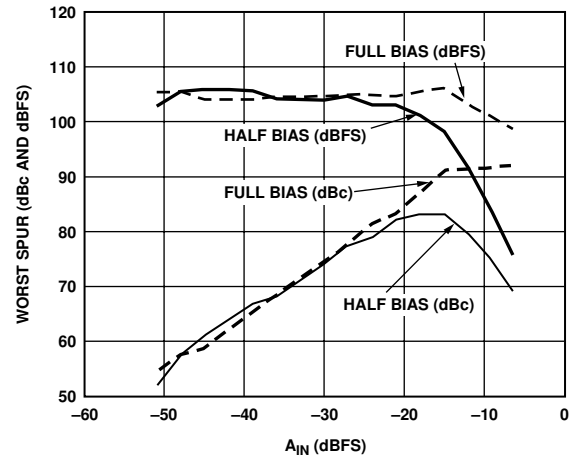


Figure 57. Two-Tone SFDR ($F_1 = 0.95$ kHz, $F_2 = 1.05$ MHz, 8x Mode, 20 MSPS)

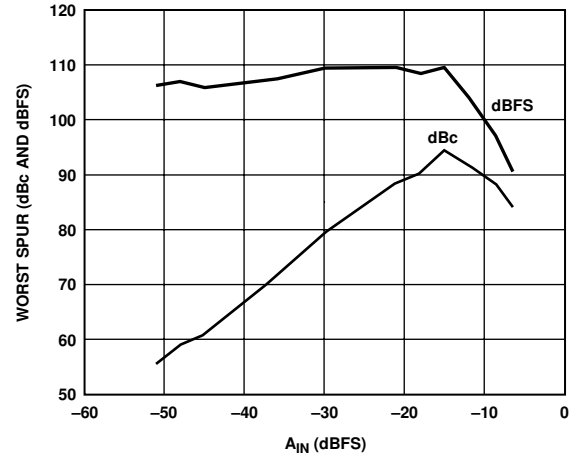


Figure 58. Two-Tone SFDR ($F_1 = 1.9$ MHz, $F_2 = 2.1$ MHz, 4x Mode 20 MSPS)

THEORY OF OPERATION

The AD9260 utilizes a new analog-to-digital converter architecture to combine sigma-delta techniques with a high speed, pipelined A/D converter. This topology allows the AD9260 to offer the high dynamic range associated with sigma-delta converters while maintaining very wide input signal bandwidth (1.25 MHz) at a very modest 8 oversampling ratio. Figure 59 provides a block diagram of the AD9260. The differential analog input is fed into a second order, multibit sigma-delta modulator. This modulator features a 5-bit flash quantizer and 5-bit feedback. In addition, a 12-bit pipelined A/D quantizes the input to the 5-bit flash to greater accuracy. A special digital modulation loop combines the output of the 12-bit pipelined A/D with the delayed output of the 5-bit flash to produce the equivalent response of a second order loop with a 12-bit quantizer and 12-bit feedback. The combination of a second order loop and multibit feedback provides inherent stability: the AD9260 is not prone to the idle tones or full-scale idiosyncrasies sometimes associated with higher order single bit sigma-delta modulators.

The output of this 12-bit modulator is fed into the digital decimation filter. The voltage level on the MODE pin establishes the configuration for the digital filter. The user may bring the data out undecimated (at the clock rate), or at a decimation factor of 2 \times , 4 \times , or a full 8 \times . The spectra for these four cases are shown in Figure 11, Figure 12, Figure 13, and Figure 14, all for a 100 kHz full-scale input and 20 MHz clock. The spectra of the undecimated output clearly shows the second order shaping characteristic of the quantization noise as it rises at frequencies above 1.25 MHz.

The on-chip decimation filter provides excellent stopband rejection to suppress any stray input signal between 1.25 MHz and 18.75 MHz, substantially easing the requirements on any

antialiasing filter for the analog input path. The decimation filters are integrated with symmetric FIR filter structures, providing a linear phase response and excellent passband flatness. The digital output driver register of the AD9260 features both READ and CHIP SELECT pins to allow easy interfacing. The digital supply of the AD9260 is designed to operate over a 2.7 V to 5.25 V supply range, though 3 V supplies are recommended to minimize digital noise on the board. A DATA AVAILABLE pin allows the user to easily synchronize to the converter's decimated output data rate. OUT-OF-RANGE (OTR) indication is given for an overflow in the pipelined A/D converter or digital filters. A RESETB function is provided to synchronize the converter's decimated data and clear any overflow condition in the analog integrators.

An on-chip reference and reference buffer are included on the AD9260. The reference can be configured in either a 2.5 V mode (providing a 4 V p-p differential input full scale), a 1 V mode (providing a 1.6 V p-p differential input full scale), or programmed with an external resistor divider to provide any voltage level between 1 V and 2.5 V. *However, optimum noise and distortion performance for the AD9260 can only be achieved with a 2.5 V reference, as shown in Figure 52.*

For users who want to operate the part at reduced clock frequencies, the bias current of the AD9260 is designed to be scalable. This scaling is accomplished through use of the proper external resistor tied to the BIAS pin: the power can be reduced roughly proportionately to clock frequency by as much as 75% (for clock rates of 5 MHz). Refer to Figure 47 to Figure 49 and Figure 53 to Figure 57 for characterization curves showing performance tradeoffs.

ANALOG INPUT AND REFERENCE OVERVIEW

Figure 60, a simplified model of the AD9260, highlights the relationship between the analog inputs, V_{INA} , V_{INB} and the reference voltage V_{REF} . Like the voltage applied to the top of the resistor ladder in a flash A/D converter, the value V_{REF} defines the maximum input voltage to the A/D converter. An internal reference buffer in the AD9260 scales the reference voltage V_{REF} before it is applied internally to the AD9260 A/D core. The scale factor of this reference buffer is 0.8.

Consequently, the maximum input voltage to the A/D core is $+0.8 \times V_{REF}$. The minimum input voltage to the A/D core is automatically defined to be $-0.8 \times V_{REF}$. With this scale factor, the maximum differential input span of 4 V p-p is obtained with a V_{REF} voltage of 2.5 V. A smaller differential input span may be obtained by using a V_{REF} voltage of less than 2.5 V at the expense of ac performance (refer to Figure 52).

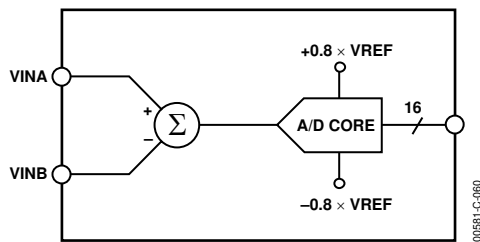


Figure 60. Simplified Input Model

INPUT SPAN

The AD9260 is implemented with a differential input structure. This structure allows the common-mode level (average voltage of the two input pins) of the input signal to be varied independently of the input span of the converter over a wide range, as shown in Figure 50. Specifically, the input to the A/D core is the difference of the voltages applied at the V_{INA} and V_{INB} input pins. Therefore, the equation,

$$V_{CORE} = V_{INA} - V_{INB} \quad (1)$$

defines the output of the differential input stage and provides the input to the A/D core.

The voltage, V_{CORE} , must satisfy the condition,

$$-0.8 \times V_{REF} \leq V_{CORE} \leq +0.8 \times V_{REF} \quad (2)$$

where V_{REF} is the voltage at the V_{REF} pin.

INPUT COMPLIANCE RANGE

In addition to the limitations on the differential span of the input signal indicated in Equation 2, an additional limitation is placed on the inputs by the analog input structure of the AD9260. The analog input structure bounds the valid operating range for V_{INA} and V_{INB} . The condition,

$$\begin{aligned} AVSS + 0.5V < V_{INA} < AVDD - 0.5V \\ AVSS + 0.5V < V_{INB} < AVDD + 0.5V \end{aligned} \quad (3)$$

where $AVSS$ is nominally 0 V and $AVDD$ is nominally +5 V, defines this requirement. Thus the valid inputs for V_{INA} and V_{INB} are any combination that satisfies both Equations 2 and 3. Note that the clock clamping method used in the differential driver circuit shown in Figure 63 is sufficient for protecting the AD9260 in an undervoltage condition.

For additional information showing the relationships between V_{INA} , V_{INB} , V_{REF} , and the digital output of the AD9260, see Table 13.

Refer to Table 12 for a summary of the various analog input and reference configurations.

ANALOG INPUT OPERATION

The analog input structure of the AD9260 is optimized to meet the performance requirements for some of the most demanding communication and data acquisition applications. This input structure is composed of a switched-capacitor network that samples the input signal applied to pins V_{INA} and V_{INB} on every rising edge of the CLK pin. The input switched capacitors are charged to the input voltage during each period of CLK . The resulting charge, q , on these capacitors is equal to $C \times V_{IN}$, where C is the input capacitor. The change in charge on these capacitors, Δq , as the capacitors are charged from a previous sample of the input signal to the next sample, is approximated in the following equation,

$$\Delta q \sim C \times \Delta V_N = C \times (V_N - V_{N-2}) \quad (4)$$

where V_N represents the present sample of the input signal and V_{N-2} represents the sample taken two clock cycles earlier. The average current flow into the input (provided from an external source) is given in the following equation,

$$I = \Delta q / T \sim C \times (V_N - V_{N-2}) \times f_{CLOCK} \quad (5)$$

where T represents the period of CLK and f_{CLOCK} represents the frequency of CLK . Equations 4 and 5 provide simplifying approximations of the operation of the analog input structure of the AD9260. A more exact, detailed description and analysis of the input operation follows.