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Evaluating the AD9265/AD9255 Analog-to-Digital Converters

FEATURES

- Full featured evaluation board for the AD9265/AD9255
- SPI interface for setup and control
- External, on-board oscillator or AD9517 clocking options
- Balun/transformer or amplifier input drive options
- LDO regulator or switching power supply options
- VisualAnalog® and SPI controller software interfaces

EQUIPMENT NEEDED

- Analog signal source and antialiasing filter
- Sample clock source (if not using the on-board oscillator)
- 2 switching power supplies (6.0 V, 2.5 A) provided, CUI, Inc., EPS060250UH-PHP-SZ
- PC running Windows® XP or Windows Vista
- USB 2.0 port recommended (USB 1.1 compatible)
- AD9265 or AD9255 evaluation board
- HSC-ADC-EVALCZ FPGA-based data capture kit

SOFTWARE NEEDED

- VisualAnalog
- SPI controller

DOCUMENTS NEEDED

- [AD9265 or AD9255 data sheet](#)
- [HSC-ADC-EVALCZ data sheet](#)
- [AN-905 Application Note, VisualAnalog Converter Evaluation Tool Version 1.0 User Manual](#)
- [AN-878 Application Note, High Speed ADC SPI Control Software](#)
- [AN-877 Application Note, Interfacing to High Speed ADCs via SPI](#)
- [AN-835 Application Note, Understanding High Speed ADC Testing and Evaluation](#)

GENERAL DESCRIPTION

This user guide describes the AD9265 and AD9255 evaluation board, which provides all of the support circuitry required to operate the AD9265 or AD9255 in its various modes and configurations. The application software used to interface with the devices is also described.

The AD9265 and AD9255 data sheets provide additional information and should be consulted when using the evaluation board. All documents and software tools are available at www.analog.com/fifo. For additional information or questions, send an email to highspeed.converters@analog.com.

EVALUATION BOARDS

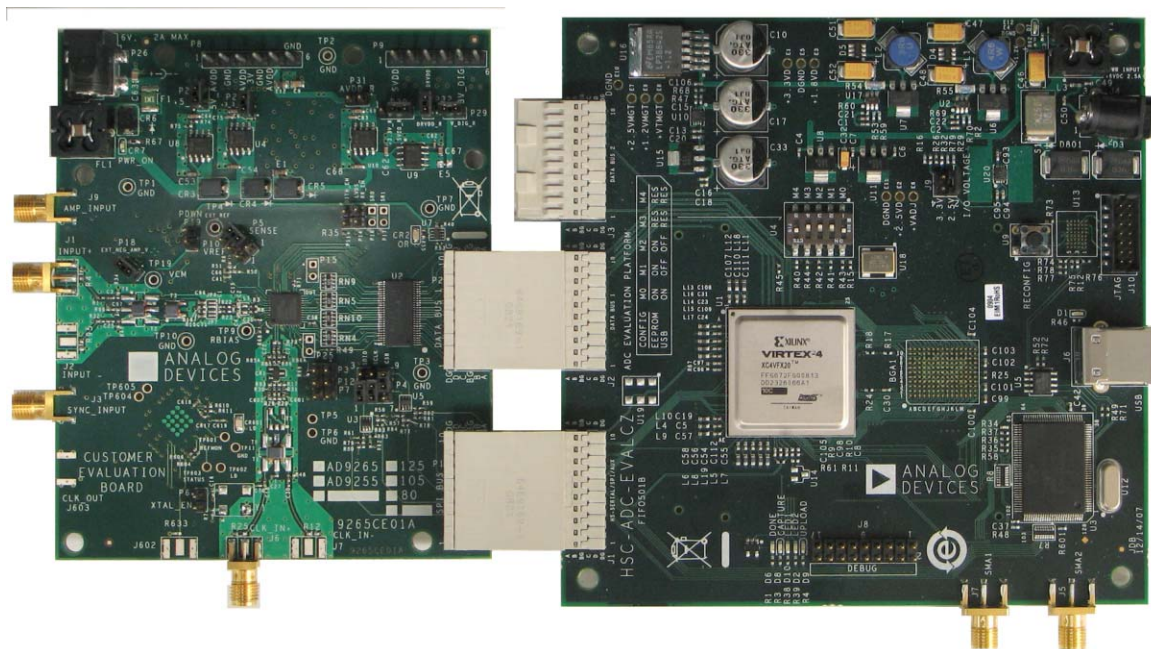


Figure 1. AD9265 and AD9255 Evaluation Board and HSC-ADC-EVALCZ Data Capture Board

08959-001

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REVISION HISTORY

1/11—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The AD9265 and AD9255 evaluation board provides all of the support circuitry required to operate these parts in their various modes and configurations. Figure 2 shows the typical bench characterization setup used to evaluate the ac performance of the AD9265 or AD9255. It is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the signal chain. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is necessary to achieve the specified noise performance.

See the Evaluation Board Software Quick Start Procedures section to get started, and see Figure 15 to Figure 28 for the complete schematics and layout diagrams. These diagrams demonstrate the routing and grounding techniques that should be applied at the system level when designing application boards using these converters.

POWER SUPPLIES

This evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to the rated 100 V ac to the 240 V ac wall outlet at 47 Hz to 63 Hz. The output from the supply is provided through a 2.1 mm inner diameter jack that connects to the printed circuit board (PCB) at P26. The 6 V supply is fused and conditioned on the PCB before connecting to the low dropout linear regulators (default configuration) that supply the proper bias to each of the various sections on the board.

The evaluation board can be powered in a nondefault condition using external bench power supplies. To do this, the P27, P28, P31, P30, P32, and P29 jumpers can be removed to disconnect the outputs from the on-board LDOs. This enables the user to bias each section of the board individually. Use P8 and P9 to connect a different supply for each section. A 1.8 V supply is needed with a 1 A current capability for AVDD, SVDD, and DRVDD; however, it is recommended that separate supplies be used for both analog and digital domains. An additional supply is also required to supply 1.8 V for digital support circuitry on the board, 3V_DIG. This should also have a 1 A current capability and can be combined with DRVDD with little or no degradation in performance.

Two additional supplies, 5V_AVDD and 3V_AVDD, are used to bias the optional input path amplifiers. If used, these supplies should each have a 1 A current capability. P18 is also necessary if an amp that requires a negative supply voltage is being used.

A second optional power supply configuration allows the replacement of the LDOs that supply the AVDD and DRVDD rails of the ADC with the ADP2108 step-down dc-to-dc converter. Using this switching controller in place of the LDO regulators to power the AVDD and DRVDD supplies of the ADC allows customers to evaluate the performance of the ADC when powered by a more efficient regulator.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise, such as the Rohde & Schwarz SMA100A, HP 8644B signal generators, or an equivalent. Use a 1 m shielded, RG-58, 50 Ω coaxial cable for connecting to the evaluation board. Enter the desired frequency and amplitude (see the Specifications section in the data sheet of the respective part). When connecting the analog input source, use of a multipole, narrow-band, band-pass filter with 50 Ω terminations is recommended. Analog Devices, Inc., uses TTE and K&L Microwave, Inc., band-pass filters. The filters should be connected directly to the evaluation board.

If an external clock source is used, it should also be supplied with a clean signal generator as previously specified. Typically, most Analog Devices evaluation boards can accept ~ 2.8 V p-p or 13 dBm sine wave input for the clock.

OUTPUT SIGNALS

The default setup uses the Analog Devices high speed converter evaluation platform (HSC-ADC-EVALCZ) for data capture. The CMOS output signals are buffered through U2 and are routed through P2 to the FPGA on the data capture board.

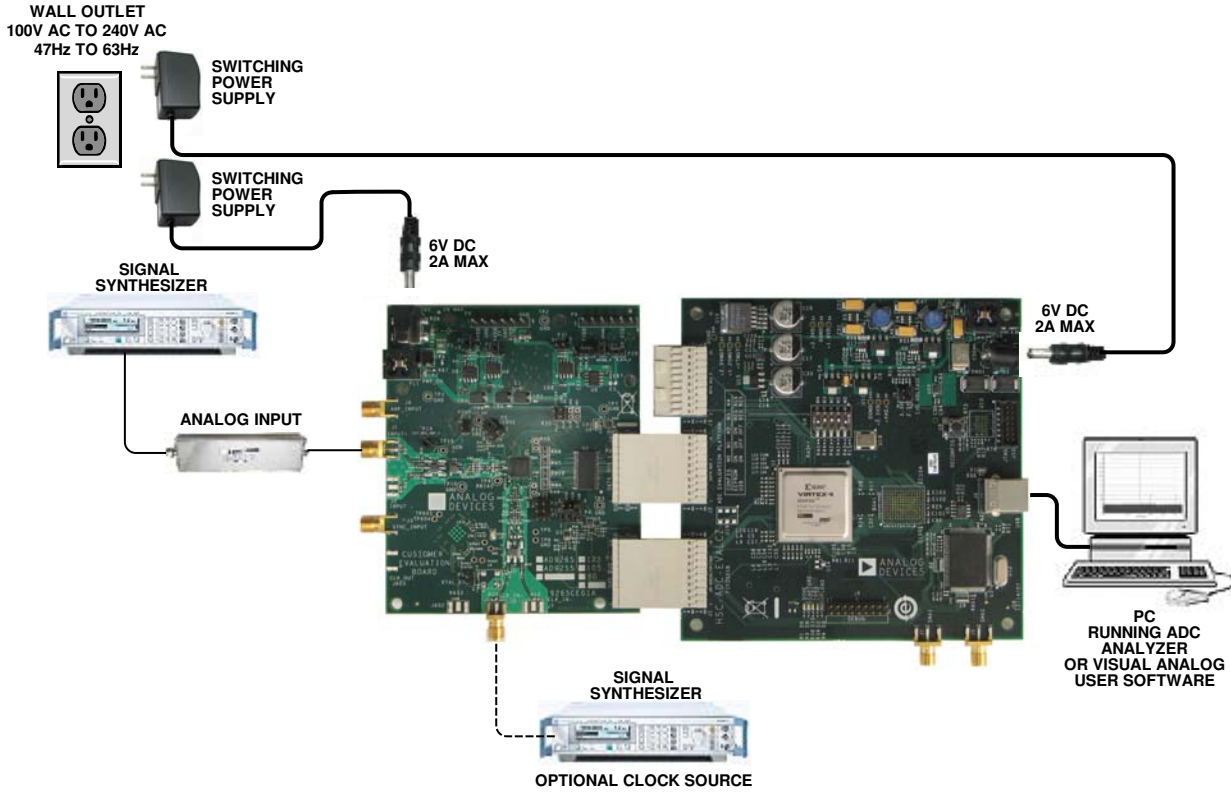


Figure 2. Evaluation Board Connection

08659-002

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

This section explains the default and optional settings or modes allowed on the [AD9265/AD9255](#) Rev. A evaluation board.

Power Circuitry

Connect the switching power supply that is supplied in the evaluation kit between P26 and a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz.

Analog Input

The inputs on the evaluation board are set up for a double balun-coupled analog input with a 50 Ω impedance. For the AD9265/AD9255, the default analog input configuration supports analog input frequencies of up to ~250 MHz (see Figure 3). This input network is optimized to support a wide frequency band. See the AD9265 and AD9255 data sheets for additional information on the recommended networks for different input frequency ranges.

Optionally, the analog input on the board can be configured to use the [ADL5562](#), which is a 3.3 GHz ultralow distortion RF/IF differential amplifier. The ADL5562 component is included on the evaluation board at U1. However, the path into and out of the ADL5562 can be configured in many different ways depending on the application; therefore, the parts in the input and output path are left unpopulated. Users should see the ADL5562 data sheet for additional information on this part and for configuring the inputs and outputs. The ADL5562 is normally held in power-down mode and can be enabled by adding a jumper on P19. The ADL5562 can also be substituted with the [ADA4937-1](#) or the [ADA4938-1](#) to allow evaluation of these parts with the ADC.

VREF

VREF is set by default to 1.0 V with SENSE connected to AGND through a jumper connecting Pin 2 and Pin 3 on Header P5. This causes the ADC to operate with the internal reference in the 2.0 V p-p differential full-scale range. The reference voltage can be changed to 0.5 V for a 1.0 V p-p full-scale range by moving the SENSE pin jumper connection on P5 from Pin 2 and Pin 3 to Pin 1 and Pin 2 (this connects the SENSE pin to the VREF pin).

To use the programmable reference mode, a resistor divider can be set up by installing R50 and R51. The jumper on P5 should be removed for this mode of operation. See the data sheet of the part for additional information on using the programmable reference mode.

RBIAS

RBIAS has a default setting of 10 kΩ (R68) to ground and is used to set the ADC core bias current. Note that using a resistor value other than a 10 kΩ, 1% resistor for RBIAS may degrade the performance of the device.

Clock Circuitry

The AD9265/AD9255 board is set by default to use an external clock generator. An external clock source capable of driving a 50 Ω terminated input should be connected to J6. This board is shipped from Valpey Fisher with a low phase noise oscillator installed. The oscillator frequency is set to match the rated speed of the part: 125 MHz, 105 MHz, or 80 MHz for the AD9265/AD9255. To enable the oscillator, install P6, and to connect it into the clock path, add a 0 Ω resistor at C70. R25 should also be removed to remove the 50 Ω termination from the output of the oscillator.

A differential LVPECL clock driver output can also be used to clock the ADC input using the [AD9517-4](#) (U601). To place the AD9517-4 into the clock path, populate R28 and R29 with 0 Ω resistors and remove R30 and R31 to disconnect the default clock path inputs. In addition, populate R85A and R86A with 0 Ω resistors and remove R85 and R86 to disconnect the default clock path outputs and insert the AD9517-4 OUT0 LVPECL. The AD9517-4 must be configured through the SPI controller software to set up the PLL and other operation modes. Consult the AD9517-4 data sheet for more information about these and other options.

PDWN

To enable the power-down feature, add a shorting jumper across P7 at Pin 1 and Pin 2 to connect the PDWN pin to DRVDD.

OEB

To disable the outputs using the OEB pin, add a shorting jumper across P3 at Pin 1 and Pin 2 to connect the OEB pin to DRVDD.

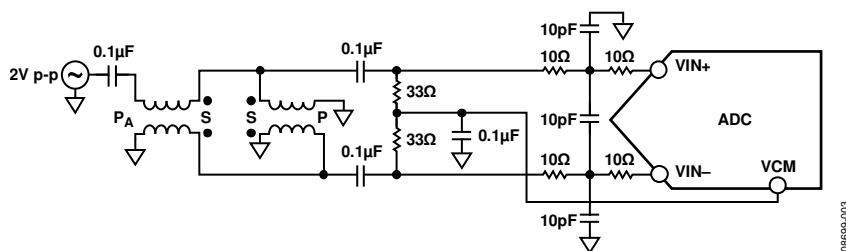


Figure 3. Default Analog Input Configuration of the AD9265/AD9255

Non-SPI Mode

For users who want to operate the device under test (DUT) without using SPI, remove the shorting jumpers on P4. This disconnects the CSB, SCLK/DFS, and SDIO/DCS pins from the SPI control bus and connects CSB to SVDD, allowing the DUT to operate in non-SPI mode. In this mode, the SCLK/DFS and SDIO/DCS pins take on their alternate functions to select the data format and enable/disable the DCS. With the SDIO/DCS jumper removed, DCS is disabled; to enable DCS, add a shorting jumper on P4 between Pin 2 and Pin 3. With the SCLK/DFS jumper removed, the data format is set to offset binary. To set the data format to twos complement, a jumper should be added on P4 between Pin 5 and Pin 6.

Switching Power Supply

Optionally, the ADC on the board can be configured to use the [ADP2108](#) dual switching power supply to provide power to the DRVDD and AVDD rails of the ADC. To configure the board to operate from the ADP2108, the following changes must be incorporated (see the Evaluation Board Schematics and Artwork and Bill of Materials sections for specific recommendations for part values):

1. Install L2 and L3.
2. Install C77, C79, C80, and C81.
3. Install E2, E3, and E11.
4. Remove P31 and E5.

Making these changes enables the switching converter to power the ADC. Using the switching converter as the ADC power source is more efficient than using the default LDOs.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

This section provides quick start procedures for using the [AD9265](#) and [AD9255](#) evaluation board. Both the default and optional settings are described.

CONFIGURING THE BOARD

Before using the software for testing, configure the evaluation board as follows:

1. Connect the evaluation board to the data capture board, as shown in Figure 1 and Figure 2.
2. Connect one 6 V, 2.5 A switching power supply (such as the CUI, Inc., EPS060250UH-PHP-SZ supplied) to the [AD9265](#) or [AD9255](#) board.
3. Connect one 6 V, 2.5 A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the HSC-ADC-EVALCZ board.
4. Connect the HSC-ADC-EVALCZ board (at J6) to the PC with a USB cable.
5. On the ADC evaluation board, confirm that three jumpers are installed on P4, one between Pin 1 and Pin 2, one between Pin 4 and Pin 5, and one between Pin 8 and Pin 9, to connect the SPI bus to the DUT.
6. Make sure a low jitter sample clock is applied at J6.
7. On the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal. Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results, use a narrow-band, band-pass filter with 50 Ω terminations and an appropriate center frequency. (Analog Devices uses TTE, Allen Avionics, and K&L Microwave band-pass filters.)

USING THE SOFTWARE FOR TESTING

Setting Up the ADC Data Capture

After configuring the board, set up the ADC data capture using the following steps:

1. Open VisualAnalog on the connected PC. The appropriate part type should be listed in the status bar of the **VisualAnalog – New Canvas** window. Select the template that corresponds to the type of testing to be performed (see Figure 4 where the AD9265 is shown as an example).

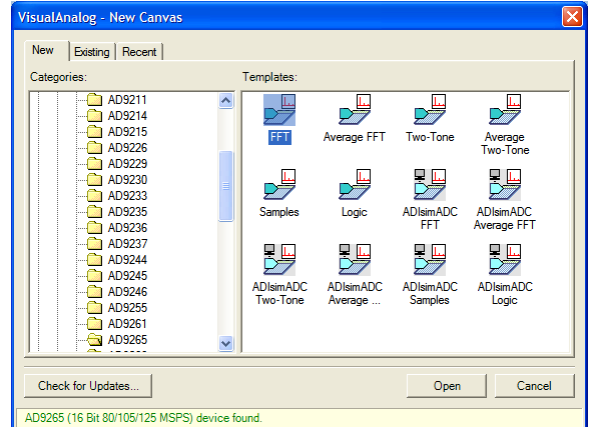


Figure 4. VisualAnalog – New Canvas Window

2. After the template is selected, a message appears asking if the default configuration can be used to program the FPGA (see Figure 5). Click **Yes** and the window closes.

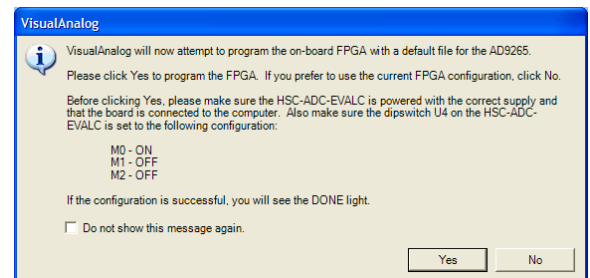


Figure 5. VisualAnalog Default Configuration Message

3. To change features to settings other than the default settings, click the **Expand Display** button, located on the bottom right corner of the window, to see what is shown in Figure 7. Detailed instructions for changing the features and capture settings can be found in the [AN-905 Application Note, VisualAnalog Converter Evaluation Tool Version 1.0 User Manual](#). After the changes are made to the capture settings, click **Collapse Display** (see Figure 7).

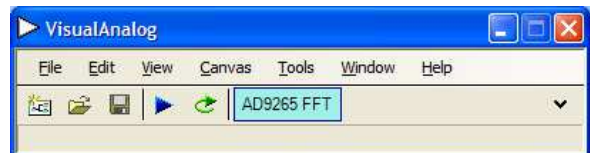


Figure 6. VisualAnalog Window Toolbar, Collapsed Display

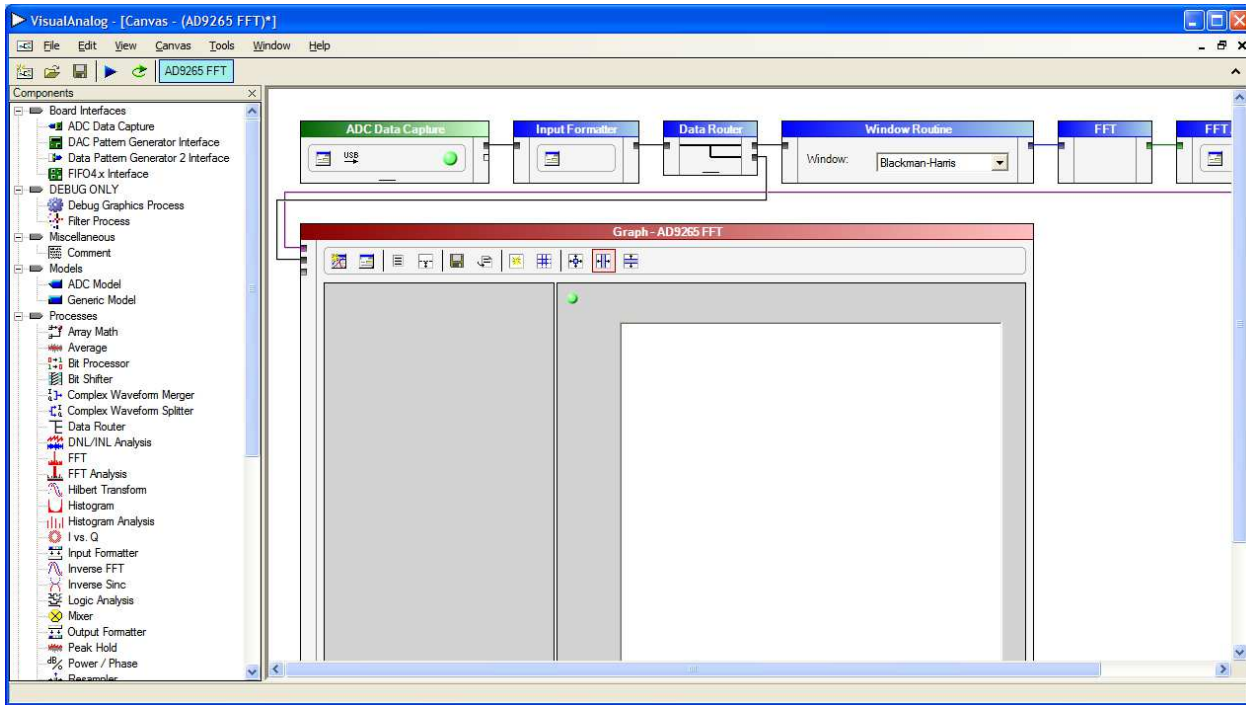


Figure 7. VisualAnalog, Main Window

Setting Up the SPI Controller Software

After the ADC data capture board setup is complete, set up the SPIController software using the following procedure:

1. Open the SPIController software by going to the **Start** menu or by double-clicking the **SPIController** software desktop icon. If prompted for a configuration file, select the appropriate one. If not, check the title bar of the window to determine which configuration is loaded. If necessary, choose **Cfg Open** from the **File** menu and select the appropriate file based on your part type. Note that the **CHIP ID(1)** field should be filled to indicate whether the correct **SPIController** configuration file is loaded (see Figure 8).

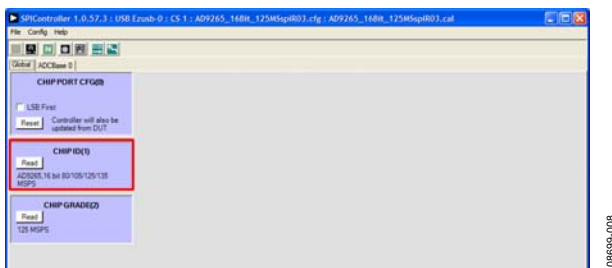


Figure 8. SPIController, CHIP ID(1) Box

2. Click the **New DUT** button in the **SPIController** window (see Figure 9).

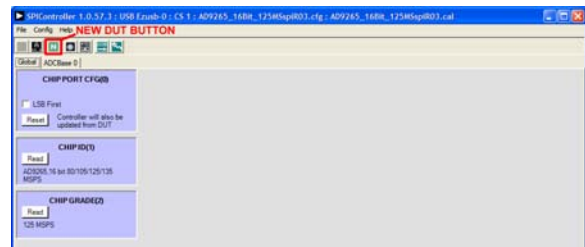


Figure 9. SPIController, New DUT Button

3. In the **ADCBASE 0** tab of the **SPIController** window, find the **CLOCK DIVIDE(B)** box (see Figure 10). If using the clock divider, use the drop-down box to select the correct clock divide ratio, if necessary. See the appropriate part data sheet; the **AN-878** Application Note, *High Speed ADC SPI Control Software*; and the **AN-877** Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information.

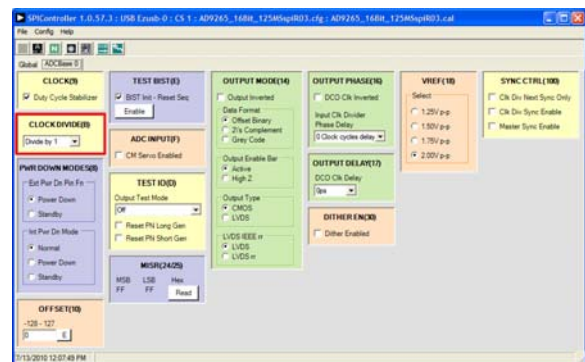


Figure 10. SPIController, CLOCK DIVIDE(B) Box

- Note that other settings can be changed on the **ADCBASE 0** tab (see Figure 10). See the appropriate part data sheet; the [AN-878](#) Application Note, *High Speed ADC SPI Control Software*; and the [AN-877](#) Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information on the available settings.

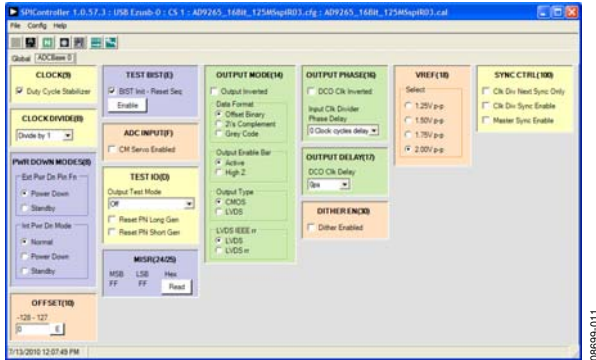


Figure 11. SPIController, Example ADCBase 0 Page

- Click the **Run** button in the **VisualAnalog** toolbar (see Figure 12).

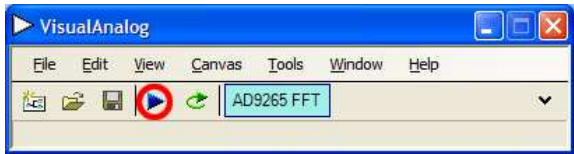


Figure 12. Run Button (Encircled in Red) in VisualAnalog Toolbar, Collapsed Display

Adjusting the Amplitude of the Input Signal

The next step is to adjust the amplitude of the input signal as follows:

- Adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the **Fund Power** reading in the left panel of the **Graph - AD9265 Average FFT** window, see Figure 13.)

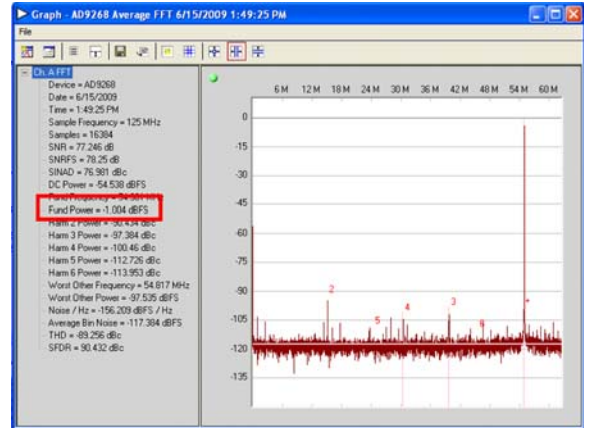


Figure 13. Graph Window of VisualAnalog

- Click the disk icon within the **Graph** window to save the performance plot data as a .csv formatted file. See Figure 14 for an example.

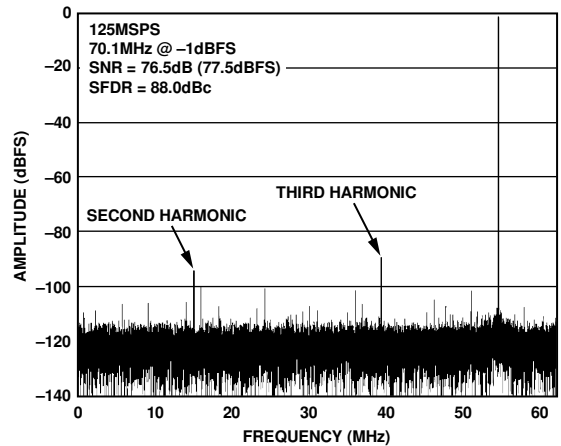


Figure 14. Typical FFT, AD9265/AD9255

Troubleshooting Tips

If the FFT plot appears abnormal, do the following:

- If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce the input level, if necessary.
- In **VisualAnalog** (see Figure 7), click the **Settings** button in the **Input Formatter** block. Check that **Number Format** is set to the correct encoding (offset binary by default). Repeat for the other channel.

If the FFT appears normal but the performance is poor, check the following:

- Make sure an appropriate filter is used on the analog input.
- Make sure the signal generators for the clock and the analog input are clean (low phase noise).
- Change the analog input frequency slightly if noncoherent sampling is being used.
- Make sure the SPI config file matches the product being evaluated.

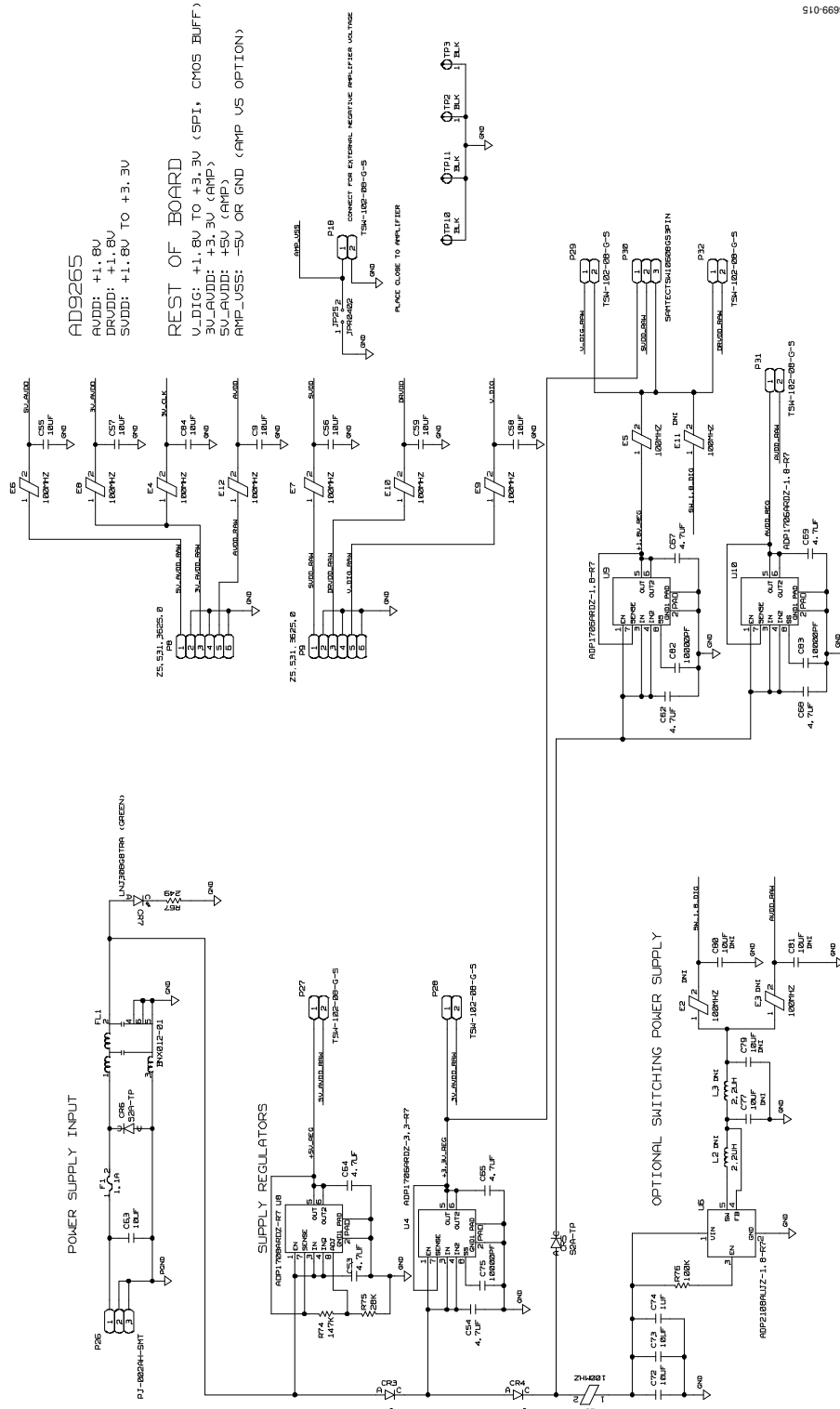
If the FFT window remains blank after clicking **Run**, do the following:

- Make sure the evaluation board is securely connected to the HSC-ADC-EVALCZ board.
- Make sure the FPGA has been programmed by verifying that the **DONE** LED is illuminated on the HSC-ADC-EVALCZ board. If this LED is not illuminated, make sure the U4 switch on the board is in the correct position for USB CONFIG.
- Make sure the correct FPGA program was installed by selecting the **Settings** button in the **ADC Data Capture** block in **VisualAnalog** (see Figure 7). Then select the **FPGA** tab and verify that the proper FPGA bin file is selected for the part.

If **VisualAnalog** indicates that the **FIFO Capture timed out** (via a pop-up window), do the following:

1. Make sure all power and USB connections are secure.
2. Probe the DCO signal at P25 (Pin 2) on the evaluation board and confirm that a clock signal is present at the ADC sampling rate.

EVALUATION BOARD SCHEMATICS AND ARTWORK



510-66980

Figure 15. Board Power Input and Supply Circuits

910-66980

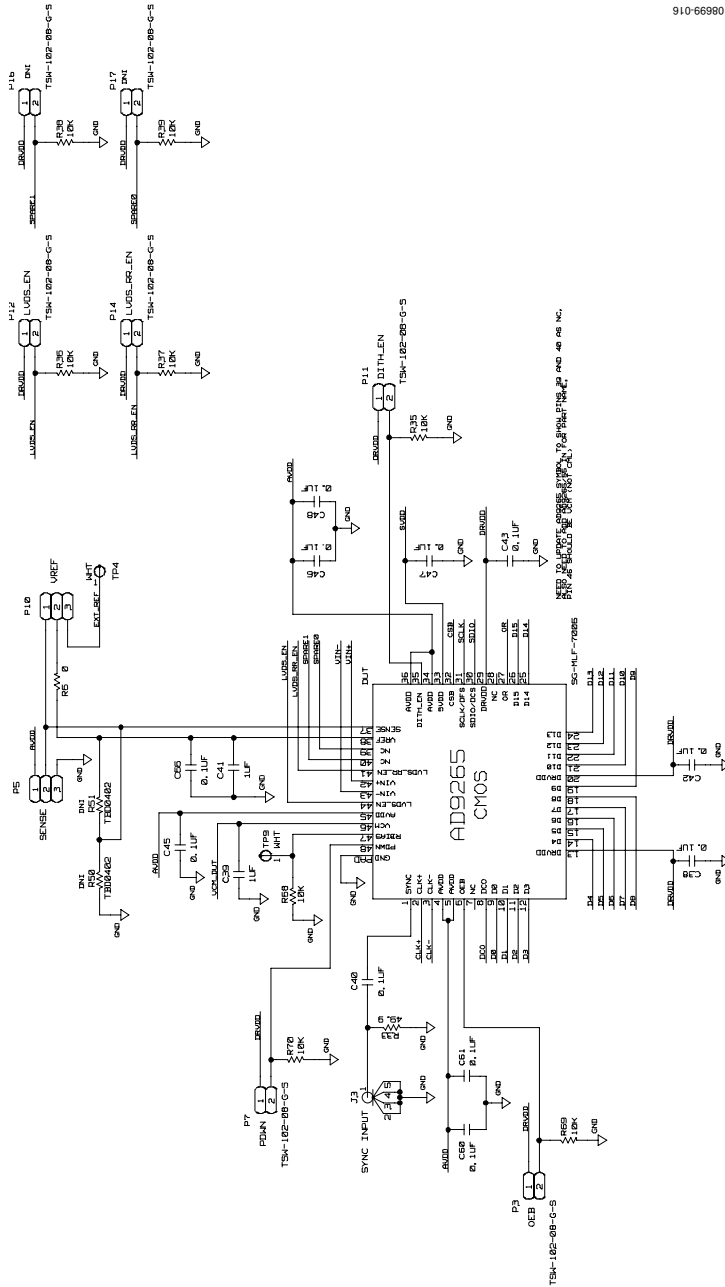


Figure 16. DUT and Related Circuits

410-6690

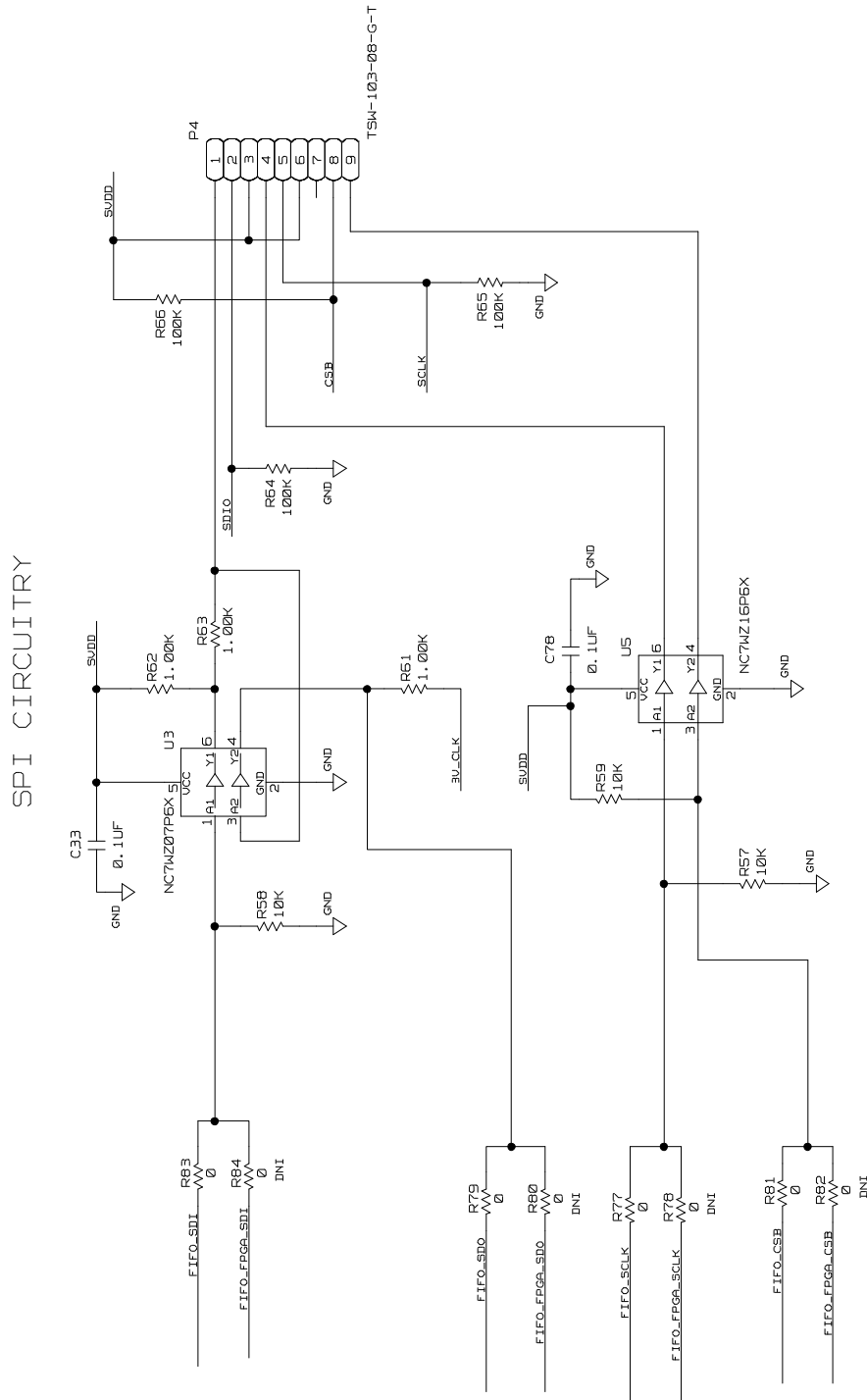


Figure 17. SPI Interface Circuit

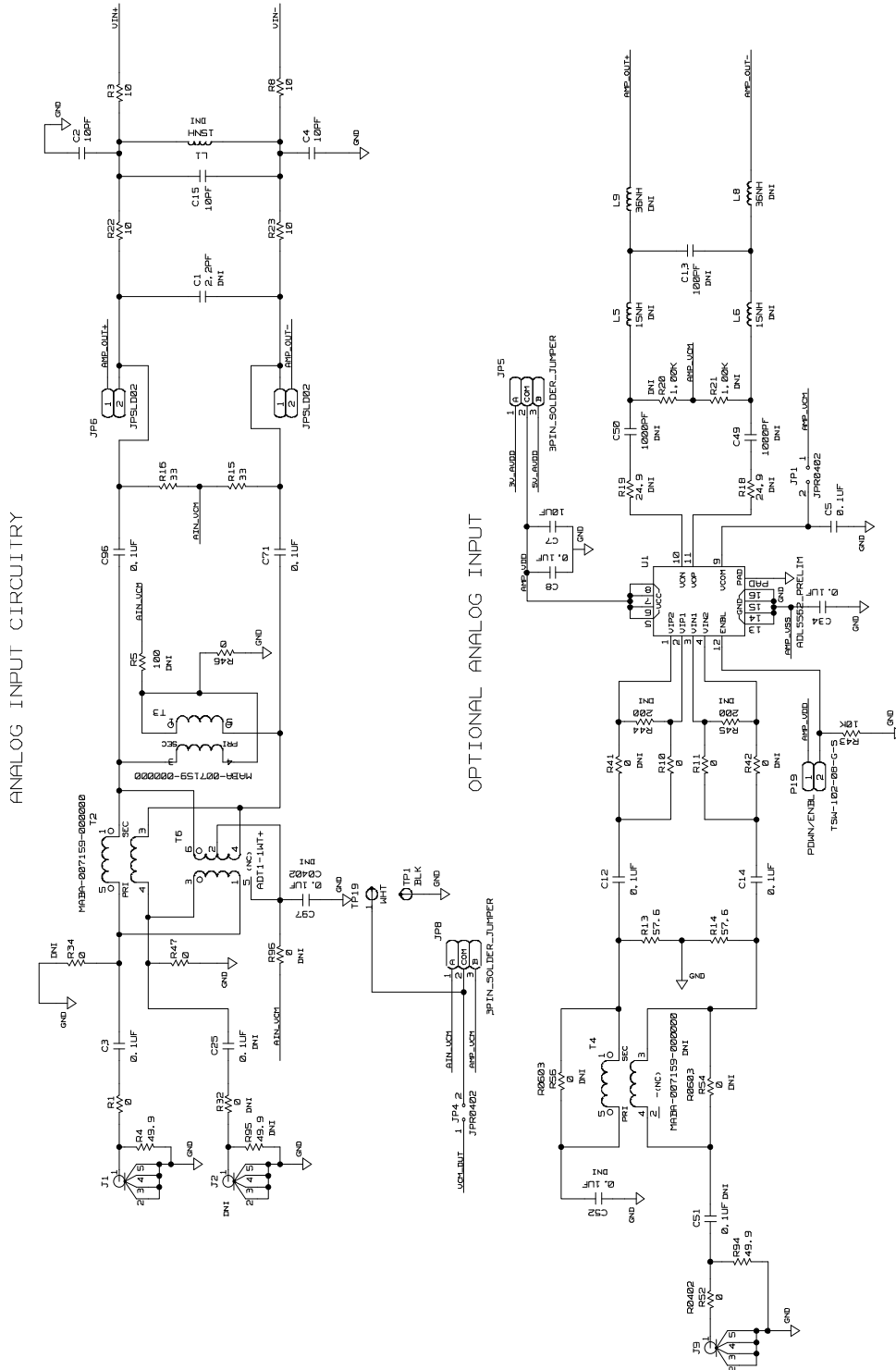


Figure 18. Analog Input Circuits

610-88-880

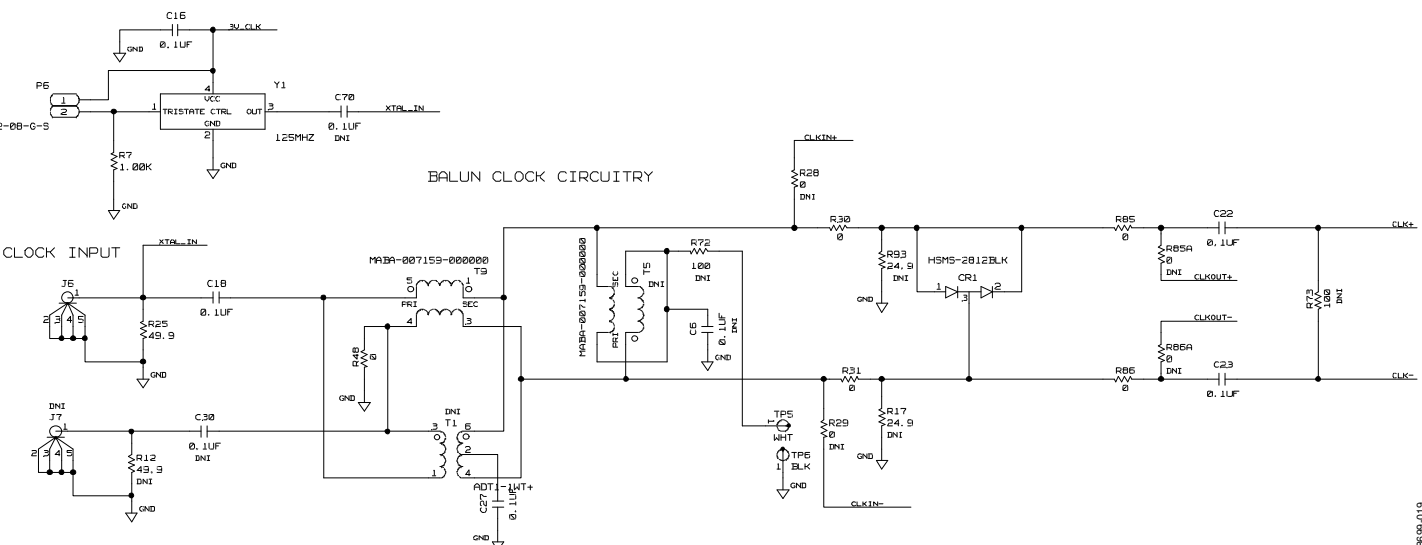


Figure 19. Default Clock Path Input Circuits

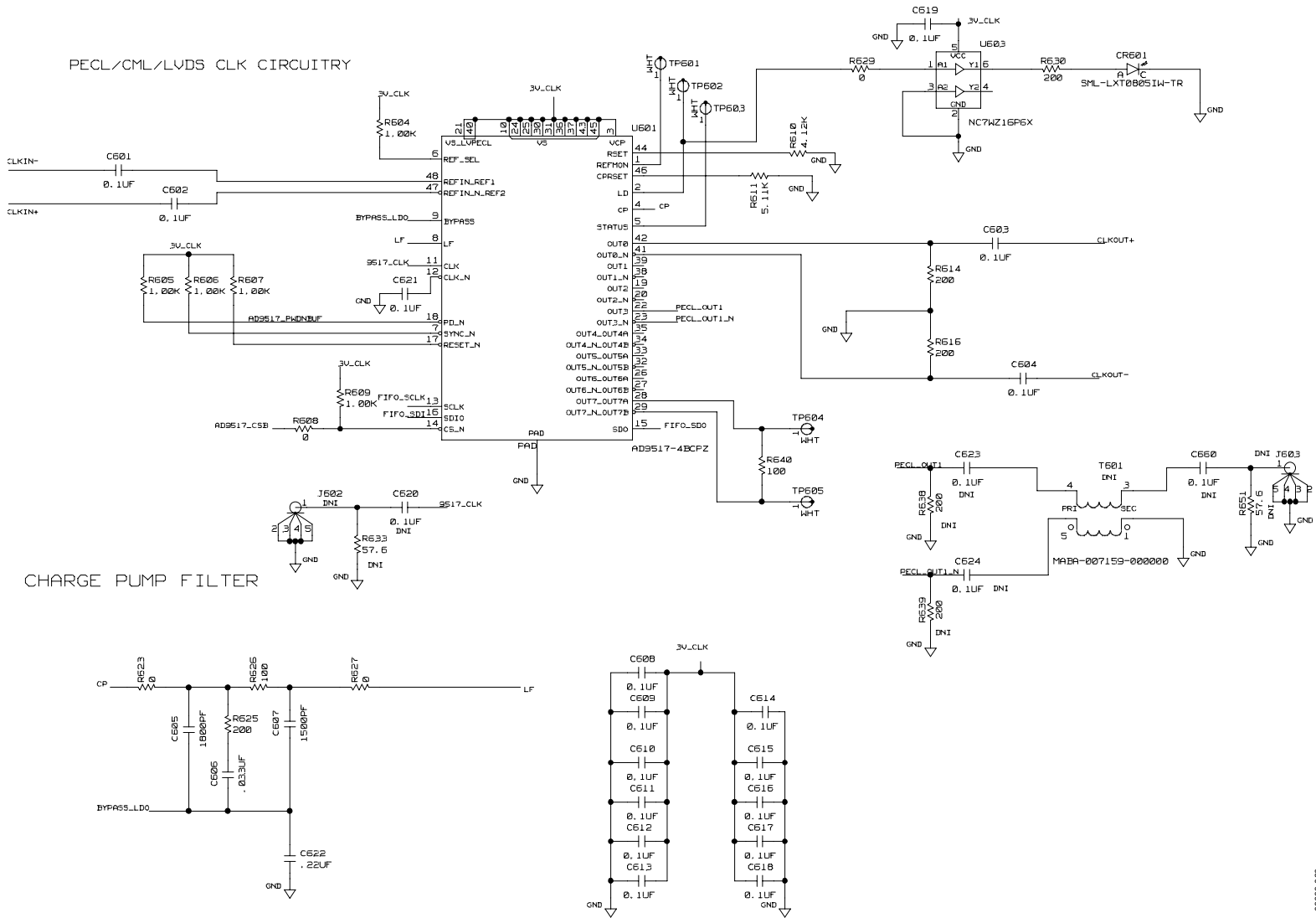


Figure 20. Optional AD9517 Clock Input Circuit

120-68880

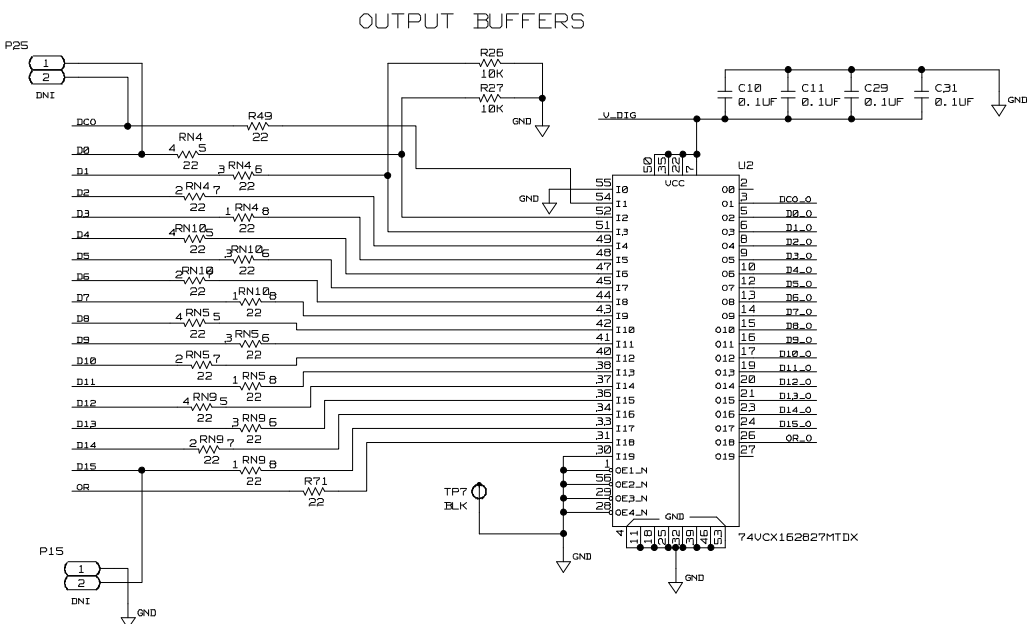
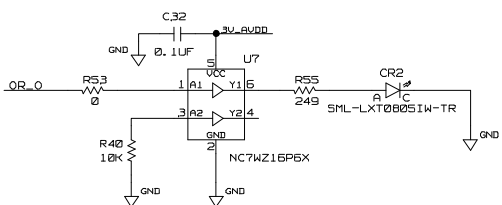


Figure 21. Output Buffer Circuits

OTR LED CIRCUIT



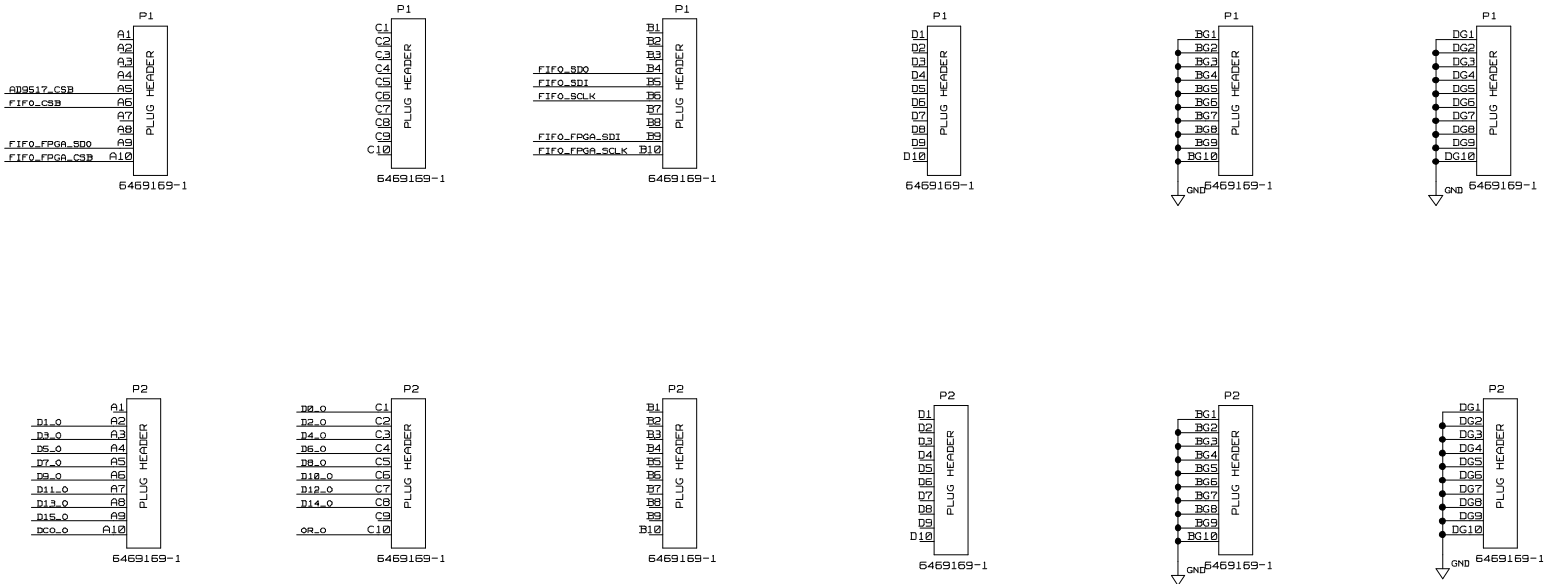


Figure 22. Capture Board Connector

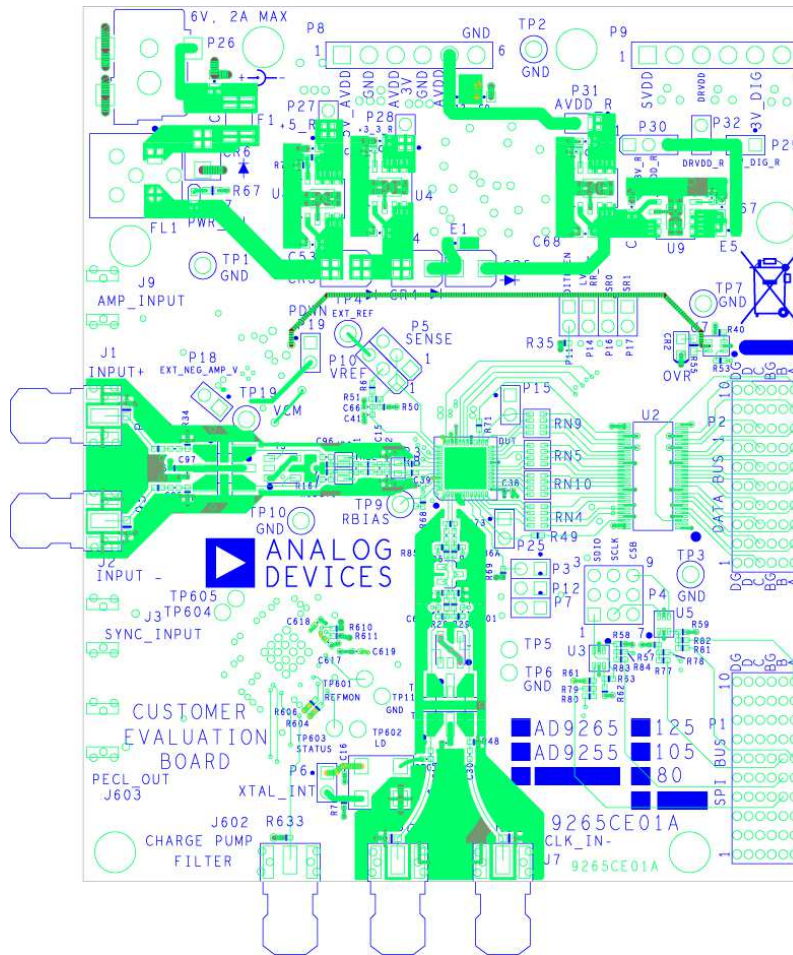


Figure 23. Top Side

06699-023

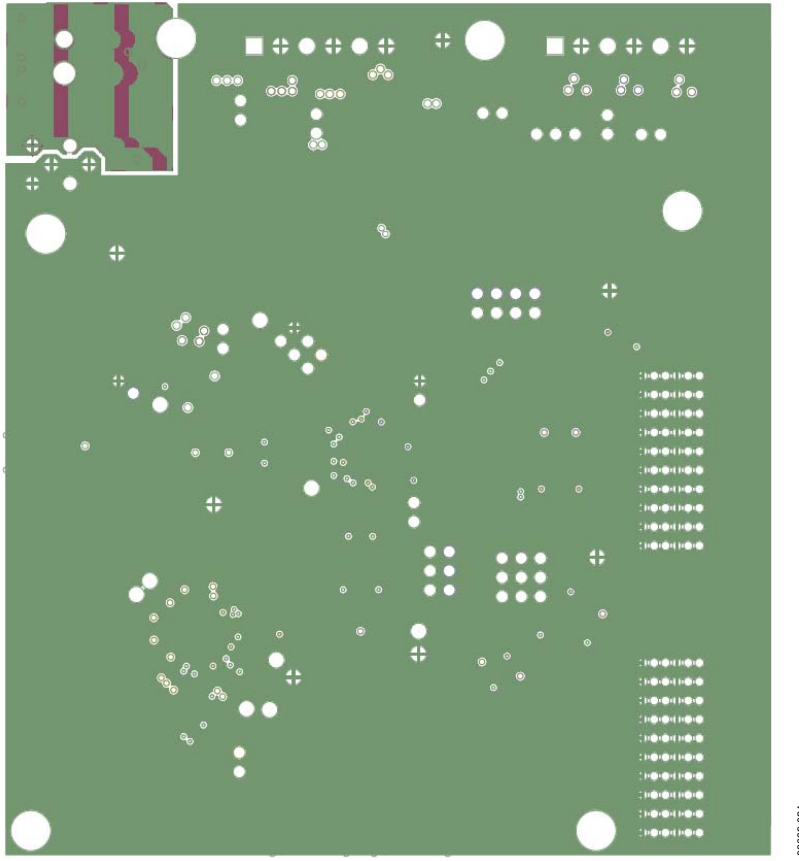


Figure 24. Ground Plane (Layer 2)

08689-024

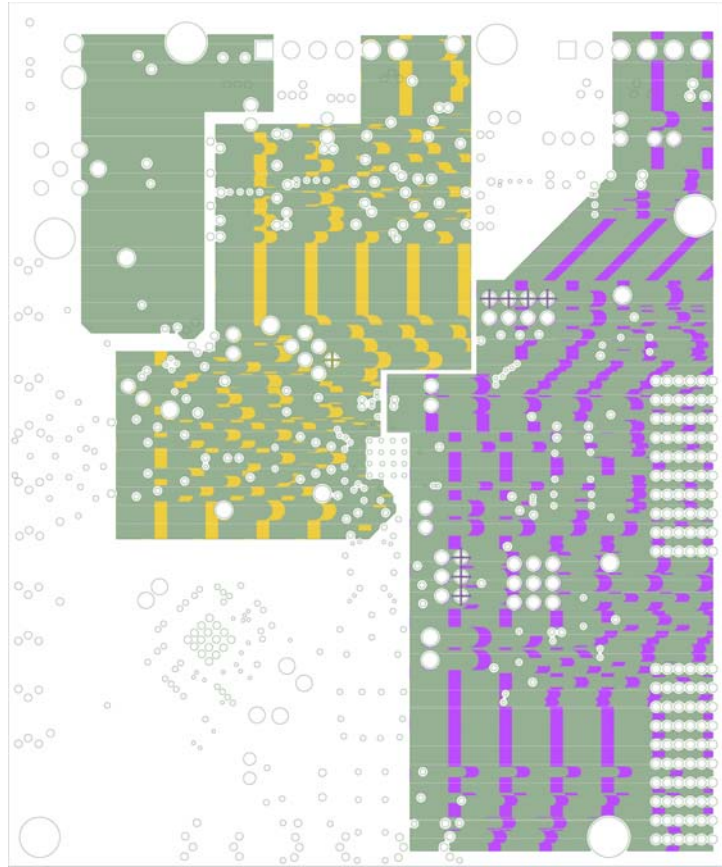


Figure 25. Power Plane (Layer 3)

08589-025

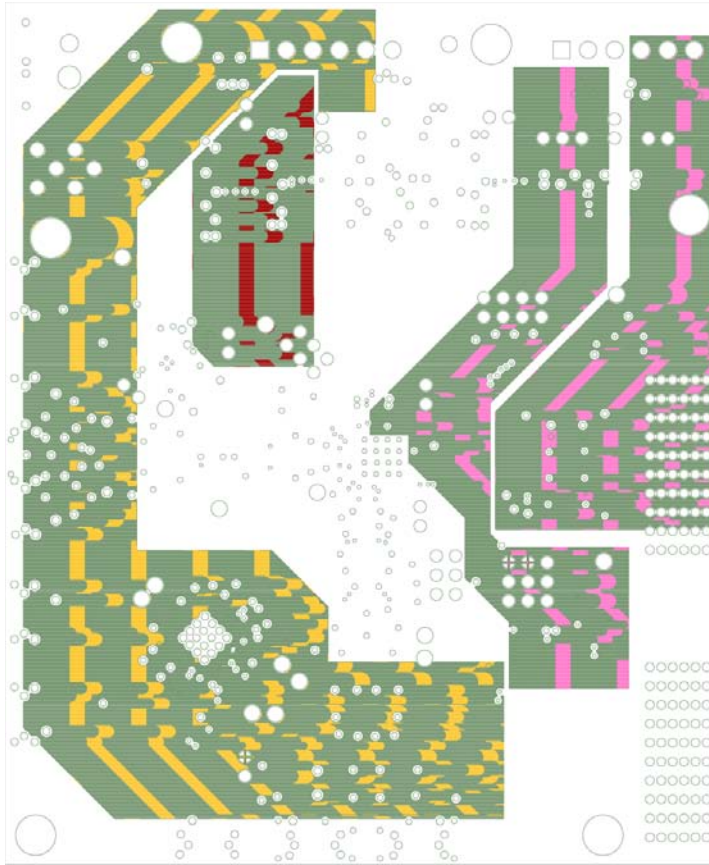


Figure 26. Power Plane (Layer 4)

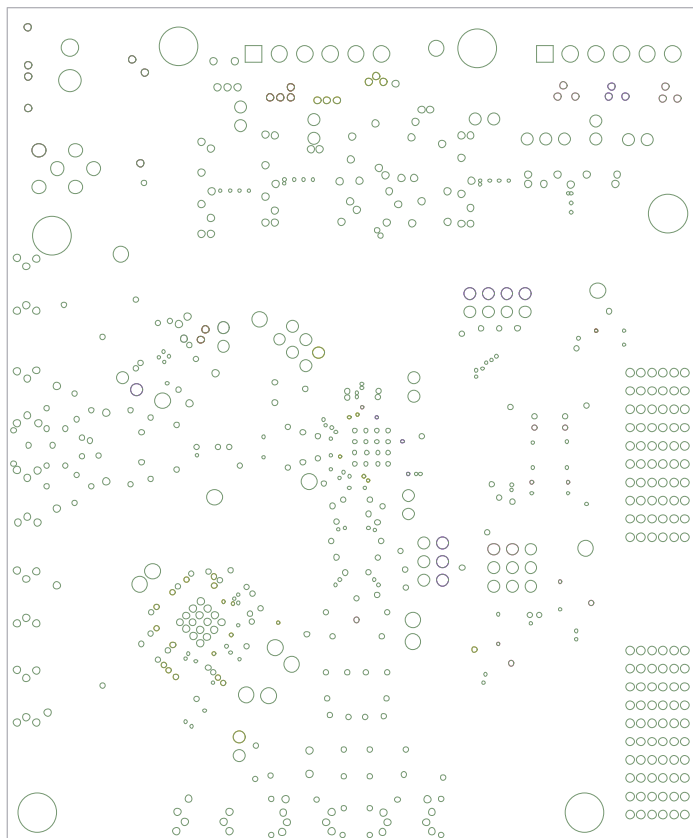


Figure 27. Ground Plane (Layer 5)

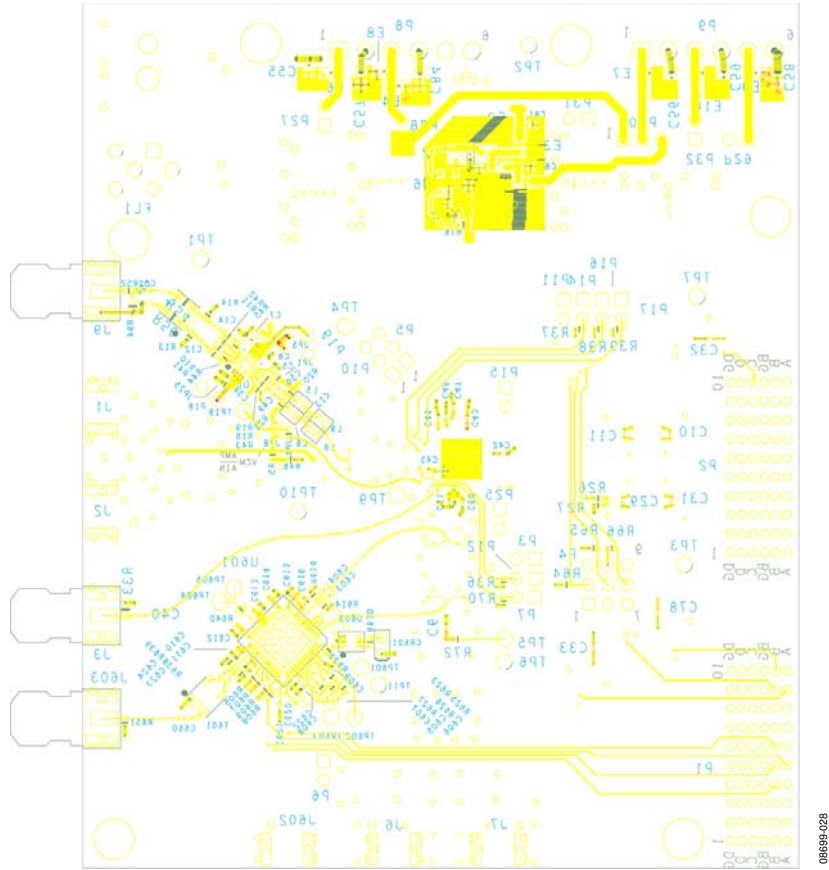


Figure 28. Bottom Side

08689-028

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. AD9265/AD9255 BOM

Item No.	Qty	Reference Designator	Description	Manufacturer/Part No.
1	1	Not applicable	Printed circuit board	
2	3	C2, C4, C15	Ceramic capacitor, multilayer, NPO, 0402, 10 pF	Phycomp (Yageo)/CC0402JRN09BN100
3	46	C3, C5, C8, C10, C11, C12, C14, C16, C18, C22, C23, C27, C29, C31, C32, C33, C34, C38, C40, C42, C43, C45, C46, C47, C48, C60, C61, C66, C71, C78, C96, C601, C602, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C621	Ceramic capacitor, 0402, 0.1 μ F	Panasonic/ECJ-0EX1C104K
4	3	C39, C41, C74	Ceramic capacitor, mono, 0402, 1 μ F	Murata/GRM155R60J105KE19D
5	8	C53, C54, C62, C64, C65, C67, C68, C69	Capacitor, 0603, X5R, 4.7 μ F	Panasonic/ECJ-1VB0J475M
6	1	C605	Ceramic capacitor, multilayer, X7R, 0402, 1800 pF	Panasonic/ECJ-0EB1E182K
7	1	C606	Ceramic capacitor, 0.033 μ F, C0402	Panasonic/0402YD333KAT2A
8	1	C607	Ceramic capacitor, 0402, 1500 pF	Panasonic/ECJ-0EB1H152K
9	1	C622	Ceramic capacitor, 0.22 μ F, C0402	Panasonic/ECJ-0EB0J224K
10	9	C7, C9, C55, C56, C57, C58, C59, C63, C84	Ceramic capacitor, monolithic, 10 μ F, C0805	Murata/GRM21BR61C106KE15L
11	2	C72, C73	Capacitor, 0603, X5R, 10 μ F	Panasonic/ECJ-1VB0J106M
12	3	C75, C82, C83	Ceramic capacitor, multilayer, X7R, 0402, 0.01 μ F	Panasonic/ECJ-0EB1E103K
13	1	CR1	Diode Schottky, dual series, SOT23	Avago/HSMS-2812BLK
14	2	CR2, CR601	LED, red, surface mount	Lumex/SML-LXT0805IW-TR
15	4	CR3, CR4, CR5, CR6	Diode, recovery rectifier, DO214AA3	Micro Commercial Components Corp/S2A-TP
16	1	CR7	LED, green, surface mount, LED0603	Panasonic/LNJ308G8TRA
17	1	DUT	Analog-to-digital converter	Analog Devices/AD9265BCPZ-80, AD9265BCPZ-105, AD9265BCPZ-125, AD9255BCPZ-80, AD9255BCPZ-105, or AD9255BCPZ-125 per build instructions
18	9	E1, E4, E5, E6, E7, E8, E9, E10, E12	Inductor ferrite bead, 100 MHz, L0805	Panasonic/EXC-ML20A390U
19	1	F1	Fuse polyswitch, PTC device 1812, 1.1 A, FTYCOMINISMDC110F	Tyco Electronics/MINISMDC110F-2
20	1	FL1	Filter noise suppression, LC combined type	Murata/BNX016-01
21	4	J1, J3, J6, J9	Conn-PCB, SMA ST, edge mount, CNSAMTECSMA-JPX-ST-EM1-MKT	Samtec/SMA-J-P-X-ST-EM1
22	2	JP5, JP8	3-pin solder jumper, JPRSLD03	Not applicable
23	2	P1, P2	Conn PCB, 60-pin RA connector, CNTYCO1469169-1	Tyco/6469169-1

Item No.	Qty	Reference Designator	Description	Manufacturer/Part No.
24	1	P26	Conn-PCB power jack surface mount, CN-2MM-PWR-JACK	CUI/PJ-002AH-SMT
25	13	P3, P6, P7, P11, P12, P14, P18, P19, P27, P28, P29, P31, P32	Conn-PCB header, 2-position, CNSAMTEC1X2H330LD36	Samtec/TSW-102-08-G-S
26	1	P4	Conn-PCB header, ST male, 9-position, CNSAMTEC3X3H338LD36	Samtec/TSW-103-08-G-T
27	3	P5, P10, P30	Conn-PCB Berg header, ST male, 3-position, CNBERG1X3H205LD36	Samtec/TSW-103-08-G-S
28	2	P8, P9	Conn-PCB header, 6-position, CNWIELAND5313625	Wieland/Z5.531.3625.0
29	22	R1, R6, R10, R11, R30, R31, R46, R47, R48, R52, R53, R77, R79, R81, R83, R85, R86, R608, R623, R627, R629, JP4	Resistor film, SMD, 0402, 0 Ω	Panasonic/ERJ-2GE0R00X
30	4	R13, R14, R15, R16	Resistor film, SMD, 0402, 33 Ω	Panasonic/ERJ-2GEJ330X
31	15	R26, R27, R35, R36, R37, R38, R39, R40, R43, R57, R58, R59, R68, R69, R70	Resistor, precision, thick film chip, R0402, 10 k Ω	Panasonic/ERJ-2RKF1002X
32	4	R3, R8, R22, R23	Resistor, precision, thick film chip, R0402, 10 Ω	Panasonic/ERJ-2RKF10R0X
33	2	R25, R33	Resistor, precision, thick film chip, R0603, 49.9 Ω	Panasonic/ERJ-3EKF49R9V
34	2	R49, R71	Resistor, precision, thick film chip, R0402, 22 Ω	Panasonic/ERJ-2RKF22R0X
35	2	R55, R67	Resistor, precision, thick film chip, R0603, 249 Ω	Panasonic/ERJ-3EKF2490V
36	1	R610	Resistor, precision, thick film chip, R0402, 4.12 k Ω	Panasonic/ERJ-2RKF4121X
37	1	R611	Resistor, precision, thick film chip, R0402, 5.11 k Ω	Panasonic/ERJ-2RKF5111X
38	4	R614, R616, R625, R630	Resistor, precision, thick film chip, R0402, 200 Ω	Panasonic/ERJ-2RKF2000X
39	2	R626, R640	Resistor, film, SMD 0402, 100 Ω	Venkel/CR0402-16W-1000FPT
40	3	R64, R65, R66	Resistor, precision, thick film chip, R0402, 100 k Ω	Panasonic/ERJ-2RKF1003X
41	9	R7, R61, R62, R63, R604, R605, R606, R607, R609	Resistor, precision, thick film chip, R0402, 1.00 k Ω	Panasonic/ERJ-2RKF1001X
42	1	R74	Resistor, precision, thick film chip, R0402, 147 k Ω	Panasonic/ERJ-2RKF1473X
43	1	R75	Resistor, precision, thick film chip, R0402, 28 k Ω	Panasonic/ERJ-2RKF2802X
44	4	RN4, RN5, RN9, RN10	Resistor network, 8-pin/4 resistor surface mount, RESNET742-4, 22 Ω	CTS/742C083220JCT
45	3	T2, T3, T9	XFMR RF 1:1, ETC1	M/A-COM/MABA-007159-000000
46	1	U1	IC, 2.6 GHz, ultralow distortion, differential IF/RF amplifier, QFN16_3X3_PAD1_5X1_5	Analog Devices/ADL5562_PRELIM
47	1	U2	IC-TTL low volt 20-bit buffer, TSSOP56	Fairchild/74VCX162827MTDX
48	1	U3	IC TinyLogic UHS dual buffer, SC70	Fairchild/NC7WZ07P6X
49	1	U4	IC, low dropout CMOS, lin reg, SO8NB-PAD3_1X2_41	Analog Devices/ADP1706ARDZ-3.3-R7
50	3	U5, U7, U603	IC TinyLogic UHS dual buffer, SC70	Fairchild/NC7WZ16P6X