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16-Bit, 125 MSPS/105 MSPS/80 MSPS, 1.8 V Analog-to-Digital Converter

Data Sheet **AD9265**

FEATURES

SNR = 79.0 dBFS at 70 MHz and 125 MSPS
SFDR = 93 dBc at 70 MHz and 125 MSPS
Low power: 373 mW at 125 MSPS
1.8 V analog supply operation
1.8 V CMOS or LVDS output supply
Integer 1-to-8 input clock divider
IF sampling frequencies to 300 MHz
−154.3 dBm/Hz small signal input noise with 200 Ω input impedance at 70 MHz and 125 MSPS
Optional on-chip dither
Programmable internal ADC voltage reference
Integrated ADC sample-and-hold inputs
Flexible analog input range: 1 V p-p to 2 V p-p
Differential analog inputs with 650 MHz bandwidth
ADC clock duty cycle stabilizer
Serial port control
User-configurable, built-in self-test (BIST) capability
Energy-saving power-down modes

APPLICATIONS

Communications
Multimode digital receivers (3G)
GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, and TD-SCDMA
Smart antenna systems
General-purpose software radios
Broadband data applications
Ultrasound equipment

PRODUCT HIGHLIGHTS

1. On-chip dither option for improved SFDR performance with low power analog input.
2. Proprietary differential input that maintains excellent SNR performance for input frequencies up to 300 MHz.
3. Operation from a single 1.8 V supply and a separate digital output driver supply accommodating 1.8 V CMOS or LVDS outputs.
4. Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock duty cycle stabilizer, DCS, power-down, test modes, and voltage reference mode.
5. Pin compatibility with the AD9255, allowing a simple migration from 16 bits down to 14 bits.

FUNCTIONAL BLOCK DIAGRAM

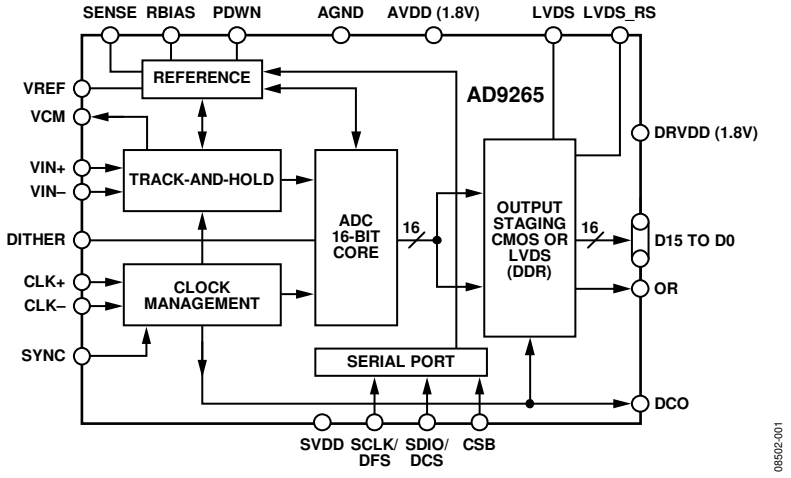

Figure 1.

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- AD9265: 16-Bit, 125 MSPS/105 MSPS/80 MSPS, 1.8 V Analog-to-Digital Converter Data Sheet

User Guides

- UG-074: Evaluating the AD9265/AD9255 Analog-to-Digital Converters

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- AD9265 Native FMC Card / ML605 Xilinx Reference Design

TOOLS AND SIMULATIONS

- Visual Analog
- AD9265 IBIS Models
- AD9255/AD9265 S-Parameters

REFERENCE DESIGNS

- CN0252

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Analog-to-Digital Converter and Drivers ICs Solutions Bulletin, Volume 10, Issue 2

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- Improve The Design Of Your Passive Wideband ADC Front-End Network
- MS-2210: Designing Power Supplies for High Speed ADC
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GENERAL DESCRIPTION

The AD9265 is a 16-bit, 125 MSPS analog-to-digital converter (ADC). The AD9265 is designed to support communications applications where high performance combined with low cost, small size, and versatility is desired.

The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic to provide 16-bit accuracy at 125 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The ADC features a wide bandwidth differential sample-and-hold analog input amplifier supporting a variety of user-selectable input ranges. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available ADCs, the AD9265 is suitable for applications in communications, instrumentation and medical imaging.

A differential clock input controls all internal conversion cycles. A duty cycle stabilizer provides the means to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance over a wide range of input clock duty cycles. An integrated voltage reference eases design considerations.

The ADC output data format is either parallel 1.8 V CMOS or LVDS (DDR). A data output clock is provided to ensure proper latch timing with receiving logic.

Programming for setup and control is accomplished using a 3-wire SPI-compatible serial interface. Flexible power-down options allow significant power savings, when desired. An optional on-chip dither function is available to improve SFDR performance with low power analog input signals.

The AD9265 is available in a Pb-free, 48-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, SVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 1.

		AD9265BCPZ-80[1]			AD9265BCPZ-105[1]			AD9265BCPZ-125[1]			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	16			16			16			Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full		±0.05	±0.25		±0.05	±0.25		±0.05	±0.25	% FSR
Gain Error	Full		±0.2	±2.5		±0.2	±2.5		±0.4	±2.5	% FSR
Differential Nonlinearity (DNL)[2]	Full	−1.0		+1.25	−1.0		+1.25	−1.0		+1.25	LSB
	25°C		±0.6			±0.65			±0.7		LSB
Integral Nonlinearity (INL)[2]	Full			±2.5			±3.5			±4.5	LSB
	25°C		±1.5			±2.0			±3.0		LSB
TEMPERATURE DRIFT											
Offset Error	Full		±2			±2			±2		ppm/°C
Gain Error	Full		±15			±15			±15		ppm/°C
INTERNAL VOLTAGE REFERENCE											
Output Voltage Error (1 V Mode)	Full		+8	±12		+8	±12		+8	±12	mV
Load Regulation at 1.0 mA	Full		3			3			3		mV
INPUT REFERRED NOISE											
VREF = 1.0 V	25°C		2.17			2.26			2.17		LSB rms
ANALOG INPUT											
Input Span, VREF = 1.0 V	Full		2			2			2		V p-p
Input Capacitance[3]	Full		8			8			8		pF
Input Common-Mode Voltage	Full		0.9			0.9			0.9		V
REFERENCE INPUT RESISTANCE	Full		6			6			6		kΩ
POWER SUPPLIES											
Supply Voltage											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
SVDD	Full	1.7		3.5	1.7		3.5	1.7		3.5	V
Supply Current											
IAVDD[2]	Full		126	131		169	176		194	202	mA
IDRVDD[2]											
1.8 V CMOS	Full		14			20			24		mA
1.8 V LVDS	Full		43			46			49		mA
POWER CONSUMPTION											
DC Input	Full		241	258		323	343		373	392	mW
Sine Wave Input[2]											
DRVDD = 1.8 V											
CMOS Output Mode	Full		254			341			394		mW
LVDS Output Mode	Full		308			391			439		mW
Standby Power[4]	Full		54			54			54		mW
Power-Down Power	Full		0.05	0.15		0.05	0.15		0.05	.015	mW

[1] The suffix following the part number refers to the model found in the Ordering Guide section.
[2] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[4] Standby power is measured with a dc input, the CLK pins (CLK+, CLK–) inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, SVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 2.

		AD9265BCPZ-80[2]			AD9265BCPZ-105[2]			AD9265BCPZ-125[2]			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)											
f_{IN} = 2.4 MHz	25°C		80.2			79.7			79.0		dBFS
f_{IN} = 70 MHz	25°C		79.7			79.2			79.0		dBFS
	Full	78.7			78.2			77.3			dBFS
f_{IN} = 140 MHz	25°C		78.4			78.3			77.5		dBFS
f_{IN} = 200 MHz	25°C		77.1			76.9			75.6		dBFS
SIGNAL-TO-NOISE-AND DISTORTION (SINAD)											
f_{IN} = 2.4 MHz	25°C		79.6			79.4			78.7		dBFS
f_{IN} = 70 MHz	25°C		79.6			78.8			78.7		dBFS
	Full	78.6			77.9			77.0			dBFS
f_{IN} = 140 MHz	25°C		77.3			77.5			77.0		dBFS
f_{IN} = 200 MHz	25°C		76.0			75.7			74.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 2.4 MHz	25°C		12.9			12.9			12.8		Bits
f_{IN} = 70 MHz	25°C		12.9			12.8			12.8		Bits
f_{IN} = 140 MHz	25°C		12.5			12.6			12.5		Bits
f_{IN} = 200 MHz	25°C		12.3			12.3			12.1		Bits
WORST SECOND OR THIRD HARMONIC											
f_{IN} = 2.4 MHz	25°C		−88			−90			−88		dBc
f_{IN} = 70 MHz	25°C		−94			−89			−93		dBc
	Full			−92			−88			−85	dBc
f_{IN} = 140 MHz	25°C		−82			−86			−89		dBc
f_{IN} = 200 MHz	25°C		−81			−81			−80		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)											
f_{IN} = 2.4 MHz	25°C		88			90			88		dBc
f_{IN} = 70 MHz	25°C		94			89			93		dBc
	Full	92			88			85			dBc
f_{IN} = 140 MHz	25°C		82			86			89		dBc
f_{IN} = 200 MHz	25°C		81			81			80		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)											
Without Dither (AIN at −23 dBFS)											
f_{IN} = 2.4 MHz	25°C		103			98			96		dBFS
f_{IN} = 70 MHz	25°C		103			96			98		dBFS
f_{IN} = 140 MHz	25°C		104			96			98		dBFS
f_{IN} = 200 MHz	25°C		102			101			97		dBFS
With On-Chip Dither (AIN at −23 dBFS)											
f_{IN} = 2.4 MHz	25°C		110			108			108		dBFS
f_{IN} = 70 MHz	25°C		110			109			110		dBFS
f_{IN} = 140 MHz	25°C		110			109			109		dBFS
f_{IN} = 200 MHz	25°C		110			109			109		dBFS

Parameter[1]	Temp	AD9265BCPZ-80[2] Min	Typ	Max	AD9265BCPZ-105[2] Min	Typ	Max	AD9265BCPZ-125[2] Min	Typ	Max	Unit
WORST OTHER (HARMONIC OR SPUR)											
Without Dither											
f_{IN} = 2.4 MHz	25°C		−106			−105			−101		dBc
f_{IN} = 70 MHz	25°C		−106			−104			−103		dBc
	Full			−97			−95			−92	dBc
f_{IN} = 140 MHz	25°C		−104			−103			−104		dBc
f_{IN} = 200 MHz	25°C		−102			−103			−100		dBc
With On-Chip Dither											
f_{IN} = 2.4 MHz	25°C		−106			−105			−102		dBc
f_{IN} = 70 MHz	25°C		−106			−105			−103		dBc
	Full			−97			−99			−98	dBc
f_{IN} = 140 MHz	25°C		−104			−103			−104		dBc
f_{IN} = 200 MHz	25°C		−101			−101			−100		dBc
TWO-TONE SFDR											
Without Dither											
f_{IN} = 29 MHz (−7 dBFS), 32 MHz (−7 dBFS)	25°C		93			90			95		dBc
f_{IN} = 169 MHz (−7 dBFS), 172 MHz (−7 dBFS)	25°C		80			78			79		dBc
ANALOG INPUT BANDWIDTH	25°C		650			650			650		MHz

[1] See Application Note AN-835, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] The suffix following the part number refers to the model found in the Ordering Guide section.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, SVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ

Parameter	Temperature	Min	Typ	Max	Unit
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		SVDD	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK/DFS)[2]					
High Level Input Voltage	Full	1.22		SVDD	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 1.8 V)	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO/DCS)[1]					
High Level Input Voltage	Full	1.22		SVDD	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
High Level Output Voltage	Full	1.70			V
Low Level Output Voltage	Full			0.2	V
LOGIC INPUTS (OEB, PDWN, DITHER, LVDS, LVDS_RS)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 1.8 V)	Full	−90		−134	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS (DRVDD = 1.8 V)					
CMOS Mode					
High Level Output Voltage					
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V
LVDS Mode					
ANSI Mode					
Differential Output Voltage (V_{OD})	Full	290	345	400	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Reduced Swing Mode					
Differential Output Voltage (V_{OD})	Full	160	200	230	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V

[1] Pull-up.
[2] Pull-down.

SWITCHING SPECIFICATIONS

−1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 4.

Parameter	Temp	AD9265BCPZ-80[1] Min	Typ	Max	AD9265BCPZ-105[1] Min	Typ	Max	AD9265BCPZ-125[1] Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS											
Input Clock Rate	Full			625			625			625	MHz
Conversion Rate[2]											
DCS Enabled	Full	20		80	20		105	20		125	MSPS
DCS Disabled	Full	10		80	10		105	10		125	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	12.5			9.5			8			ns
CLK Pulse Width High (t_{CH})											
Divide-by-1 Mode, DCS Enabled	Full	3.75	6.25	8.75	2.85	4.75	6.65	2.4	4	5.6	ns
Divide-by-1 Mode, DCS Disabled		5.9	6.25	6.6	4.5	4.75	5.0	3.8	4	4.2	ns
Divide-by-3 Mode, Divide-by-5 Mode, and Divide-by-7 Mode, DCS Enabled[3]	Full	0.8			0.8			0.8			ns
Divide-by-2 Mode, Divide-by-4 Mode, Divide-by-6 Mode and Divide-by-8 Mode, DCS Enabled or DCS Disabled[3]	Full	0.8			0.8			0.8			ns
Aperture Delay (t_A)	Full		1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.07			0.07			0.07		ps rms
DATA OUTPUT PARAMETERS											
CMOS Mode											
Data Propagation Delay (t_{PD})	Full	2.4	2.8	3.4	2.4	2.8	3.4	2.4	2.8	3.4	ns
DCO Propagation Delay (t_{DCO})[4]	Full	2.7	3.4	4.2	2.7	3.4	4.2	2.7	3.4	4.2	ns
DCO to Data Skew (t_{SKEW})	Full	0.3	0.6	0.9	0.3	0.6	0.9	0.3	0.6	0.9	ns
Pipeline Delay (Latency)	Full		12			12			12		Cycles
LVDS Mode											
Data Propagation Delay (t_{PD})	Full	2.6	3.4	4.2	2.6	3.4	4.2	2.6	3.4	4.2	ns
DCO Propagation Delay (t_{DCO})[4]	Full	3.3	3.8	4.3	3.3	3.8	4.3	3.3	3.8	4.3	ns
DCO to Data Skew (t_{SKEW})	Full	−0.3	0.4	1.2	−0.3	0.4	1.2	−0.3	0.4	1.2	ns
Pipeline Delay (Latency)	Full		12.5			12.5			12.5		Cycles
Wake-Up Time[5]	Full		500			500			500		µs
OUT-OF-RANGE RECOVERY TIME	Full		2			2			2		Cycles

[1] The suffix following the part number refers to the model found in the Ordering Guide section.
[2] Conversion rate is the clock rate after the divider.
[3] See the Input Clock Divider section for additional information on using the DCS with the input clock divider.
[4] Additional DCO delay can be added by writing to Bit 0 through Bit 4 in SPI Register 0x17 (see Table 17).
[5] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to rising edge of CLK setup time		0.30		ns
t_{HSYNC}	SYNC to rising edge of CLK hold time		0.40		ns
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	SCLK pulse width high	10			ns
t_{LOW}	SCLK pulse width low	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

Timing Diagrams

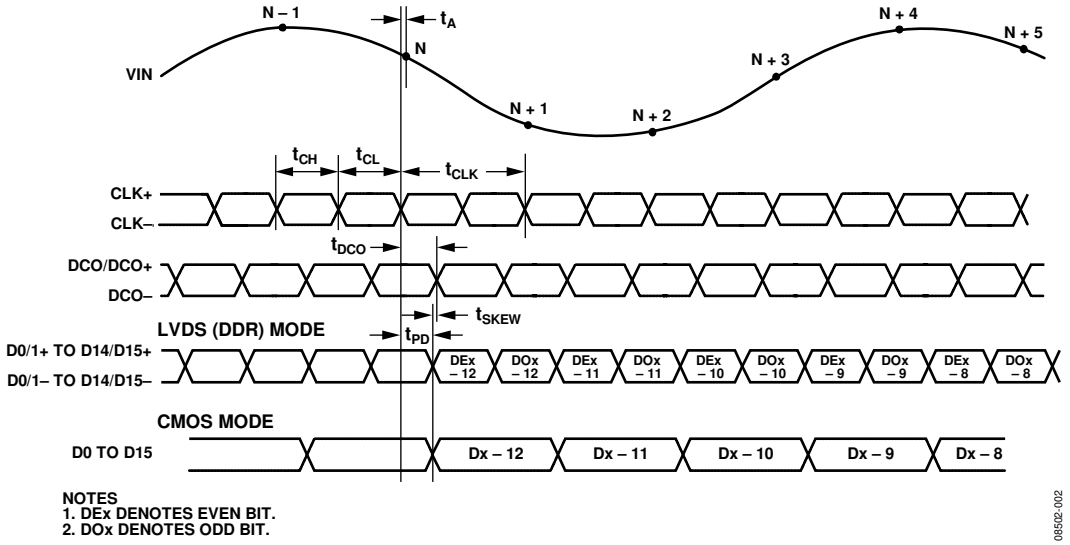

Figure 2. LVDS (DDR) and CMOS Output Mode Data Output Timing

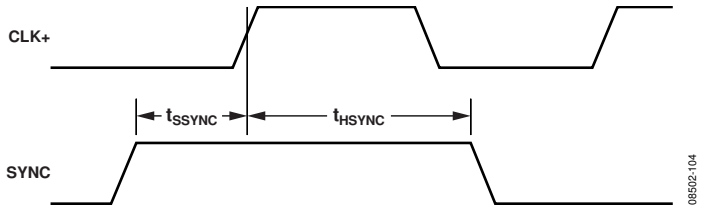

Figure 3. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0V
SVDD to AGND	−0.3 V to +3.6 V
VIN+, VIN− to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to SVDD +0.3 V
SCLK/DFS to AGND	−0.3 V to SVDD +0.3 V
SDIO/DCS to AGND	−0.3V to SVDD + 0.3 V
OEB to AGND	−0.3 V to DRVDD + 0.2 V
PDWN to AGND	−0.3 V to DRVDD + 0.2 V
LVDS to AGND	−0.3 V to AVDD + 0.2 V
LVDS_RS to AGND	−0.3 V to AVDD + 0.2 V
DITHER to AGND	−0.3 V to AVDD + 0.2 V
D0 through D15 to AGND	−0.3 V to DRVDD + 0.2 V
DCO to AGND	−0.3 V to DRVDD + 0.2 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints and maximizes the thermal capability of the package.

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/s)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Unit
48-Lead LFCSP (CP-48-8)	0	24.5	1.3	12.7	°C/W
	1.0	21.4			°C/W
	2.5	19.2			°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

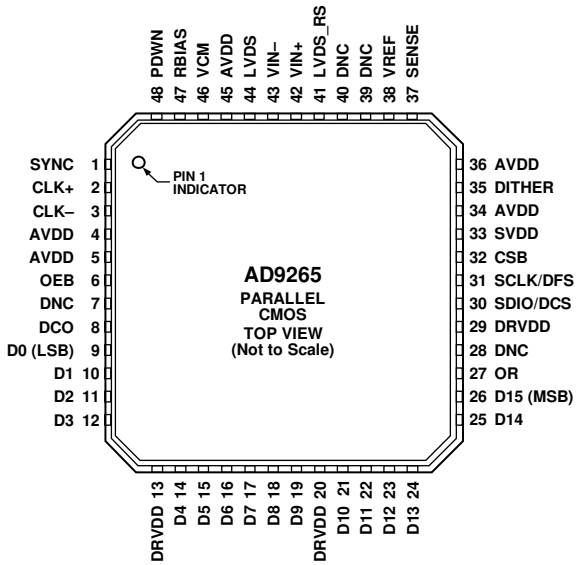

Figure 4. LFCSP Parallel CMOS Pin Configuration (Top View)

Table 8. Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
13, 20, 29	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
4, 5, 34, 36, 45	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
33	SVDD	Supply	SPI Input/Output Voltage.
7, 28, 39, 40	DNC		Do Not Connect.
0	AGND	Ground	Analog Ground. The exposed thermal pad on the bottom of the package provides the analog ground for the input. This exposed pad must be connected to ground for proper operation.
ADC Analog			
42	VIN+	Input	Differential Analog Input Pin (+).
43	VIN–	Input	Differential Analog Input Pin (–).
38	VREF	Input/output	Voltage Reference Input/Output.
37	SENSE	Input	Voltage Reference Mode Select. See Table 11 for details.
47	RBIAS	Input/output	External Reference Bias Resistor.
46	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
2	CLK+	Input	ADC Clock Input—True.
3	CLK–	Input	ADC Clock Input—Complement.
Digital Input			
1	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
9	D0 (LSB)	Output	CMOS Output Data.
10	D1	Output	CMOS Output Data.
11	D2	Output	CMOS Output Data.
12	D3	Output	CMOS Output Data.
14	D4	Output	CMOS Output Data.
15	D5	Output	CMOS Output Data.
16	D6	Output	CMOS Output Data.
17	D7	Output	CMOS Output Data.
18	D8	Output	CMOS Output Data.

Pin No.	Mnemonic	Type	Description
19	D9	Output	CMOS Output Data.
21	D10	Output	CMOS Output Data.
22	D11	Output	CMOS Output Data.
23	D12	Output	CMOS Output Data.
24	D13	Output	CMOS Output Data.
25	D14	Output	CMOS Output Data.
26	D15 (MSB)	Output	CMOS Output Data.
27	OR	Output	Overrange Output.
8	DCO	Output	Data Clock Output.
SPI Control			
31	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
30	SDIO/DCS	Input/output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
32	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
6	OEB	Input	Output Enable Input (Active Low).
35	DITHER	Input	In external pin mode, this pin sets dither to on (active high). Pull low for control via SPI in SPI mode.
41	LVDS_RS	Input	In external pin mode, this pin sets LVDS reduced swing output mode (active high). Pull low for control via SPI in SPI mode.
44	LVDS	Input	In external pin mode, this pin sets LVDS output mode (active high). Pull low for control via SPI in SPI mode.
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.

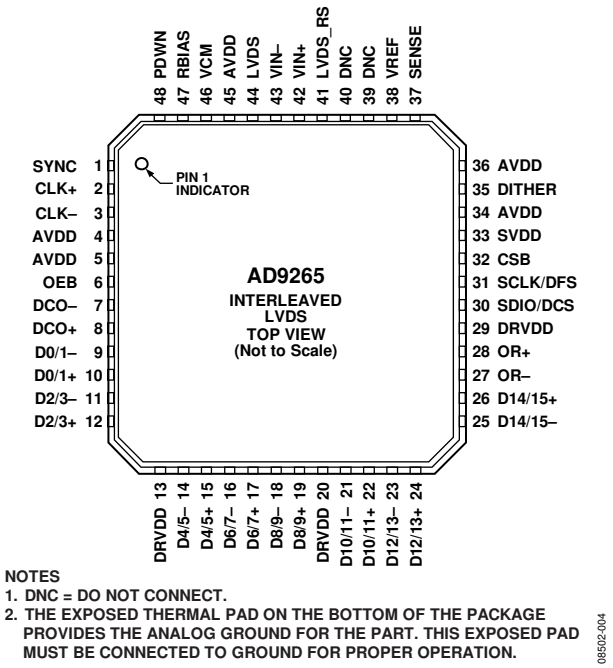

Figure 5. LFCSP Interleaved Parallel LVDS Pin Configuration (Top View)

Table 9. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
13, 20, 29	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
4, 5, 34, 36, 45	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
33	SVDD	Supply	SPI Input/Output Voltage.
39, 40	DNC		Do Not Connect.
0	AGND	Ground	Analog Ground. The exposed thermal pad on the bottom of the package provides the analog ground for the input. This exposed pad must be connected to ground for proper operation.
ADC Analog			
42	VIN+	Input	Differential Analog Input Pin (+).
43	VIN–	Input	Differential Analog Input Pin (–).
38	VREF	Input/output	Voltage Reference Input/Output.
37	SENSE	Input	Voltage Reference Mode Select. See Table 11 for details.
47	RBIAS	Input/output	External Reference Bias Resistor.
46	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
2	CLK+	Input	ADC Clock Input—True.
3	CLK–	Input	ADC Clock Input—Complement.
Digital Input			
1	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
10	D0/1+	Output	LVDS Output Data Bit 0/Bit 1 (LSB)—True.
9	D0/1–	Output	LVDS Output Data Bit 0/Bit 1 (LSB)—Complement.
12	D2/3+	Output	LVDS Output Data Bit 2/Bit 3—True.
11	D2/3–	Output	LVDS Output Data Bit 2/Bit 3—Complement.
15	D4/5+	Output	LVDS Output Data Bit 4/Bit 5—True.
14	D4/5–	Output	LVDS Output Data Bit 4/Bit 5—Complement.
17	D6/7+	Output	LVDS Output Data Bit 6/Bit 7—True.
16	D6/7–	Output	LVDS Output Data Bit 6/Bit 7—Complement.
19	D8/9+	Output	LVDS Output Data Bit 8/Bit 9 —True.
18	D8/9–	Output	LVDS Output Data Bit 8/Bit 9—Complement.

Pin No.	Mnemonic	Type	Description
22	D10/11+	Output	LVDS Output Data Bit 10/Bit 11—True.
21	D10/11−	Output	LVDS Output Data Bit 10/Bit 11—Complement.
24	D12/13+	Output	LVDS Output Data Bit 12/Bit 13—True.
23	D12/13−	Output	LVDS Output Data Bit 12/Bit 13—Complement.
26	D14/15+	Output	LVDS Output Data Bit 14/Bit 15 (MSB)—True.
25	D14/15−	Output	LVDS Output Data Bit 14/Bit 15 (MSB)—Complement.
28	OR+	Output	LVDS Overrange Output—True.
27	OR−	Output	LVDS Overrange Output—Complement.
8	DCO+	Output	LVDS Data Clock Output—True.
7	DCO−	Output	LVDS Data Clock Output—Complement.
SPI Control			
31	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
30	SDIO/DCS	Input/output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
32	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
6	OEB	Input	Output Enable Input (Active Low).
35	DITHER	Input	In external pin mode, this pin sets dither to on (active high). Pull low for control via SPI in SPI mode.
41	LVDS_RS	Input	In external pin mode, this pin sets LVDS reduced swing output mode (active high). Pull low for control via SPI in SPI mode.
44	LVDS	Input	In external pin mode, this pin sets LVDS output mode (active high). Pull low for control via SPI in SPI mode.
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, SVDD = 1.8 V, sample rate = 125 MSPS, DCS enabled, 1.0 V internal reference, 2 V p-p differential input, VIN = −1.0 dBFS, and 32k sample, T_A = 25°C, unless otherwise noted.

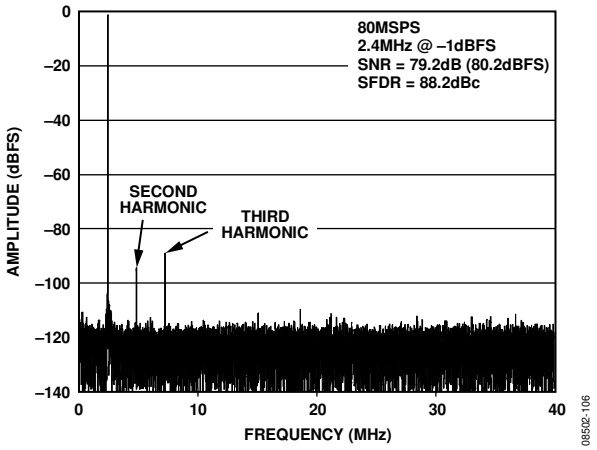

Figure 6. AD9265-80 Single-Tone FFT with f_{IN} = 2.4 MHz

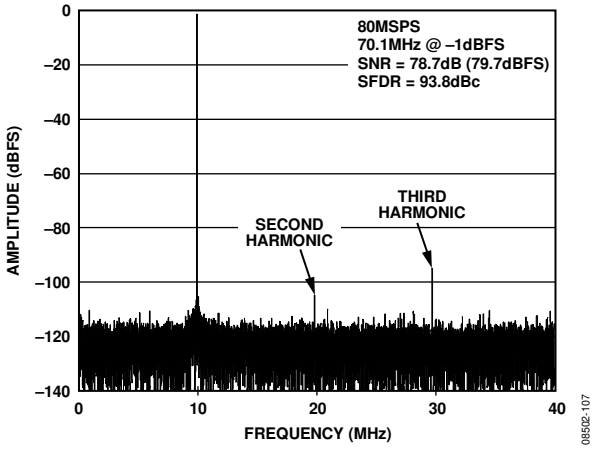

Figure 7. AD9265-80 Single-Tone FFT with f_{IN} = 70.1 MHz

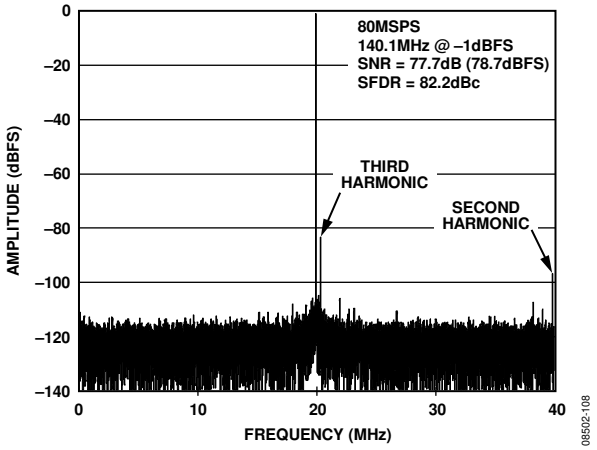

Figure 8. AD9265-80 Single-Tone FFT with f_{IN} = 140.1 MHz

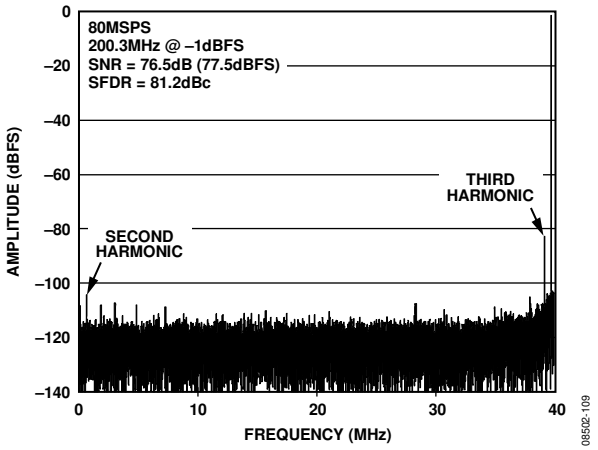

Figure 9. AD9265-80 Single-Tone FFT with f_{IN} = 200.3 MHz

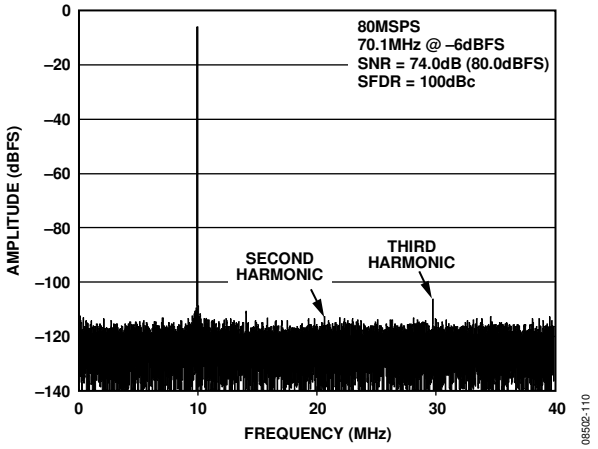

Figure 10. AD9265-80 Single-Tone FFT with f_{IN} = 70.1 MHz @ −6 dBFS with Dither Enabled

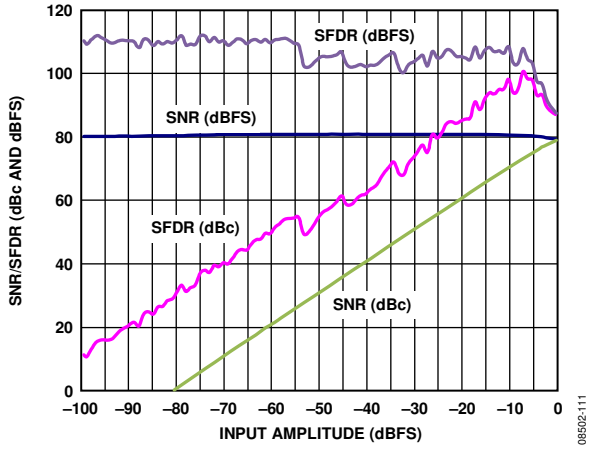

Figure 11. AD9265-80 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 98.12 MHz

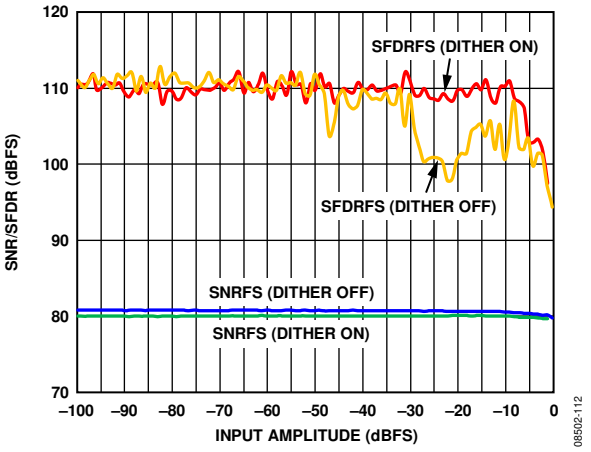

Figure 12. AD9265-80 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 30 MHz With and Without Dither Enabled

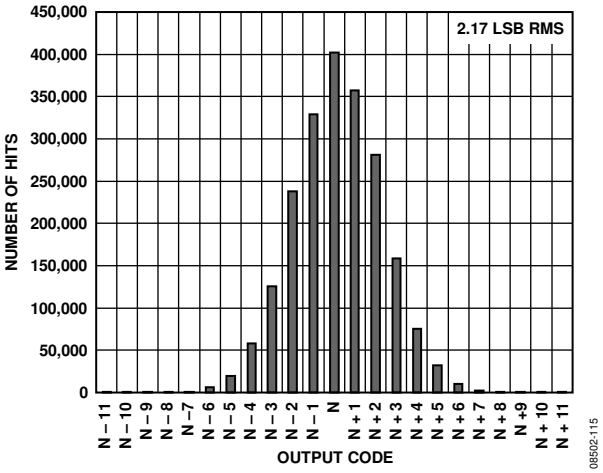

Figure 15. AD9265-80 Grounded Input Histogram

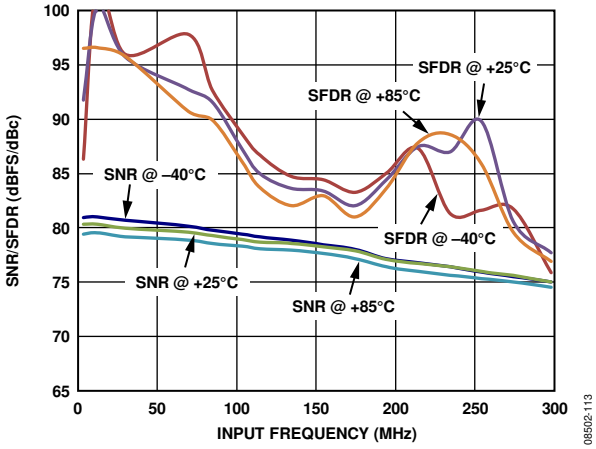

Figure 13. AD9265-80 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2 V p-p Full Scale

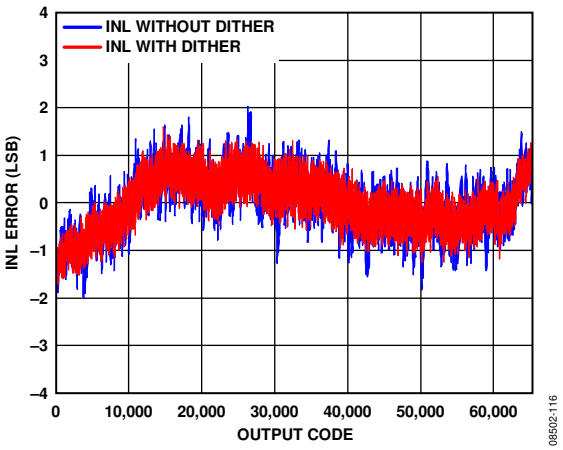

Figure 16. AD9265-80 INL with f_{IN} = 12.5 MHz

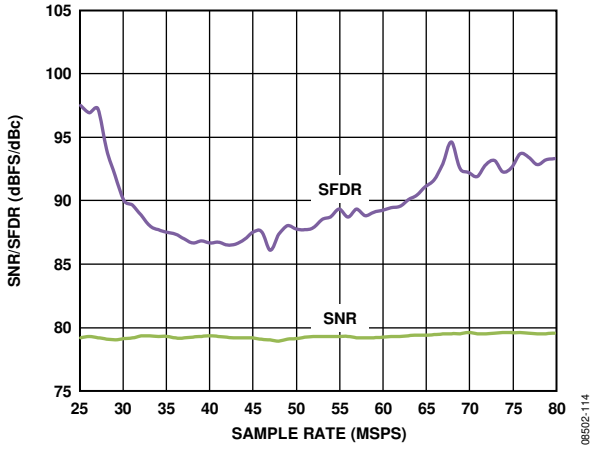

Figure 14. AD9265-80 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 70.1 MHz

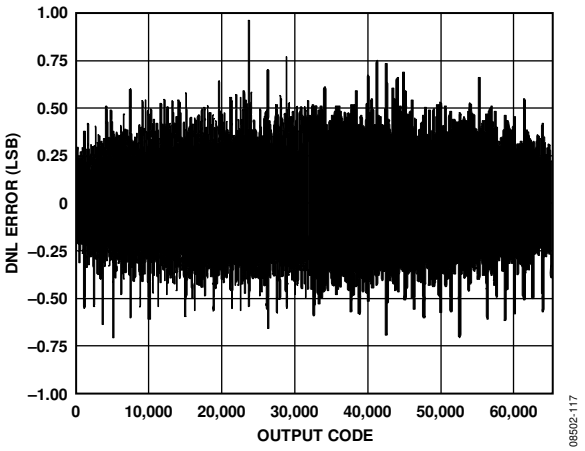

Figure 17. AD9265-80 DNL with f_{IN} = 12.5 MHz

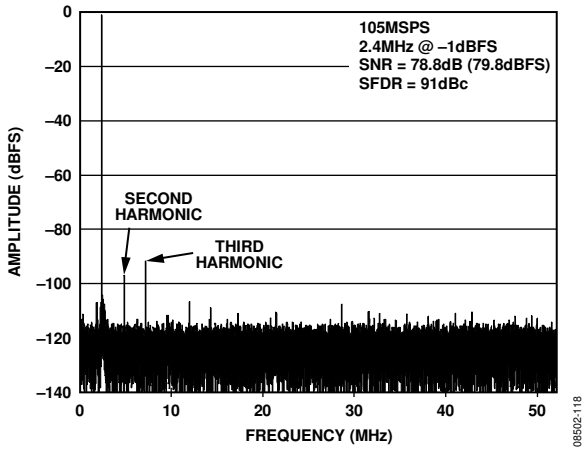

Figure 18. AD9265-105 Single-Tone FFT with f_{IN} = 2.4 MHz

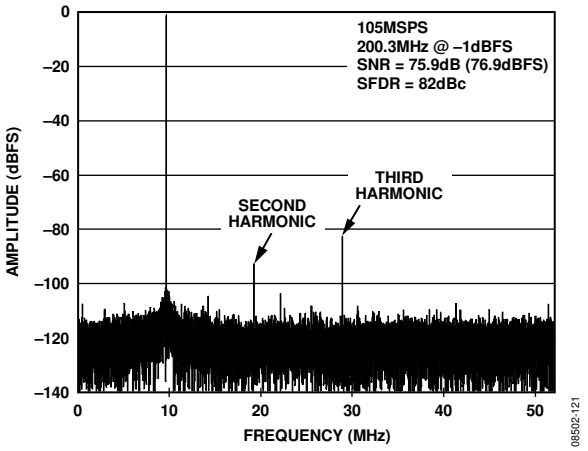

Figure 21. AD9265-105 Single-Tone FFT with f_{IN} = 200.3 MHz

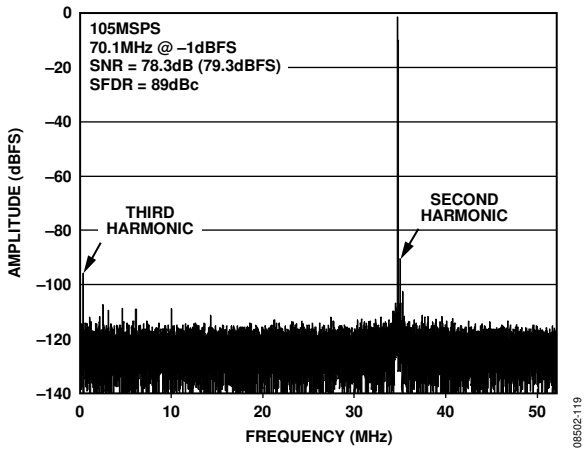

Figure 19. AD9265-105 Single-Tone FFT with f_{IN} = 70.1 MHz

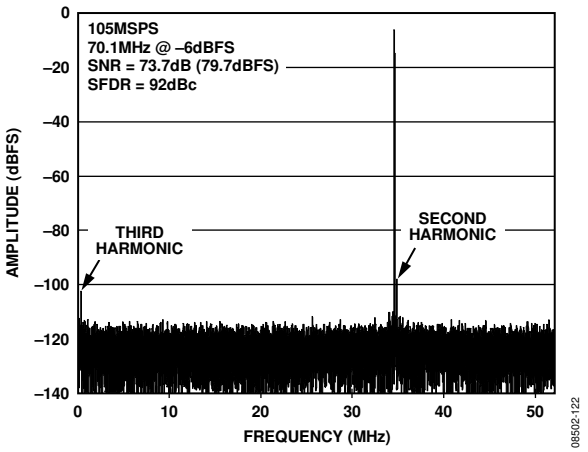

Figure 22. AD9265-105 Single-Tone FFT with f_{IN} = 70.1 MHz at –6dBFS with Dither Enabled

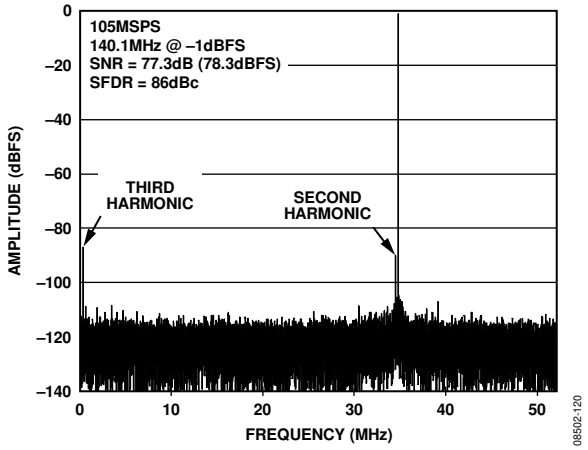

Figure 20. AD9265-105 Single-Tone FFT with f_{IN} = 140.1 MHz

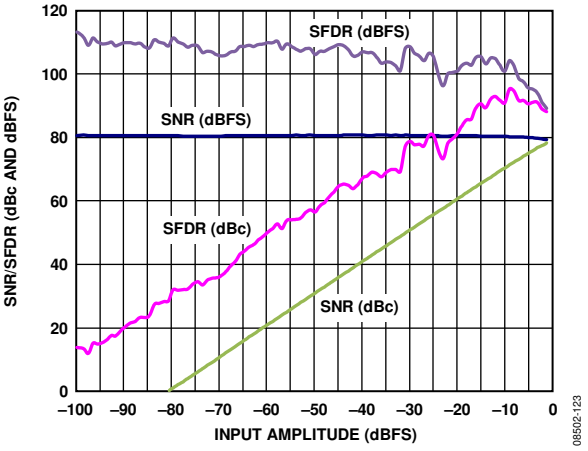

Figure 23. AD9265-105 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 98.12 MHz

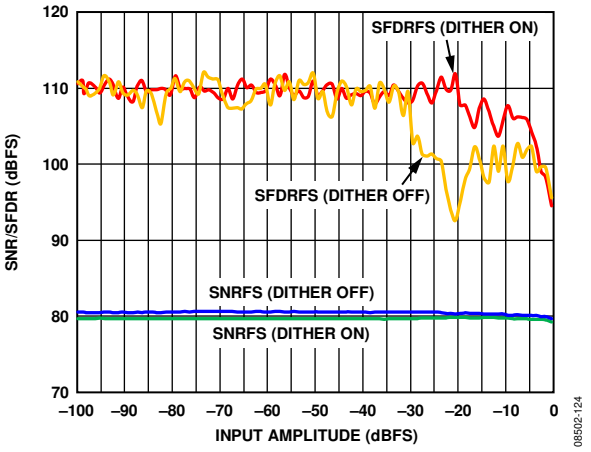

Figure 24. AD9265-105 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 30 MHz with and without Dither Enabled

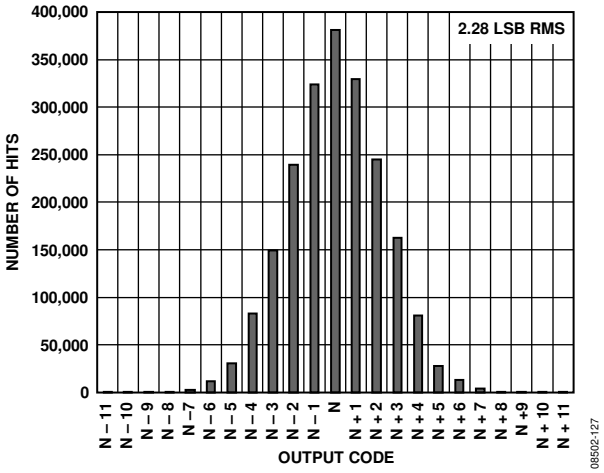

Figure 27. AD9265-105 Grounded Input Histogram

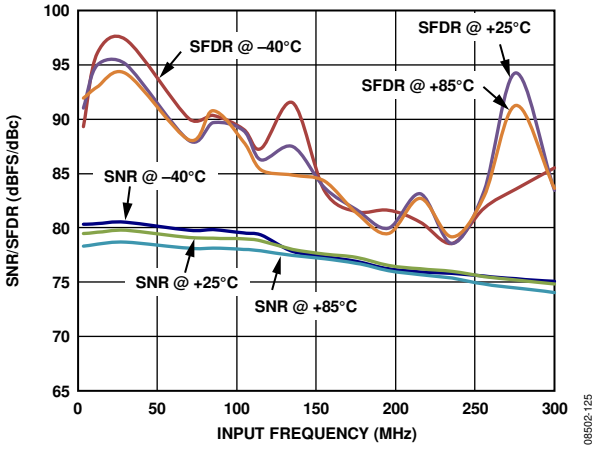

Figure 25. AD9265-105 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2 V p-p Full Scale

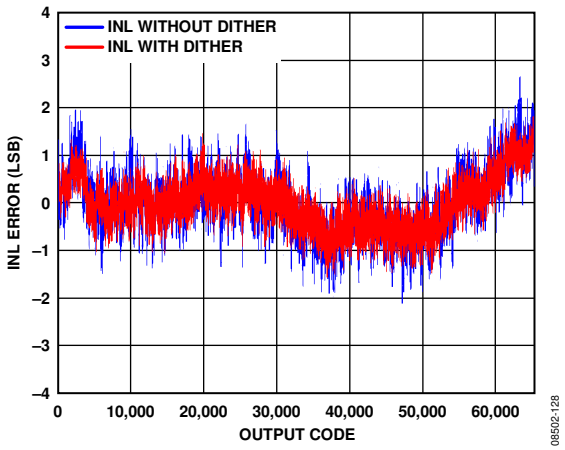

Figure 28. AD9265-105 INL with f_{IN} = 12.5 MHz

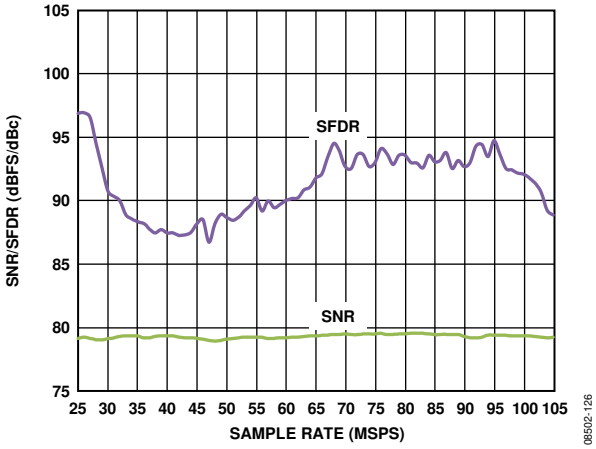

Figure 26. AD9265-105 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 70.1 MHz

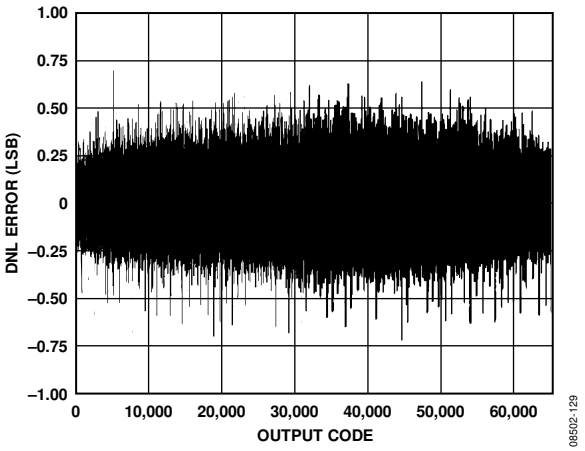

Figure 29. AD9265-105 DNL with f_{IN} = 12.5 MHz

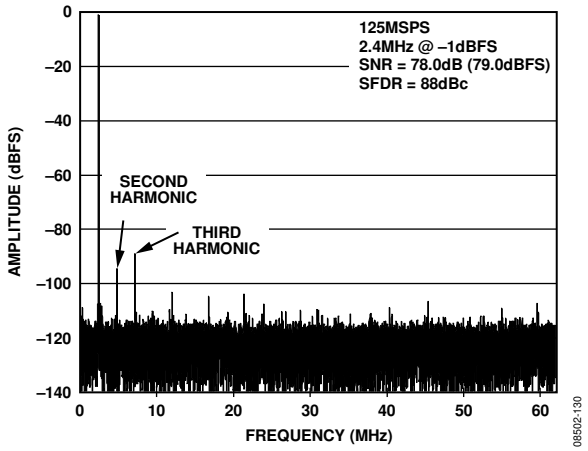

Figure 30. AD9265-125 Single-Tone FFT with f_{IN} = 2.4 MHz

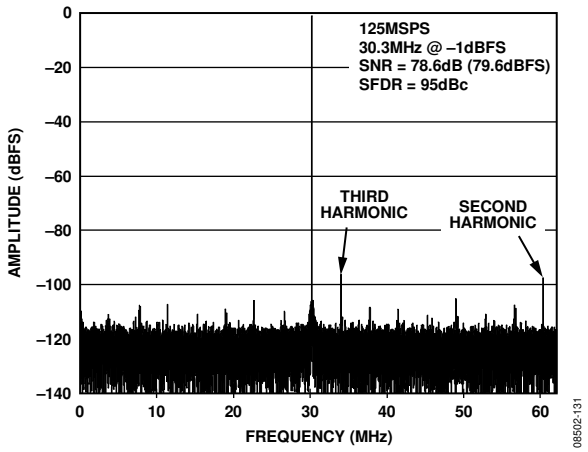

Figure 31. AD9265-125 Single-Tone FFT with f_{IN} = 30.3 MHz

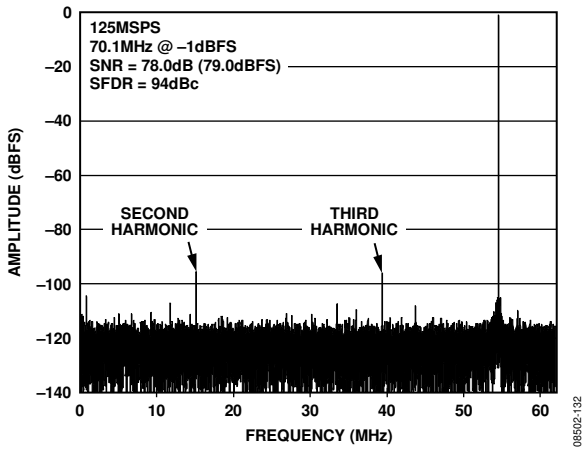

Figure 32. AD9265-125 Single-Tone FFT with f_{IN} = 70.1 MHz

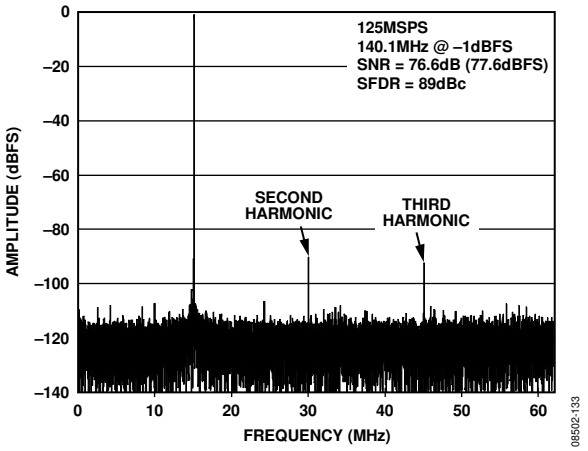

Figure 33. AD9265-125 Single-Tone FFT with f_{IN} = 140.1 MHz

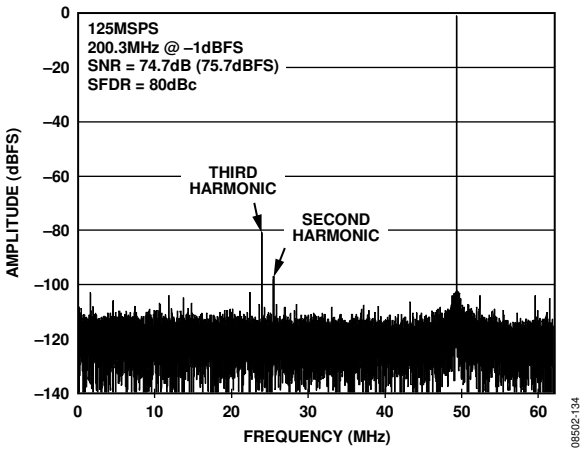

Figure 34. AD9265-125 Single-Tone FFT with f_{IN} = 200.3 MHz

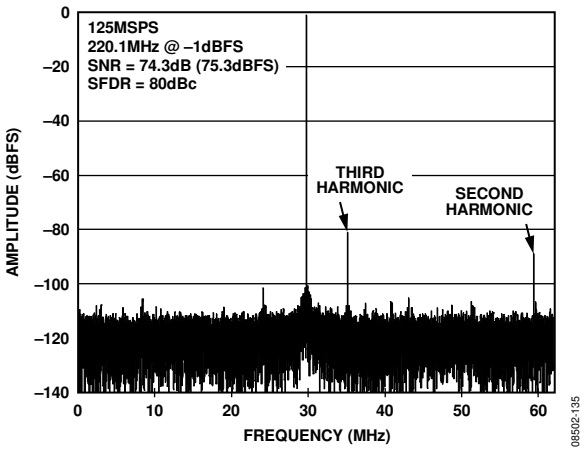

Figure 35. AD9265-125 Single-Tone FFT with f_{IN} = 220.1 MHz

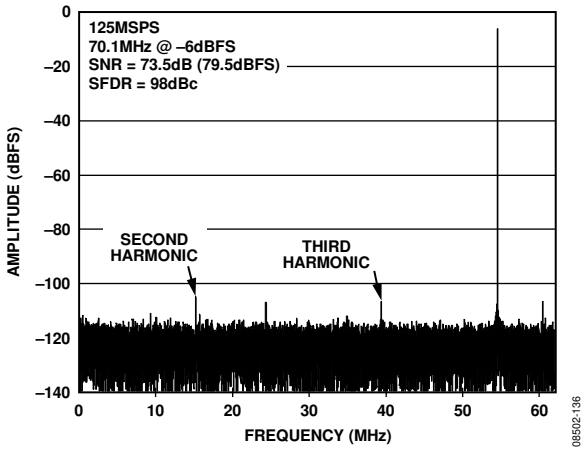

Figure 36. AD9265-125 Single-Tone FFT with f_{IN} = 70.1 MHz at –6 dBFS with Dither Enabled

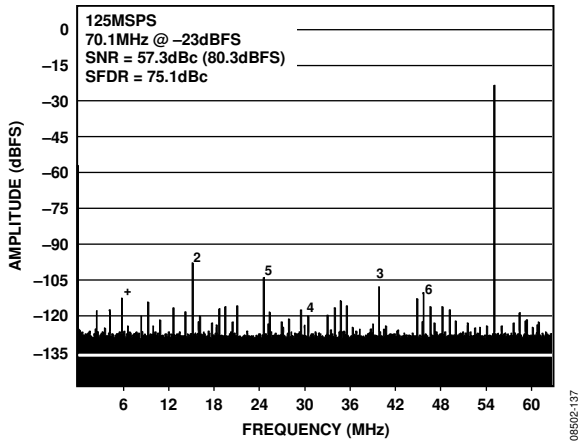

Figure 37. AD9265-125 Single-Tone FFT with f_{IN} = 70.1 MHz at –23 dBFS with Dither Disabled, 1M Sample

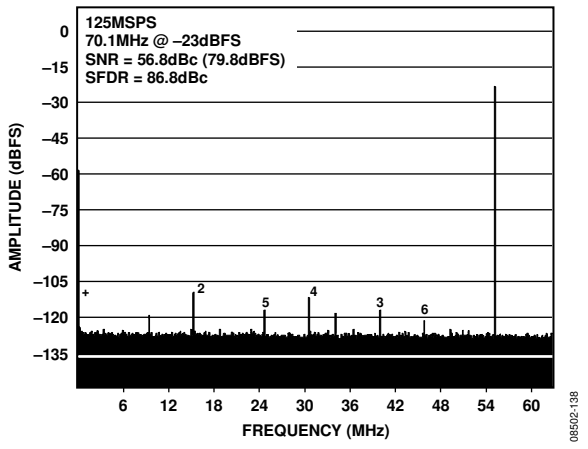

Figure 38. AD9265-125 Single-Tone FFT with f_{IN} = 70.1 MHz at –23 dBFS with Dither Enabled, 1M Sample

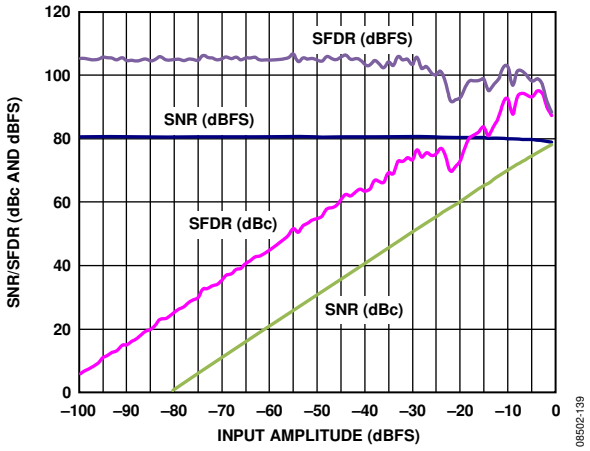

Figure 39. AD9265-125 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 2.4 MHz

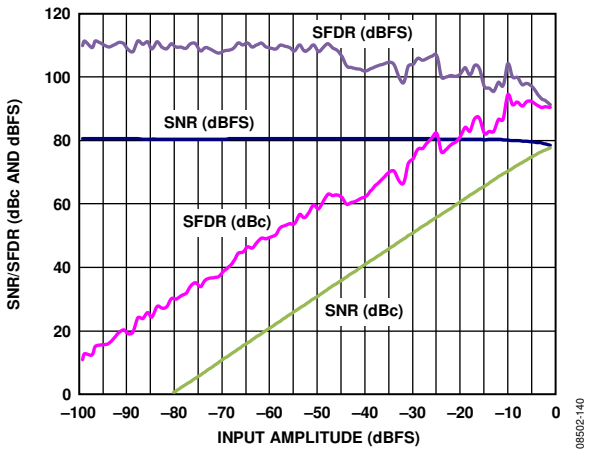

Figure 40. AD9265-125 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 98.12 MHz

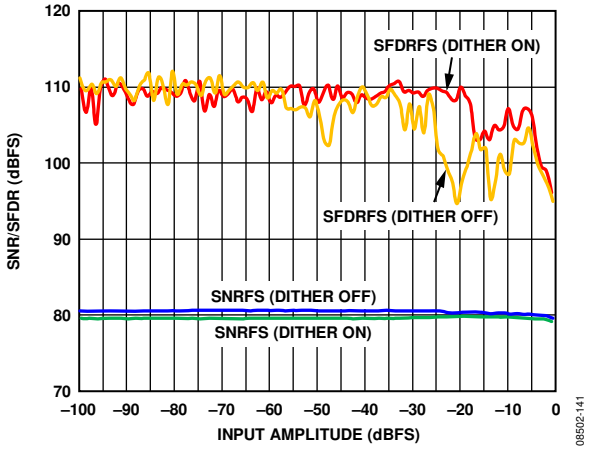

Figure 41. AD9265-125 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 30 MHz With and Without Dither Enabled

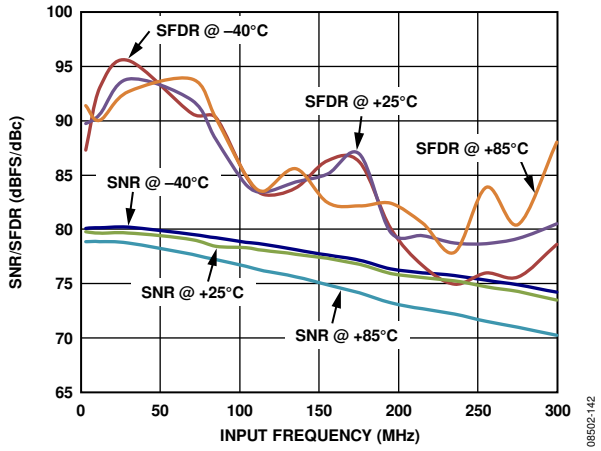

Figure 42. AD9265-125 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2 V p-p Full Scale

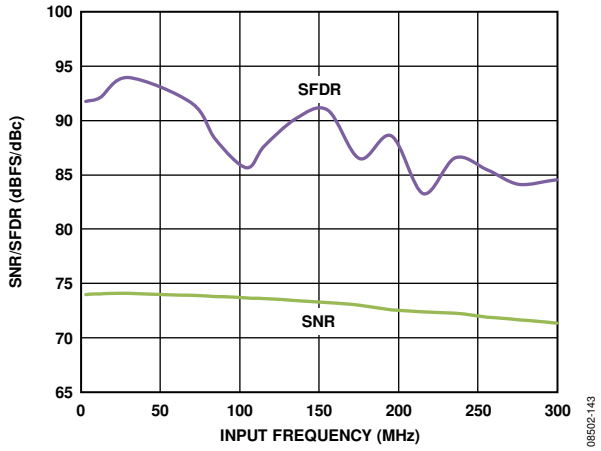

Figure 43. AD9265-125 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) with 1 V p-p Full Scale

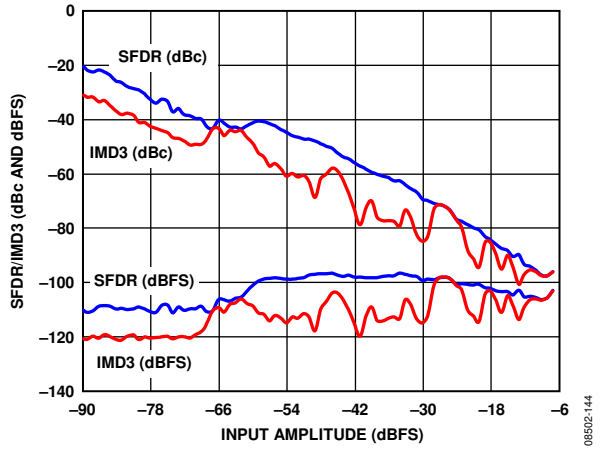

Figure 44. AD9265-125 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 29.1 MHz, f_{IN2} = 32.1 MHz, f_S = 125 MSPS

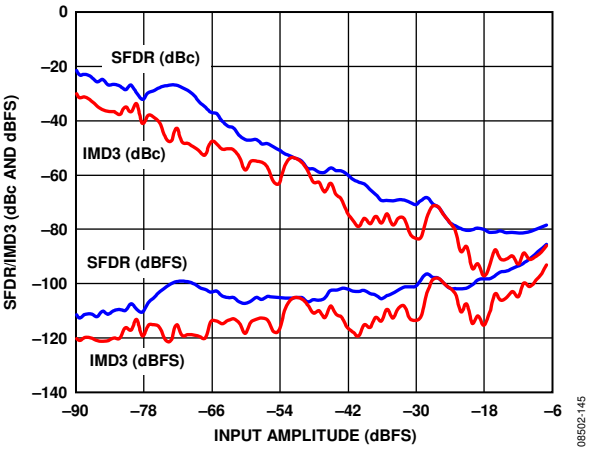

Figure 45. AD9265-125 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 169.1 MHz, f_{IN2} = 172.1 MHz, f_S = 125 MSPS

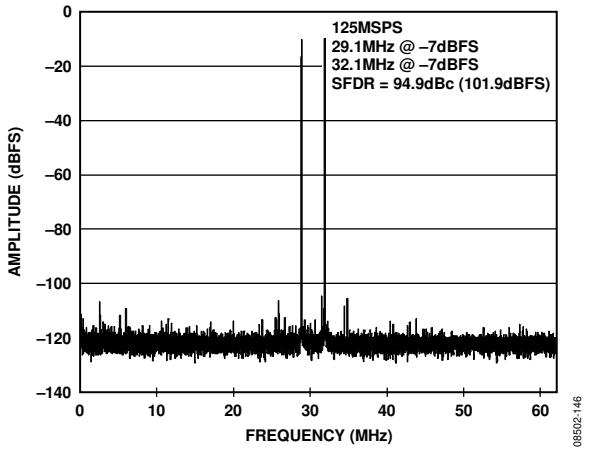

Figure 46. AD9265-125 Two-Tone FFT with f_{IN1} = 29.1 MHz and f_{IN2} = 32.1 MHz

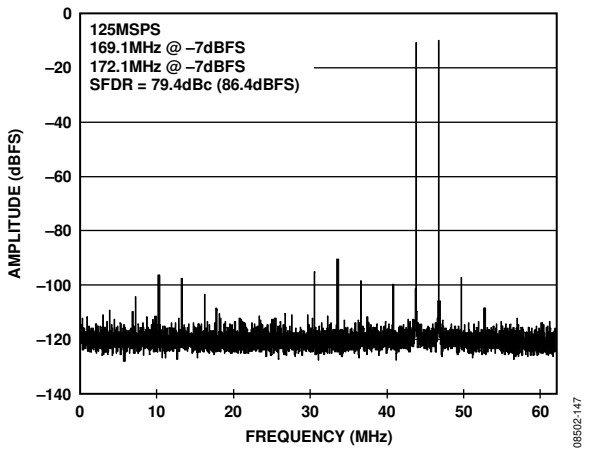

Figure 47. AD9265-125 Two-Tone FFT with f_{IN1} = 169.1 MHz and f_{IN2} = 172.1 MHz

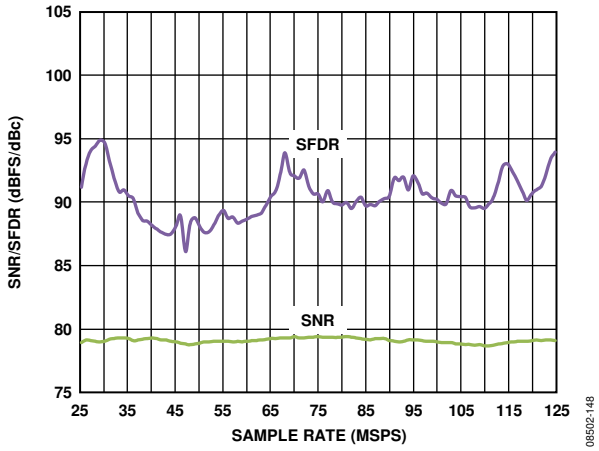

Figure 48. AD9265-125 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 70.1 MHz

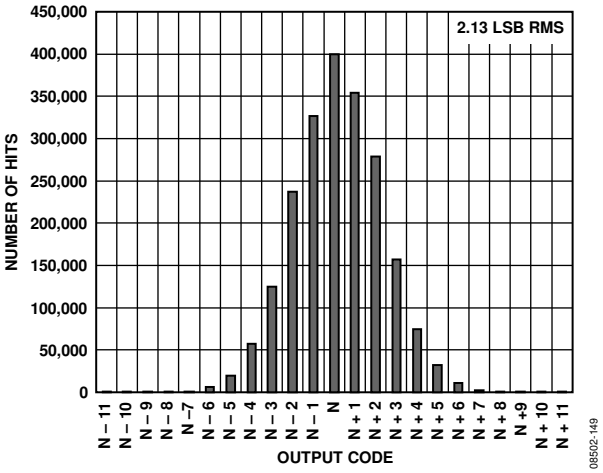

Figure 49. AD9265-125 Grounded Input Histogram

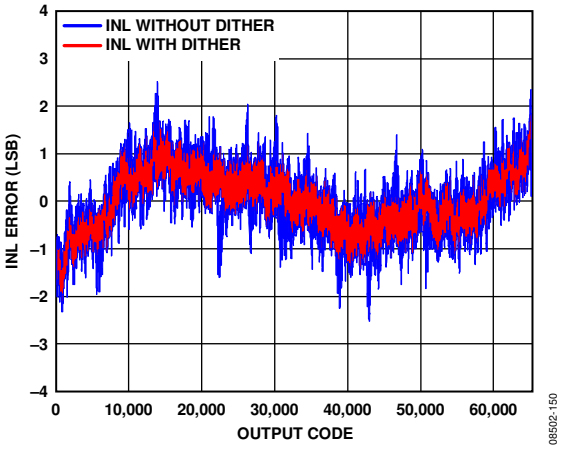

Figure 50. AD9265-125 INL with f_{IN} = 9.7 MHz

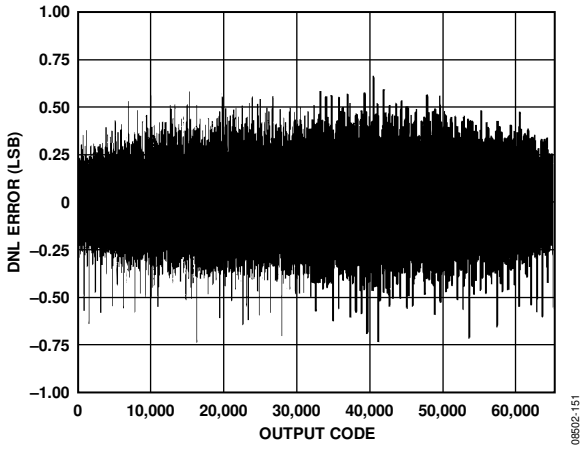

Figure 51. AD9265-125 DNL with f_{IN} = 9.7 MHz

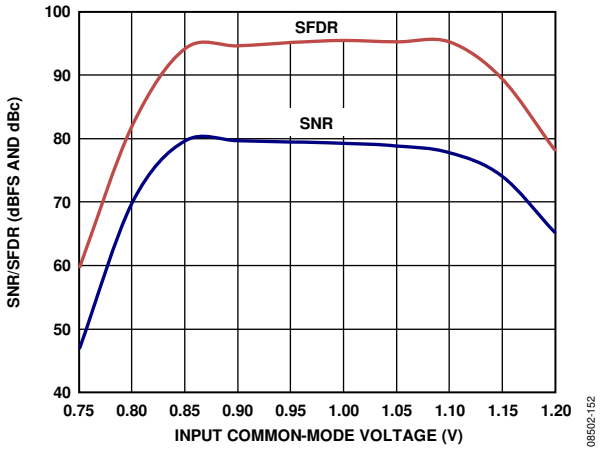

Figure 52. AD9265-125 SNR/SFDR vs. Input Common Mode (VCM) with f_{IN} = 30 MHz

EQUIVALENT CIRCUITS

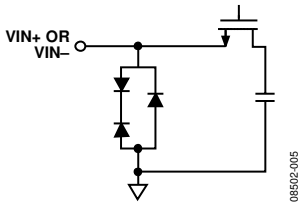

Figure 53. Equivalent Analog Input Circuit

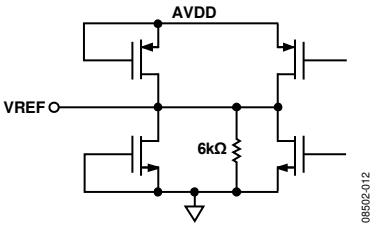

Figure 57. Equivalent VREF Circuit

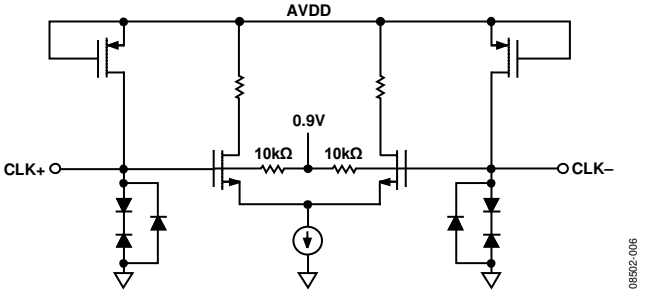

Figure 54. Equivalent Clock Input Circuit

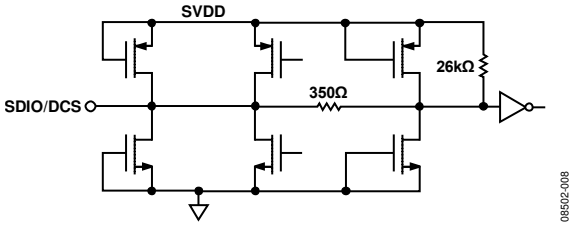

Figure 58. Equivalent SDIO/DCS Circuit

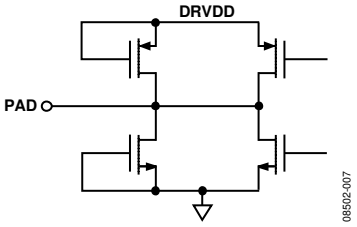

Figure 55. Digital Output

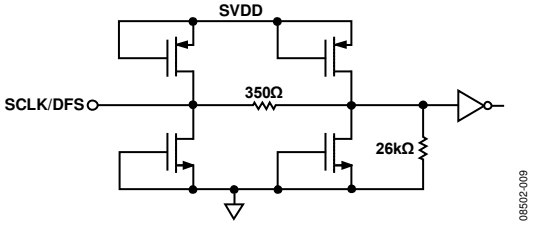

Figure 59. Equivalent SCLK/DFS Input Circuit

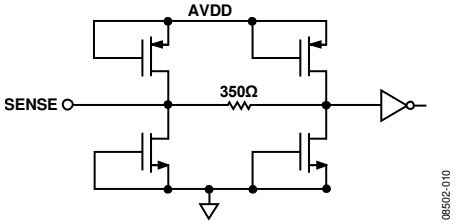

Figure 56. Equivalent SENSE Circuit

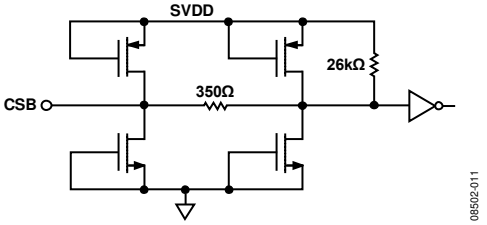

Figure 60. Equivalent CSB Input Circuit

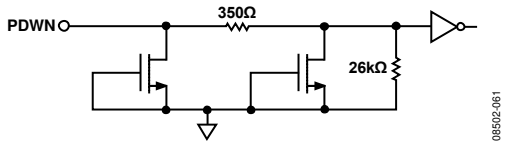

Figure 61. Equivalent PDWN Circuit

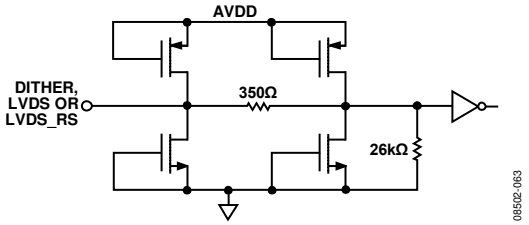

Figure 63. Equivalent DITHER, LVDS, and LVDS_RS Input Circuit

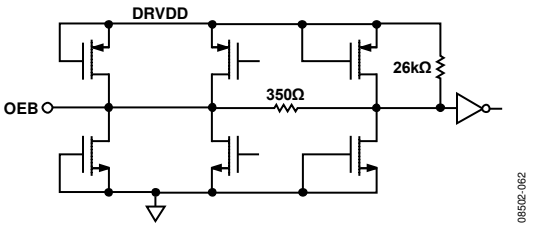

Figure 62. Equivalent OEB Input Circuit