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16-Bit, 20 MSPS/40 MSPS/65 MSPS/80 MSPS, 1.8 V Analog-to-Digital Converter

Data Sheet **AD9266**

FEATURES

1.8 V analog supply operation
1.8 V to 3.3 V output supply
SNR
- **77.6 dBFS at 9.7 MHz input**
- **71.1 dBFS at 200 MHz input**

SFDR
- **93 dBc at 9.7 MHz input**
- **80 dBc at 200 MHz input**

Low power
- **56 mW at 20 MSPS**
- **113 mW at 80 MSPS**

Differential input with 700 MHz bandwidth
On-chip voltage reference and sample-and-hold circuit
2 V p-p differential analog input
DNL = −0.6/+1.1 LSB
Interleaved data output for reduced pin-count interface
Serial port control options
- **Offset binary, Gray code, or twos complement data format**
- **Optional clock duty cycle stabilizer**
- **Integer 1-to-8 input clock divider**
- **Built-in selectable digital test pattern generation**
- **Energy-saving power-down modes**
- **Data clock output (DCO) with programmable clock and data alignment**

APPLICATIONS

Communications
Diversity radio systems
Multimode digital receivers
- **GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA**

Smart antenna systems
Battery-powered instruments
Handheld scope meters
Portable medical imaging
Ultrasound
Radar/LIDAR
PET/SPECT imaging

FUNCTIONAL BLOCK DIAGRAM

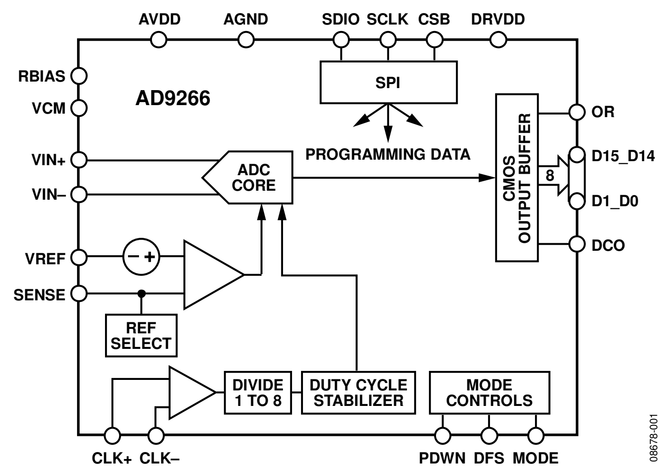

Figure 1.

PRODUCT HIGHLIGHTS

1. The AD9266 operates from a single 1.8 V analog power supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
2. The sample-and-hold circuit maintains excellent performance for input frequencies up to 200 MHz and is designed for low cost, low power, and ease of use.
3. A standard serial port interface supports various product features and functions, such as data output formatting, internal clock divider, power-down, DCO and data output (D15_D14 to D1_D0) timing and offset adjustments, and voltage reference modes.
4. The AD9266 is packaged in a 32-lead RoHS-compliant LFCSP that is pin compatible with the AD9609 10-bit ADC, the AD9629 12-bit ADC, and the AD9649 14-bit ADC, enabling a simple migration path between 10-bit and 16-bit converters sampling from 20 MSPS to 80 MSPS.

Rev. B **Document Feedback**

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AD9266* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9266 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-878: High Speed ADC SPI Control Software
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9266-DSCC: Military Data Sheet
- AD9266-EP: Enhanced Product Data Sheet
- AD9266: 16-Bit, 20/40/65/80 MSPS, 1.8 V Analog-to-Digital Converter Data Sheet

User Guides

- Evaluating the AD9266/AD9649/AD9629/AD9609 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD9266 IBIS Model
- AD9269LFCSP/AD9266LFCSP S Parameter

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Analog-to-Digital Converter and Drivers ICs Solutions Bulletin, Volume 10, Issue 2

Technical Articles

- Improve The Design Of Your Passive Wideband ADC Front-End Network
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9266 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9266 EngineerZone Discussions.

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4/10—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9266 is a monolithic, single-channel 1.8 V supply, 16-bit, 20 MSPS/40 MSPS/65 MSPS/80 MSPS analog-to-digital converter (ADC). It features a high performance sample-and-hold circuit and on-chip voltage reference.

The product uses multistage differential pipeline architecture with output error correction logic to provide 16-bit accuracy at 80 MSPS data rates and to guarantee no missing codes over the full operating temperature range.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

A differential clock input with a selectable internal 1-to-8 divide ratio controls all internal conversion cycles. An optional duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance.

The interleaved digital output data is presented in offset binary, gray code, or twos complement format. A DCO is provided to ensure proper latch timing with receiving logic. Both 1.8 V and 3.3 V CMOS levels are supported.

The AD9266 is available in a 32-lead RoHS-compliant LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

Table 1.

Parameter	Temp	AD9266-20/AD9266-40			AD9266-65			AD9266-80			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION	Full	16			16			16			Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full		+0.05	±0.30		+0.05	±0.30		+0.05	±0.30	% FSR
Gain Error[1]	Full		−2.5/−2.0			−1.0			+1.0		% FSR
Differential Nonlinearity (DNL)[2]	Full			−0.9/+1.2			−0.9/+1.7			−0.9/+1.7	LSB
	25°C		−0.5/+0.6			−0.5/+1.0			−0.6/+1.1		LSB
Integral Nonlinearity (INL)[2]	Full			±5.5			±6.5			±6.2	LSB
	25°C		±1.8			±2.4			±3.5		LSB
TEMPERATURE DRIFT											
Offset Error	Full		±2			±2			±2		ppm/°C
INTERNAL VOLTAGE REFERENCE											
Output Voltage (1 V Mode)	Full	0.983	0.995	1.007	0.983	0.995	1.007	0.983	0.995	1.007	V
Load Regulation Error at 1.0 mA	Full		2			2			2		mV
INPUT-REFERRED NOISE											
VREF = 1.0 V	25°C		2.8			2.8			2.8		LSB rms
ANALOG INPUT											
Input Span, VREF = 1.0 V	Full		2			2			2		V p-p
Input Capacitance[3]	Full		6.5			6.5			6.5		pF
Input Common-Mode Voltage	Full		0.9			0.9			0.9		V
Input Common-Mode Range	Full	0.5		1.3	0.5		1.3	0.5		1.3	V
REFERENCE INPUT RESISTANCE	Full		7.5			7.5			7.5		kΩ
POWER SUPPLIES											
Supply Voltage											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7		3.6	1.7		3.6	1.7		3.6	V
Supply Current											
IAVDD[2]	Full		31.4/40.7	33.2/42.5		54.5	57.6		62.5	65.7	mA
IDRVDD[2] (1.8 V)	Full		1.7/3.3			5.2			6.3		mA
IDRVDD[2] (3.3 V)	Full		3.0/5.9			9.3			11.6		mA
POWER CONSUMPTION											
DC Input	Full		57/73			98			113		mW
Sine Wave Input[2] (DRVDD = 1.8 V)	Full		60/79	63/82		107	113		124	130	mW
Sine Wave Input[2] (DRVDD = 3.3 V)	Full		66/93			129			151		mW
Standby Power[4]	Full		40			44			44		mW
Power-Down Power	Full		0.5			0.5			0.5		mW

[1] Measured with 1.0 V external reference.
[2] Measured with a 10 MHz input frequency at rated sample rate, full-scale sine wave, with approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between the differential inputs.
[4] Standby power is measured with a dc input and the CLK active.

AC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

Table 2.

Parameter[1]	Temp	AD9266-20/AD9266-40 Min	AD9266-20/AD9266-40 Typ	AD9266-20/AD9266-40 Max	AD9266-65 Min	AD9266-65 Typ	AD9266-65 Max	AD9266-80 Min	AD9266-80 Typ	AD9266-80 Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)											
f_{IN} = 9.7 MHz	25°C		78.2			77.9			77.6		dBFS
f_{IN} = 30.5 MHz	25°C		77.6			77.5			77.3		dBFS
	Full	76.7			76.6						dBFS
f_{IN} = 70 MHz	25°C		75.8/76.4			76.6			76.6		dBFS
	Full							75.5			dBFS
f_{IN} = 200 MHz	25°C								72.1		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)											
f_{IN} = 9.7 MHz	25°C		78.0			77.7			77.4		dBFS
f_{IN} = 30.5 MHz	25°C		77.5			77.3			77.1		dBFS
	Full	76.2			76.2						dBFS
f_{IN} = 70 MHz	25°C		75.7/76.3			76.5			76.6		dBFS
	Full							75.5			dBFS
f_{IN} = 200 MHz	25°C								69.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 9.7 MHz	25°C		12.7			12.6			12.6		Bits
f_{IN} = 30.5 MHz	25°C		12.6			12.5			12.5		Bits
f_{IN} = 70 MHz	25°C		12.3/12.4			12.4			12.4		Bits
f_{IN} = 200 MHz	25°C								11.2		Bits
WORST SECOND OR THIRD HARMONIC											
f_{IN} = 9.7 MHz	25°C		−97			−96			−95		dBc
f_{IN} = 30.5 MHz	25°C		−96/−93			−94			−93		dBc
	Full			−80			−80				dBc
f_{IN} = 70 MHz	25°C		−97/−95			−98			−95		dBc
	Full									−80	dBc
f_{IN} = 200 MHz	25°C								−80		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)											
f_{IN} = 9.7 MHz	25°C		95			95			94		dBc
f_{IN} = 30.5 MHz	25°C		93			92			92		dBc
	Full	80			80						dBc
f_{IN} = 70 MHz	25°C		93			95			93		dBc
	Full							80			dBc
f_{IN} = 200 MHz	25°C								80		dBc
WORST OTHER (HARMONIC OR SPUR)											
f_{IN} = 9.7 MHz	25°C		−102			−101			−99		dBc
f_{IN} = 30.5 MHz	25°C		−102			−101			−98		dBc
	Full			−89			−89				dBc
f_{IN} = 70 MHz	25°C		−101			−100			−98		dBc
	Full									−89	dBc
f_{IN} = 200 MHz	25°C								−86		dBc
TWO-TONE SFDR											
f_{IN} = 30.5 MHz (−7 dBFS), 32.5 MHz (−7 dBFS)	25°C		90			90			90		dBc
ANALOG INPUT BANDWIDTH	25°C		700			700			700		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

Table 3.

Parameter	Temp	AD9266-20/AD9266-40/AD9266-65/AD9266-80 Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.2		3.6	V p-p
Input Voltage Range	Full	GND − 0.3		AVDD + 0.2	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full	8	10	12	kΩ
Input Capacitance	Full		4		pF
LOGIC INPUTS (SCLK/DFS, MODE, SDIO/PDWN)[1]					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−50		−75	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		30		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (CSB)[2]					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		135	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
DIGITAL OUTPUTS					
DRVDD = 3.3 V					
High Level Output Voltage, I_{OH} = 50 µA	Full	3.29			V
High Level Output Voltage, I_{OH} = 0.5 mA	Full	3.25			V
Low Level Output Voltage, I_{OL} = 1.6 mA	Full			0.2	V
Low Level Output Voltage, I_{OL} = 50 µA	Full			0.05	V
DRVDD = 1.8 V					
High Level Output Voltage, I_{OH} = 50 µA	Full	1.79			V
High Level Output Voltage, I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage, I_{OL} = 1.6 mA	Full			0.2	V
Low Level Output Voltage, I_{OL} = 50 µA	Full			0.05	V

[1] Internal 30 kΩ pull-down.
[2] Internal 30 kΩ pull-up.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

Table 4.

		AD9266-20/AD9266-40			AD9266-65			AD9266-80			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS											
Input Clock Rate	Full			80/320			520			625	MHz
Conversion Rate[1]	Full	3		20/40	3		65	3		80	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	50/25			15.38			12.5			ns
CLK Pulse Width High (t_{CH})			25.0/12.5			7.69			6.25		ns
Aperture Delay (t_A)	Full		1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1			0.1		ps rms
DATA OUTPUT PARAMETERS											
Data Propagation Delay (t_{PD})	Full	1.84	3	3.90	1.84	3	3.90	1.84	3	3.90	ns
DCO Propagation Delay (t_{DCO})	Full	1.86	3	4.04	1.86	3	4.04	1.86	3	4.04	ns
DCO to Data Skew (t_{SKEW})	Full	−0.53	0.1	0.72	−0.53	0.1	0.72	−0.53	0.1	0.72	ns
Pipeline Delay (Latency)	Full		8			8			8		Cycles
Wake-Up Time[2]	Full		350			350			350		µs
Standby	Full		600/400			300			260		ns
OUT-OF-RANGE RECOVERY TIME	Full		2			2			2		Cycles

[1] Conversion rate is the clock rate after the CLK divider.
[2] Wake-up time is dependent on the value of the decoupling capacitors.

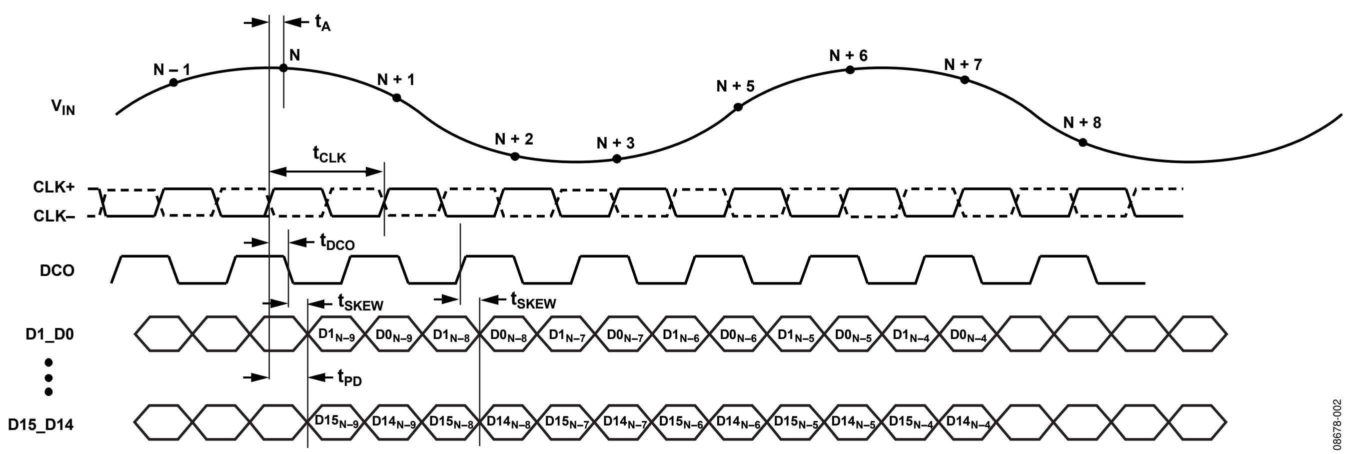


Figure 2. CMOS Output Data Timing

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_{S}	Setup time between CSB and SCLK	2			ns
t_{H}	Hold time between CSB and SCLK	2			ns
t_{HIGH}	SCLK pulse width high	10			ns
t_{LOW}	SCLK pulse width low	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +3.9 V
VIN+, VIN− to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.3 V
SCLK/DFS to AGND	−0.3 V to DRVDD + 0.3 V
SDIO/PDWN to AGND	−0.3 V to DRVDD + 0.3 V
MODE/OR to AGND	−0.3 V to DRVDD + 0.3 V
D1_D0 Through D15_D14 to AGND	−0.3 V to DRVDD + 0.3 V
DCO to AGND	−0.3 V to DRVDD + 0.3 V
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The exposed paddle is the only ground connection for the chip. The exposed paddle must be soldered to the AGND plane of the user's circuit board. Soldering the exposed paddle to the user's board also increases the reliability of the solder joints and maximizes the thermal capability of the package.

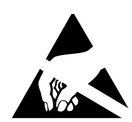
Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Ψ_{JT}[1,2]	Unit
32-Lead LFCSP, 5 mm × 5 mm	0	37.1	3.1	20.7	0.3	°C/W
	1.0	32.4			0.5	°C/W
	2.5	29.1			0.8	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown in Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

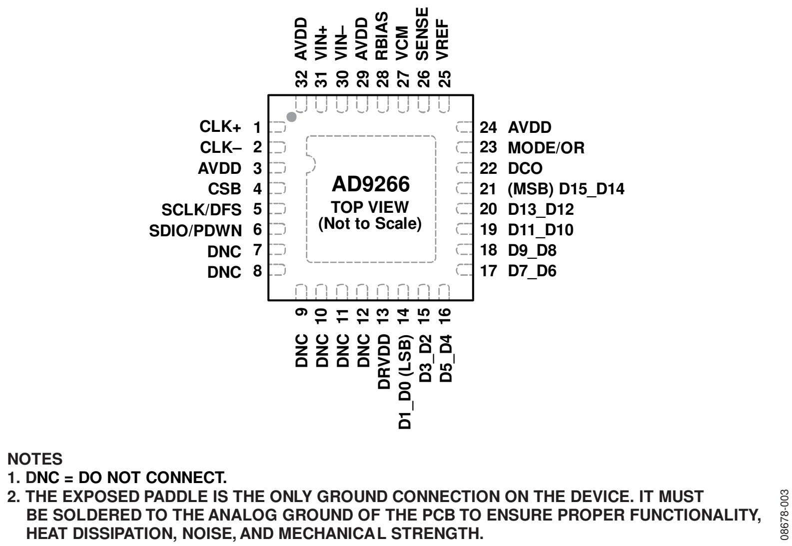


Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	EPAD	Exposed Paddle. The exposed paddle is the only ground connection on the device. It must be soldered to the analog ground of the PCB to ensure proper functionality, heat dissipation, noise, and mechanical strength.
1, 2	CLK+, CLK−	Differential Encode Clock for PECL, LVDS, or 1.8 V CMOS Inputs.
3, 24, 29, 32	AVDD	1.8 V Supply Pin for ADC Core Domain.
4	CSB	SPI Chip Select. Active low enable, 30 kΩ internal pull-up.
5	SCLK/DFS	SPI Clock Input in SPI Mode (SCLK). 30 kΩ internal pull-down. Data Format Select in Non-SPI Mode (DFS). Static control of data output format. 30 kΩ internal pull-down. DFS high = twos complement output; DFS low = offset binary output.
6	SDIO/PDWN	SPI Data Input/Output (SDIO). Bidirectional SPI data I/O with 30 kΩ internal pull-down. Non-SPI Mode Power-Down (PDWN). Static control of chip power-down with 30 kΩ internal pull-down. See Table 14 for details.
7 to 12	DNC	Do Not Connect.
14 to 21	D1_D0 (LSB) to (MSB) D15_D14	ADC Digital Outputs.
13	DRVDD	1.8 V to 3.3 V Supply Pin for Output Driver Domain.
22	DCO	Data Clock Digital Output.
23	MODE/OR	Chip Mode Select Input (MODE)/Out-of-Range Digital Output in SPI Mode (OR). Default = out-of-range (OR) digital output (SPI Register 0x2A, Bit 0 = 1). Option = chip mode select input (SPI Register 0x2A, Bit 0 = 0). Chip power-down (SPI Register 0x08, Bits[7:5] = 100b). Chip standby (SPI Register 0x08, Bits[7:5] = 101b). Normal operation, output disabled (SPI Register 0x08, Bits[7:5] = 110b). Normal operation, output enabled (SPI Register 0x08, Bits[7:5] = 111b). Out-of-range (OR) digital output only in non-SPI mode.
25	VREF	1.0 V Voltage Reference Input/Output. See Table 10.
26	SENSE	Reference Mode Selection. See Table 10.
27	VCM	Analog Output Voltage at Mid AVDD Supply. Sets common mode of the analog inputs.
28	RBIAS	Set Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
30, 31	VIN−, VIN+	ADC Analog Inputs.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9266-80

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

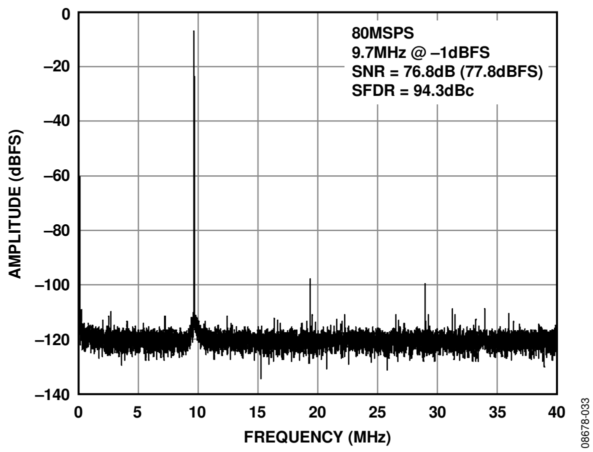


Figure 4. AD9266-80 Single-Tone FFT with f_{IN} = 9.7 MHz

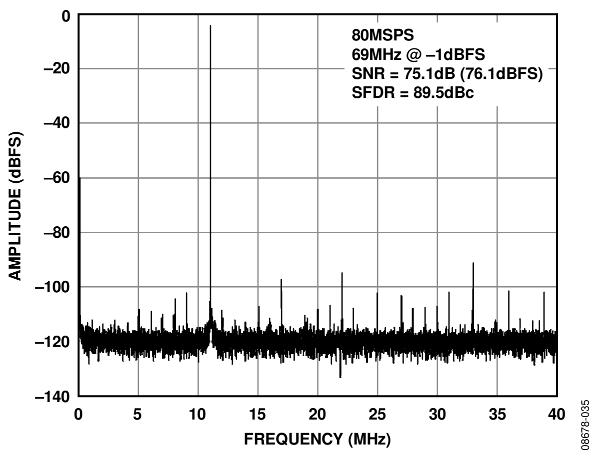


Figure 5. AD9266-80 Single-Tone FFT with f_{IN} = 69 MHz

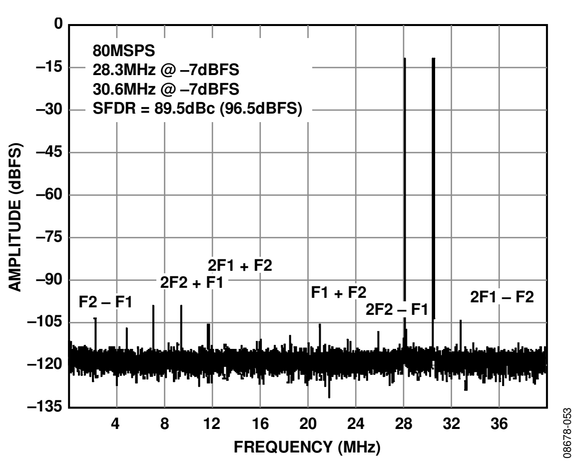


Figure 6. AD9266-80 Two-Tone FFT with f_{IN1} = 28.3 MHz and f_{IN2} = 30.6 MHz

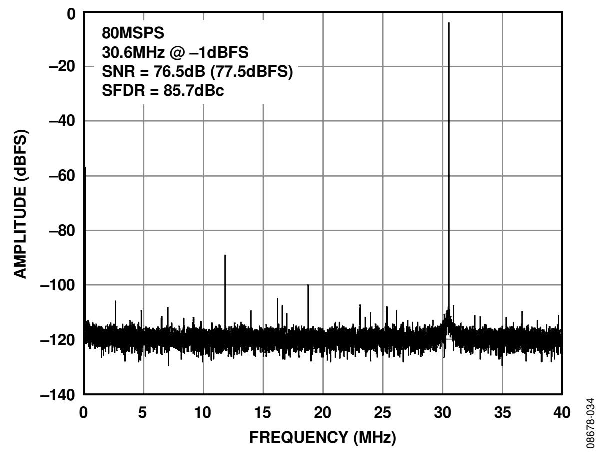


Figure 7. AD9266-80 Single-Tone FFT with f_{IN} = 30.6 MHz

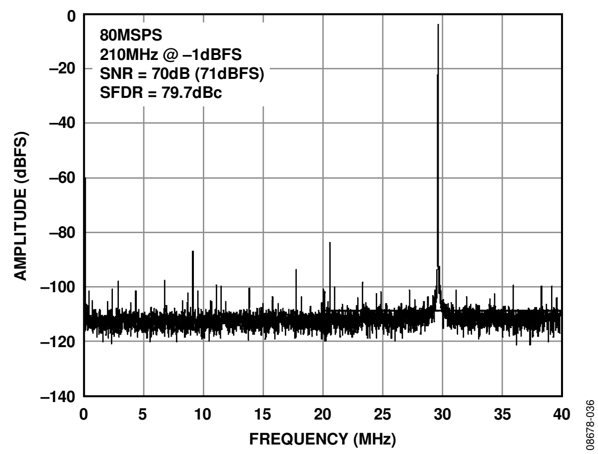


Figure 8. AD9266-80 Single-Tone FFT with f_{IN} = 210 MHz

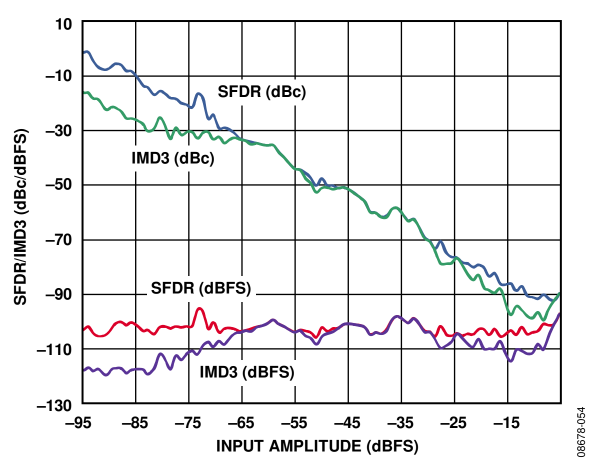


Figure 9. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with f_{IN1} = 28.3 MHz and f_{IN2} = 30.6 MHz

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

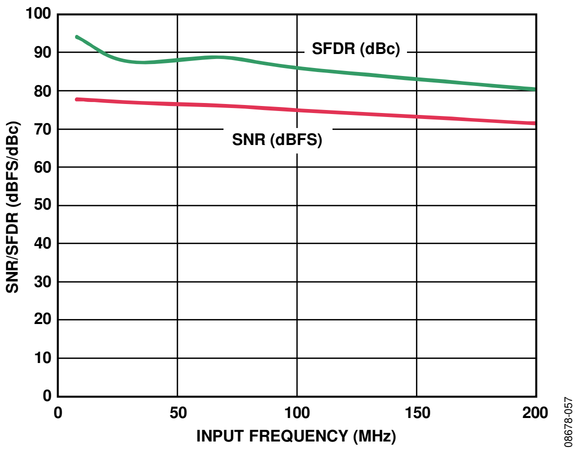


Figure 10. AD9266-80 SNR/SFDR vs. Input Frequency (AIN) with 2 V p-p Full Scale

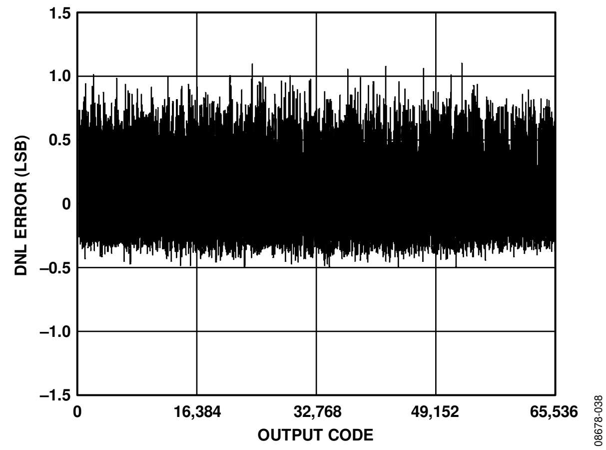


Figure 13. DNL Error with f_{IN} = 9.7 MHz

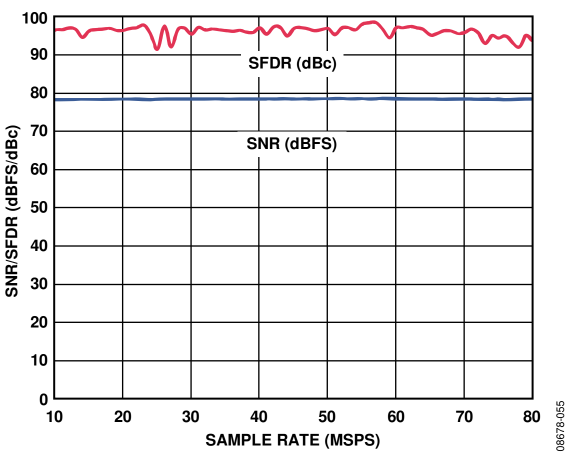


Figure 11. AD9266-80 SNR/SFDR vs. Sample Rate with AIN = 9.7 MHz

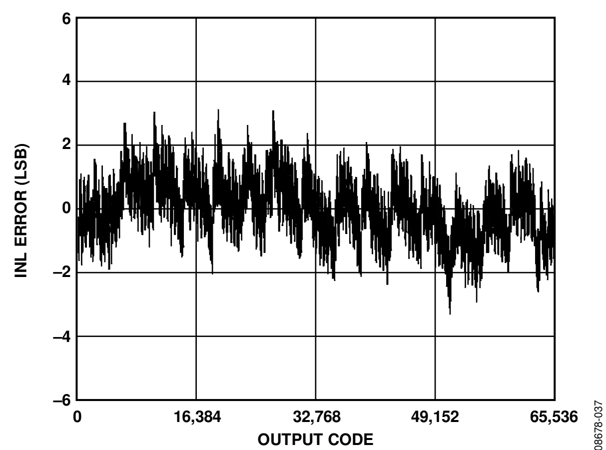


Figure 14. INL with f_{IN} = 9.7 MHz

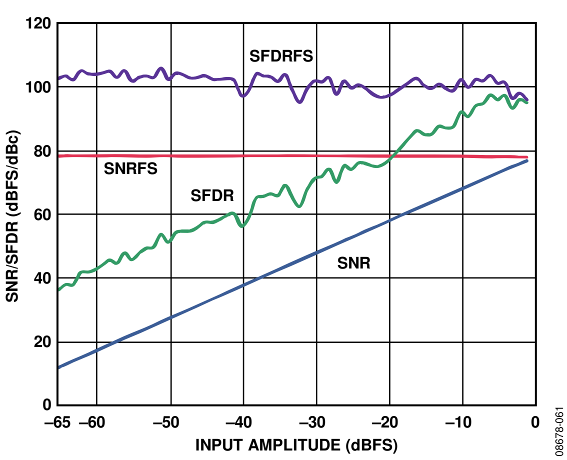


Figure 12. AD9266-80 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

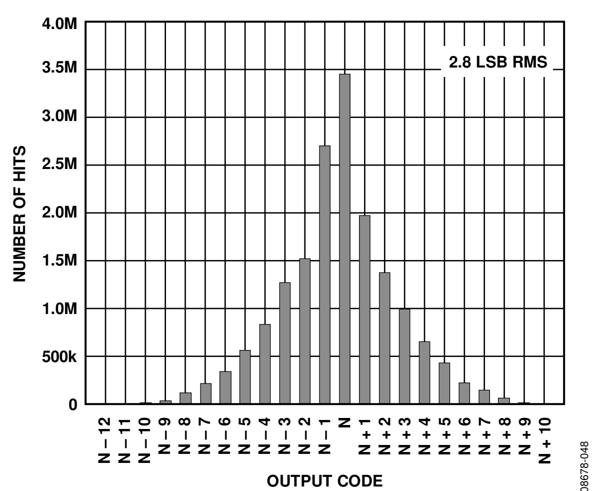


Figure 15. Grounded Input Histogram

AD9266-65

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

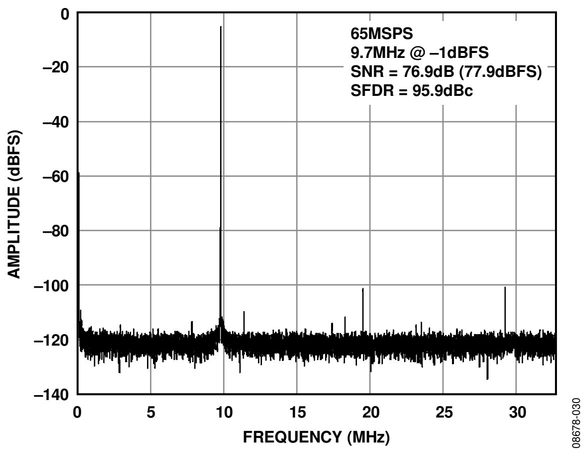


Figure 16. AD9266-65 Single-Tone FFT with f_{IN} = 9.7 MHz

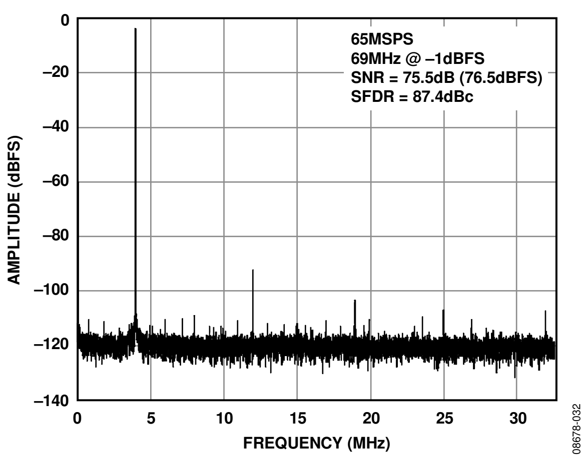


Figure 17. AD9266-65 Single-Tone FFT with f_{IN} = 69 MHz

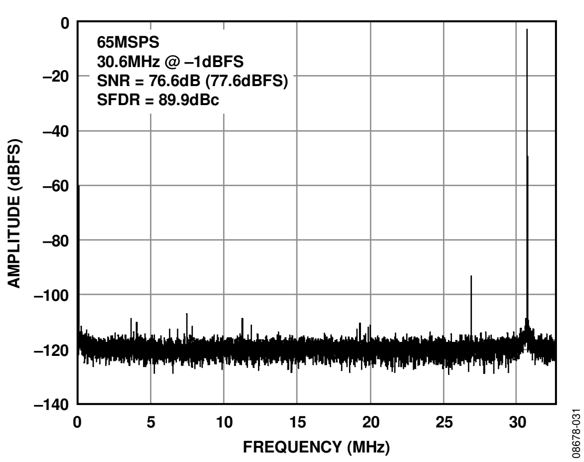


Figure 18. AD9266-65 Single-Tone FFT with f_{IN} = 30.6 MHz

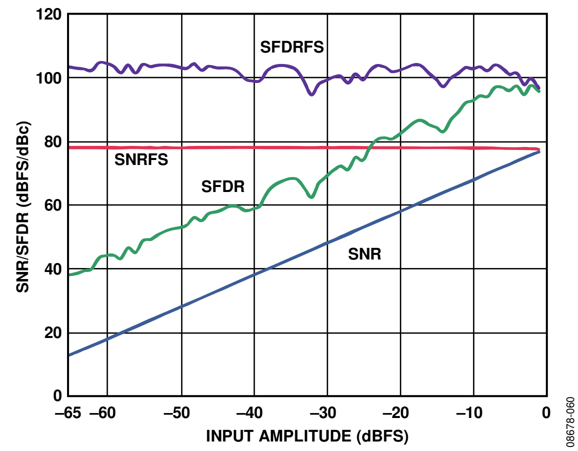


Figure 19. AD9266-65 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

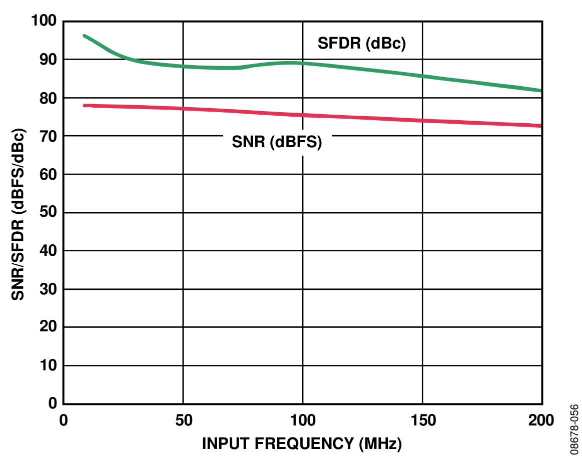


Figure 20. AD9266-65 SNR/SFDR vs. Input Frequency (AIN) with 2 V p-p Full Scale

AD9266-40

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

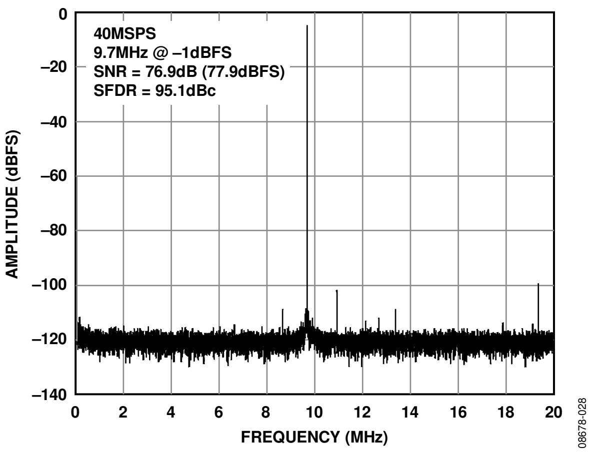


Figure 21. AD9266-40 Single-Tone FFT with f_{IN} = 9.7 MHz

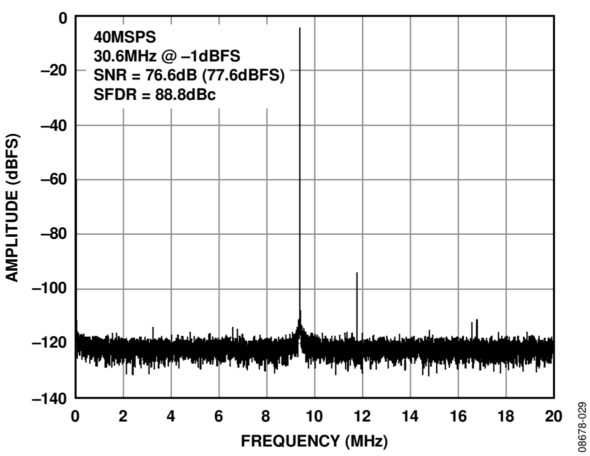


Figure 22. AD9266-40 Single-Tone FFT with f_{IN} = 30.6 MHz

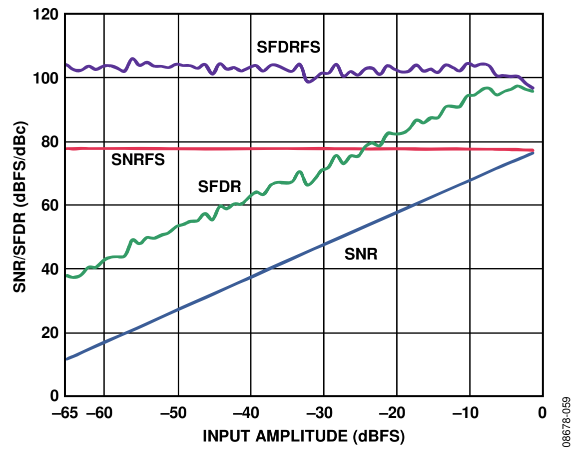


Figure 23. AD9266-40 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

AD9266-20

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

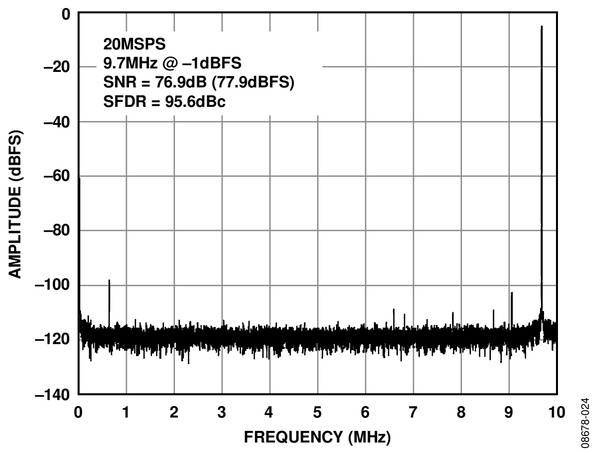


Figure 24. AD9266-20 Single-Tone FFT with f_{IN} = 9.7 MHz

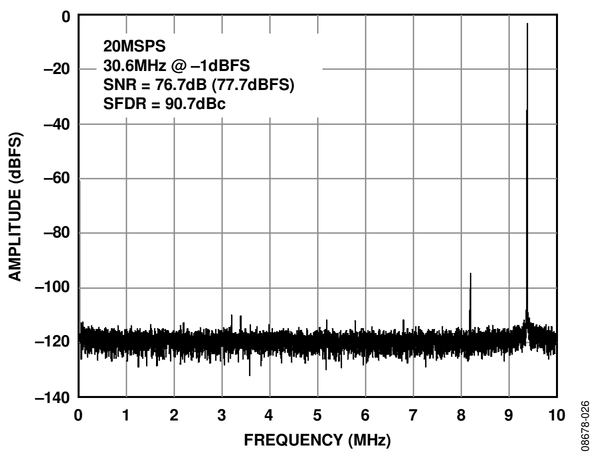


Figure 25. AD9266-20 Single-Tone FFT with f_{IN} = 30.6 MHz

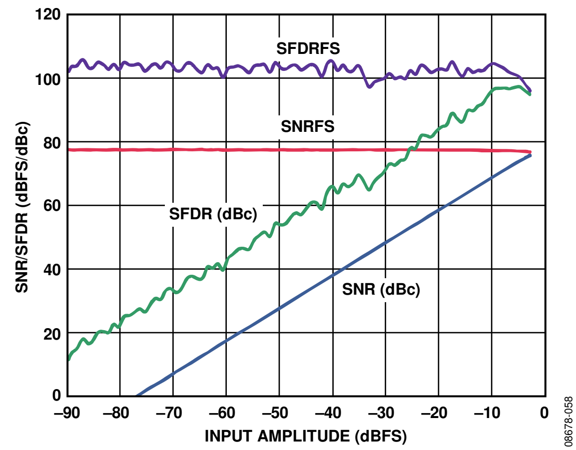


Figure 26. AD9266-20 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

EQUIVALENT CIRCUITS

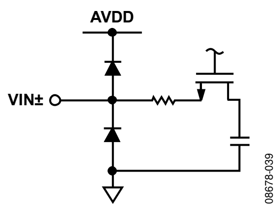


Figure 27. Equivalent Analog Input Circuit

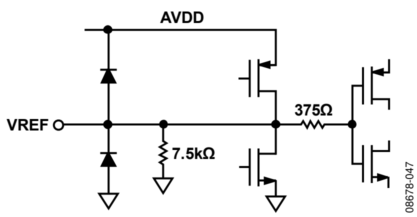


Figure 28. Equivalent VREF Circuit

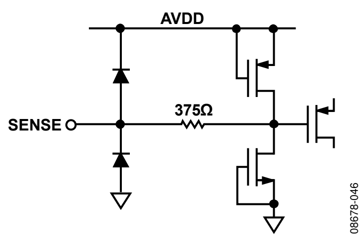


Figure 29. Equivalent SENSE Circuit

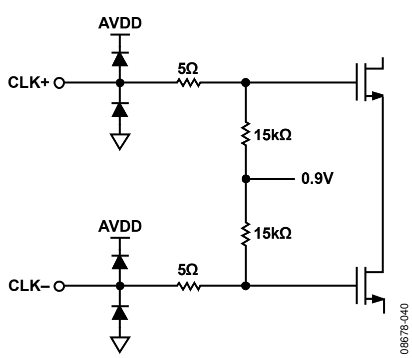


Figure 30. Equivalent Clock Input Circuit

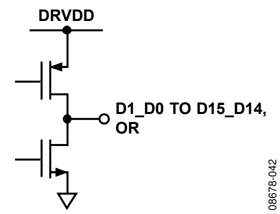


Figure 31. Equivalent D1_D0 to D15_D14 and OR Digital Output Circuit

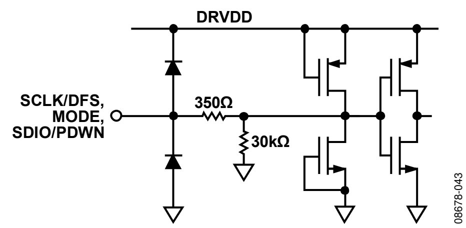


Figure 32. Equivalent SCLK/DFS, MODE, and SDIO/PDWN Input Circuit

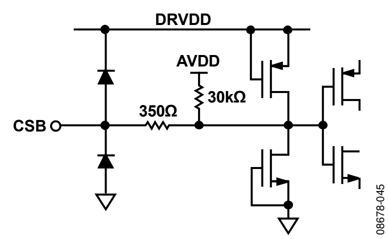


Figure 33. Equivalent CSB Input Circuit

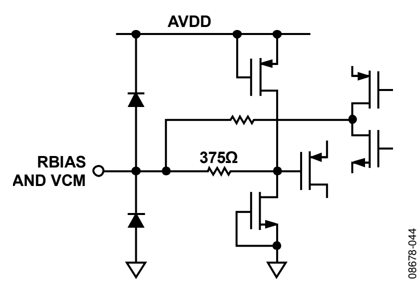


Figure 34. Equivalent RBIAS and VCM Circuit

THEORY OF OPERATION

The AD9266 architecture consists of a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 16-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample, whereas the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the CMOS output buffers. The output buffers are powered from a separate (DRVDD) supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9266 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

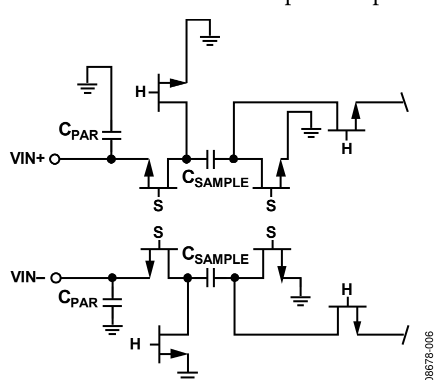


Figure 35. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample-and-hold mode (see Figure 35). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

Input Common Mode

The analog inputs of the AD9266 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide a dc bias externally. Setting the device so that VCM = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 36.

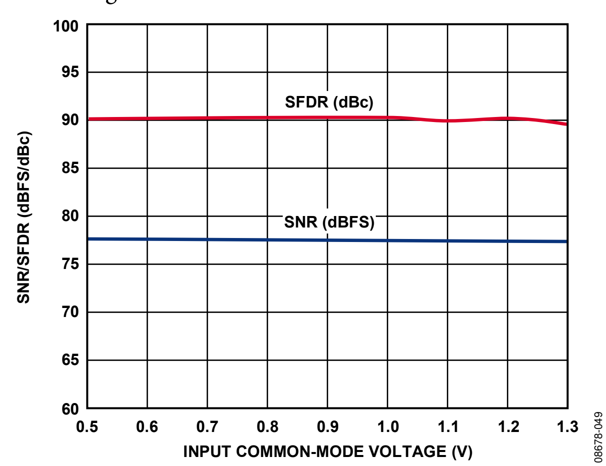


Figure 36. SNR/SFDR vs. Input Common-Mode Voltage, f_{IN} = 32.5 MHz, f_S = 80 MSPS

An on-board, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section.

Differential Input Configurations

Optimum performance is achieved while driving the AD9266 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4938-2 is easily set with the VCM pin of the AD9266 (see Figure 37), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

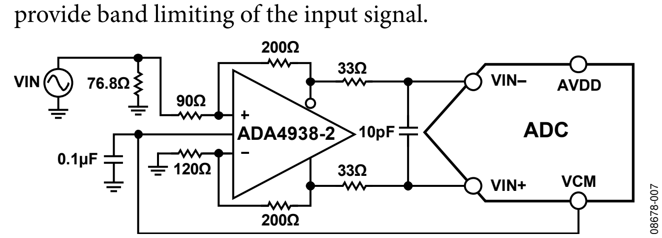


Figure 37. Differential Input Configuration Using the ADA4938-2

For baseband applications less than approximately 10 MHz where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 38. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

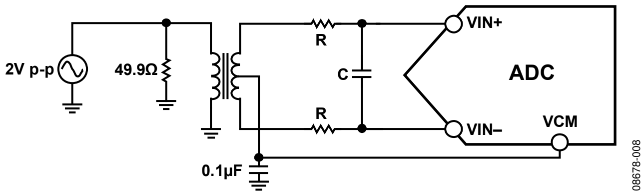


Figure 38. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9266. For applications greater than approximately 10 MHz where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 40).

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use the AD8352 differential driver. An example is shown in Figure 41. See the AD8352 data sheet for more information.

In any configuration, the value of Shunt Capacitor C is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 9 displays the suggested values to set the RC network. However, these values are dependent on the input signal and should be used only as a starting guide.

Table 9. Example RC Network

Frequency Range (MHz)	R Series (Ω Each)	C Differential (pF)
0 to 70	33	22
70 to 200	125	Open

Single-Ended Input Configuration

A single-ended input can provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the source impedances on each input are matched, there should be little effect on SNR performance. Figure 39 shows a typical single-ended input configuration.

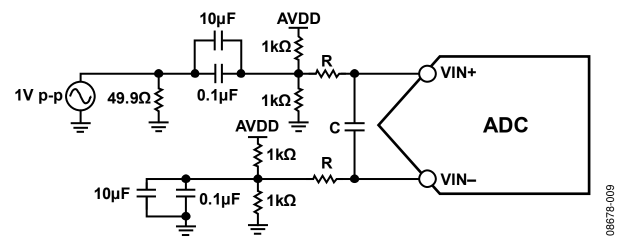


Figure 39. Single-Ended Input Configuration

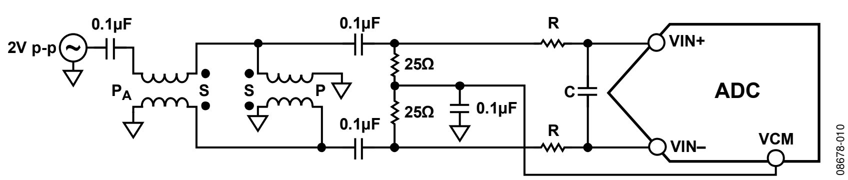


Figure 40. Differential Double Balun Input Configuration

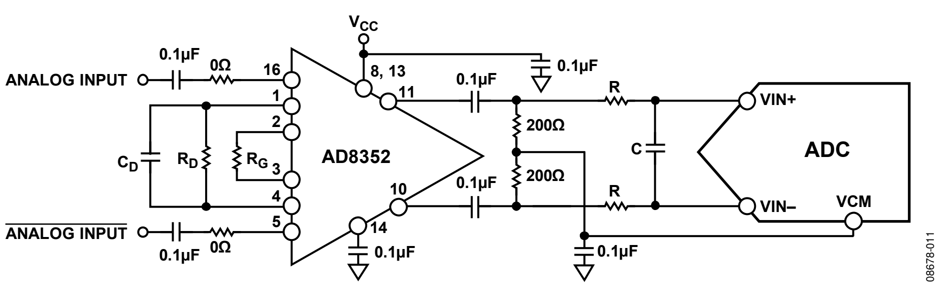


Figure 41. Differential Input Configuration Using the AD8352

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9266. The VREF can be configured using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the sections that follow. The Reference Decoupling section describes the best practices for PCB layout of VREF.

Internal Reference Connection

A comparator within the AD9266 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 10. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 42), setting VREF to 1.0 V.

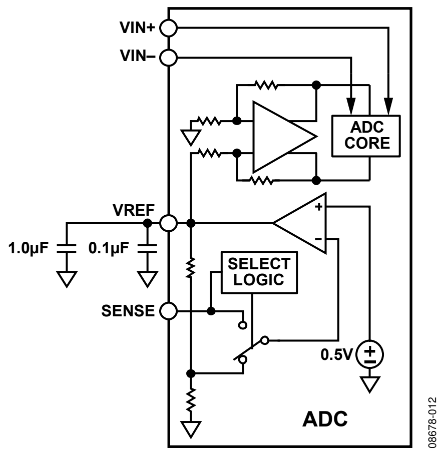


Figure 42. Internal Reference Configuration

If the internal reference of the AD9266 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 43 shows how the internal reference voltage is affected by loading.

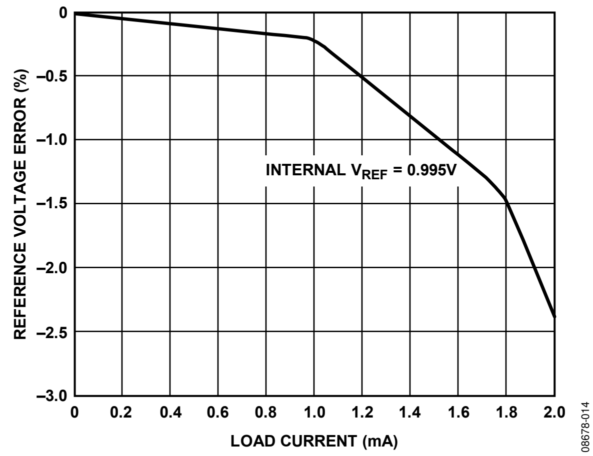


Figure 43. V_{REF} Accuracy vs. Load Current

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 44 shows the typical drift characteristics of the internal reference in 1.0 V mode.

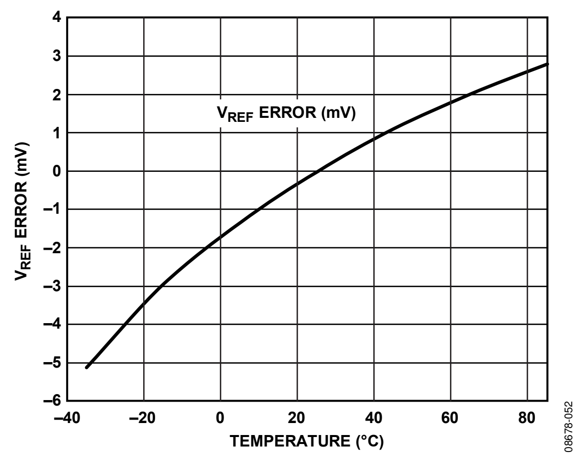


Figure 44. Typical V_{REF} Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load (see Figure 28). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.0 V.

Table 10. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting VREF (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	AGND to 0.2	1.0 internal	2.0
Fixed External Reference	AVDD	1.0 applied to external VREF pin	2.0

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9266 sample clock inputs, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally (see Figure 45) and require no external bias.

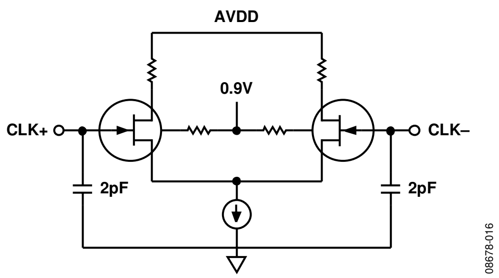


Figure 45. Equivalent Clock Input Circuit

Clock Input Options

The AD9266 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of great concern, as described in the Jitter Considerations section.

Figure 46 and Figure 47 show two preferred methods for clocking the AD9266 (at clock rates up to 625 MHz when using the internal clock divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

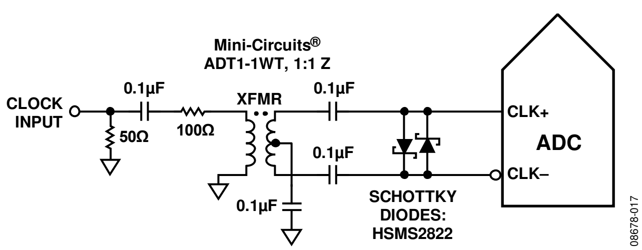


Figure 46. Transformer-Coupled Differential Clock (Up to 200 MHz)

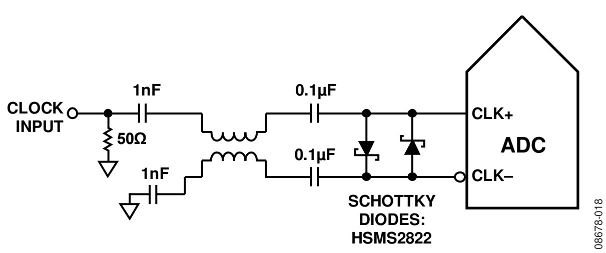


Figure 47. Balun-Coupled Differential Clock (Up to 625 MHz)

The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz.

The back-to-back Schottky diodes across the transformer/balun secondary limit clock excursions into the AD9266 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9266 while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 48. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 clock drivers offer excellent jitter performance.

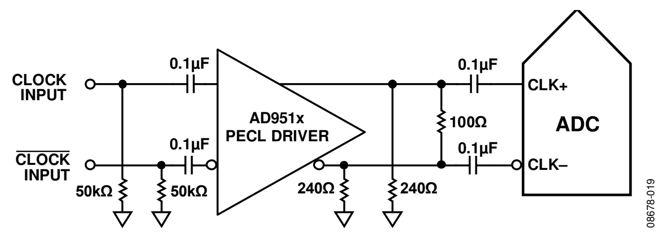


Figure 48. Differential PECL Sample Clock (Up to 625 MHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 49. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 clock drivers offer excellent jitter performance.

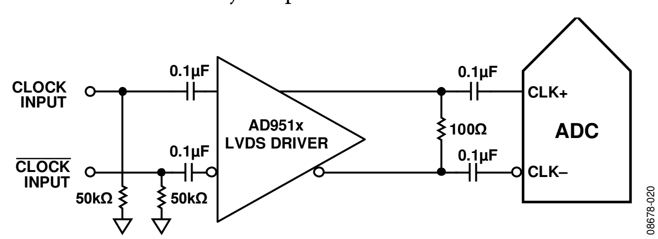


Figure 49. Differential LVDS Sample Clock (Up to 625 MHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK− pin to ground with a 0.1 µF capacitor (see Figure 50).

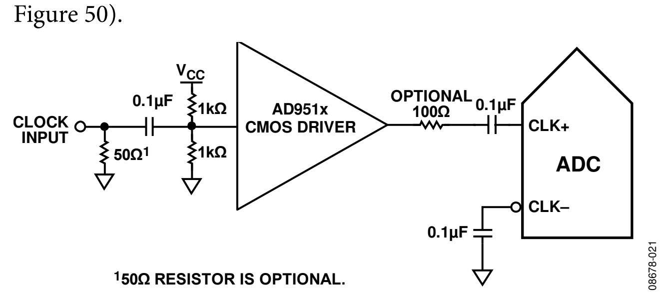


Figure 50. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9266 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. Optimum performance can be obtained by enabling the internal duty cycle stabilizer (DCS) when using divide ratios other than 1, 2, or 4.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9266 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9266. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS on, as shown in Figure 51.

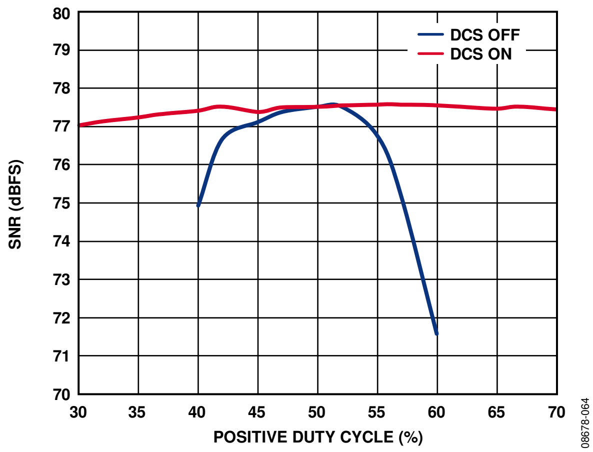


Figure 51. SNR vs. DCS On/Off

Jitter in the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 20 MHz nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR from the low frequency SNR (SNR_{LF}) at a given input frequency (f_{INPUT}) due to jitter (t_{JRMS}) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{INPUT} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the previous equation, the rms aperture jitter represents the clock input jitter specification. IF undersampling applications are particularly sensitive to jitter, as illustrated in Figure 52.

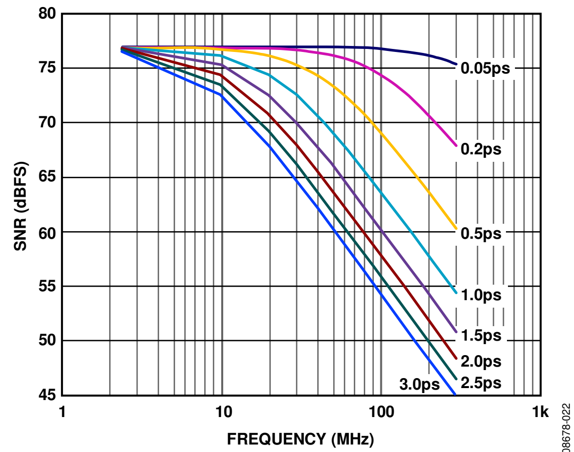


Figure 52. SNR vs. Input Frequency and Jitter

Treat the clock input as an analog signal when aperture jitter may affect the dynamic range of the AD9266. To avoid modulating the clock signal with digital noise, keep power supplies for clock drivers separate from the ADC output driver supplies. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step.

For more information, see the AN-501 Application Note and the AN-756 Application Note.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 53, the analog core power dissipated by the AD9266 is proportional to its sample rate. The digital power dissipation of the CMOS outputs are determined primarily by the strength of the digital drivers and the load on each output bit.

The maximum DRVDD current (IDRVDD) can be calculated as

$$IDRVDD = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where N is the number of output bits (nine, in the case of the AD9266).

This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency of $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the sample rate and the characteristics of the analog input signal.

Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 53 was taken using the same operating conditions as those used for the Typical Performance Characteristics, with a 5 pF load on each output driver.

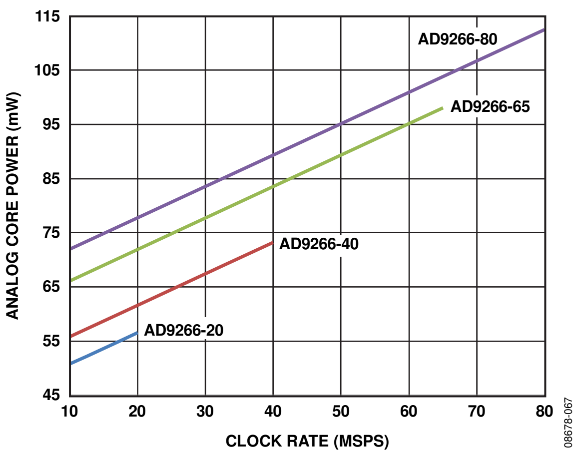


Figure 53. Analog Core Power vs. Clock Rate

In SPI mode, the AD9266 can be placed in power-down mode directly via the SPI port, or by using the programmable external MODE pin. In non-SPI mode, power-down is achieved by asserting the PDWN pin high. In this state, the ADC typically dissipates 500 µW. During power-down, the output drivers are placed in a high impedance state. Asserting PDWN low (or the MODE pin in SPI mode) returns the AD9266 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more details.

DIGITAL OUTPUTS

The AD9266 output drivers can be configured to interface with 1.8 V to 3.3 V CMOS logic families. Output data can also be multiplexed onto a single output bus to reduce the total number of traces required.

The CMOS output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies and may affect converter performance.

Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

The output data format can be selected to be either offset binary or twos complement by setting the SCLK/DFS pin when operating in the external pin mode (see Table 11).

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

Table 11. SCLK/DFS and SDIO/PDWN Mode Selection (External Pin Mode)

Voltage at Pin	SCLK/DFS	SDIO/PDWN
AGND	Offset binary (default)	Normal operation (default)
DRVDD	Twos complement	Outputs disabled

Digital Output Enable Function (OEB)

When using the SPI interface, the data outputs and DCO can be independently three-stated by using the programmable external MODE pin. The MODE pin (OEB) function is enabled via Bits[6:5] of Register 0x08.

If the MODE pin is configured to operate in traditional OEB mode and the MODE pin is low, the output data drivers and DCOs are enabled. If the MODE pin is high, the output data drivers and DCOs are placed in a high impedance state. This OEB function is not intended for rapid access to the data bus. Note that the MODE pin is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

TIMING

The AD9266 provides latched data with a pipeline delay of eight clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

Minimize the length of the output data lines and loads placed on them to reduce transients within the AD9266. These transients can degrade converter dynamic performance.

The lowest typical conversion rate of the AD9266 is 3 MSPS. At clock rates below 3 MSPS, dynamic performance may degrade.

Data Clock Output (DCO)

The AD9266 provides a DCO signal that is intended for capturing the data in an external register. The CMOS data outputs are valid on the rising and falling edge of DCO. See Figure 2 for a graphical timing description.

Table 12. Output Data Format

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode	OR
VIN+ − VIN−	< −VREF − 0.5 LSB	0000 0000 0000 0000	1000 0000 0000 0000	1
VIN+ − VIN−	= −VREF	0000 0000 0000 0000	1000 0000 0000 0000	0
VIN+ − VIN−	= 0	1000 0000 0000 0000	0000 0000 0000 0000	0
VIN+ − VIN−	= +VREF − 1.0 LSB	1111 1111 1111 1111	0111 1111 1111 1111	0
VIN+ − VIN−	> +VREF − 0.5 LSB	1111 1111 1111 1111	0111 1111 1111 1111	1

OUTPUT TEST

The AD9266 includes various output test options to place predictable values on the outputs of the AD9266.

OUTPUT TEST MODES

The output test options are described in Table 16 at Address 0x0D. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.