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16-Bit, 20/40/65/80 MSPS, 1.8 V Dual Analog-to-Digital Converter

Data Sheet **AD9269**

FEATURES

1.8 V analog supply operation
1.8 V to 3.3 V output supply
Integrated quadrature error correction (QEC)
SNR
- **77.6 dBFS at 9.7 MHz input**
- **71 dBFS at 200 MHz input**

SFDR
- **93 dBc at 9.7 MHz input**
- **80 dBc at 200 MHz input**

Low power
- **44 mW per channel at 20 MSPS**
- **100 mW per channel at 80 MSPS**

Differential input with 700 MHz bandwidth
On-chip voltage reference and sample-and-hold circuit
2 V p-p differential analog input
DNL = −0.5/+1.1 LSB
Serial port control options
- **Offset binary, gray code, or twos complement data format**
- **Optional clock duty cycle stabilizer (DCS)**
- **Integer 1-to-6 input clock divider**
- **Data output multiplex option**
- **Built-in selectable digital test pattern generation**
- **Energy-saving power-down modes**
- **Data clock output (DCO) with programmable clock and data alignment**

APPLICATIONS

Communications
Diversity radio systems
Multimode digital receivers
- **GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA**

I/Q demodulation systems
Smart antenna systems
Battery-powered instruments
Handheld scope meters
Portable medical imaging
Ultrasound
Radar/LIDAR

FUNCTIONAL BLOCK DIAGRAM

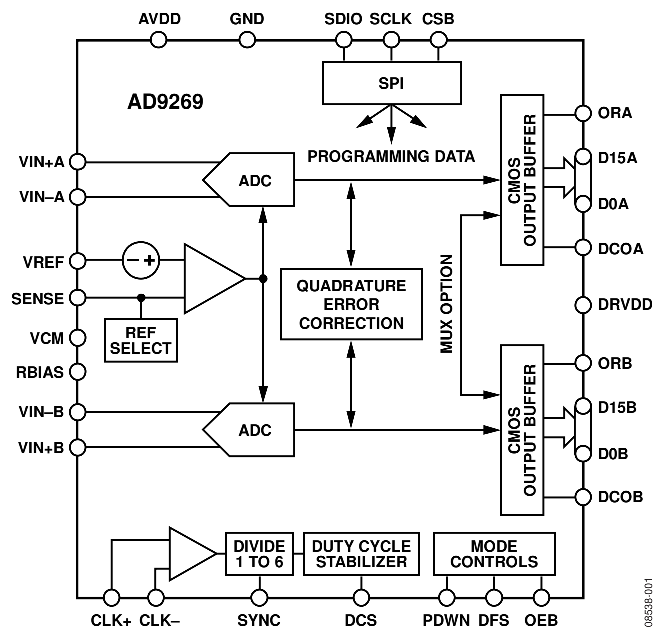

Figure 1.

PRODUCT HIGHLIGHTS

1. The AD9269 operates from a single 1.8 V analog power supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
2. The patented sample-and-hold circuit maintains excellent performance for input frequencies up to 200 MHz and is designed for low cost, low power, and ease of use.
3. An optional SPI selectable dc correction and quadrature error correction (QEC) feature corrects for dc offset, gain, and phase mismatches between the two channels.
4. A standard serial port interface (SPI) supports various product features and functions, such as data output formatting, internal clock divider, power-down, DCO/data timing and offset adjustments, and voltage reference modes.
5. The AD9269 is packaged in a 64-lead RoHS-compliant LFCSP that is pin compatible with the AD9268 16-bit ADC, the AD9258 14-bit ADC, the AD9251 14-bit ADC the AD9231 12-bit ADC, the AD6659 12-bit baseband diversity receiver, and the AD9204 10-bit ADC, enabling a simple migration path between 10-bit and 16-bit converters sampling from 20 MSPS to 125 MSPS.

Rev. A **Document Feedback**

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AD9269* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9269 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-878: High Speed ADC SPI Control Software
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9269: 16-Bit, 20/40/65/80 MSPS, 1.8 V Dual Analog-to-Digital Converter Data Sheet

User Guides

- UG-003: Evaluating the AD9650/AD9268/AD9258/ AD9251/AD9231/AD9204 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD9269 IBIS Model
- AD9269LFCSP/AD9266LFCSP S Parameter

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Solutions Bulletins & Brochures

- Analog-to-Digital Converter and Drivers ICs Solutions Bulletin, Volume 10, Issue 2

Technical Articles

- Improve The Design Of Your Passive Wideband ADC Front-End Network
- MS-2210: Designing Power Supplies for High Speed ADC
- Semiconductors Simplify Direct-Conversion Design

DESIGN RESOURCES

- AD9269 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9269 EngineerZone Discussions.

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TABLE OF CONTENTS

REVISION HISTORY

8/2016—Rev. 0 to Rev. A

1/2010—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9269 is a monolithic, dual-channel, 1.8 V supply, 16-bit, 20/40/65/80 MSPS analog-to-digital converter (ADC). It features a high performance sample-and-hold circuit and on-chip voltage reference.

The product uses multistage differential pipeline architecture with output error correction logic to provide 16-bit accuracy at 80 MSPS data rates and to guarantee no missing codes over the full operating temperature range.

The AD9269 incorporates an optional integrated dc correction and quadrature error correction block (QEC) that corrects for dc offset, gain, and phase mismatch between the two channels. This functional block can be very beneficial to complex signal processing applications such as direct conversion receivers.

The ADC also contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

A differential clock input controls all internal conversion cycles. An optional duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance.

The digital output data is presented in offset binary, gray code, or twos complement format. A data output clock (DCO) is provided for each ADC channel to ensure proper latch timing with receiving logic. Both 1.8 V and 3.3 V CMOS levels are supported, and output data can be multiplexed onto a single output bus.

The AD9269 is available in a 64-lead RoHS-compliant LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

Table 1.

		AD9269-20/AD9269-40			AD9269-65			AD9269-80			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	16			16			16			Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full		±0.05	±0.40		±0.05	±0.50		±0.05	±0.50	% FSR
Gain Error[1]	Full		−2.0			−2.0			−2.0		% FSR
Differential Nonlinearity (DNL)[2]	Full			−0.9/+1.2			−0.9/+1.4			−0.9/+1.65	LSB
	25°C		−0.5/+0.6			−0.5/+1.1			−0.5/+1.1		LSB
Integral Nonlinearity (INL)[2]	Full			±5.50			±6.50			±6.50	LSB
	25°C		±2.0			±2.2			±3.3		LSB
MATCHING CHARACTERISTICS											
Offset Error	25°C		±0.0	±0.50		±0.0	±0.55		±0.0	±0.65	% FSR
Gain Error[1]	25°C		±0.2			±0.2			±0.2		% FSR
TEMPERATURE DRIFT											
Offset Error	Full		±2			±2			±2		ppm/°C
INTERNAL VOLTAGE REFERENCE											
Output Voltage (1 V Mode)	Full	0.981	0.993	1.005	0.981	0.993	1.005	0.981	0.993	1.005	V
Load Regulation Error at 1.0 mA	Full		2			2			2		mV
INPUT-REFERRED NOISE											
VREF = 1.0 V	25°C		2.8			2.8			2.8		LSB rms
ANALOG INPUT											
Input Span, VREF = 1.0 V	Full		2			2			2		V p-p
Input Capacitance[3]	Full		6.5			6.5			6.5		pF
Input Common-Mode Voltage	Full		0.9			0.9			0.9		V
Input Common-Mode Range	Full	0.5		1.3	0.5		1.3	0.5		1.3	V
REFERENCE INPUT RESISTANCE	Full		7.5			7.5			7.5		kΩ
POWER SUPPLIES											
Supply Voltage											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7		3.6	1.7		3.6	1.7		3.6	V
Supply Current											
IAVDD[2]	Full		50.0/69.3	52.5/72.6		96.6	101.2		113	119	mA
IDRVDD[2] (1.8 V)	Full		3.9/6.4			9.6			11.8		mA
IDRVDD[2] (3.3 V)	Full		7.4/12.4			18.7			23		mA

Parameter	Temp	AD9269-20/AD9269-40			AD9269-65			AD9269-80			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER CONSUMPTION											
DC Input	Full		87.7/121.7			170.7			200		mW
Sine Wave Input[2] (DRVDD = 1.8 V)	Full		96.9/136.3	102.0/142.3		191.2	199.8		224.6	240	mW
Sine Wave Input[2] (DRVDD = 3.3 V)	Full		114.4/165.7			235.6			279		mW
Standby Power[4]	Full		37/37			37			37		mW
Power-Down Power	Full		1.0			1.0			1.0		mW

[1] Measured with a 1.0 V external reference.
[2] Measured with a 10 MHz input frequency at a rated sample rate, full-scale sine wave, with approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[4] Standby power is measured with a dc input and the CLK+, CLK– active.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

Table 2.

		AD9269-20/AD9269-40			AD9269-65			AD9269-80			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)											
f_{IN} = 9.7 MHz	25°C		78.0			77.5			77.6		dBFS
f_{IN} = 30.5 MHz	25°C		77.5			77.5			77.2		dBFS
	Full	76.5			76.5						dBFS
f_{IN} = 70 MHz	25°C		76.5			76.5			76.3		dBFS
	Full							75.5			dBFS
f_{IN} = 200 MHz	25°C								71.0		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)											
f_{IN} = 9.7 MHz	25°C		77.9			77.4			77.4		dBFS
f_{IN} = 30.5 MHz	25°C		77.2			77.2			76.9		dBFS
	Full	76.0			76.0						dBFS
f_{IN} = 70 MHz	25°C		76.4			76.4			76.1		dBFS
	Full							75.0			dBFS
f_{IN} = 200 MHz	25°C								69.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 9.7 MHz	25°C		12.6			12.6			12.6		Bits
f_{IN} = 30.5 MHz	25°C		12.5			12.5			12.5		Bits
f_{IN} = 70 MHz	25°C		12.4			12.4			12.3		Bits
f_{IN} = 200 MHz	25°C								11.2		Bits
WORST SECOND OR THIRD HARMONIC											
f_{IN} = 9.7 MHz	25°C		−95			−97			−93		dBc
f_{IN} = 30.5 MHz	25°C		−90			−93			−92		dBc
	Full			−80			−80				dBc
f_{IN} = 70 MHz	25°C		−89			−97			−90		dBc
	Full									−80	dBc
f_{IN} = 200 MHz	25°C								−80		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)											
f_{IN} = 9.7 MHz	25°C		95			95			93		dBc
f_{IN} = 30.5 MHz	25°C		90			91			92		dBc
	Full	80			80						dBc
f_{IN} = 70 MHz	25°C		89			95			90		dBc
	Full							80			dBc
f_{IN} = 200 MHz	25°C								80		dBc
WORST OTHER (HARMONIC OR SPUR)											
f_{IN} = 9.7 MHz	25°C		−99			−89			−99		dBc
f_{IN} = 30.5 MHz	25°C		−100			−100			−99		dBc
	Full			−90			−91				dBc
f_{IN} = 70 MHz	25°C		−99			−100			−97		dBc
	Full									−89	dBc
f_{IN} = 200 MHz	25°C								−86		dBc
TWO-TONE SFDR											
f_{IN} = 30.5 MHz (−7 dBFS), 32.5 MHz (−7 dBFS)	25°C		90			90			90		dBc
CROSSTALK[2]	Full		−110			−110			−110		dBc
ANALOG INPUT BANDWIDTH	25°C		700			700			700		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

Table 3.

		AD9269-20/AD9269-40/AD9269-65/AD9269-80			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Unit**
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.2		3.6	V p-p
Input Voltage Range	Full	GND − 0.3		AVDD + 0.2	V
High Level Input Current	Full	−10		+10	μA
Low Level Input Current	Full	−10		+10	μA
Input Resistance	Full	8	10	12	kΩ
Input Capacitance	Full		4		pF
LOGIC INPUTS (SCLK/DFS, SYNC, PDWN)[1]					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−50		−75	μA
Low Level Input Current	Full	−10		+10	μA
Input Resistance	Full		30		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (CSB)[2]					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	μA
Low Level Input Current	Full	40		135	μA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SDIO/DCS)[2]					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	μA
Low Level Input Current	Full	40		130	μA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
DRVDD = 3.3 V					
High Level Output Voltage, I_{OH} = 50 μA	Full	3.29			V
High Level Output Voltage, I_{OH} = 0.5 mA	Full	3.25			V
Low Level Output Voltage, I_{OL} = 1.6 mA	Full			0.2	V
Low Level Output Voltage, I_{OL} = 50 μA	Full			0.05	V
DRVDD = 1.8 V					
High Level Output Voltage, I_{OH} = 50 μA	Full	1.79			V
High Level Output Voltage, I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage, I_{OL} = 1.6 mA	Full			0.2	V
Low Level Output Voltage, I_{OL} = 50 μA	Full			0.05	V

[1] Internal 30 kΩ pull-down.
[2] Internal 30 kΩ pull-up.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

Table 4.

Parameter	Temp	AD9269-20/AD9269-40 Min	Typ	Max	AD9269-65 Min	Typ	Max	AD9269-80 Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS											
Input Clock Rate	Full			480			480			480	MHz
Conversion Rate[1]	Full	3		20/40	3		65	3		80	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	50/25			15.38			12.5			ns
CLK Pulse Width High (t_{CH})			25.0/12.5			7.69			6.25		ns
Aperture Delay (t_A)	Full		1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1			0.1		ps rms
DATA OUTPUT PARAMETERS											
Data Propagation Delay (t_{PD})	Full		3			3			3		ns
DCO Propagation Delay (t_{DCO})	Full		3			3			3		ns
DCO to Data Skew (t_{SKEW})	Full		0.1			0.1			0.1		ns
Pipeline Delay (Latency)	Full		9			9			9		Cycles
With QEC Active	Full		11			11			11		Cycles
Wake-Up Time[2]	Full		350			350			350		μs
Standby	Full		600/400			300			260		ns
OUT-OF-RANGE RECOVERY TIME	Full		2			2			2		Cycles

[1] Conversion rate is the clock rate after the CLK divider.
[2] Wake-up time is dependent on the value of the decoupling capacitors.

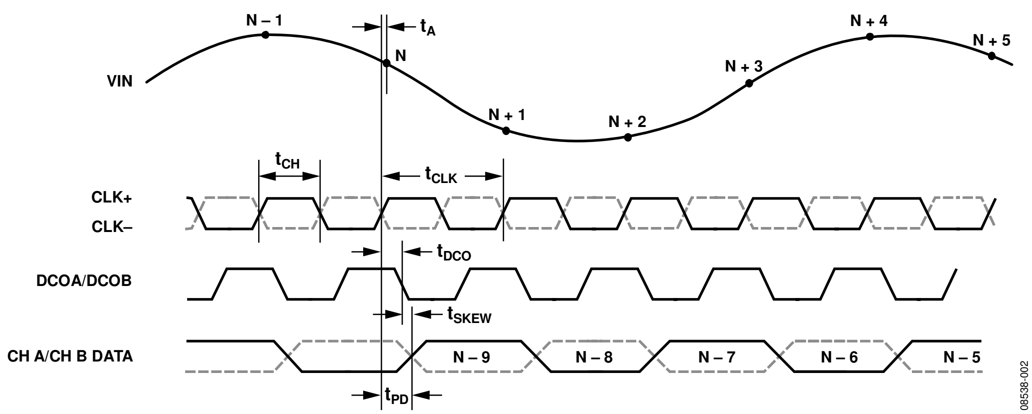


Figure 2. CMOS Output Data Timing

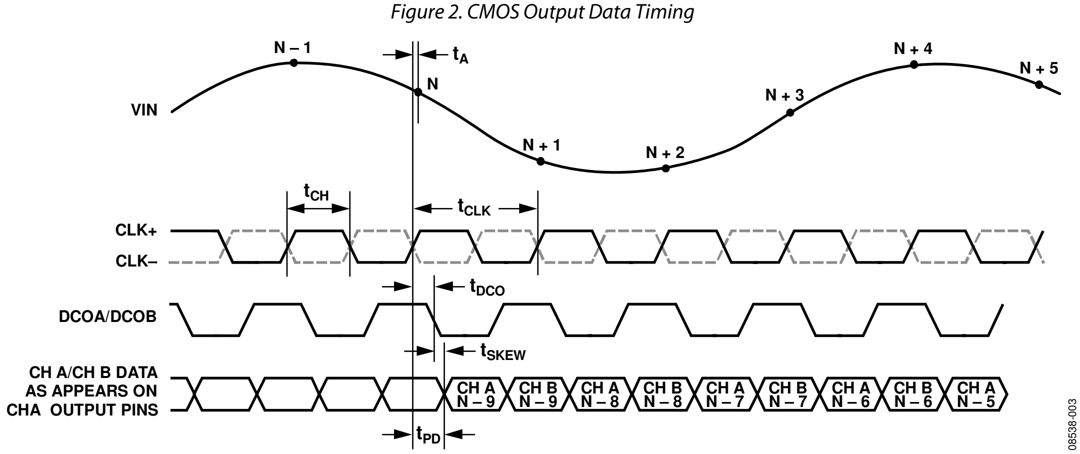


Figure 3. CMOS Interleaved Output Timing, Output as Appears on Channel A Output Pins

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to rising edge of CLK setup time		0.24		ns
t_{HSYNC}	SYNC to rising edge of CLK hold time		0.40		ns
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	SCLK pulse width high	10			ns
t_{LOW}	SCLK pulse width low	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

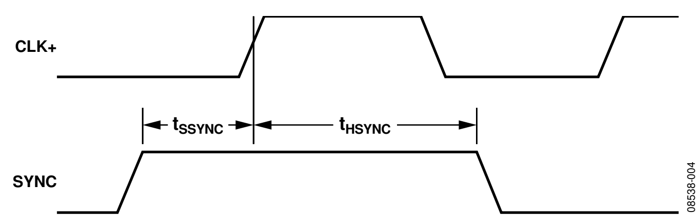


Figure 4. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +3.9 V
VIN+A, VIN+B, VIN−A, VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to DRVDD + 0.3 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.3 V
SCLK/DFS to AGND	−0.3 V to DRVDD + 0.3 V
SDIO/DCS to AGND	−0.3 V to DRVDD + 0.3 V
OEB to AGND	−0.3 V to DRVDD + 0.3 V
PDWN to AGND	−0.3 V to DRVDD + 0.3 V
D0x through D15x to AGND	−0.3 V to DRVDD + 0.3 V
DCOx to AGND	−0.3 V to DRVDD + 0.3 V
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The exposed paddle is the only ground connection for the chip. The exposed paddle must be soldered to the AGND plane of the user PCB. Soldering the exposed paddle to the user board also increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Unit
64-Lead LFCSP 9 mm × 9 mm (CP-64-4)	0	23	2.0		°C/W
	1.0	20		12	°C/W
	2.5	18			°C/W

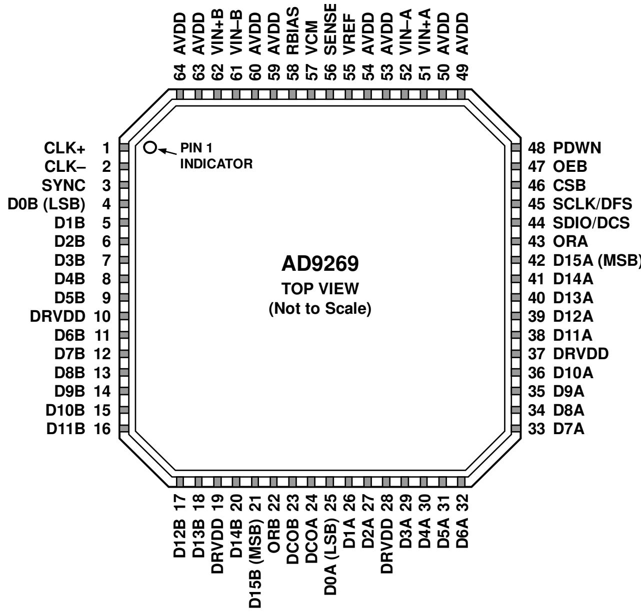
[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown in Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PADDLE MUST BE SOLDERED TO THE PCB ANALOG GROUND TO ENSURE PROPER HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

08538-005

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
0, EP	AGND	The exposed paddle is the only ground connection. It must be soldered to the PCB analog ground to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.
1, 2	CLK+, CLK−	Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.
3	SYNC	Digital Input. SYNC input to clock divider. 30 kΩ internal pull-down.
4 to 9, 11 to 18, 20, 21	D0B (LSB) to D15B (MSB)	Channel B Digital Outputs. D0B is the LSB; D15B is the MSB.
10, 19, 28, 37	DRVDD	Digital Output Driver Supply (1.8 V to 3.3 V).
22	ORB	Channel B Out-of-Range Digital Output.
23	DCOB	Channel B Data Clock Digital Output.
24	DCOA	Channel A Data Clock Digital Output.
25 to 27, 29 to 36, 38 to 42	D0A (LSB) to D15A (MSB)	Channel A Digital Outputs. D0A is the LSB; D15A is the MSB.
43	ORA	Channel A Out-of-Range Digital Output.
44	SDIO/DCS	SPI Data Input/Output (SDIO). Bidirectional SPI data I/O in SPI mode. 30 kΩ internal pull-down in SPI mode. Duty Cycle Stabilizer (DCS). Static enable input for duty cycle stabilizer in non-SPI mode. 30 kΩ internal pull-up in non-SPI (DCS) mode.
45	SCLK/DFS	SPI Clock (SCLK). Input in SPI mode. 30 kΩ internal pull-down. Data Format Select (DFS). Static control of data output format in non-SPI mode. 30 kΩ internal pull-down. DFS high: twos complement output. DFS low: offset binary output.
46	CSB	SPI Chip Select. Active low enable; 30 kΩ internal pull-up.
47	OEB	Digital Input. 30 kΩ internal pull-down. Low: enable Channel A and Channel B digital outputs. High: three-state outputs.
48	PDWN	Digital Input. 30 kΩ internal pull-down. High: power down device. Low: run device, normal operation.

Pin No.	Mnemonic	Description
49, 50, 53, 54, 59, 60, 63, 64	AVDD	1.8 V Analog Supply Pins.
51, 52	VIN+A, VIN−A	Channel A Analog Inputs.
55	VREF	Voltage Reference Input/Output.
56	SENSE	Reference Mode Selection.
57	VCM	Analog Output Voltage at Midsupply. Sets the common mode of the analog inputs.
58	RBIAS	Set Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
61, 62	VIN−B, VIN+B	Channel B Analog Inputs.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9269-80

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

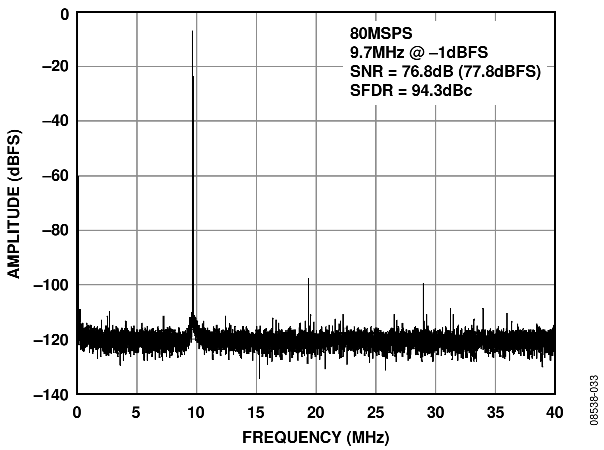


Figure 6. AD9269-80 Single-Tone FFT with f_{IN} = 9.7 MHz

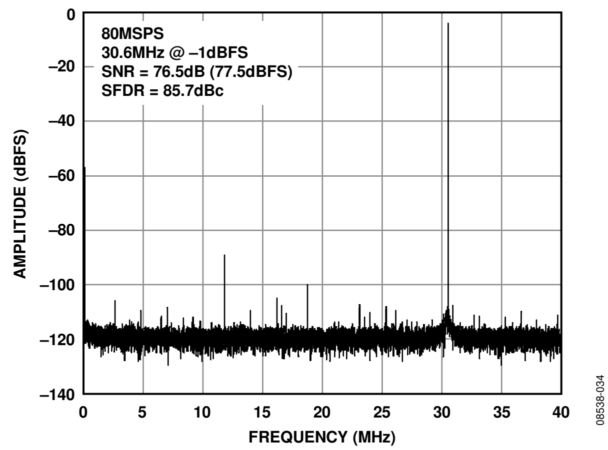


Figure 9. AD9269-80 Single-Tone FFT with f_{IN} = 30.6 MHz

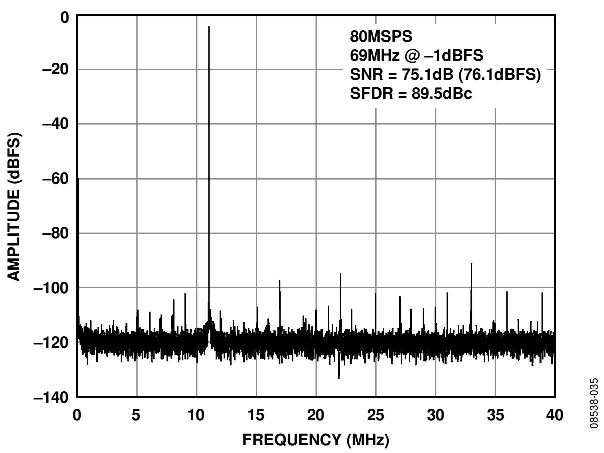


Figure 7. AD9269-80 Single-Tone FFT with f_{IN} = 69 MHz

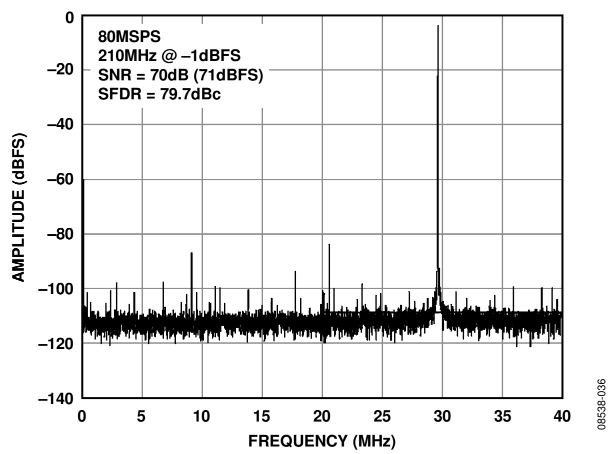


Figure 10. AD9269-80 Single-Tone FFT with f_{IN} = 210 MHz

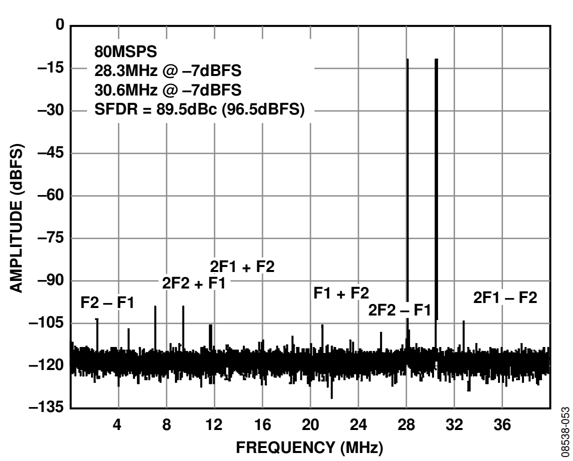


Figure 8. AD9269-80 Two-Tone FFT with f_{IN1} = 28.3 MHz and f_{IN2} = 30.6 MHz

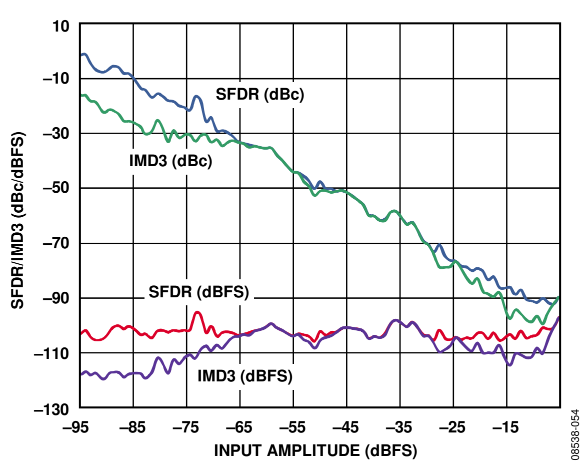


Figure 11. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with fIN1 = 28.3 MHz and fIN2 = 30.6 MHz

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

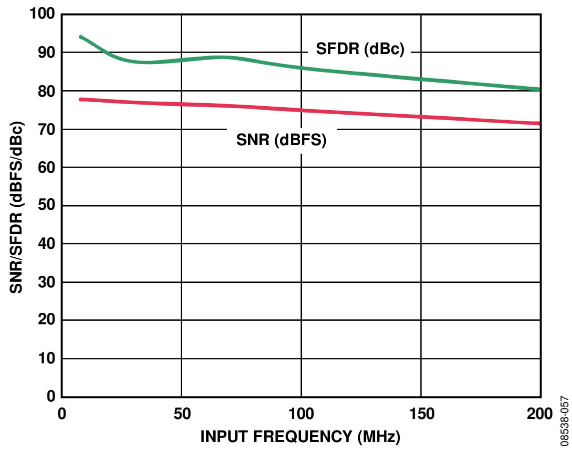


Figure 12. AD9269-80 SNR/SFDR vs. Input Frequency (AIN) with 2 V p-p Full Scale

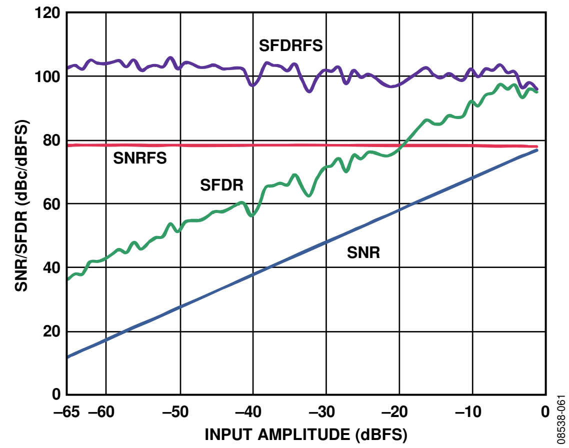


Figure 15. AD9269-80 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

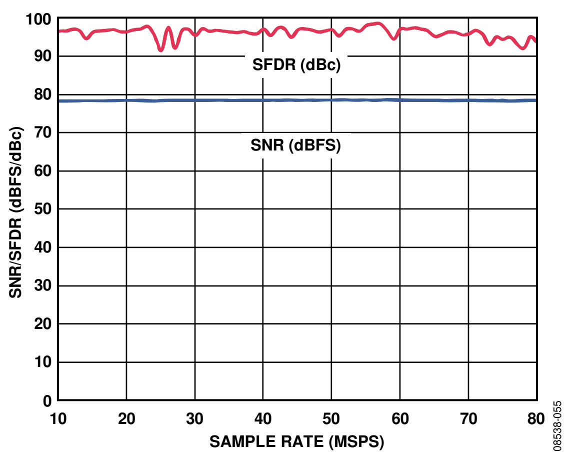


Figure 13. AD9269-80 SNR/SFDR vs. Sample Rate with AIN = 9.7 MHz

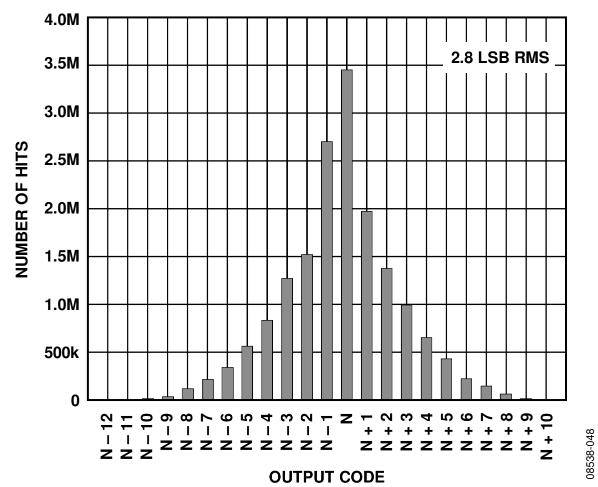


Figure 16. Grounded Input Histogram

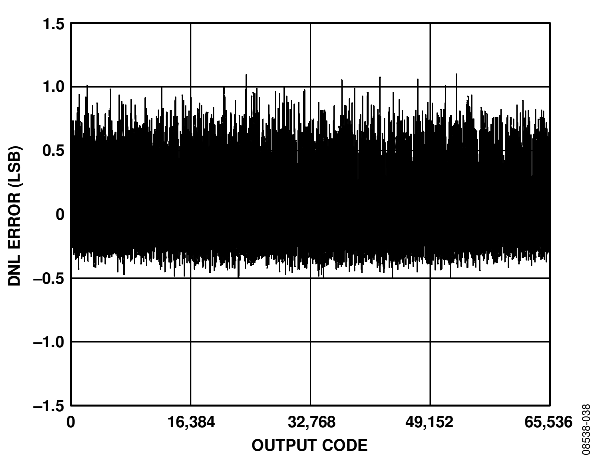


Figure 14. DNL Error with f_{IN} = 9.7 MHz

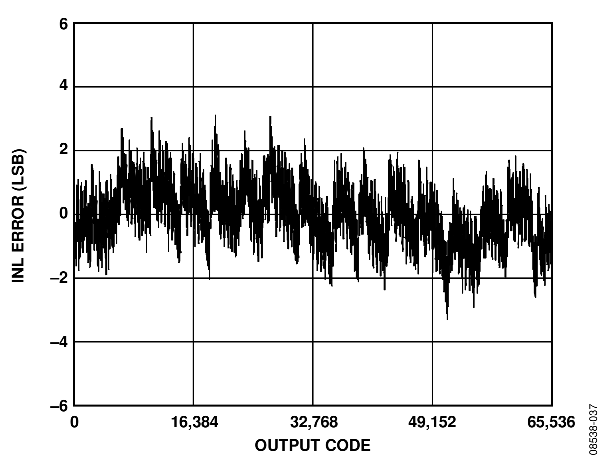


Figure 17. INL with f_{IN} = 9.7 MHz

AD9269-65

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

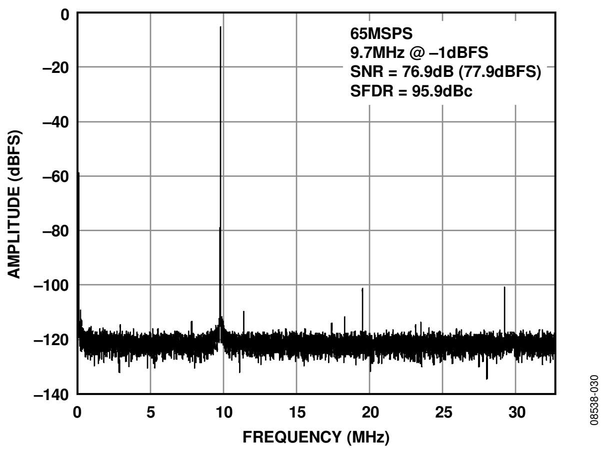


Figure 18. AD9269-65 Single-Tone FFT with f_{IN} = 9.7 MHz

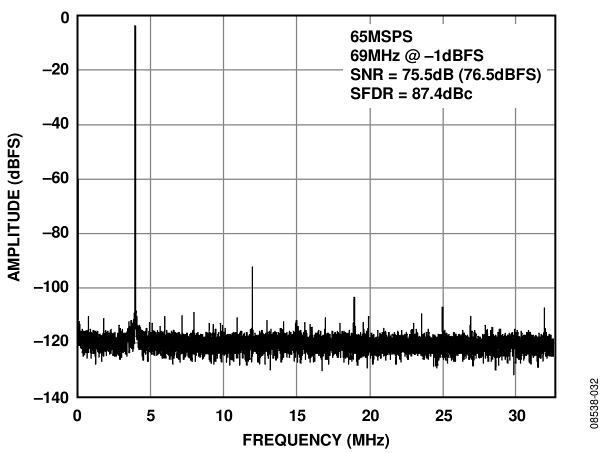


Figure 19. AD9269-65 Single-Tone FFT with f_{IN} = 69 MHz

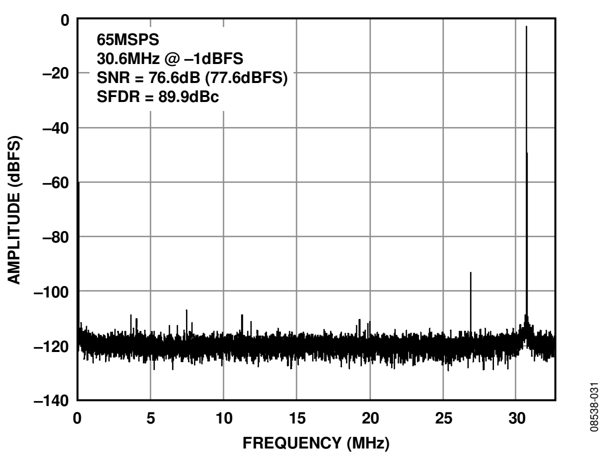


Figure 20. AD9269-65 Single-Tone FFT with f_{IN} = 30.6 MHz

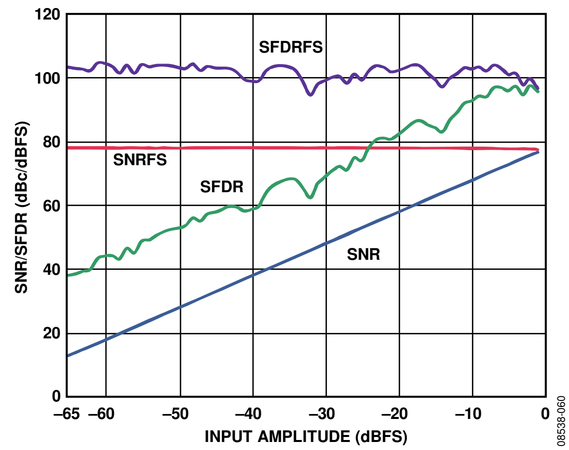


Figure 21. AD9269-65 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

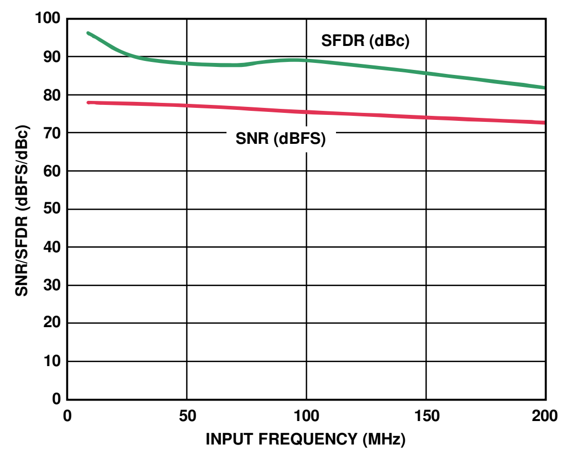


Figure 22. AD9269-65 SNR/SFDR vs. Input Frequency (AIN) with 2 V p-p Full Scale

AD9269-40

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

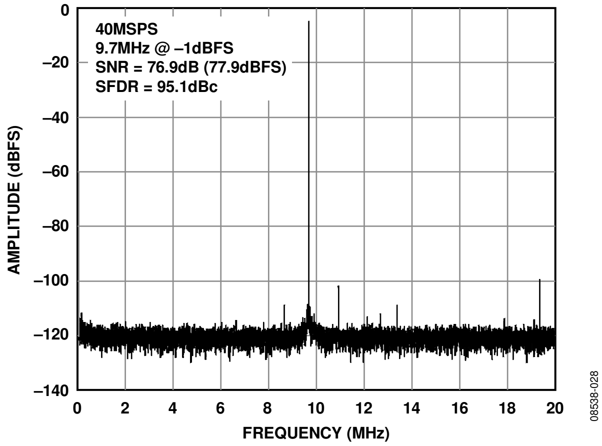


Figure 23. AD9269-40 Single-Tone FFT with f_{IN} = 9.7 MHz

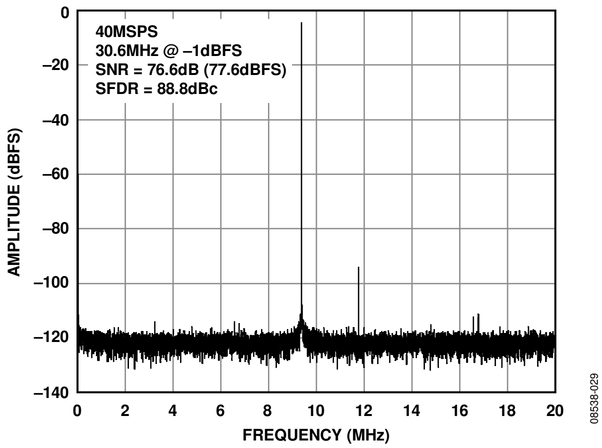


Figure 24. AD9269-40 Single-Tone FFT with f_{IN} = 30.6 MHz

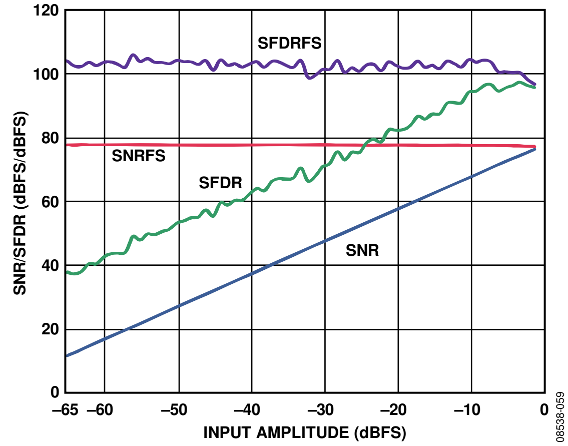


Figure 25. AD9269-40 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

AD9269-20

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

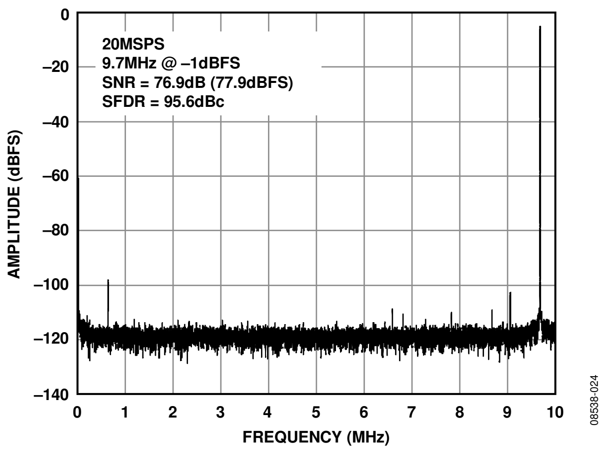


Figure 26. AD9269-20 Single-Tone FFT with f_{IN} = 9.7 MHz

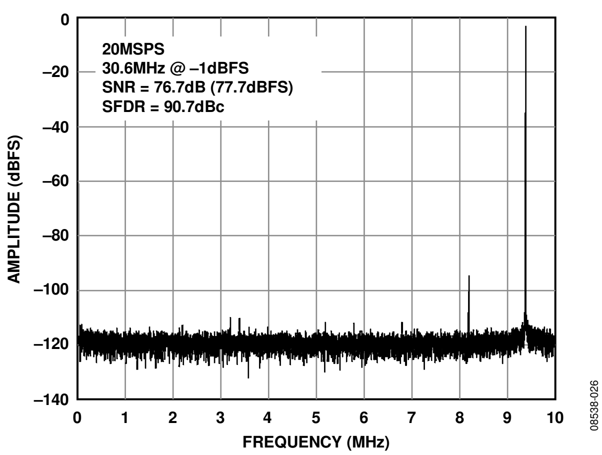


Figure 27. AD9269-20 Single-Tone FFT with f_{IN} = 30.6 MHz

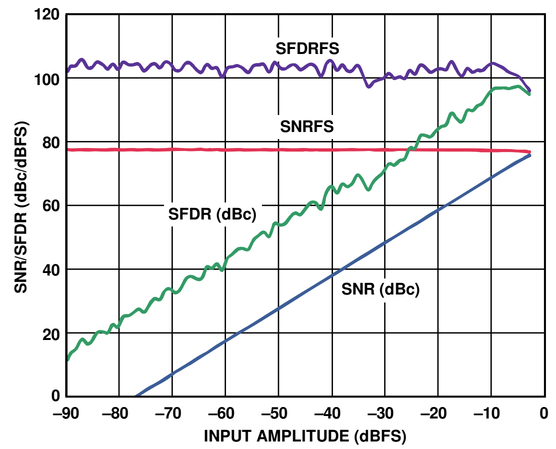


Figure 28. AD9269-20 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

EQUIVALENT CIRCUITS

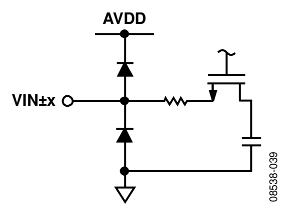


Figure 29. Equivalent Analog Input Circuit

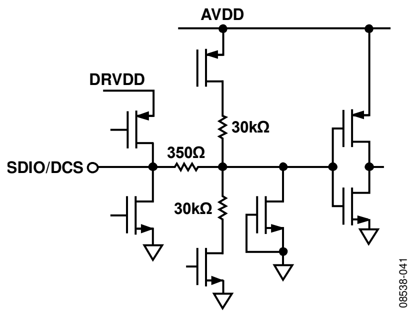


Figure 30. Equivalent SDIO/DCS Input Circuit

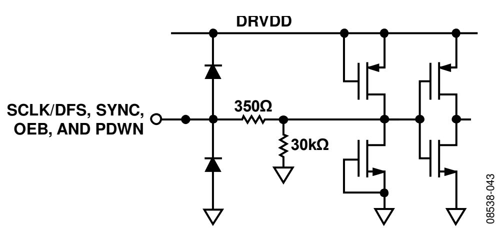


Figure 31. Equivalent SCLK/DFS, SYNC, OEB, and PDWN Input Circuit

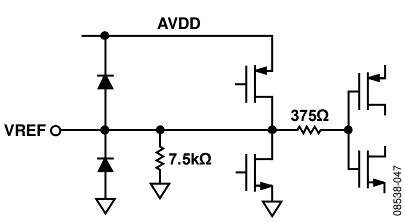


Figure 32. Equivalent VREF Circuit

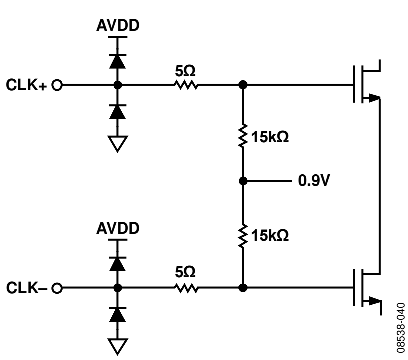


Figure 33. Equivalent Clock Input Circuit

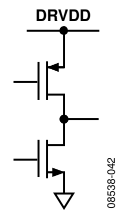


Figure 34. Equivalent Digital Output Circuit

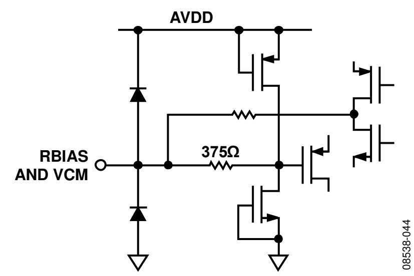


Figure 35. Equivalent RBIAS, VCM Circuit

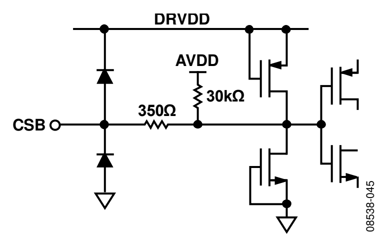


Figure 36. Equivalent CSB Input Circuit

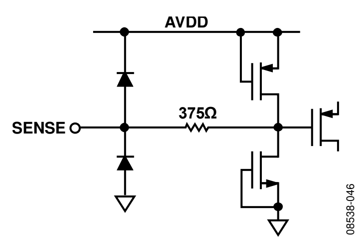


Figure 37. Equivalent SENSE Circuit

THEORY OF OPERATION

The AD9269 dual-channel ADC design can be used for diversity reception of signals, where the ADCs are operating identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample any $f_S/2$ frequency segment from dc to 200 MHz, using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 300 MHz analog input is permitted, but it occurs at the expense of increased ADC noise and distortion.

In nondiversity applications, the AD9269 can be used as a baseband or direct downconversion receiver, in which one ADC is used for I input data and the other is used for Q input data.

The AD9269 incorporates an optional, integrated dc correction and quadrature error correction block (QEC) that can correct for dc offset, gain, and phase mismatch between the two channels. This functional block can be very beneficial to complex signal processing applications such as direct conversion receivers.

Synchronization capability is provided to allow synchronized timing between multiple channels or multiple devices.

Programming and control of the AD9269 are accomplished using a 3-wire SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9269 architecture consists of a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 16-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the CMOS output buffers. The output buffers are powered from a separate (DRVDD) supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9269 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 38). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle.

A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs* (see www.analog.com); and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

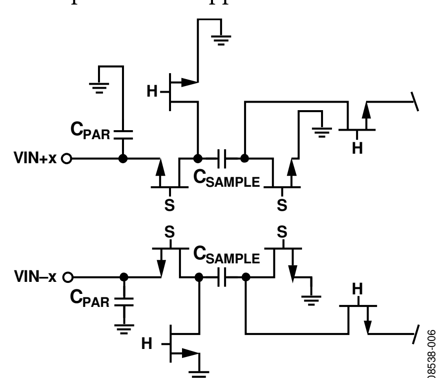


Figure 38. Switched-Capacitor Input Circuit

Input Common Mode

The analog inputs of the AD9269 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide a dc bias externally. Setting the device so that VCM = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 39.

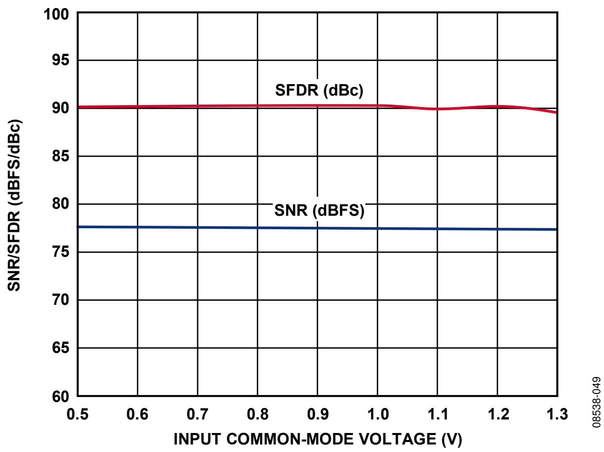


Figure 39. SNR/SFDR vs. Input Common-Mode Voltage, f_{IN} = 32.5 MHz, f_S = 80 MSPS

An on-board, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section.

Differential Input Configurations

Optimum performance is achieved while driving the AD9269 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4938-2 is easily set with the VCM pin of the AD9269 (see Figure 40), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

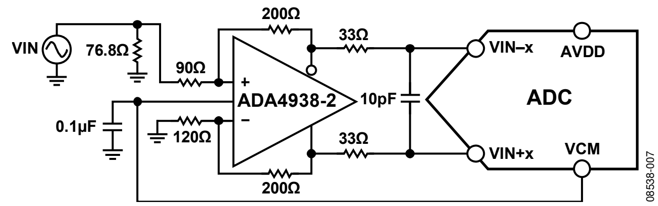


Figure 40. Differential Input Configuration Using the ADA4938-2

For baseband applications below ~10 MHz where SNR is a key parameter, differential transformer-coupling is the recommended input configuration (see Figure 41). To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

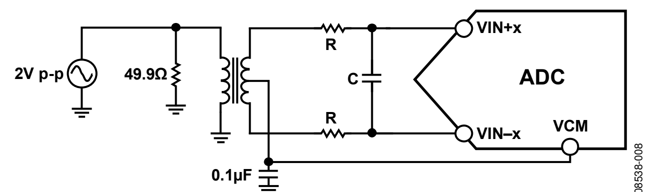


Figure 41. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9269. For applications above ~10 MHz where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 42).

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use the AD8352 differential driver (see Figure 43). Refer to the AD8352 data sheet for more information.

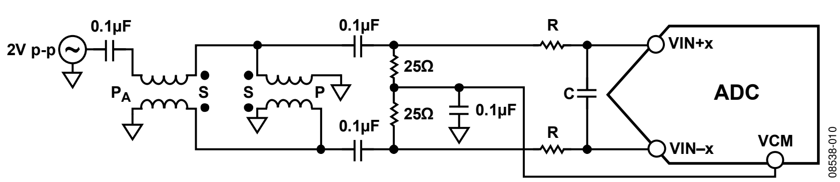


Figure 42. Differential Double Balun Input Configuration

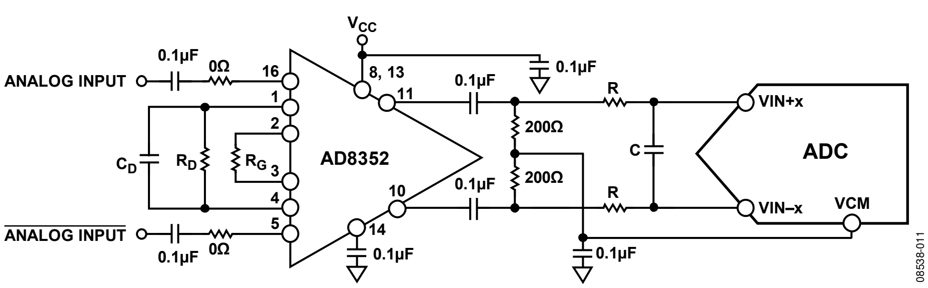


Figure 43. Differential Input Configuration Using the AD8352

In any configuration, the value of Shunt Capacitor C is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 9 displays the suggested values to set the RC network. However, these values are dependent on the input signal and should be used only as a starting guide.

Table 9. Example RC Network

Frequency Range (MHz)	R Series (Ω Each)	C Differential (pF)
0 to 70	33	22
70 to 200	125	Open

Single-Ended Input Configuration

A single-ended input can provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the source impedances on each input are matched, there should be little effect on SNR performance. Figure 44 shows a typical single-ended input configuration.

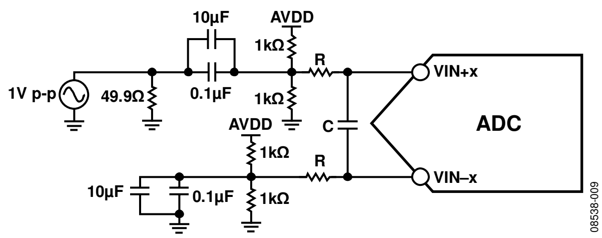


Figure 44. Single-Ended Input Configuration

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9269. V_{REF} can be configured using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the sections that follow. The Reference Decoupling section describes the best-practices PCB layout of the reference.

Internal Reference Connection

A comparator within the AD9269 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 10. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 45), setting V_{REF} to 1.0 V.

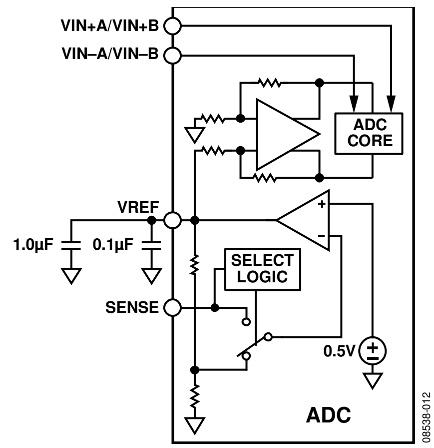


Figure 45. Internal Reference Configuration

If the internal reference of the AD9269 drives multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 46 shows how the internal reference voltage is affected by loading.

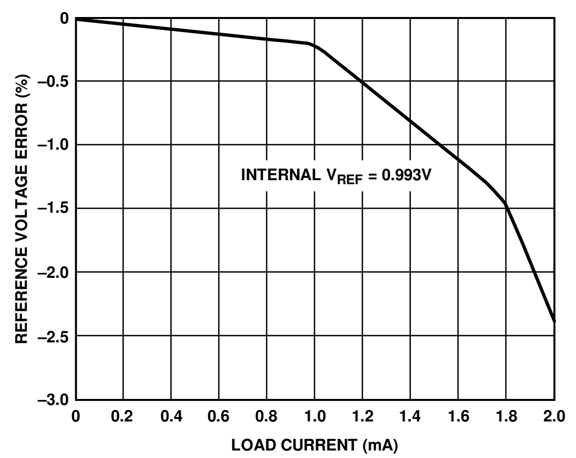


Figure 46. V_{REF} Accuracy vs. Load Current

Table 10. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting V_{REF} (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	AGND to 0.2	1.0 internal	2.0
Fixed External Reference	AVDD	1.0 applied to external VREF pin	2.0

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. Figure 47 shows the typical drift characteristics of the internal reference in 1.0 V mode.

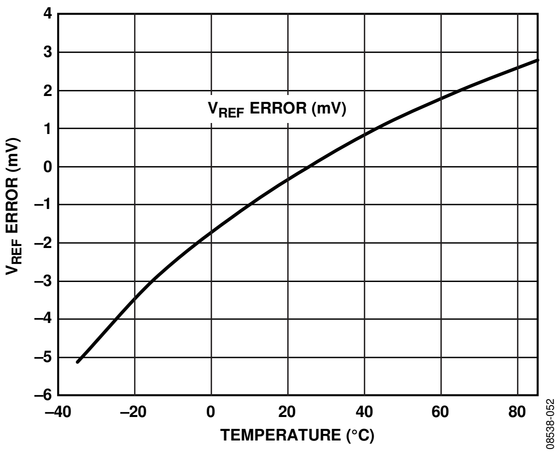


Figure 47. Typical V_{REF} Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load (see Figure 32). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.0 V.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9269 sample clock inputs, CLK+ and CLK–, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally (see Figure 48) and require no external bias.

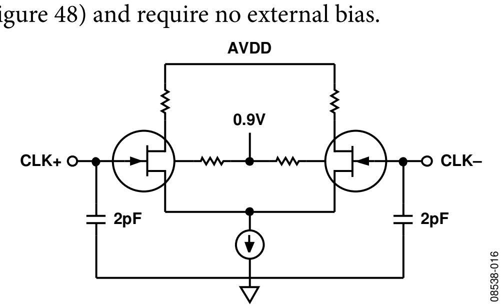


Figure 48. Equivalent Clock Input Circuit

Clock Input Options

The AD9269 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 49 and Figure 50 show two preferred methods for clocking the AD9269 (at rates up to 6× the specified sample rate when using the internal clock divider function). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF balun or an RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 480 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer/balun secondary limit clock excursions into the AD9269 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9269 while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

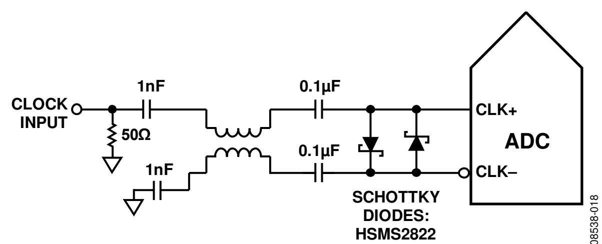


Figure 49. Balun-Coupled Differential Clock (Up to 480 MHz)

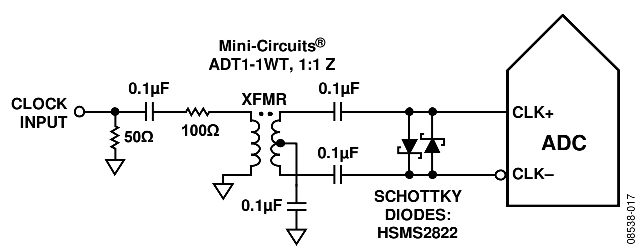


Figure 50. Transformer-Coupled Differential Clock (Up to 200 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 51. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

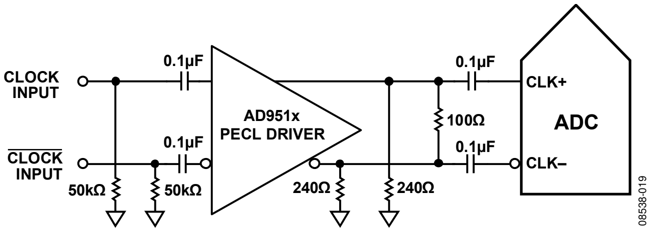


Figure 51. Differential PECL Sample Clock (Up to 480 MHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 52. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

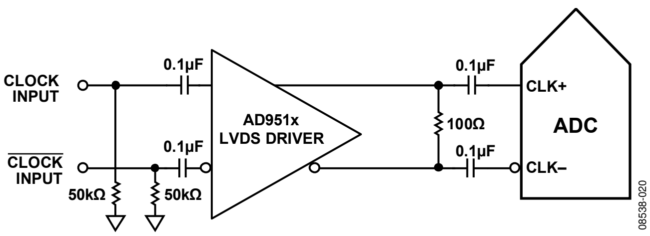


Figure 52. Differential LVDS Sample Clock (Up to 480 MHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK– pin to ground with a 0.1 µF capacitor (see Figure 53).

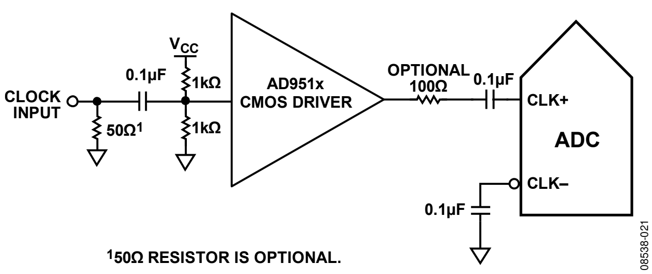


Figure 53. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9269 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 6. Optimum performance is obtained by enabling the internal duty cycle stabilizer (DCS) when using divide ratios other than 1, 2, or 4.

The AD9269 clock divider can be synchronized using the external SYNC input. Bits[2:1] in Register 0x100 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to the initial state. This synchronization feature allows multiple devices to have the clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9269 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9269. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS on, as shown in Figure 54.

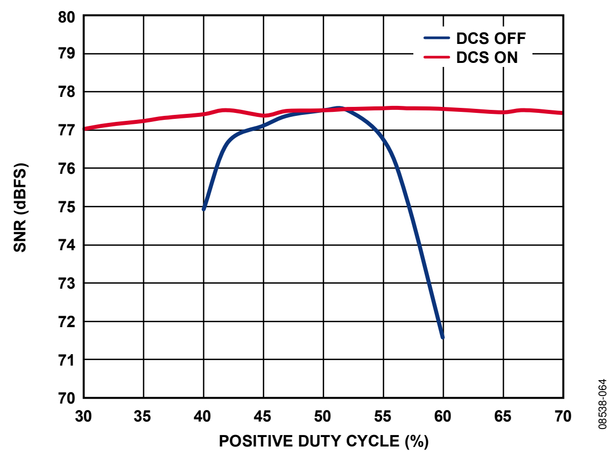


Figure 54. SNR vs. Duty Cycle Stabilizer On/Off

Jitter in the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 20 MHz nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after the dynamic clock frequency increases or decreases before the DCS loop is relocked to the input signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR from the low frequency SNR (SNR_{LF}) at a given input frequency (f_{INPUT}) due to jitter (t_{JRMS}) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{INPUT} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the previous equation, the rms aperture jitter represents the clock input jitter specification. IF undersampling applications are particularly sensitive to jitter, as illustrated in Figure 55.

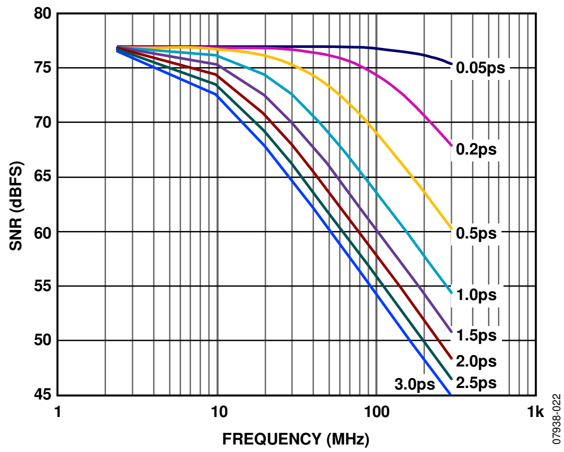


Figure 55. SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases in which aperture jitter may affect the dynamic range of the AD9269. To avoid modulating the clock signal with digital noise, keep power supplies for clock drivers separate from the ADC output driver supplies. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step.

For more information, see the AN-501 Application Note and the AN-756 Application Note, available on www.analog.com.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 56, the analog core power dissipated by the AD9269 is proportional to the sample rate. The digital power dissipation of the CMOS outputs is determined primarily by the strength of the digital drivers and the load on each output bit.

The maximum DRVDD current (IDRVDD) can be calculated as

$$IDRVDD = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where *N* is the number of output bits (34, in the case of the AD9269).

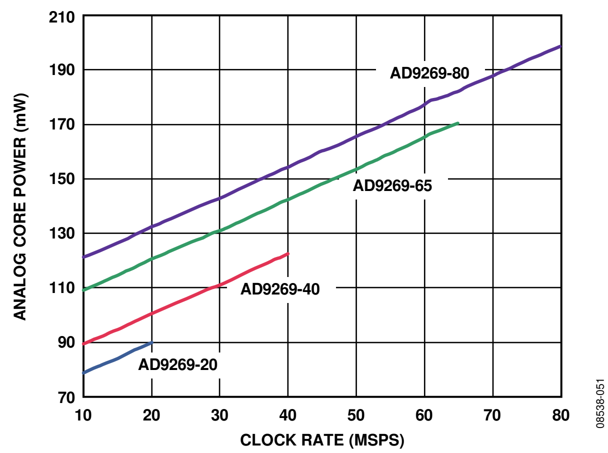


Figure 56. Analog Core Power vs. Clock Rate

This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency of $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the sample rate and the characteristics of the analog input signal.

Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 56 was taken using the same operating conditions as those used for the Typical Performance Characteristics, with a 5 pF load on each output driver.