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Octal LNA/VGA/AAF/ADC and Crosspoint Switch

AD9272

FEATURES

- 8 channels of LNA, VGA, AAF, and ADC
- Low noise preamplifier (LNA)
  - Input-referred noise voltage = 0.75 nV/√Hz (gain = 21.3 dB) @ 5 MHz typical
  - SPI-programmable gain = 15.6 dB/17.9 dB/21.3 dB
  - Single-ended input; V_{IN} maximum = 733 mV p-p/550 mV p-p/367 mV p-p
  - Dual-mode active input impedance matching
  - Bandwidth (BW) > 100 MHz
  - Full-scale (FS) output = 4.4 V p-p differential
- Variable gain amplifier (VGA)
  - Attenuator range = −42 dB to 0 dB
  - SPI-programmable PGA gain = 21 dB/24 dB/27 dB/30 dB
  - Linear-in-dB gain control
- Antialiasing filter (AAF)
  - Programmable 2nd-order low-pass filter (LPF) from 8 MHz to 18 MHz
  - Programmable high-pass filter (HPF)
- Analog-to-digital converter (ADC)
  - 12 bits at 10 MSPS to 80 MSPS
  - SNR = 70 dB
  - SFDR = 75 dB
  - Serial LVDS (ANSI-644, IEEE 1596.3 reduced range link)
  - Data and frame clock outputs
- Includes an 8 × 8 differential crosspoint switch to support continuous wave (CW) Doppler
- Low power, 195 mW per channel at 12 bits/40 MSPS (TGC)
- 120 mW per channel in CW Doppler
- Flexible power-down modes
- Overload recovery in <10 ns
- Fast recovery from low power standby mode, <2 µs
- 100-lead TQFP

APPLICATIONS

- Medical imaging/ultrasound
- Automotive radar

GENERAL DESCRIPTION

The AD9272 is designed for low cost, low power, small size, and ease of use. It contains eight channels of a low noise preamplifier (LNA) with a variable gain amplifier (VGA), an antialiasing filter (AAF), and a 12-bit, 10 MSPS to 80 MSPS analog-to-digital converter (ADC).

Each channel features a variable gain range of 42 dB, a fully differential signal path, an active input preamplifier termination, a maximum gain of up to 52 dB, and an ADC with a conversion rate of up to 80 MSPS. The channel is optimized for dynamic performance and low power in applications where a small package size is critical.

FUNCTIONAL BLOCK DIAGRAM

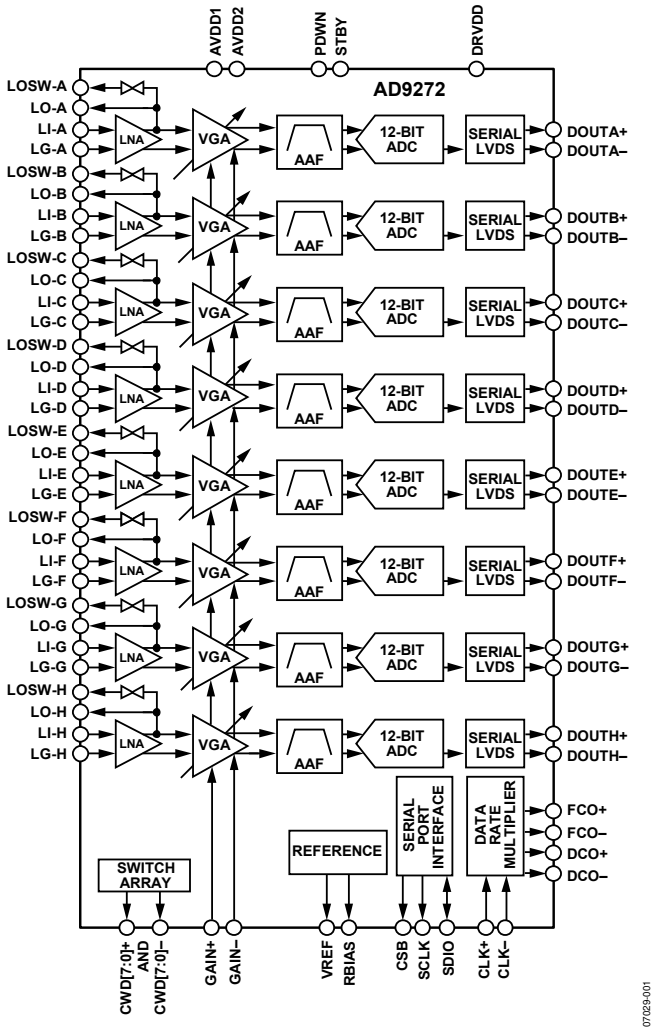

Figure 1.

The LNA has a single-ended-to-differential gain that is selectable through the SPI. The LNA input-referred noise voltage is typically 0.75 nV/√Hz at a gain of 21.3 dB, and the combined input-referred noise voltage of the entire channel is 0.85 nV/√Hz at maximum gain. Assuming a 15 MHz noise bandwidth (NBW) and a 21.3 dB LNA gain, the input SNR is about 92 dB. In CW Doppler mode, the LNA output drives a transconductance amp that is switched through an 8 × 8 differential crosspoint switch. The switch is programmable through the SPI.

Rev. C

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9272 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-1210: Powering the AD9272 Octal Ultrasound ADC/LNA/VGA/AAF with the ADP5020 Switching Regulator PMU for Increased Efficiency
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-737: How ADIsimADC Models an ADC
- AN-812: MicroController-Based Serial Port Interface (SPI) Boot Circuit
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9272: Octal LNA/VGA/AAF/ADC and Crosspoint Switch Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- UG-001: Evaluation Board User Guide

TOOLS AND SIMULATIONS

- Visual Analog
- AD9272 IBIS Models

REFERENCE MATERIALS

Press

- Industry's First Octal Ultrasound Receiver with Digital I/Q Demodulator and Decimation Filter Reduces Processor Overhead in Ultrasound Systems
- Low Cost, Octal Ultrasound Receiver with On-Chip RF Decimator and JESD204B Serial Interface

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC
- New Components Offer Fexibility in Ultrasound System Design
- Powering High-Speed Analog-to-Digital Converters with Switching Power Supplies
- Processors for Ultrasound Improve Image Quality

DESIGN RESOURCES

- AD9272 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9272 EngineerZone Discussions.

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4/09—Revision A: Initial Version

The AD9272 requires a LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock (DCO±) for capturing data on the output and a frame clock (FCO±) trigger for signaling a new output byte are provided.

Powering down individual channels is supported to increase battery life for portable applications. There is also a standby mode option that allows quick power-up for power cycling. In CW Doppler operation, the VGA, antialiasing filter (AAF), and ADC are powered down. The power of the time gain control (TGC) path scales with selectable speed grades.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable clock, data alignment, and programmable digital test pattern generation. The digital test patterns include built-in fixed patterns, built-in pseudorandom patterns, and custom user-defined test patterns entered via the serial port interface.

Fabricated in an advanced CMOS process, the AD9272 is available in a 16 mm × 16 mm, RoHS-compliant, 100-lead TQFP. It is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Small Footprint. Eight channels are contained in a small, space-saving package. A full TGC path, ADC, and crosspoint switch are contained within a 100-lead, 16 mm × 16 mm TQFP.
2. Low Power of 195 mW Per Channel at 40 MSPS.
3. Integrated Crosspoint Switch. This switch allows numerous multichannel configuration options to enable the CW Doppler mode.
4. Ease of Use. A data clock output (DCO±) operates up to 480 MHz and supports double data rate (DDR) operation.
5. User Flexibility. Serial port interface (SPI) control offers a wide range of flexible features to meet specific system requirements.
6. Integrated Second-Order Antialiasing Filter. This filter is placed between the VGA and the ADC and is programmable from 8 MHz to 18 MHz.

SPECIFICATIONS

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, f_{IN} = 5 MHz, R_S = 50 Ω, LNA gain = 21.3 dB, LNA bias = high, PGA gain = 27 dB, GAIN− = 0.8 V, AAF LPF cutoff = f_{SAMPLE}/4.5, HPF = LPF cutoff/20.7 (default), full temperature, ANSI-644 LVDS mode, unless otherwise noted.

Table 1.

		AD9272-40			AD9272-65			AD9272-80			
Parameter[1]	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
LNA CHARACTERISTICS											
Gain	Single-ended input to differential output		15.6/17.9/21.3			15.6/17.9/21.3			15.6/17.9/21.3		dB
	Single-ended input to single-ended output		9.6/11.9/15.3			9.6/11.9/15.3			9.6/11.9/15.3		dB
Input Voltage Range	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, LNA output limited to 4.4 V p-p differential output		733/550/367			733/550/367			733/550/367		mV p-p SE[2]
Input Common Mode			0.9			0.9			0.9		V
Input Resistance	R_{FB} = 250 Ω		50			50			50		Ω
	R_{FB} = 500 Ω		100			100			100		Ω
	R_{FB} = ∞		15			15			15		kΩ
Input Capacitance	LI-x		22			22			22		pF
−3 dB Bandwidth			100			100			100		MHz
Input-Referred Noise Voltage	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, R_S = 0 Ω, R_{FB} = ∞		0.98/0.86/0.75			0.98/0.86/0.75			0.98/0.86/0.75		nV/√Hz
Input Noise Current	R_{FB} = ∞		1			1			1		pA/√Hz
1 dB Input Compression Point	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, GAIN+ = 0 V		1.0/0.8/0.5			1.0/0.8/0.5			1.0/0.8/0.5		mV p-p
Noise Figure	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB										
Active Termination Matched	R_S = 50 Ω, R_{FB} = 200 Ω/ 250 Ω/350 Ω		4.8/4.1/3.2			4.8/4.1/3.2			4.8/4.0/3.2		dB
Unterminated	R_{FB} = ∞		3.4/2.8/2.3			3.4/2.8/2.3			3.4/2.8/2.3		dB
FULL-CHANNEL (TGC) CHARACTERISTICS											
AAF Low-Pass Filter Cutoff -In Range	−3 dB, programmable		8 to 18			8 to 18			8 to 18		MHz
AAF Low-Pass Filter Cutoff - Out of Range[3]	−3 dB, programmable, AAF Bandwidth Tolerance		5 to 8 and 18 to 35			5 to 8 and 18 to 35			5 to 8 and 18 to 35		MHz
AAF Bandwidth Tolerance -In Range			±10			±10			±10		%

Parameter[1]	Conditions	AD9272-40 Min	AD9272-40 Typ	AD9272-40 Max	AD9272-65 Min	AD9272-65 Typ	AD9272-65 Max	AD9272-80 Min	AD9272-80 Typ	AD9272-80 Max	Unit
Group Delay Variation	f = 1 MHz to 18 MHz, GAIN+ = 0 V to 1.6 V		±2			±2			±2		ns
Input-Referred Noise Voltage	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, R_{FB} = ∞		1.26/1.04/0.85			1.26/1.04/0.85			1.26/1.04/0.85		nV/√Hz
Noise Figure	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB										
Active Termination Matched	R_S = 50 Ω, R_{FB} = 200 Ω/ 250 Ω/350 Ω		8.0/6.6/4.7			7.7/6.2/4.5			7.6/6.1/4.4		dB
Unterminated	R_{FB} = ∞		4.7/3.7/2.8			4.6/3.6/2.8			4.5/3.6/2.7		dB
Correlated Noise Ratio	No signal, correlated/ uncorrelated		−30			−30			−30		dB
Output Offset		−35		+35	−35		+35	−35		+35	LSB
Signal-to-Noise Ratio (SNR)	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		65			64			63		dBFS
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		57			56			54.5		dBFS
Harmonic Distortion											
Second Harmonic	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		−62			−58			−55		dBc
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		−60			−61			−58		dBc
Third Harmonic	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		−71			−60			−60		dBc
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		−57			−55			−56		dBc
Two-Tone IMD3 (2 × F1 − F2) Distortion	f_{IN1} = 5.0 MHz at −1 dBFS, f_{IN2} = 5.01 MHz at −21 dBFS, GAIN+ = 1.6 V, LNA gain = 21.3 dB		−75			−75			−75		dBc
Channel-to-Channel Crosstalk	f_{IN1} = 5.0 MHz at −1 dBFS		−70			−70			−70		dB
	Overrange condition[4]		−65			−65			−65		dB
Channel-to-Channel Delay Variation	Full TGC path, f_{IN} = 5 MHz, GAIN+ = 0 V to 1.6 V		0.3			0.3			0.3		Degrees
PGA GAIN	Differential input to differential output		21/24/27/30			21/24/27/30			21/24/27/30		dB

Parameter[1]	Conditions	AD9272-40 Min	AD9272-40 Typ	AD9272-40 Max	AD9272-65 Min	AD9272-65 Typ	AD9272-65 Max	AD9272-80 Min	AD9272-80 Typ	AD9272-80 Max	Unit
GAIN ACCURACY	25°C										
Gain Law Conformance Error	0 V < GAIN+ < 0.16 V		1.5			1.5			1.5		dB
	0.16 V < GAIN+ < 1.44 V	−1.5		+1.5	−1.5		+1.5	−1.6		+1.6	dB
	1.44 V < GAIN+ < 1.6 V		−2.5			−2.5			−2.5		dB
Linear Gain Error	GAIN+ = 0.8 V, normalized for ideal AAF loss	−1.5		+1.5	−1.5		+1.5	−1.6		+1.6	dB
Channel-to-Channel Matching	0.16 V < GAIN+ < 1.44 V		0.1			0.1			0.1		dB
GAIN CONTROL INTERFACE											
Normal Operating Range		0		1.6	0		1.6	0		1.6	V
Gain Range	GAIN+ = 0 V to 1.6 V		42			42			42		dB
Scale Factor			28.5			28.5			28.5		dB/V
Response Time	42 dB change		750			750			750		ns
Gain+ Impedance	Single-ended		10			10			10		MΩ
Gain− Impedance	Single-ended		70			70			70		kΩ
CW DOPPLER MODE											
Transconductance (differential)	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB		5.4/7.3/10.9			5.4/7.3/10.9			5.4/7.3/10.9		mA/V
Output Level Range (differential)	CW Doppler output pins	1.5		3.6	1.5		3.6	1.5		3.6	V
Input-Referred Noise Voltage	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, R_S = 0 Ω, R_{FB} = ∞, R_L = 675 Ω		2.35/1.82/1.31			2.35/1.82/1.31			2.35/1.82/1.31		nV/√Hz
Input-Referred Dynamic Range	LNA gain = 15.6 dB/ 17.9 dB/ 21.3 dB, R_S = 0 Ω, R_{FB} = ∞		161/161/160			161/161/160			161/161/160		dBFS/√Hz
Two-Tone IMD3 (2 × F1 − F2) Distortion	f_{IN1} = 5.0 MHz at −1 dBFS (FS at LNA input), f_{IN2} = 5.01 MHz at −21 dBFS (FS at LNA input), LNA gain = 21.3 dB		−70			−70			−70		dBc
Output DC Bias (single-ended)	Per channel		2.4			2.4			2.4		mA
Maximum Output Swing (single-ended)	Per channel		±2			±2			±2		mA p-p
POWER SUPPLY											
AVDD1		1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
AVDD2		2.7	3.0	3.6	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD		1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V

Parameter[1]	Conditions	AD9272-40 Min	AD9272-40 Typ	AD9272-40 Max	AD9272-65 Min	AD9272-65 Typ	AD9272-65 Max	AD9272-80 Min	AD9272-80 Typ	AD9272-80 Max	Unit
I_{AVDD1}	Full-channel mode		210			280			335		mA
	CW Doppler mode with four channels enabled		32			32			32		mA
I_{AVDD2}	Full-channel mode		365			365			365		mA
	CW Doppler mode with four channels enabled		140			140			140		mA
I_{DRVDD}			49			51			52		mA
Total Power Dissipation	Includes output drivers, full-channel mode, no signal		1560	1713		1690	1860		1780	1975	mW
	CW Doppler mode with four channels enabled		475			475			475		mW
Power-Down Dissipation				5			5			5	mW
Standby Power Dissipation				175			200			210	mW
Power Supply Rejection Ratio (PSRR)			1.6			1.6			1.6		mV/V
ADC RESOLUTION			12			12			12		Bits
ADC REFERENCE											
Output Voltage Error	VREF = 1 V			±20			±20			±20	mV
Load Regulation	At 1.0 mA, VREF = 1 V		2			2			2		mV
Input Resistance			6			6			6		kΩ

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.
[2] SE = single-ended.
[3] AAF settings < 5 MHz are out of range and not supported.
[4] The overrange condition is specified as being 6 dB more than the full-scale input range.

DIGITAL SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, f_{IN} = 5 MHz, full temperature, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
LOGIC INPUTS (PDWN, STBY, SCLK)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		70		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (SDIO)					
Logic 1 Voltage	Full	1.2		DRVDD + 0.3	V
Logic 0 Voltage	Full	0		0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (DOUTx+, DOUTx–), IN ANSI-644 MODE[1]					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V
Output Coding (Default)			Offset binary		
DIGITAL OUTPUTS (DOUTx+, DOUTx–), WITH LOW POWER, REDUCED SIGNAL OPTION[1]					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	V
Output Coding (Default)			Offset binary		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, f_{IN} = 5 MHz, full temperature, unless otherwise noted.

Table 3.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK[2]					
Clock Rate	Full	10		80	MSPS
Clock Pulse Width High (t_{EH})	Full		6.25		ns
Clock Pulse Width Low (t_{EL})	Full		6.25		ns
OUTPUT PARAMETERS[2, 3]					
Propagation Delay (t_{PD})	Full	(t_{SAMPLE}/2) + 1.5	(t_{SAMPLE}/2) + 2.3	(t_{SAMPLE}/2) + 3.1	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO± Propagation Delay (t_{FCO})	Full	(t_{SAMPLE}/2) + 1.5	(t_{SAMPLE}/2) + 2.3	(t_{SAMPLE}/2) + 3.1	ns
DCO± Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/24)		ns
DCO± to Data Delay (t_{DATA})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
DCO± to FCO± Delay (t_{FRAME})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
Data-to-Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±100	±350	ps
Wake-Up Time (Standby), GAIN+ = 0.8 V	25°C		2		µs
Wake-Up Time (Power-Down)	25°C		1		ms
Pipeline Latency	Full		8		Clock cycles
APERTURE					
Aperture Uncertainty (Jitter)	25°C		<1		ps rms

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.
[2] Can be adjusted via the SPI.
[3] Measurements were made using a part soldered to FR-4 material.
[4] t_{SAMPLE}/24 is based on the number of bits divided by 2 because the delays are based on half duty cycles.

ADC Timing Diagrams

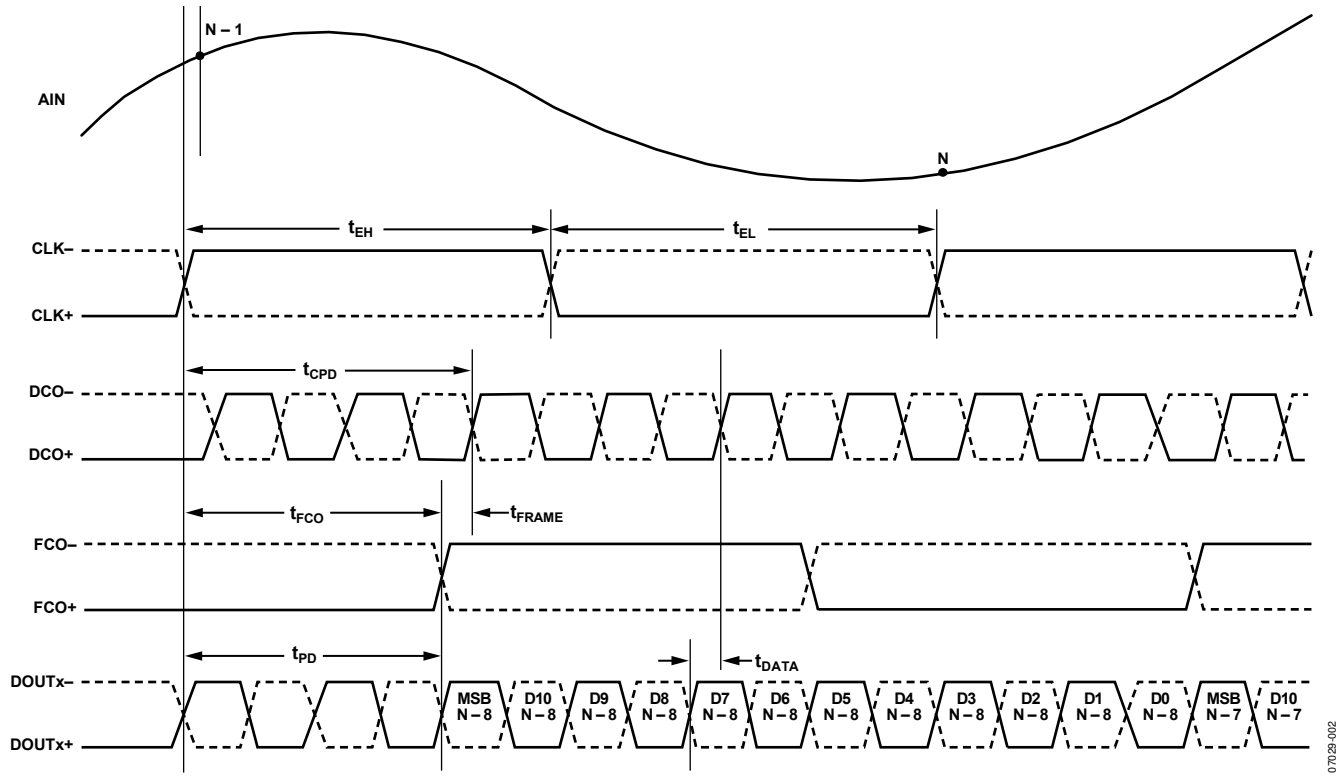


Figure 2. 12-Bit Data Serial Stream (Default)

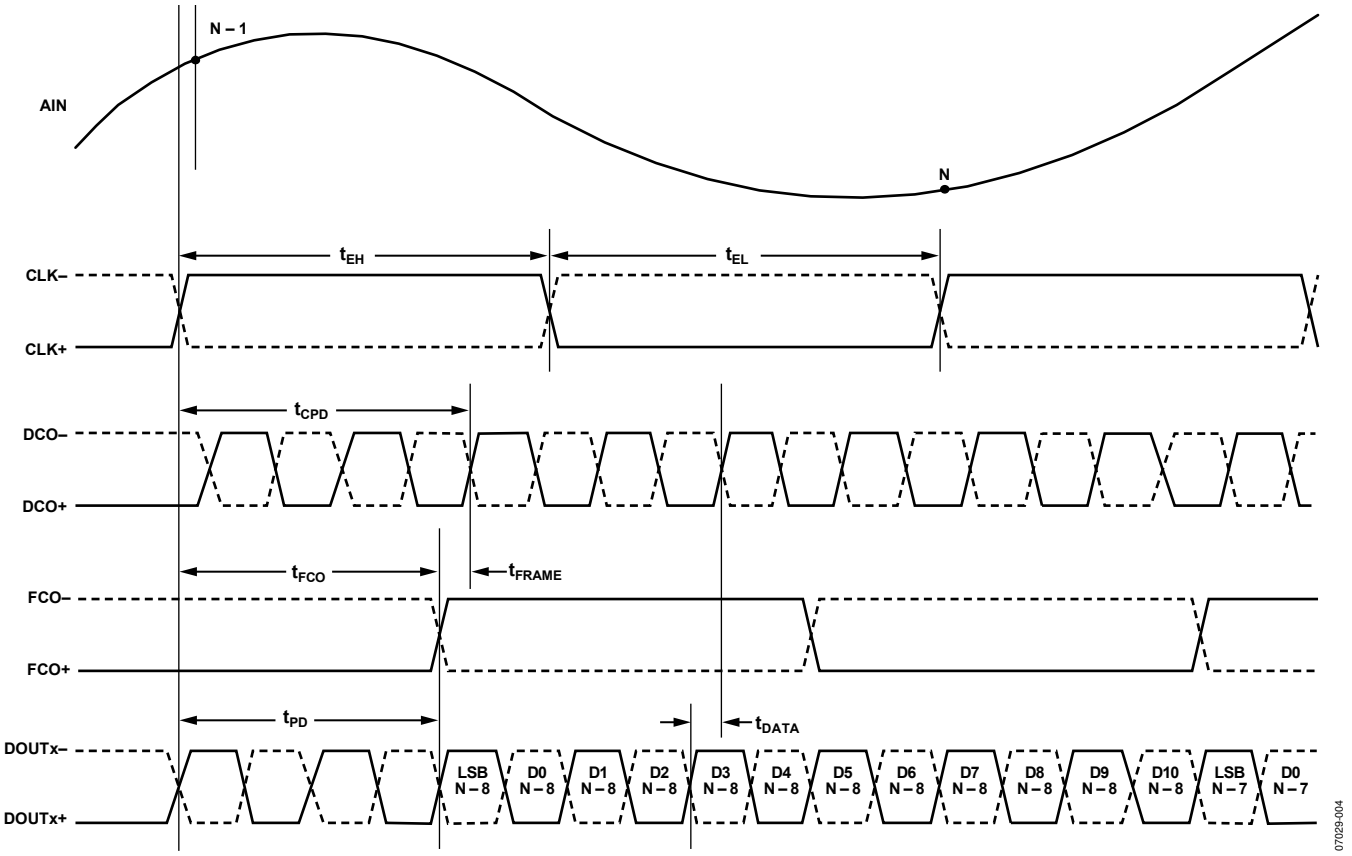


Figure 3. 12-Bit Data Serial Stream, LSB First

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect To	Rating
Electrical		
AVDD1	GND	−0.3 V to +2.0 V
AVDD2	GND	−0.3 V to +3.9 V
DRVDD	GND	−0.3 V to +2.0 V
GND	GND	−0.3 V to +0.3 V
AVDD2	AVDD1	−2.0 V to +3.9 V
AVDD1	DRVDD	−2.0 V to +2.0 V
AVDD2	DRVDD	−2.0 V to +3.9 V
Digital Outputs (DOUTx+, DOUTx−, DCO+, DCO−, FCO+, FCO−)	GND	−0.3 V to +2.0 V
CLK+, CLK−, GAIN+,GAIN−	GND	−0.3 V to +3.9 V
LI-x, LO-x, LOSW-x	LG-x	−0.3 V to +2.0 V
CWDx−, CWDx+	GND	−0.3 V to +3.9 V
	GND	−0.3 V to +2.0 V
PDWN, STBY, SCLK, CSB	GND	−0.3 V to +3.9 V
RBIAS, VREF, SDIO	GND	−0.3 V to +2.0 V
Environmental		
Operating Temperature Range (Ambient)		−40°C to +85°C
Storage Temperature Range (Ambient)		−65°C to +150°C
Maximum Junction Temperature		150°C
Lead Temperature (Soldering, 10 sec)		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE

Table 5.

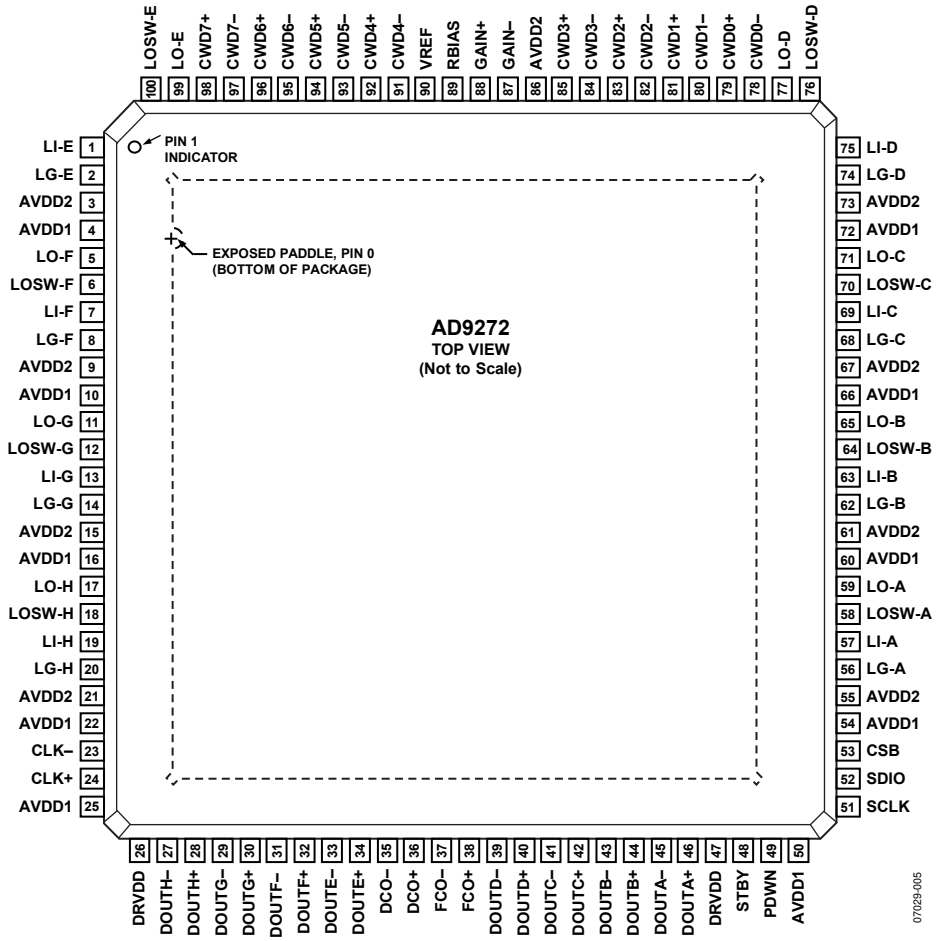
Air Flow Velocity (m/sec)	θ_{JA}[1]	θ_{JB}	θ_{JC}	Unit
0.0	20.3	N/A	N/A	°C/W
1.0	14.4	7.6	4.7	°C/W
2.5	12.9	N/A	N/A	°C/W

[1] θ_{JA} is for a 4-layer PCB with a solid ground plane (simulated). The exposed pad is soldered to the PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD SHOULD BE TIED TO A QUIET ANALOG GROUND.

Figure 4. TQFP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Name	Description
0	GND	Ground (exposed paddle should be tied to a quiet analog ground)
4, 10, 16, 22, 25, 50, 54, 60, 66, 72	AVDD1	1.8 V Analog Supply
3, 9, 15, 21, 55, 61, 67, 73, 86	AVDD2	3.0 V Analog Supply
26, 47	DRVDD	1.8 V Digital Output Driver Supply
1	LI-E	LNA Analog Input for Channel E
2	LG-E	LNA Ground for Channel E
5	LO-F	LNA Analog Inverted Output for Channel F
6	LOSW-F	LNA Analog Switched Output for Channel F
7	LI-F	LNA Analog Input for Channel F
8	LG-F	LNA Ground for Channel F
11	LO-G	LNA Analog Inverted Output for Channel G
12	LOSW-G	LNA Analog Switched Output for Channel G
13	LI-G	LNA Analog Input for Channel G
14	LG-G	LNA Ground for Channel G
17	LO-H	LNA Analog Inverted Output for Channel H
18	LOSW-H	LNA Analog Switched Output for Channel H
19	LI-H	LNA Analog Input for Channel H

Pin No.	Name	Description
20	LG-H	LNA Ground for Channel H
23	CLK–	Clock Input Complement
24	CLK+	Clock Input True
27	DOUTH–	ADC H Digital Output Complement
28	DOUTH+	ADC H Digital Output True
29	DOUTG–	ADC G Digital Output Complement
30	DOUTG+	ADC G Digital Output True
31	DOUTF–	ADC F Digital Output Complement
32	DOUTF+	ADC F Digital Output True
33	DOUTE–	ADC E Digital Output Complement
34	DOUTE+	ADC E Digital Output True
35	DCO–	Digital Clock Output Complement
36	DCO+	Digital Clock Output True
37	FCO–	Frame Clock Digital Output Complement
38	FCO+	Frame Clock Digital Output True
39	DOUTD–	ADC D Digital Output Complement
40	DOUTD+	ADC D Digital Output True
41	DOUTC–	ADC C Digital Output Complement
42	DOUTC+	ADC C Digital Output True
43	DOUTB–	ADC B Digital Output Complement
44	DOUTB+	ADC B Digital Output True
45	DOUTA–	ADC A Digital Output Complement
46	DOUTA+	ADC A Digital Output True
48	STBY	Standby Power-Down
49	PDWN	Full Power-Down
51	SCLK	Serial Clock
52	SDIO	Serial Data Input/Output
53	CSB	Chip Select Bar
56	LG-A	LNA Ground for Channel A
57	LI-A	LNA Analog Input for Channel A
58	LOSW-A	LNA Analog Switched Output for Channel A
59	LO-A	LNA Analog Inverted Output for Channel A
62	LG-B	LNA Ground for Channel B
63	LI-B	LNA Analog Input for Channel B
64	LOSW-B	LNA Analog Switched Output for Channel B
65	LO-B	LNA Analog Inverted Output for Channel B
68	LG-C	LNA Ground for Channel C
69	LI-C	LNA Analog Input for Channel C
70	LOSW-C	LNA Analog Switched Output for Channel C
71	LO-C	LNA Analog Inverted Output for Channel C
74	LG-D	LNA Ground for Channel D
75	LI-D	LNA Analog Input for Channel D
76	LOSW-D	LNA Analog Switched Output for Channel D
77	LO-D	LNA Analog Inverted Output for Channel D
78	CWD0–	CW Doppler Output Complement for Channel 0
79	CWD0+	CW Doppler Output True for Channel 0
80	CWD1–	CW Doppler Output Complement for Channel 1
81	CWD1+	CW Doppler Output True for Channel 1
82	CWD2–	CW Doppler Output Complement for Channel 2
83	CWD2+	CW Doppler Output True for Channel 2
84	CWD3–	CW Doppler Output Complement for Channel 3
85	CWD3+	CW Doppler Output True for Channel 3
87	GAIN–	Gain Control Voltage Input Complement

Pin No.	Name	Description
88	GAIN+	Gain Control Voltage Input True
89	RBIAS	External Resistor to Set the Internal ADC Core Bias Current
90	VREF	Voltage Reference Input/Output
91	CWD4−	CW Doppler Output Complement for Channel 4
92	CWD4+	CW Doppler Output True for Channel 4
93	CWD5−	CW Doppler Output Complement for Channel 5
94	CWD5+	CW Doppler Output True for Channel 5
95	CWD6−	CW Doppler Output Complement for Channel 6
96	CWD6+	CW Doppler Output True for Channel 6
97	CWD7−	CW Doppler Output Complement for Channel 7
98	CWD7+	CW Doppler Output True for Channel 7
99	LO-E	LNA Analog Inverted Output for Channel E
100	LOSW-E	LNA Analog Switched Output for Channel E

TYPICAL PERFORMANCE CHARACTERISTICS

f_{SAMPLE} = 40 MSPS, f_{IN} = 5 MHz, R_S = 50 Ω, LNA gain = 21.3 dB, LNA bias = high, PGA gain = 27 dB, AAF LPF cutoff = f_{SAMPLE}/4.5, HPF = LPF cutoff/20.7 (default), unless otherwise noted.

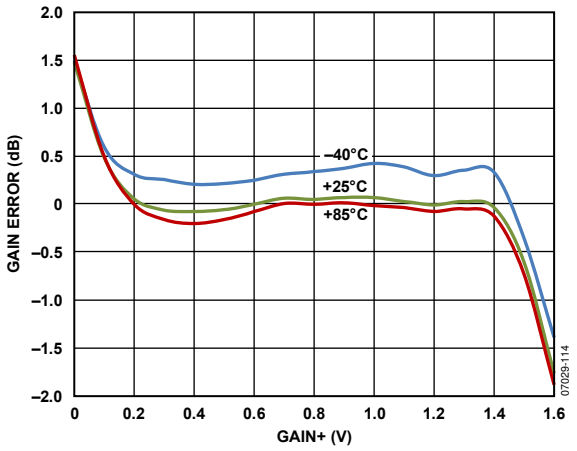


Figure 5. Gain Error vs. GAIN+ at Three Temperatures

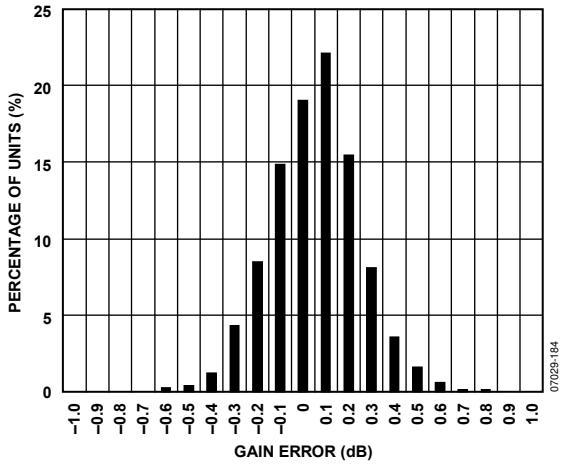


Figure 6. Gain Error Histogram, GAIN+ = 0.16 V

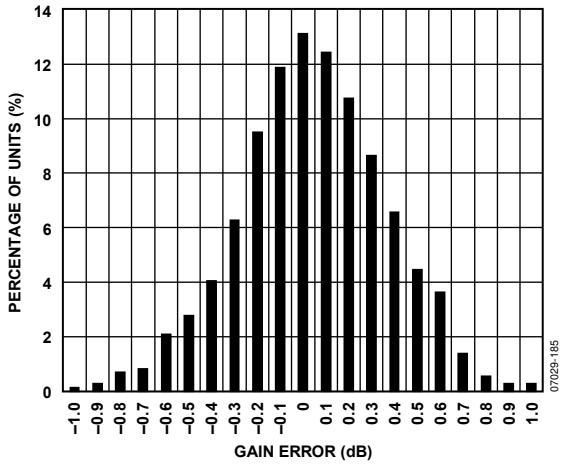


Figure 7. Gain Error Histogram, GAIN+ = 0.8 V

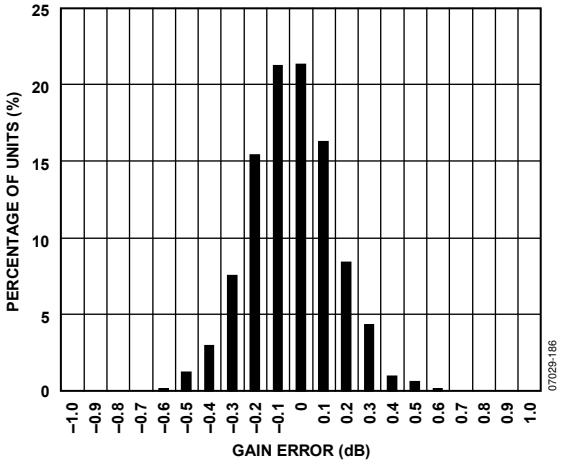


Figure 8. Gain Error Histogram, GAIN+ = 1.44 V

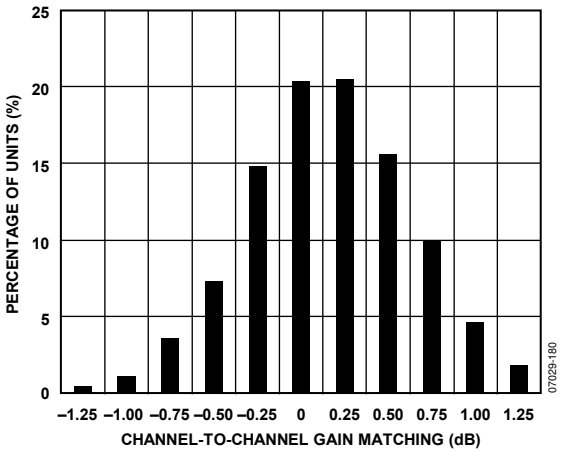


Figure 9. Gain Match Histogram, GAIN+ = 0.3 V

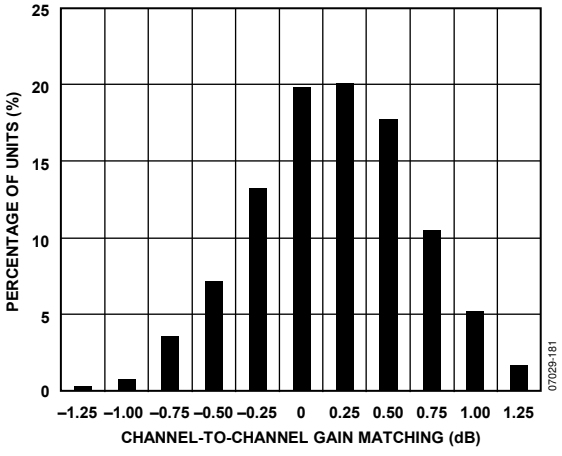


Figure 10. Gain Match Histogram, GAIN+ = 1.3 V

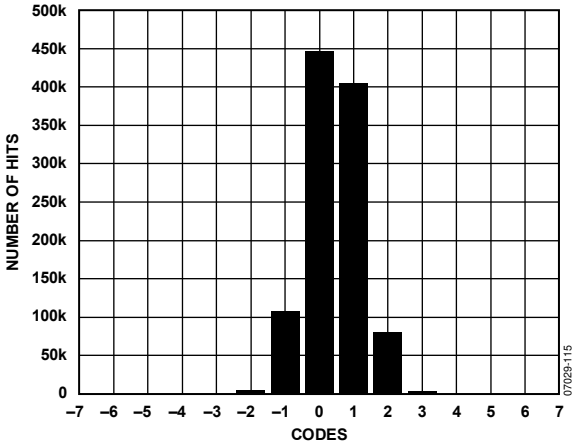


Figure 11. Output-Referred Noise Histogram, GAIN+ = 0 V

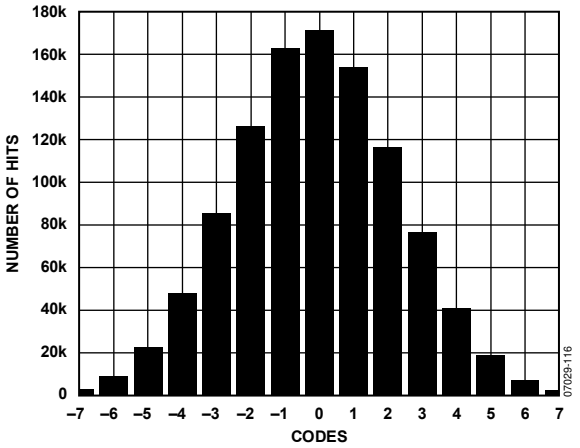


Figure 12. Output-Referred Noise Histogram, GAIN+ = 1.6 V

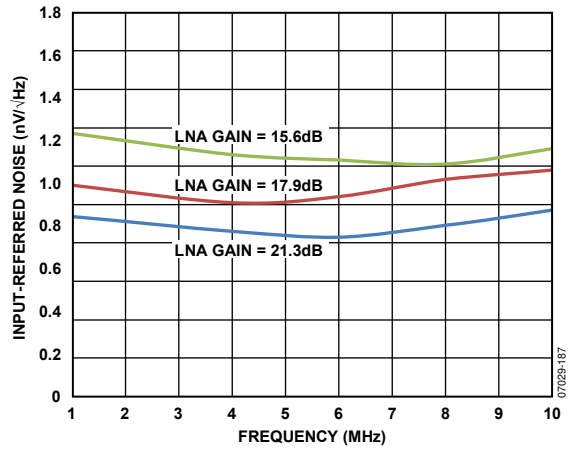


Figure 13. Short-Circuit, Input-Referred Noise vs. Frequency, PGA Gain = 30 dB, GAIN+ = 1.6 V

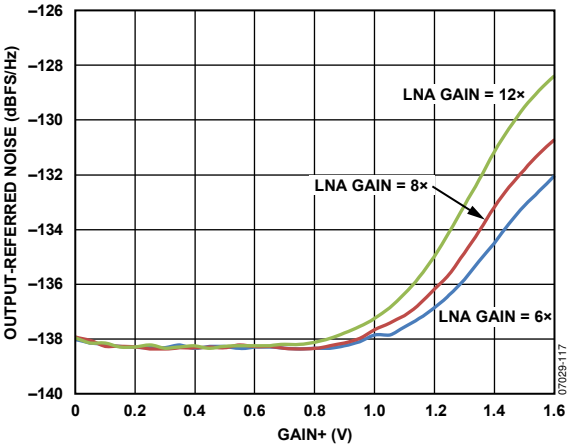


Figure 14. Short-Circuit, Output-Referred Noise vs. GAIN+

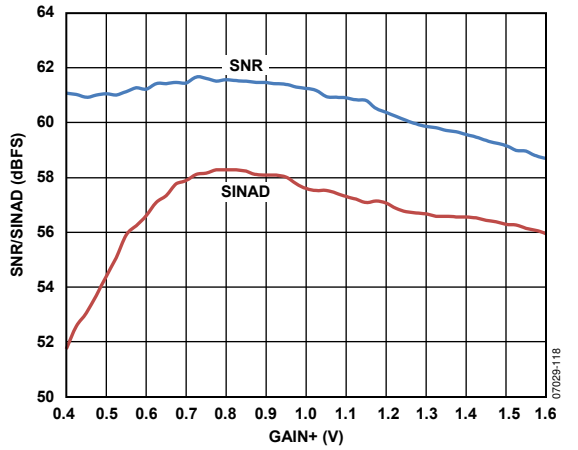


Figure 15. SNR/SINAD vs. GAIN+, AIN = –1 dBFS

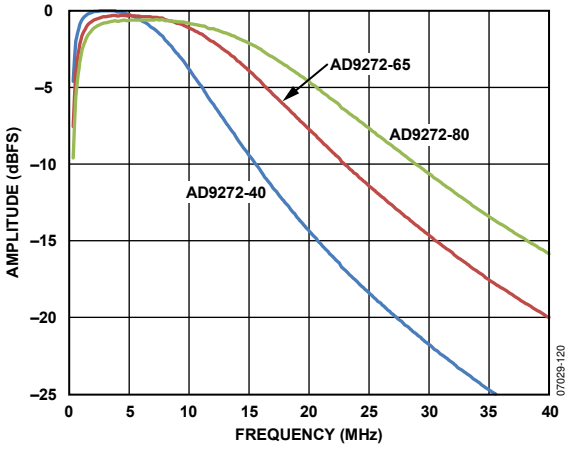


Figure 16. Antialiasing Filter (AAF) Pass-Band Response, LPF Cutoff = 1 × (1/4.5) × f_{SAMPLE}

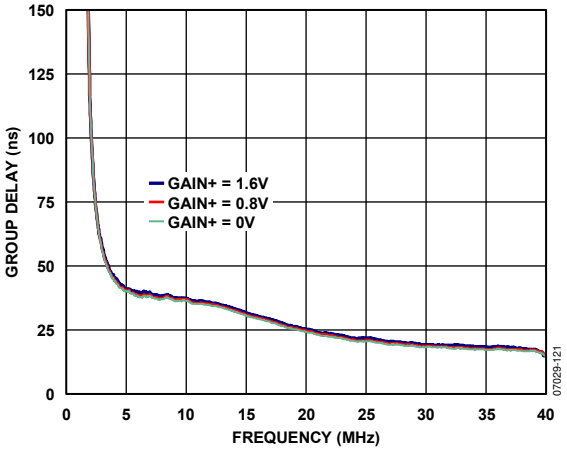


Figure 17. Antialiasing Filter (AAF) Group Delay Response

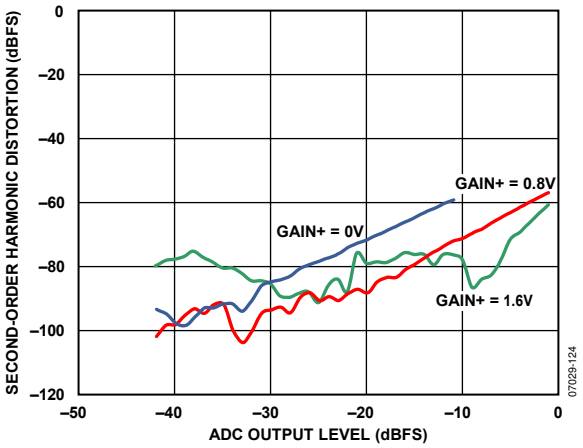


Figure 20. Second-Order Harmonic Distortion vs. ADC Output

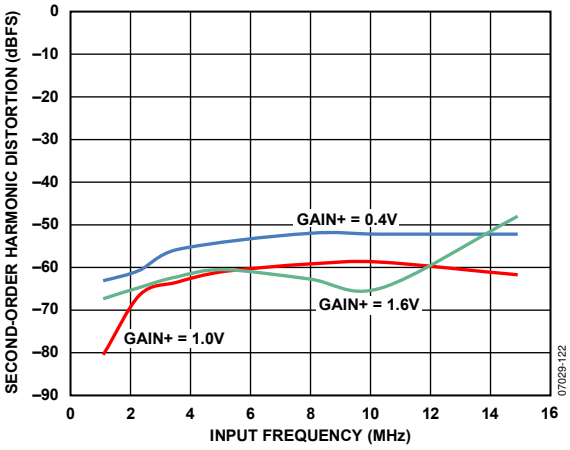


Figure 18. Second-Order Harmonic Distortion vs. Frequency, AIN = −1 dBFS

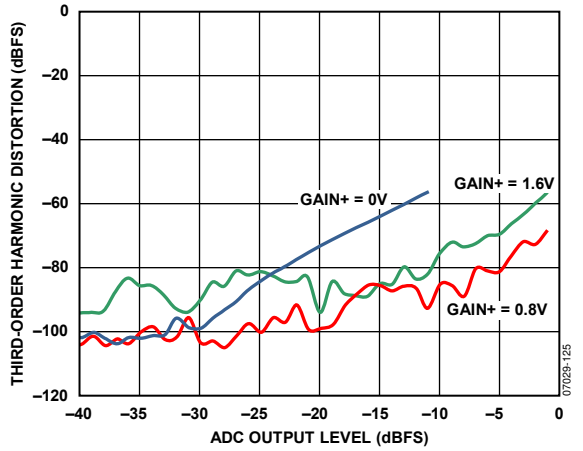


Figure 21. Third-Order Harmonic Distortion vs. ADC Output Level

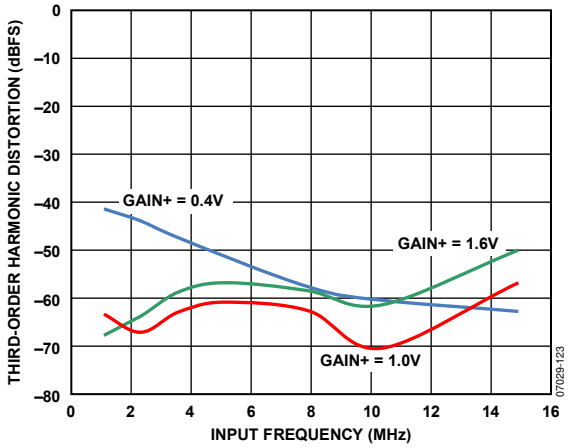


Figure 19. Third-Order Harmonic Distortion vs. Frequency, AIN = −1 dBFS

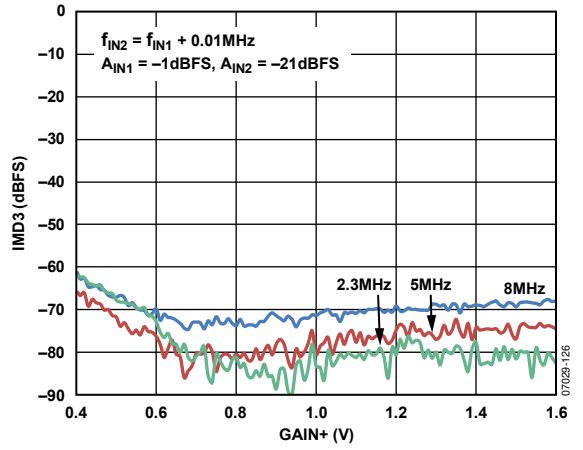


Figure 22. IMD3 vs. GAIN+

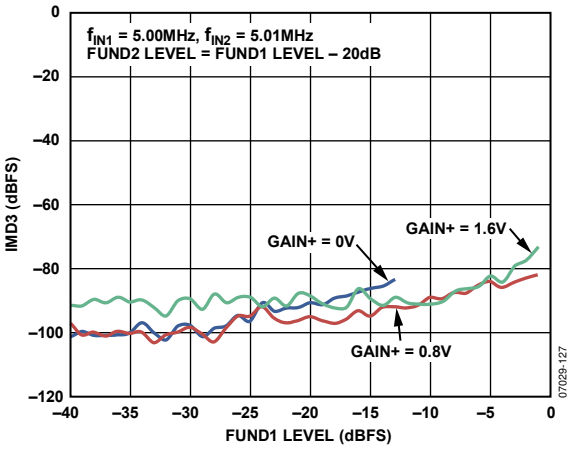


Figure 23. IMD3 vs. Fundamental 1 Amplitude Level

EQUIVALENT CIRCUITS

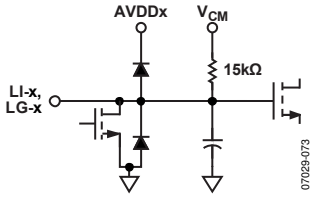


Figure 24. Equivalent LNA Input Circuit

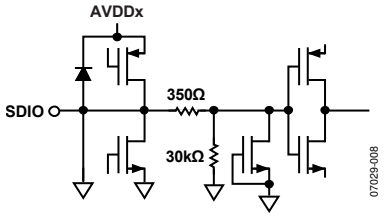


Figure 27. Equivalent SDIO Input Circuit

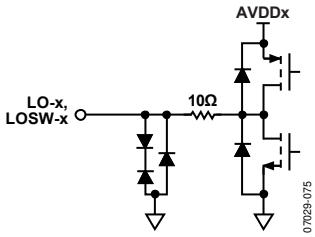


Figure 25. Equivalent LNA Output Circuit

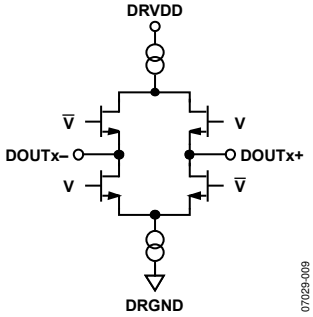


Figure 28. Equivalent Digital Output Circuit

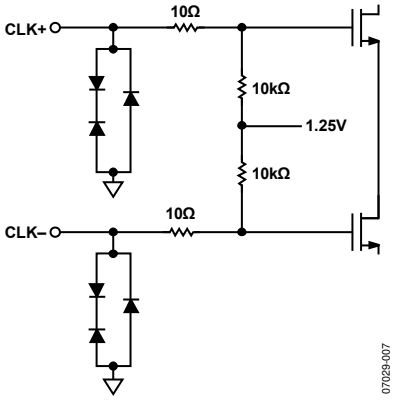


Figure 26. Equivalent Clock Input Circuit

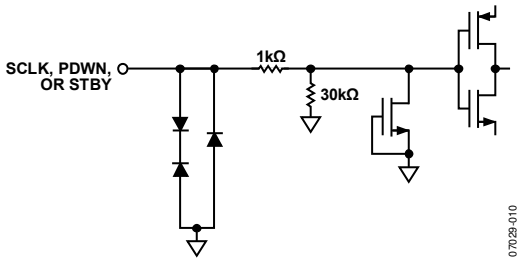


Figure 29. Equivalent SCLK, PDWN, or STBY Input Circuit

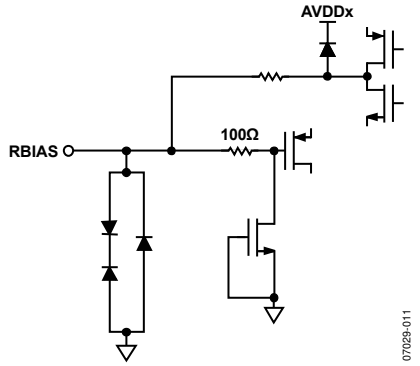


Figure 30. Equivalent RBIAS Circuit

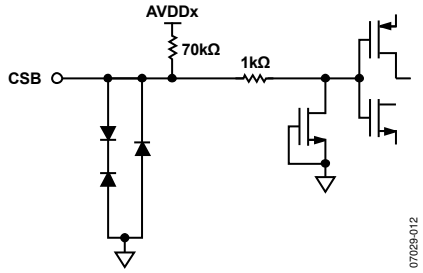


Figure 31. Equivalent CSB Input Circuit

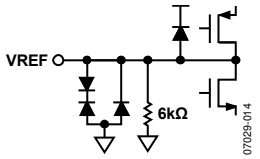


Figure 32. Equivalent VREF Circuit

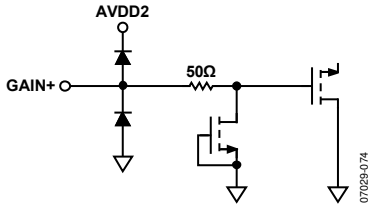


Figure 33. Equivalent GAIN+ Input Circuit

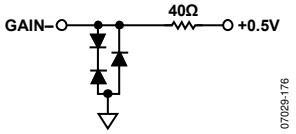


Figure 34. Equivalent GAIN– Input Circuit

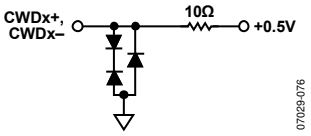


Figure 35. Equivalent CWDx± Output Circuit

THEORY OF OPERATION

ULTRASOUND

The primary application for the AD9272 is medical ultrasound. Figure 36 shows a simplified block diagram of an ultrasound system. A critical function of an ultrasound system is the time gain control (TGC) compensation for physiological signal attenuation. Because the attenuation of ultrasound signals is exponential with respect to distance (time), a linear-in-dB VGA is the optimal solution.

Key requirements in an ultrasound signal chain are very low noise, active input termination, fast overload recovery, low power, and differential drive to an ADC. Because ultrasound machines use beam-forming techniques requiring large binary-weighted numbers (for example, 32 to 512) of channels, using the lowest power at the lowest possible noise is of chief importance.

Most modern machines use digital beam forming. In this technique, the signal is converted to digital format immediately following the TGC amplifier, and then beam forming is accomplished digitally.

The ADC resolution of 12 bits with up to 80 MSPS sampling satisfies the requirements of both general-purpose and high-end systems.

Power conservation and low cost are two of the most important factors in low-end and portable ultrasound machines, and the AD9272 is designed to meet these criteria.

For additional information regarding ultrasound systems, refer to "How Ultrasound System Considerations Influence Front-End Component Choice," *Analog Dialogue*, Volume 36, Number 1, May–July 2002, and "The AD9271—A Revolutionary Solution for Portable Ultrasound," *Analog Dialogue*, Volume 41, Number 3, July 2007.

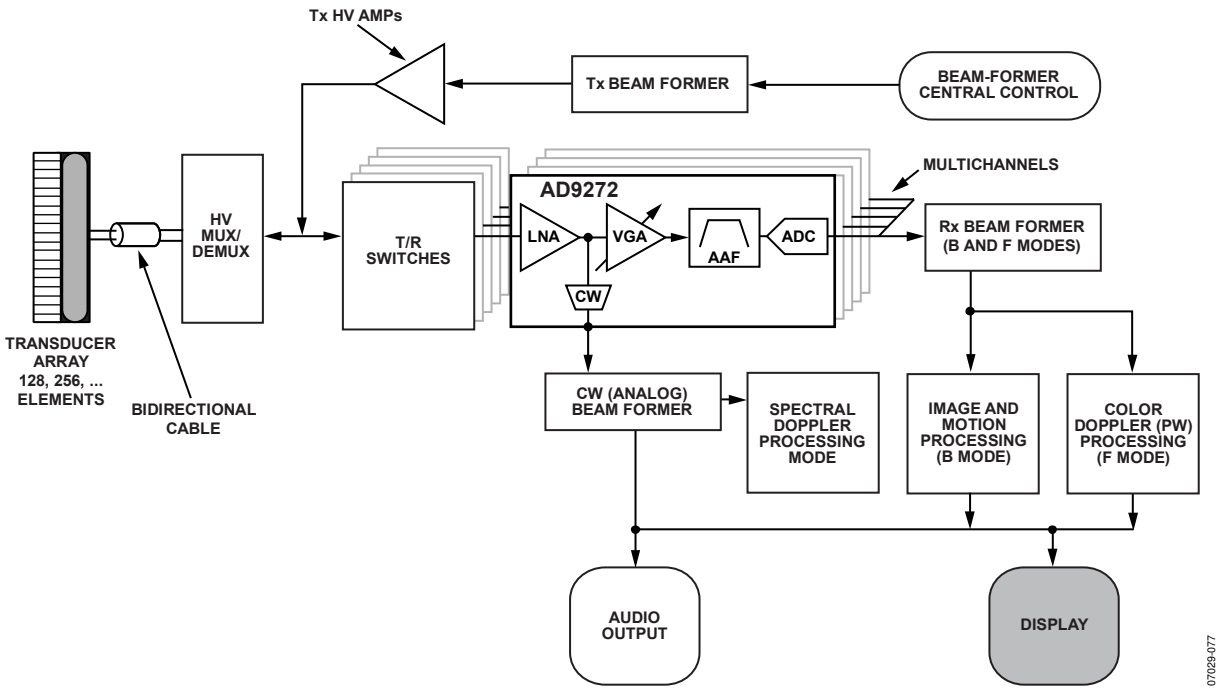


Figure 36. Simplified Ultrasound System Block Diagram

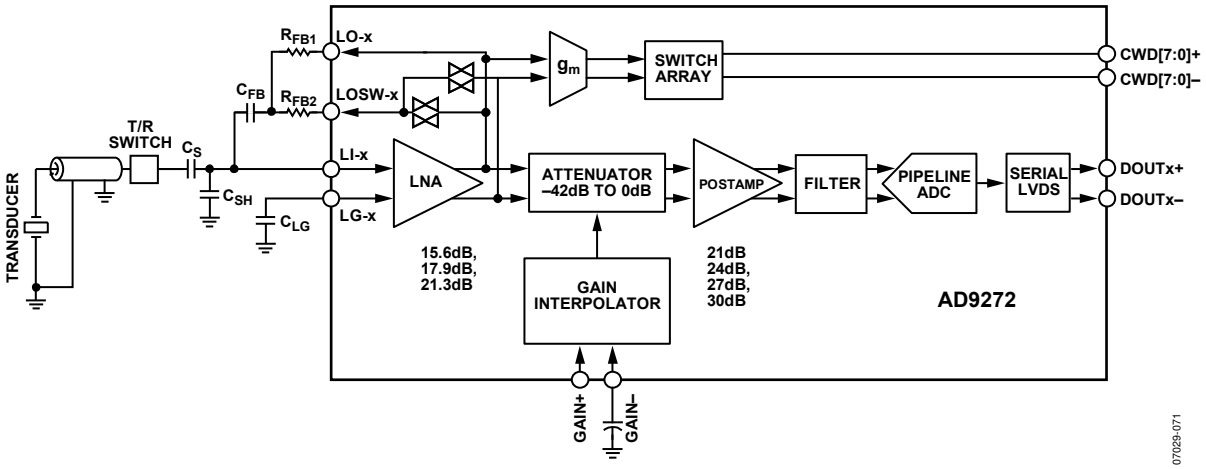


Figure 37. Simplified Block Diagram of a Single Channel

CHANNEL OVERVIEW

Each channel contains both a TGC signal path and a CW Doppler signal path. Common to both signal paths, the LNA provides user-adjustable input impedance termination. The CW Doppler path includes a transconductance amplifier and a crosspoint switch. The TGC path includes a differential X-AMP® VGA, an antialiasing filter, and an ADC. Figure 37 shows a simplified block diagram with external components.

The signal path is fully differential throughout to maximize signal swing and reduce even-order distortion; however, the LNA is designed to be driven from a single-ended signal source.

Low Noise Amplifier (LNA)

Good noise performance relies on a proprietary ultralow noise LNA at the beginning of the signal chain, which minimizes the noise contribution in the following VGA. Active impedance control optimizes noise performance for applications that benefit from input impedance matching.

A simplified schematic of the LNA is shown in Figure 38. LI-x is capacitively coupled to the source. An on-chip bias generator establishes dc input bias voltages of around 0.9 V and centers the output common-mode levels at 1.5 V (AVDD2 divided by 2). A capacitor, C_{LG}, of the same value as the input coupling capacitor, C_S, is connected from the LG-x pin to ground.

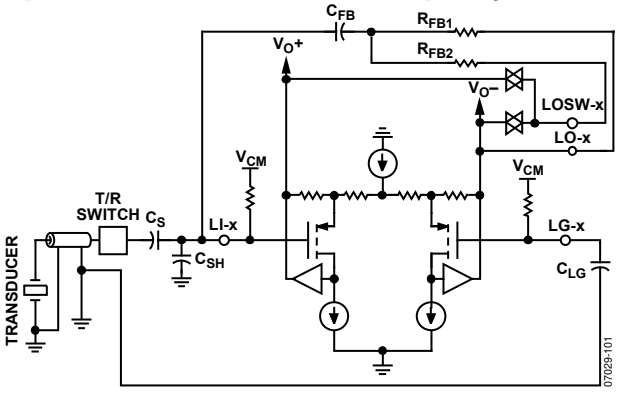


Figure 38. Simplified LNA Schematic

The LNA supports differential output voltages as high as 4.4 V p-p with positive and negative excursions of ±1.1 V from a common-mode voltage of 1.5 V. The LNA differential gain sets the maximum input signal before saturation. One of three gains is set through the SPI. The corresponding full-scale input for the gain settings of 6, 8, and 12 is 733 mV p-p, 550 mV p-p, and 367 mV p-p, respectively. Overload protection ensures quick recovery time from large input voltages. Because the inputs are capacitively coupled to a bias voltage near midsupply, very large inputs can be handled without interacting with the ESD protection.

Low value feedback resistors and the current-driving capability of the output stage allow the LNA to achieve a low input-referred noise voltage of 0.75 nV/√Hz (at a gain of 21.3 dB). This is achieved with a current consumption of only 27 mA per channel (80 mW). On-chip resistor matching results in precise single-ended gains, which are critical for accurate impedance control. The use of a fully differential topology and negative feedback minimizes distortion. Low second-order harmonic distortion is particularly important in second harmonic ultrasound imaging applications. Differential signaling enables smaller swings at each output, further reducing third-order distortion.

Recommendation

It is highly recommended that the LG-x pins form a Kelvin type connection to the input or probe connection ground. Simply connecting the LG pin to ground near the device can allow differences in potential to be amplified through the LNA. This generally shows up as a dc offset voltage that can vary from channel to channel and part to part given the application and layout of the PCB (see Figure 38).

Active Impedance Matching

The LNA consists of a single-ended voltage gain amplifier with differential outputs, and the negative output is externally available. For example, with a fixed gain of 8× (17.9 dB), an active input termination is synthesized by connecting a feedback resistor between the negative output pin, LO-x, and the positive input pin, LI-x. This is a well known technique used for interfacing multiple probe impedances to a single system. The input resistance is shown in Equation 1.

$$R_{IN} = \frac{R_{FB}}{(1+\frac{A}{2})} \quad (1)$$

where $A/2$ is the single-ended gain or the gain from the LI-x inputs to the LO-x outputs, and R_{FB} is the resulting impedance of the R_{FB1} and R_{FB2} combination (see Figure 38).

Because the amplifier has a gain of 8× from its input to its differential output, it is important to note that the gain A/2 is the gain from Pin LI-x to Pin LO-x, and it is 6 dB less than the gain of the amplifier or 12.1 dB (4×). The input resistance is reduced by an internal bias resistor of 15 kΩ in parallel with the source resistance connected to Pin LI-x, with Pin LG-x ac grounded. Equation 2 can be used to calculate the needed R_{FB} for a desired R_{IN}, even for higher values of R_{IN}.

$$R_{IN} = \frac{R_{FB}}{(1+3)} \| 15\,\text{k}\Omega \quad (2)$$

For example, to set R_{IN} to 200 Ω, the value of R_{FB} must be 1000 Ω. If the simplified equation (Equation 2) is used to calculate R_{IN}, the value is 188 Ω, resulting in a gain error less than 0.6 dB. Some factors, such as the presence of a dynamic source resistance, might influence the absolute gain accuracy more significantly. At higher frequencies, the input capacitance of the LNA must be considered. The user must determine the level of matching accuracy and adjust R_{FB} accordingly.

The bandwidth (BW) of the LNA is greater than 100 MHz. Ultimately, the BW of the LNA limits the accuracy of the synthesized R_{IN}. For $R_{IN} = R_S$ up to about 200 Ω, the best match is between 100 kHz and 10 MHz, where the lower frequency limit is determined by the size of the ac-coupling capacitors, and the upper limit is determined by the LNA BW. Furthermore, the input capacitance and R_S limit the BW at higher frequencies. Figure 39 shows R_{IN} vs. frequency for various values of R_{FB}.

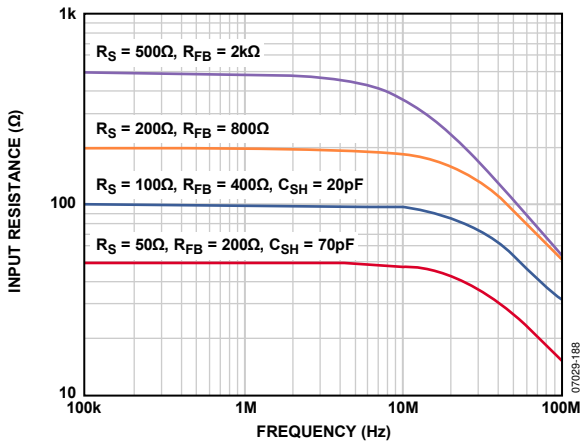


Figure 39. R_{IN} vs. Frequency for Various Values of R_{FB} (Effects of R_S and C_{SH} Are Also Shown)

Note that at the lowest value (50 Ω), R_{IN} peaks at frequencies greater than 10 MHz. This is due to the BW roll-off of the LNA, as mentioned previously.

However, as can be seen for larger R_{IN} values, parasitic capacitance starts rolling off the signal BW before the LNA can produce peaking. C_{SH} further degrades the match; therefore, C_{SH} should not be used for values of R_{IN} that are greater than 100 Ω. Table 7 lists the recommended values for R_{FB} and C_{SH} in terms of R_{IN}.

C_{FB} is needed in series with R_{FB} because the dc levels at Pin LO-x and Pin LI-x are unequal.

Table 7. Active Termination External Component Values

LNA Gain (dB)	R_{IN} (Ω)	R_{FB} (Ω)	Minimum C_{SH} (pF)	BW (MHz)
15.6	50	200	90	57
17.9	50	250	70	69
21.3	50	350	50	88
15.6	100	400	30	57
17.9	100	500	20	69
21.3	100	700	10	88
15.6	200	800	N/A	72
17.9	200	1000	N/A	72
21.3	200	1400	N/A	72

LNA Noise

The short-circuit noise voltage (input-referred noise) is an important limit on system performance. The short-circuit input-referred noise voltage for the LNA is 0.85 nV/√Hz at a gain of 21.3 dB, including the VGA noise at a VGA postamp gain of 27 dB. These measurements, which were taken without a feedback resistor, provide the basis for calculating the input noise and noise figure (NF) performance of the configurations shown in Figure 40.

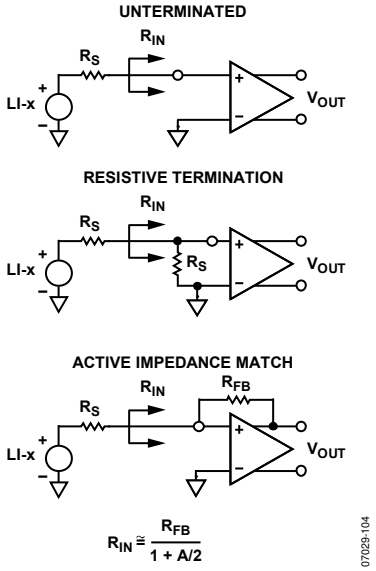


Figure 40. Input Configurations

Figure 41 and Figure 42 are simulations of noise figure vs. R_S results using these configurations and an input-referred noise voltage of 3.8 nV/√Hz for the VGA. Unterminated ($R_{FB} = \infty$) operation exhibits the lowest equivalent input noise and noise figure. Figure 42 shows the noise figure vs. source resistance rising at low R_S—where the LNA voltage noise is large compared with the source noise—and at high R_S due to the noise contribution from R_{FB}. The lowest NF is achieved when R_S matches R_{IN}.

The main purpose of input impedance matching is to improve the transient response of the system. With resistive termination, the input noise increases due to the thermal noise of the matching resistor and the increased contribution of the input voltage noise generator of the LNA. With active impedance matching, however, the contributions of both are smaller (by a factor of 1/(1 + *LNA Gain*)) than they would be for resistive termination.

Figure 41 shows the relative noise figure performance. In this graph, the input impedance was swept with R_S to preserve the match at each point. The noise figures for a source impedance of 50 Ω are 7.3 dB, 4.2 dB, and 2.8 dB for the resistive termination, active termination, and unterminated configurations, respectively. The noise figures for 200 Ω are 4.5 dB, 1.7 dB, and 1 dB, respectively.

Figure 42 shows the noise figure as it relates to R_S for various values of R_{IN}, which is helpful for design purposes.

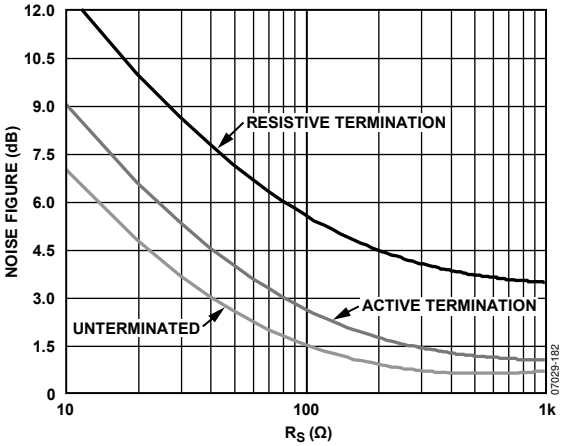


Figure 41. Noise Figure vs. R_S for Resistive Termination, Active Termination Matched, and Unterminated Inputs, V_{GAIN} = 0.8 V

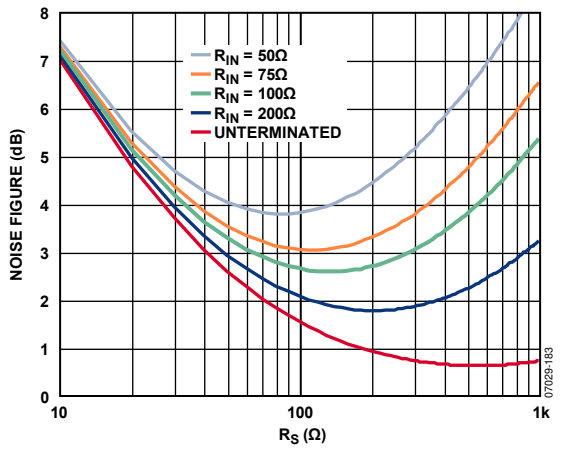


Figure 42. Noise Figure vs. R_S for Various Fixed Values of R_{IN}, Active Termination Matched Inputs, V_{GAIN} = 0.8 V