Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Octal LNA/VGA/AAF/12-Bit ADC and CW I/Q Demodulator

AD9276

FEATURES

8 channels of LNA, VGA, AAF, ADC, and I/Q demodulator
Low noise preamplifier (LNA)
- **Input-referred noise: 0.75 nV/√Hz typical at 5 MHz (gain = 21.3 dB)**
- **SPI-programmable gain: 15.6 dB/17.9 dB/21.3 dB**
- **Single-ended input: V_{IN} maximum = 733 mV p-p/550 mV p-p/367 mV p-p**
- **Dual-mode active input impedance matching**
- **Bandwidth (BW) > 100 MHz**
- **Full-scale (FS) output: 4.4 V p-p differential**

Variable gain amplifier (VGA)
- **Attenuator range: −42 dB to 0 dB**
- **Postamp gain: 21 dB/24 dB/27 dB/30 dB**
- **Linear-in-dB gain control**

Antialiasing filter (AAF)
- **Programmable second-order LPF from 8 MHz to 18 MHz**
- **Programmable HPF**

Analog-to-digital converter (ADC)
- **12 bits at 10 MSPS to 80 MSPS**
- **SNR: 70 dB**
- **SFDR: 75 dB**
- **Serial LVDS (ANSI-644, IEEE 1596.3 reduced range link)**
- **Data and frame clock outputs**

CW mode I/Q demodulator
- **Individual programmable phase rotation**
- **Output dynamic range per channel >160 dBFS/√Hz**

Low power: 195 mW per channel at 12 bits/40 MSPS (TGC), 94 mW per channel for CW Doppler
Flexible power-down modes
Overload recovery in <10 ns
Fast recovery from low power standby mode: <2 µs
100-lead TQFP_EP

APPLICATIONS

Medical imaging/ultrasound
Automotive radar

PRODUCT HIGHLIGHTS

1. Small Footprint.
   Eight channels are contained in a small, space-saving package. Full TGC path, ADC, and I/Q demodulator contained within a 100-lead, 16 mm × 16 mm TQFP.
2. Low Power.
   In TGC mode, low power of 195 mW per channel at 40 MSPS. In CW mode, ultralow power of 94 mW per channel.
3. Integrated High Dynamic Range I/Q Demodulator with Phase Rotation.
4. Ease of Use.
   A data clock output (DCO±) operates up to 480 MHz and supports double data rate (DDR) operation.
5. User Flexibility.
   Serial port interface (SPI) control offers a wide range of flexible features to meet specific system requirements.
6. Integrated Second-Order Antialiasing Filter.
   This filter is placed before the ADC and is programmable from 8 MHz to 18 MHz.

FUNCTIONAL BLOCK DIAGRAM

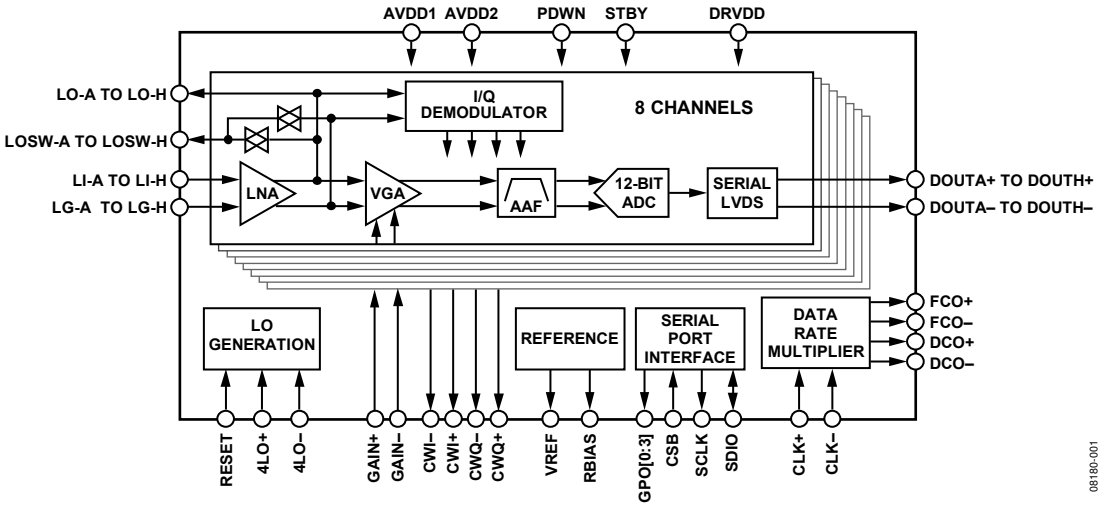


Figure 1.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

AD9276* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9276 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9276: Octal LNA/VGA/AAF/12-Bit ADC and CW I/Q Demodulator Data Sheet

User Guides

- UG-016: Evaluation Board User Guide

TOOLS AND SIMULATIONS

- Visual Analog
- AD9276 IBIS Models

REFERENCE MATERIALS

Press

- Industry's First Octal Ultrasound Receiver with Digital I/Q Demodulator and Decimation Filter Reduces Processor Overhead in Ultrasound Systems

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9276 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9276 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

7/09—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9276 is designed for low cost, low power, small size, and ease of use. It contains eight channels of a variable gain amplifier (VGA) with a low noise preamplifier (LNA); an anti-aliasing filter (AAF); a 12-bit, 10 MSPS to 80 MSPS analog-to-digital converter (ADC); and an I/Q demodulator with programmable phase rotation.

Each channel features a variable gain range of 42 dB, a fully differential signal path, an active input preamplifier termination, a maximum gain of up to 52 dB, and an ADC with a conversion rate of up to 80 MSPS. The channel is optimized for dynamic performance and low power in applications where a small package size is critical.

The LNA has a single-ended-to-differential gain that is selectable through the SPI. The LNA input noise is typically 0.75 nV/√Hz at a gain of 21.3 dB, and the combined input-referred noise of the entire channel is 0.85 nV/√Hz at maximum gain. Assuming a 15 MHz noise bandwidth (NBW) and a 21.3 dB LNA gain, the input SNR is roughly 92 dB. In CW Doppler mode, each LNA output drives an I/Q demodulator. Each demodulator has independently programmable phase rotation through the SPI with 16 phase settings.

The AD9276 requires a LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock (DCO±) for capturing data on the output and a frame clock (FCO±) trigger for signaling a new output byte are provided.

Powering down individual channels is supported to increase battery life for portable applications. A standby mode option allows quick power-up for power cycling. In CW Doppler operation, the VGA, AAF, and ADC are powered down. The power of the TGC path scales with selectable ADC speed power modes.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable clock, data alignment, and programmable digital test pattern generation. The digital test patterns include built-in fixed patterns, built-in pseudo-random patterns, and custom user-defined test patterns entered via the serial port interface.

Fabricated in an advanced CMOS process, the AD9276 is available in a 16 mm × 16 mm, RoHS compliant, 100-lead TQFP. It is specified over the industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, f_{IN} = 5 MHz, R_S = 50 Ω, LNA gain = 21.3 dB, LNA bias = high, PGA gain = 27 dB, GAIN− = 0.8 V, AAF LPF cutoff = f_{SAMPLE}/3 (Mode I/Mode II), f_{SAMPLE}/4.5 (Mode III), HPF cutoff = LPF cutoff/20.7 (default), Mode I = f_{SAMPLE} = 40 MSPS, Mode II = f_{SAMPLE} = 65 MSPS, Mode III = f_{SAMPLE} = 80 MSPS, full temperature, ANSI-644 LVDS mode, unless otherwise noted.

Table 1.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
LNA CHARACTERISTICS					
Gain	Single-ended input to differential output		15.6/17.9/21.3		dB
	Single-ended input to single-ended output		9.6/11.9/15.3		dB
Input Voltage Range (Single-Ended)	LNA output limited to 4.4 V p-p differential output				
	LNA gain = 15.6 dB		733		mV p-p
	LNA gain = 17.9 dB		550		mV p-p
	LNA gain = 21.3 dB		367		mV p-p
Input Common Mode (LI-x, LG-x)			1.0		V
Output Common Mode (LO-x)			1.5		V
Output Common Mode (LOSW-x)	Switch off		High-Z		Ω
	Switch on		1.5		V
Input Resistance (LI-x)	R_{FB} = 250 Ω		50		Ω
	R_{FB} = 500 Ω		100		Ω
	R_{FB} = ∞		15		kΩ
Input Capacitance (LI-x)			22		pF
−3 dB Bandwidth			100		MHz
Input Noise Voltage	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		0.98		nV/√Hz
	LNA gain = 17.9 dB		0.86		nV/√Hz
	LNA gain = 21.3 dB		0.75		nV/√Hz
Input Noise Current	R_{FB} = ∞		1		pA/√Hz
1 dB Input Compression Point	GAIN+ = 0 V				
	LNA gain = 15.6 dB		1.0		V p-p
	LNA gain = 17.9 dB		0.8		V p-p
	LNA gain = 21.3 dB		0.5		V p-p
Noise Figure	R_S = 50 Ω				
Active Termination Matched	LNA gain = 15.6 dB, R_{FB} = 200 Ω		4.8		dB
	LNA gain = 17.9 dB, R_{FB} = 250 Ω		4.1		dB
	LNA gain = 21.3 dB, R_{FB} = 350 Ω		3.2		dB
Unterminated	LNA gain = 15.6 dB, R_{FB} = ∞		3.4		dB
	LNA gain = 17.9 dB, R_{FB} = ∞		2.8		dB
	LNA gain = 21.3 dB, R_{FB} = ∞		2.3		dB
FULL-CHANNEL (TGC) CHARACTERISTICS					
AAF Low-Pass Cutoff					
In Range	−3 dB, programmable	8		18	MHz
In Range AAF Bandwidth Tolerance			±10		%
Group Delay Variation	f = 1 MHz to 18 MHz, GAIN+ = 0 V to 1.6 V		±0.5		ns
Input-Referred Noise Voltage	GAIN+ = 1.6 V, R_{FB} = ∞				
	LNA gain = 15.6 dB		1.26		nV/√Hz
	LNA gain = 17.9 dB		1.04		nV/√Hz
	LNA gain = 21.3 dB		0.85		nV/√Hz

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Noise Figure	GAIN+ = 1.6 V, R_S = 50 Ω				
Active Termination Matched Mode I/Mode II/Mode III	LNA gain = 15.6 dB, R_{FB} = 200 Ω		8.0/7.7/7.6		dB
	LNA gain = 17.9 dB, R_{FB} = 250 Ω		6.6/6.2/6.1		dB
	LNA gain = 21.3 dB, R_{FB} = 350 Ω		4.7/4.5/4.4		dB
Unterminated	LNA gain = 15.6 dB, R_{FB} = ∞		4.7		dB
	LNA gain = 17.9 dB, R_{FB} = ∞		3.7		dB
	LNA gain = 21.3 dB, R_{FB} = ∞		2.8		dB
Correlated Noise Ratio	No signal, correlated/uncorrelated		−30		dB
Output Offset		−35		+35	LSB
Signal-to-Noise Ratio (SNR) Mode I/Mode II/Mode III	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		65/64/63		dBFS
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		57/56/54.5		dBFS
Harmonic Distortion Mode I/Mode II/Mode III					
Second Harmonic	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		−62/−58/−55		dBc
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		−60/−61/−58		dBc
Third Harmonic	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		−71/−60/−60		dBc
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		−57/−55/−56		dBc
Two-Tone Intermodulation (IMD3)	f_{RF1} = 5.015 MHz, f_{RF2} = 5.020 MHz, A_{RF1} = 0 dB, A_{RF2} = −20 dB, GAIN+ = 1.6 V, IMD3 relative to A_{RF2}		−55		dBc
Channel-to-Channel Crosstalk	f_{IN} = 5 MHz at −1 dBFS		−70		dB
	Overrange condition[2]		−65		dB
Channel-to-Channel Delay Variation	Full TGC path, f_{IN} = 5 MHz, GAIN+ = 0 V to 1.6 V		0.3		Degrees
PGA Gain	Differential input to differential output		21/24/27/30		dB
GAIN ACCURACY	25°C				
Gain Law Conformance Error Mode I/Mode II/Mode III	0 < GAIN+ < 0.16 V		1.5		dB
	0.16 V < GAIN+ < 1.44 V	−1.5/−1.5/−1.6		+1.5/+1.5/+1.6	dB
	1.44 V < GAIN+ < 1.6 V	−1.5/−1.5/−1.6	−2.5	+1.5/+1.5/+1.6	dB
Linear Gain Error	GAIN+ = 0.8 V, normalized for ideal AAF loss	−1.5		+1.5	dB
Channel-to-Channel Matching	0.16 V < GAIN+ < 1.44 V		0.1		dB
GAIN CONTROL INTERFACE					
Normal Operating Range		0		1.6	V
Gain Range	GAIN+ = 0 V to 1.6 V	−42		0	dB
Scale Factor			28.5		dB/V
Response Time	42 dB change		750		ns
GAIN+ Impedance	Single-ended		10		MΩ
GAIN− Impedance	Single-ended		70		kΩ
CW DOPPLER MODE					
LO Frequency	$f_{LO} = f_{4LO}/4$	1		10	MHz
Phase Increment	Per channel		22.5		Degrees
Output DC Bias (Single-Ended)	CWI+, CWI−, CWQ+, CWQ−		1.5		V
Maximum Output Swing	Per CWI+, CWI−, CWQ+, CWQ−, per channel enabled			±1.25	mA
Transconductance (Differential)	Demodulated I_{OUT}/V_{IN}, each I or Q output				
	LNA gain = 15.6 dB		1.8		mA/V
	LNA gain = 17.9 dB		2.4		mA/V
	LNA gain = 21.3 dB		3.5		mA/V

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Input-Referred Noise Voltage	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		1.5		nV/√Hz
	LNA gain = 17.9 dB		1.4		nV/√Hz
	LNA gain = 21.3 dB		1.3		nV/√Hz
Noise Figure	R_S = 50 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		5.7		dB
	LNA gain = 17.9 dB		5.3		dB
	LNA gain = 21.3 dB		4.8		dB
Input-Referred Dynamic Range	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		164		dBFS/√Hz
	LNA gain = 17.9 dB		162		dBFS/√Hz
	LNA gain = 21.3 dB		160		dBFS/√Hz
Output-Referred SNR	−3 dBFS input, f_{RF} = 2.5 MHz, f_{4LO} = 10 MHz, 1 kHz offset		155		dBc/√Hz
Two-Tone Intermodulation (IMD3)	f_{RF1} = 5.015 MHz, f_{RF2} = 5.020 MHz, f_{4LO} = 20 MHz, A_{RF1} = 0 dB, A_{RF2} = −20 dB, IMD3 relative to A_{RF2}		−58		dB
Quadrature Phase Error	I to Q, all phases, 1 σ		0.15		Degrees
I/Q Amplitude Imbalance	I to Q, all phases, 1 σ		0.015		dB
Channel-to-Channel Matching	Phase I to I, Q to Q, 1 σ		0.5		Degrees
	Amplitude I to I, Q to Q, 1 σ		0.25		dB
POWER SUPPLY					
Mode I/Mode II/Mode III					
AVDD1		1.7	1.8	1.9	V
AVDD2		2.7	3.0	3.6	V
DRVDD		1.7	1.8	1.9	V
I_{AVDD1}	TGC mode		190/263/317		mA
	CW Doppler mode		15		mA
I_{AVDD2}	TGC mode, no signal		365		mA
	CW Doppler mode per channel enabled, no signal		30		mA
I_{DRVDD}			49/51/52		mA
Total Power Dissipation (Including Output Drivers)	TGC mode, no signal		1560/1690/1780	1800/1940/2050	mW
	CW Doppler mode with eight channels enabled, no signal		750		mW
Power-Down Dissipation				5	mW
Standby Power Dissipation				175/200/210	mW
Power Supply Rejection Ratio (PSRR)			1.6		mV/V
ADC RESOLUTION			12		Bits
ADC REFERENCE					
Output Voltage Error	VREF = 1 V			±20	mV
Load Regulation at 1.0 mA	VREF = 1 V		2		mV
Input Resistance			6		kΩ

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.

[2] The overrange condition is specified as being 6 dB more than the full-scale input range.

DIGITAL SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, f_{IN} = 5 MHz, full temperature, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
CW 4LO INPUTS (4LO+, 4LO–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
LOGIC INPUTS (PDWN, STBY, SCLK, RESET)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		70		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (SDIO)					
Logic 1 Voltage	Full	1.2		DRVDD + 0.3	V
Logic 0 Voltage	Full	0		0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (DOUTx+, DOUTx–), (ANSI-644)[1]					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V
Output Coding (Default)			Offset binary		
DIGITAL OUTPUTS (DOUTx+, DOUTx–), (LOW POWER, REDUCED SIGNAL OPTION)[1]					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	V
Output Coding (Default)			Offset binary		
LOGIC OUTPUTS (GPO0, GPO1, GPO2, GPO3)					
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, f_{IN} = 5 MHz, full temperature, unless otherwise noted.

Table 3.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK[2]					
Clock Rate					
40 MSPS (Mode I)	Full	10		40	MHz
65 MSPS (Mode II)	Full	10		65	MHz
80 MSPS (Mode III)	Full	10		80	MHz
Clock Pulse Width High (t_{EH})	Full		6.25		ns
Clock Pulse Width Low (t_{EL})	Full		6.25		ns
OUTPUT PARAMETERS[2, 3]					
Propagation Delay (t_{PD})	Full	(t_{SAMPLE}/2) + 1.5	(t_{SAMPLE}/2) + 2.3	(t_{SAMPLE}/2) + 3.1	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO Propagation Delay (t_{FCO})	Full	(t_{SAMPLE}/2) + 1.5	(t_{SAMPLE}/2) + 2.3	(t_{SAMPLE}/2) + 3.1	ns
DCO Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/24)		ns
DCO to Data Delay (t_{DATA})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
DCO to FCO Delay (t_{FRAME})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
Data-to-Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±100	±350	ps
Wake-Up Time (Standby), GAIN+ = 0.5 V	25°C		2		µs
Wake-Up Time (Power-Down)	25°C		1		ms
Pipeline Latency	Full		8		Clock cycles
APERTURE					
Aperture Uncertainty (Jitter)	25°C		<1		ps rms
LO GENERATION					
4LO Frequency	Full	4		40	MHz
LO Divider RESET Setup Time[5]	Full	5			ns
LO Divider RESET Hold Time[5]	Full	5			ns
LO Divider RESET High Pulse Width	Full	20			ns

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.
[2] Can be adjusted via the SPI.
[3] Measurements were made using a part soldered to FR-4 material.
[4] t_{SAMPLE}/24 is based on the number of bits divided by 2 because the delays are based on half duty cycles.
[5] RESET edge to rising 4LO edge.

ADC TIMING DIAGRAMS

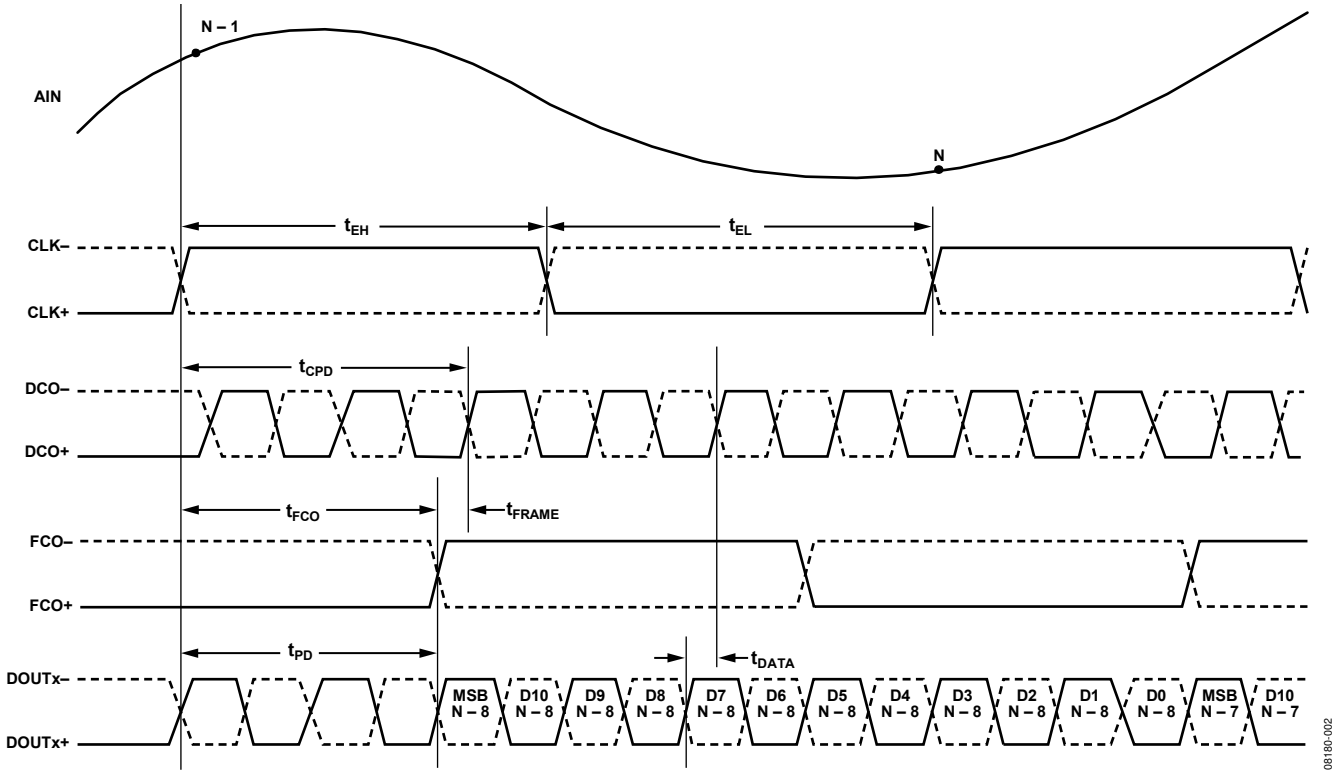


Figure 2. 12-Bit Data Serial Stream (Default)

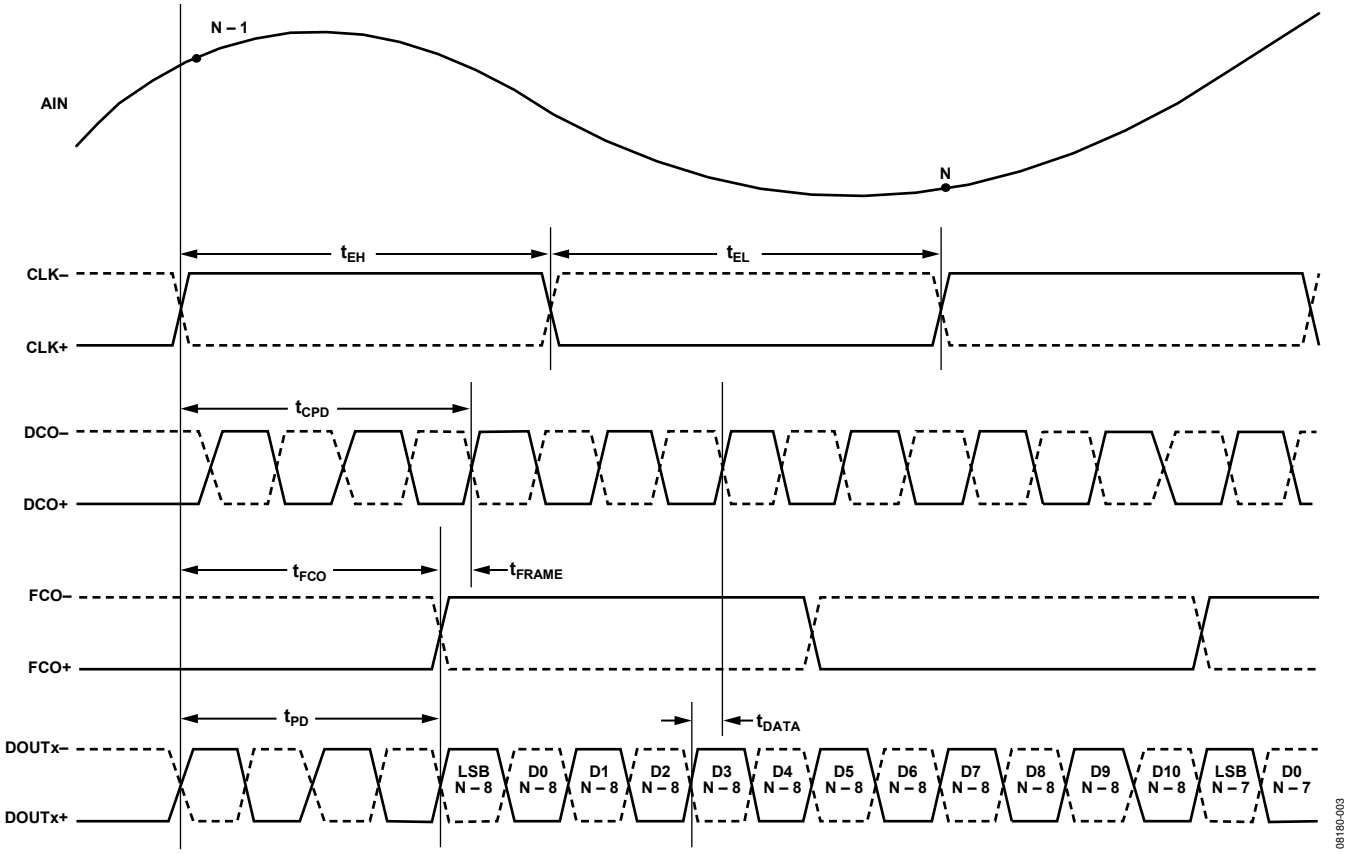


Figure 3. 12-Bit Data Serial Stream, LSB First

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD1 to GND	−0.3 V to +2.0 V
AVDD2 to GND	−0.3 V to +3.9 V
DRVDD to GND	−0.3 V to +2.0 V
GND to GND	−0.3 V to +0.3 V
AVDD2 to AVDD1	−2.0 V to +3.9 V
AVDD1 to DRVDD	−2.0 V to +2.0 V
AVDD2 to DRVDD	−2.0 V to +3.9 V
Digital Outputs (DOUTx+, DOUTx−, DCO+, DCO−, FCO+, FCO−) to GND	−0.3 V to +2.0 V
CLK+, CLK−, SDIO to GND	−0.3 V to +2.0 V
LI-x, LO-x, LOSW-x to GND	−0.3 V to +3.9 V
CWI−, CWI+, CWQ−, CWQ+ to GND	−0.3 V to +3.9 V
PDWN, STBY, SCLK, CSB to GND	−0.3 V to +2.0 V
GAIN+, GAIN−, RESET, 4LO+, 4LO−, GPO0, GPO1, GPO2, GPO3 to GND	−0.3 V to +3.9 V
RBIAS, VREF to GND	−0.3 V to +2.0 V
Operating Temperature Range (Ambient)	−40°C to +85°C
Storage Temperature Range (Ambient)	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE

Table 5.

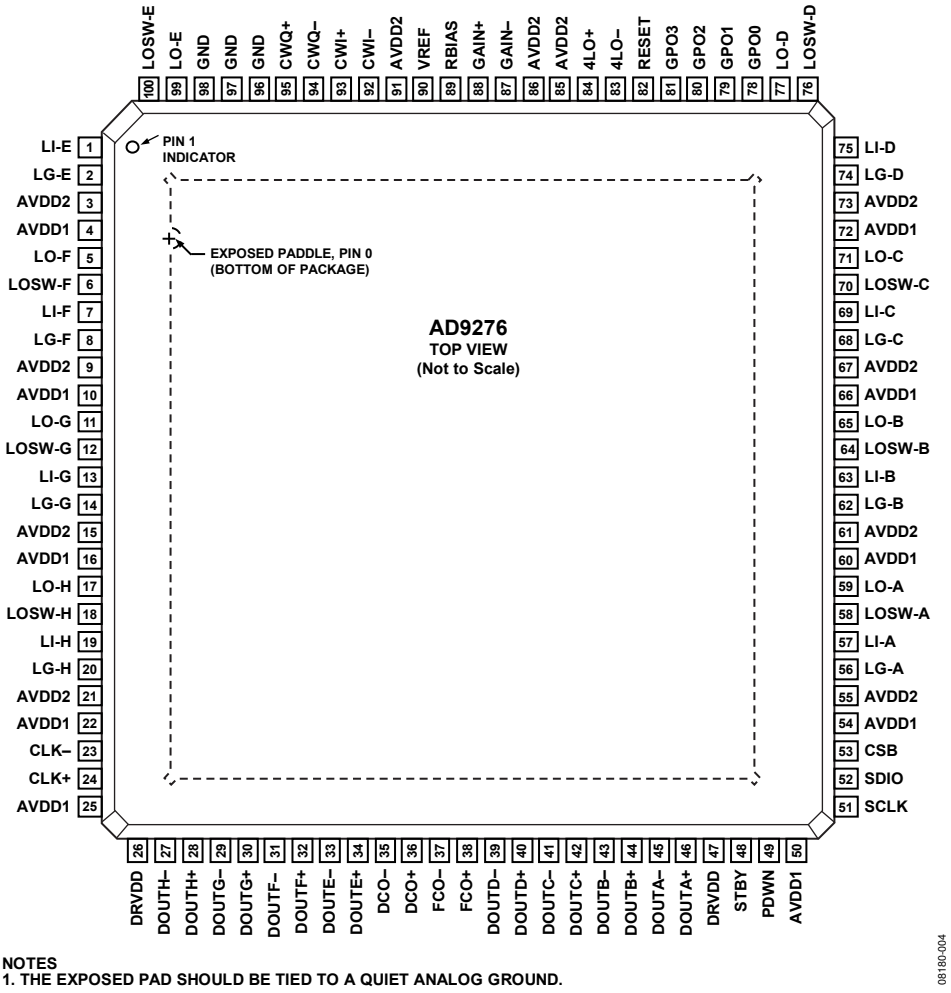
Airflow Velocity (m/s)	θ_{JA}[1]	θ_{JB}	θ_{JC}	Unit
0.0	20.3			°C/W
1.0	14.4	7.6	4.7	°C/W
2.5	12.9			°C/W

[1] θ_{JA} for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD SHOULD BE TIED TO A QUIET ANALOG GROUND.

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Name	Description
0, 96, 97, 98	GND	Ground. Exposed paddle should be tied to a quiet analog ground.
1	LI-E	LNA Analog Input for Channel E.
2	LG-E	LNA Ground for Channel E.
3, 9, 15, 21, 55, 61, 67, 73, 85, 86, 91	AVDD2	3.0 V Analog Supply.
4, 10, 16, 22, 25, 50, 54, 60, 66, 72	AVDD1	1.8 V Analog Supply.
5	LO-F	LNA Analog Inverted Output for Channel F.
6	LOSW-F	LNA Analog Switched Output for Channel F.
7	LI-F	LNA Analog Input for Channel F.
8	LG-F	LNA Ground for Channel F.
11	LO-G	LNA Analog Inverted Output for Channel G.
12	LOSW-G	LNA Analog Switched Output for Channel G.
13	LI-G	LNA Analog Input for Channel G.
14	LG-G	LNA Ground for Channel G.
17	LO-H	LNA Analog Inverted Output for Channel H.
18	LOSW-H	LNA Analog Switched Output for Channel H.
19	LI-H	LNA Analog Input for Channel H.
20	LG-H	LNA Ground for Channel H.

Pin No.	Name	Description
23	CLK−	Clock Input Complement.
24	CLK+	Clock Input True.
26, 47	DRVDD	1.8 V Digital Output Driver Supply.
27	DOUTH−	ADC H Digital Output Complement.
28	DOUTH+	ADC H Digital Output True.
29	DOUTG−	ADC G Digital Output Complement.
30	DOUTG+	ADC G Digital Output True.
31	DOUTF−	ADC F Digital Output Complement.
32	DOUTF+	ADC F Digital Output True.
33	DOUTE−	ADC E Digital Output Complement.
34	DOUTE+	ADC E Digital Output True.
35	DCO−	Digital Clock Output Complement.
36	DCO+	Digital Clock Output True.
37	FCO−	Digital Frame Clock Output Complement.
38	FCO+	Digital Frame Clock Output True.
39	DOUTD−	ADC D Digital Output Complement.
40	DOUTD+	ADC D Digital Output True.
41	DOUTC−	ADC C Digital Output Complement.
42	DOUTC+	ADC C Digital Output True.
43	DOUTB−	ADC B Digital Output Complement.
44	DOUTB+	ADC B Digital Output True.
45	DOUTA−	ADC A Digital Output Complement.
46	DOUTA+	ADC A Digital Output True.
48	STBY	Standby Power-Down.
49	PDWN	Full Power-Down.
51	SCLK	Serial Clock.
52	SDIO	Serial Data Input/Output.
53	CSB	Chip Select Bar.
56	LG-A	LNA Ground for Channel A.
57	LI-A	LNA Analog Input for Channel A.
58	LOSW-A	LNA Analog Switched Output for Channel A.
59	LO-A	LNA Analog Inverted Output for Channel A.
62	LG-B	LNA Ground for Channel B.
63	LI-B	LNA Analog Input for Channel B.
64	LOSW-B	LNA Analog Switched Output for Channel B.
65	LO-B	LNA Analog Inverted Output for Channel B.
68	LG-C	LNA Ground for Channel C.
69	LI-C	LNA Analog Input for Channel C.
70	LOSW-C	LNA Analog Switched Output for Channel C.
71	LO-C	LNA Analog Inverted Output for Channel C.
74	LG-D	LNA Ground for Channel D.
75	LI-D	LNA Analog Input for Channel D.
76	LOSW-D	LNA Analog Switched Output for Channel D.
77	LO-D	LNA Analog Inverted Output for Channel D.
78	GPO0	General-Purpose Open-Drain Output 0.
79	GPO1	General-Purpose Open-Drain Output 1.
80	GPO2	General-Purpose Open-Drain Output 2.
81	GPO3	General-Purpose Open-Drain Output 3.
82	RESET	Reset for Synchronizing 4LO Divide-by-4 Counter.
83	4LO−	CW Doppler 4LO Input Complement.
84	4LO+	CW Doppler 4LO Input True.
87	GAIN−	Gain Control Voltage Input Complement.
88	GAIN+	Gain Control Voltage Input True.

Pin No.	Name	Description
89	RBIAS	External Resistor to Set the Internal ADC Core Bias Current.
90	VREF	Voltage Reference Input/Output.
92	CWI–	CW Doppler I Output Complement.
93	CWI+	CW Doppler I Output True.
94	CWQ–	CW Doppler Q Output Complement.
95	CWQ+	CW Doppler Q Output True.
99	LO-E	LNA Analog Inverted Output for Channel E.
100	LOSW-E	LNA Analog Switched Output for Channel E.

TYPICAL PERFORMANCE CHARACTERISTICS

TGC MODE

f_{SAMPLE} = 40 MSPS, f_{IN} = 5 MHz, R_S = 50 Ω, LNA gain = 21.3 dB, LNA bias = high, PGA gain = 27 dB, AAF LPF cutoff = f_{SAMPLE}/3, HPF cutoff = LPF cutoff/20.7 (default).

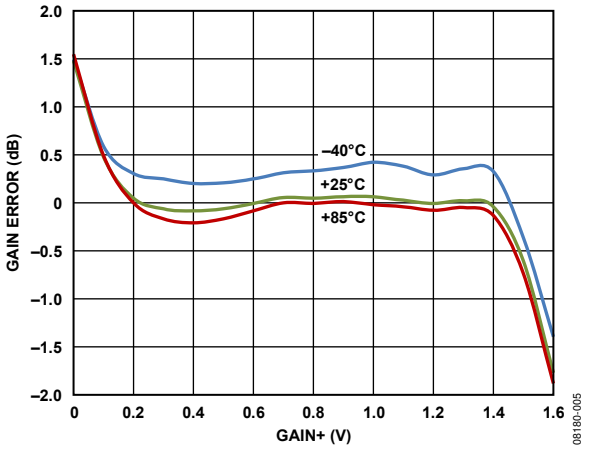


Figure 5. Gain Error vs. GAIN+ at Three Temperatures

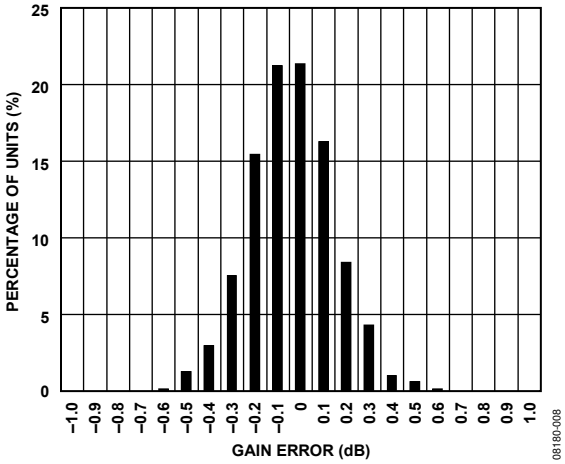


Figure 8. Gain Error Histogram, GAIN+ = 1.44 V

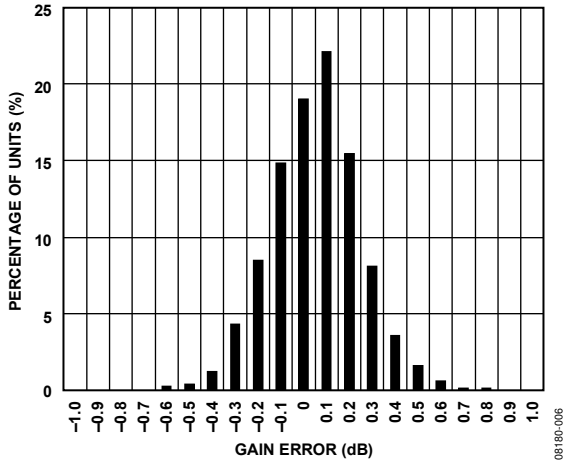


Figure 6. Gain Error Histogram, GAIN+ = 0.16 V

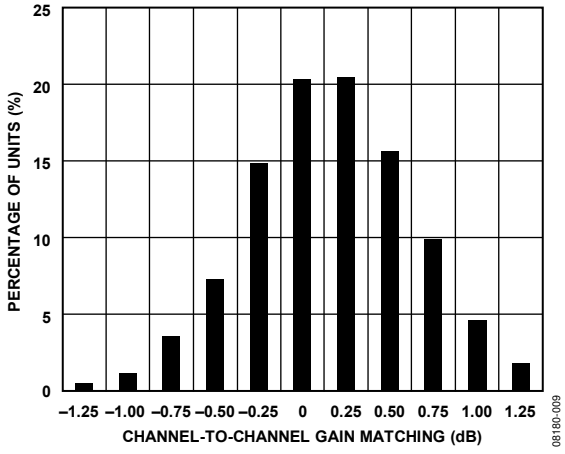


Figure 9. Gain Match Histogram, GAIN+ = 0.3 V

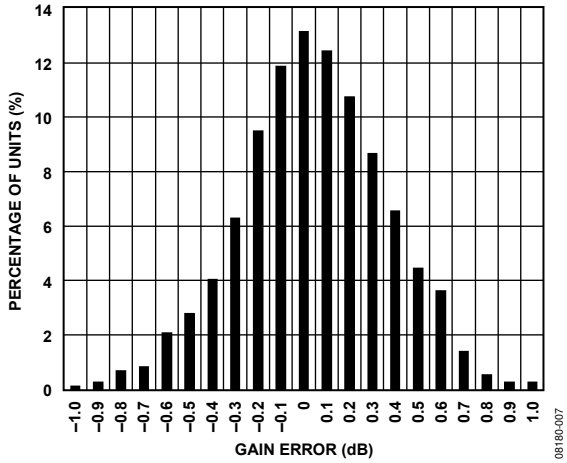


Figure 7. Gain Error Histogram, GAIN+ = 0.8 V

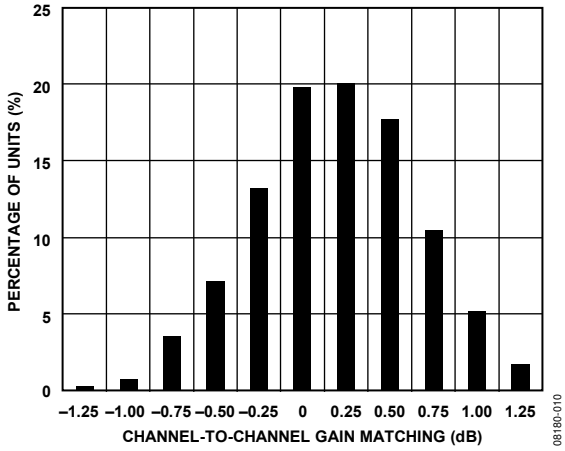


Figure 10. Gain Match Histogram, GAIN+ = 1.3 V

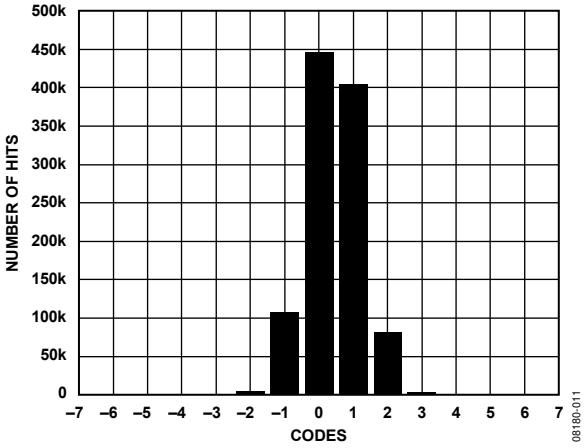


Figure 11. Output-Referred Noise Histogram, GAIN+ = 0.0 V

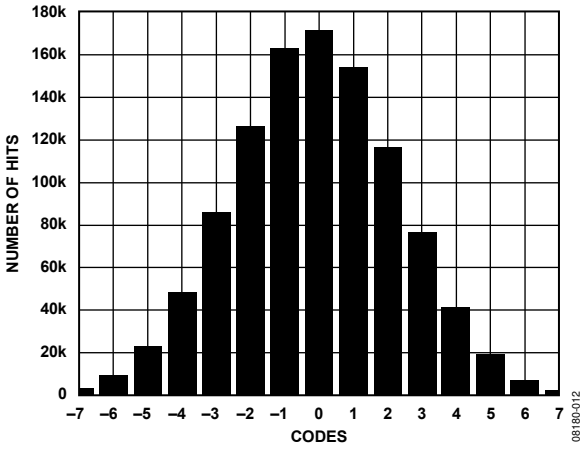


Figure 12. Output-Referred Noise Histogram, GAIN+ = 1.6 V

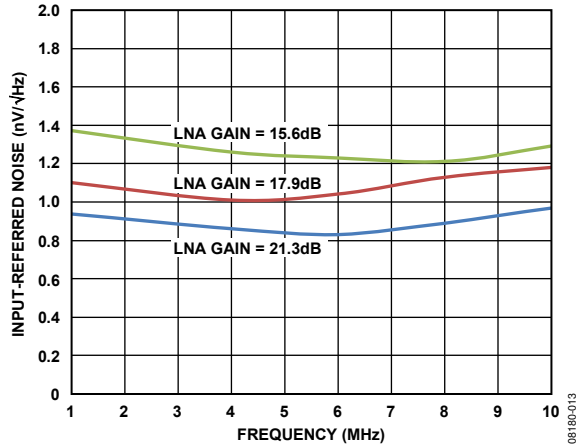


Figure 13. Short-Circuit, Input-Referred Noise vs. Frequency, PGA Gain = 30 dB, GAIN+ = 1.6 V

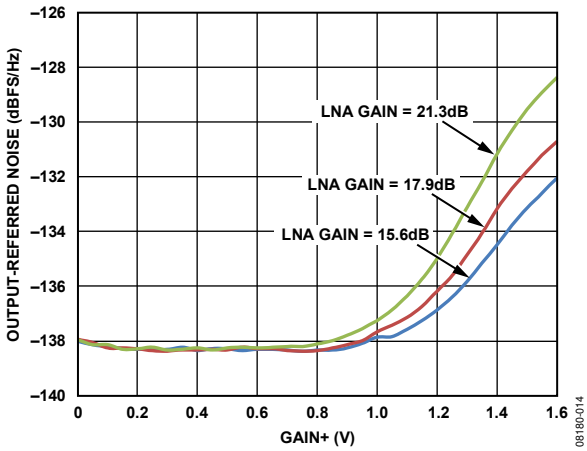


Figure 14. Short-Circuit, Output-Referred Noise vs. GAIN+

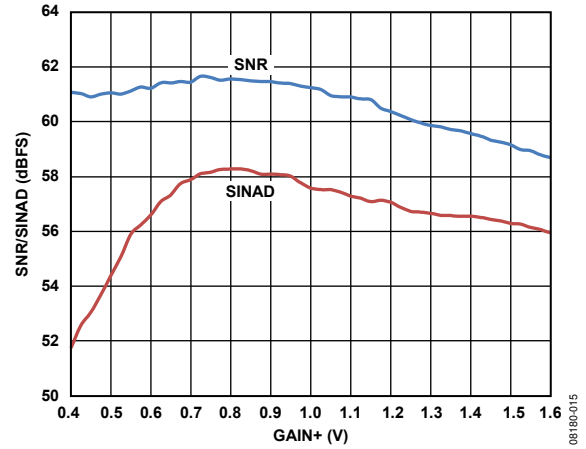


Figure 15. SNR/SINAD vs. GAIN+, AIN = −1.0 dBFS

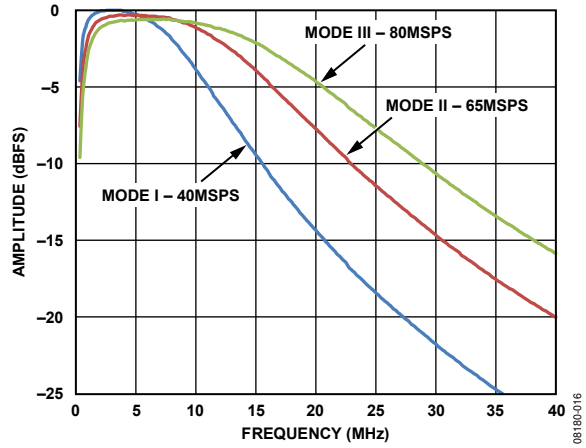


Figure 16. Antialiasing Filter (AAF) Pass-Band Response, LPF Cutoff = $f_{SAMPLE}/3$ (Mode I and Mode II), $f_{SAMPLE}/4.5$ (Mode III)

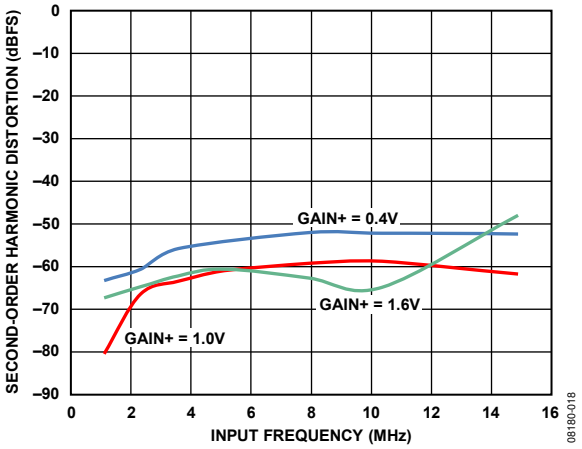


Figure 17. Second-Order Harmonic Distortion vs. Frequency, AIN = −1.0 dBFS

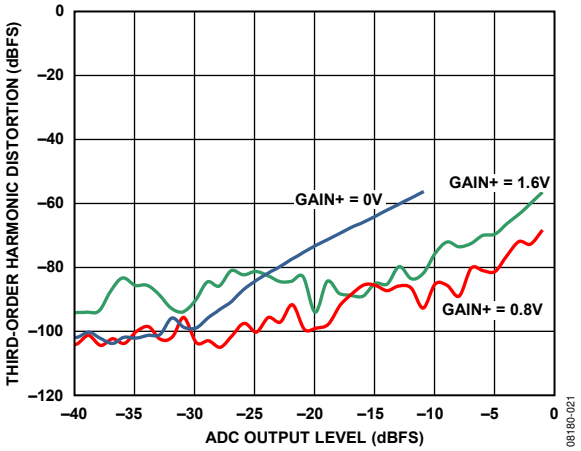


Figure 20. Third-Order Harmonic Distortion vs. ADC Output Level

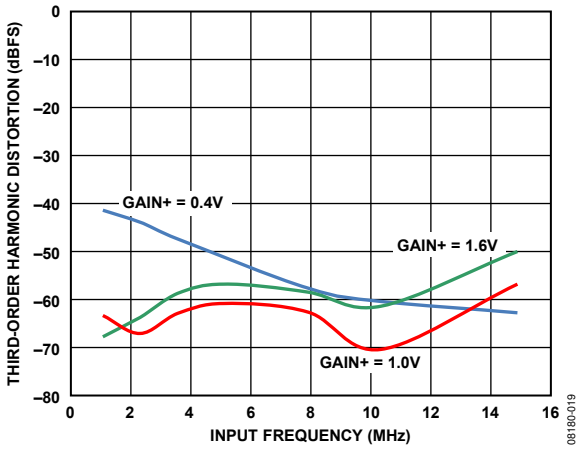


Figure 18. Third-Order Harmonic Distortion vs. Frequency, AIN = −1.0 dBFS

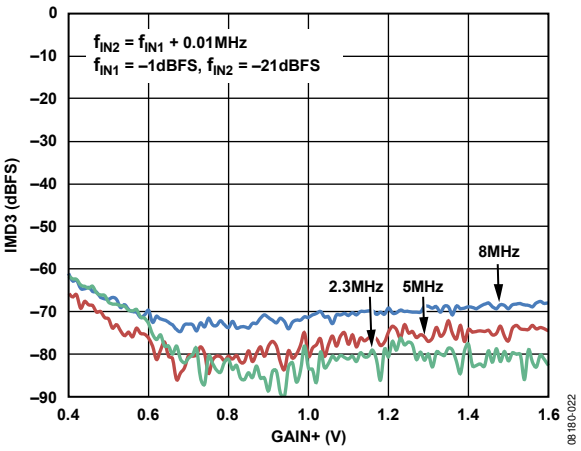


Figure 21. IMD3 vs. GAIN+

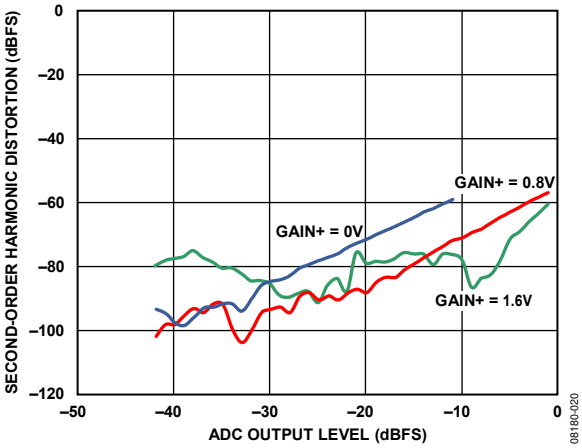


Figure 19. Second-Order Harmonic Distortion vs. ADC Output Level

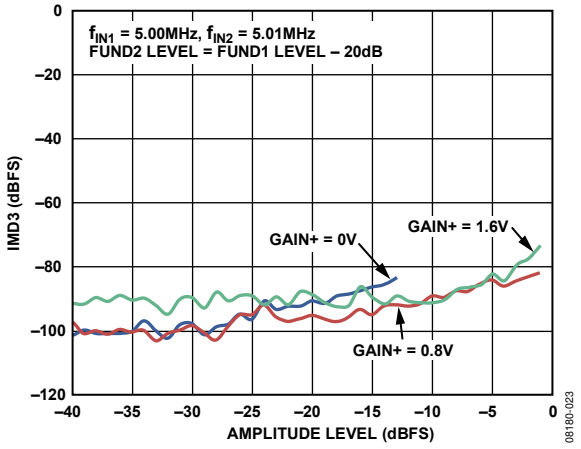


Figure 22. IMD3 vs. Amplitude Level

CW DOPPLER MODE

f_{RF} = 2.5 MHz at −3 dBFS, f_{4LO} = 10 MHz, R_S = 50 Ω, LNA gain = 21.3 dB, LNA bias = high, all CW channels enabled, phase rotation 0°.

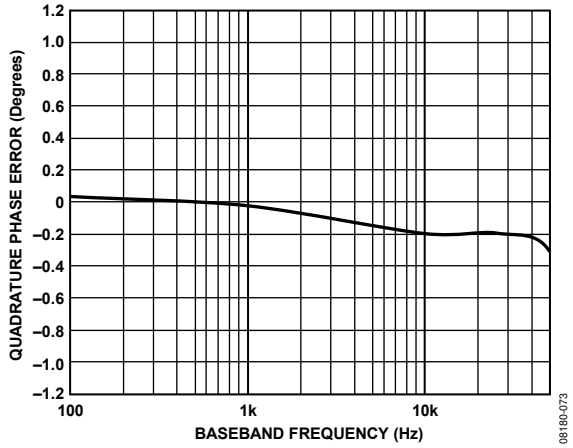


Figure 23. Quadrature Phase Error vs. Baseband Frequency

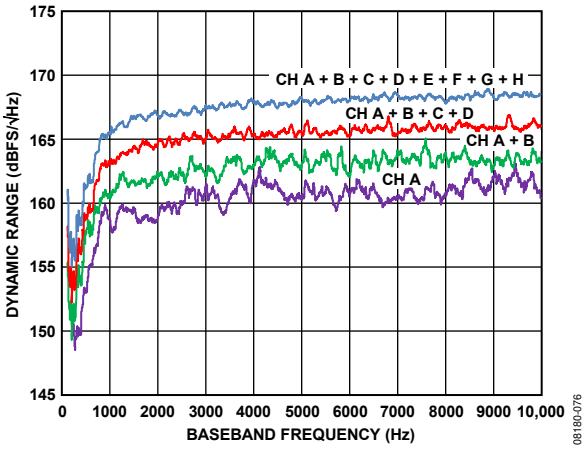


Figure 26. Small-Signal Dynamic Range

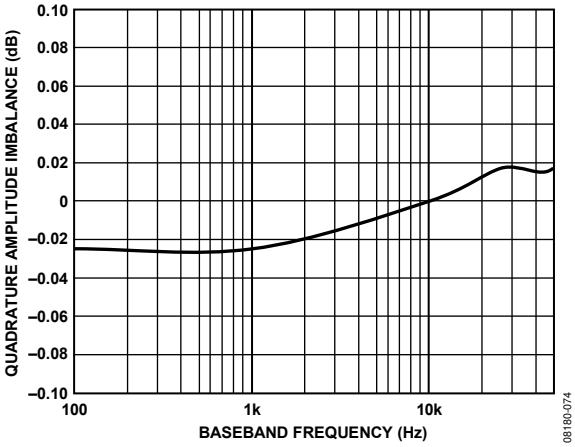


Figure 24. Quadrature Amplitude Imbalance vs. Baseband Frequency

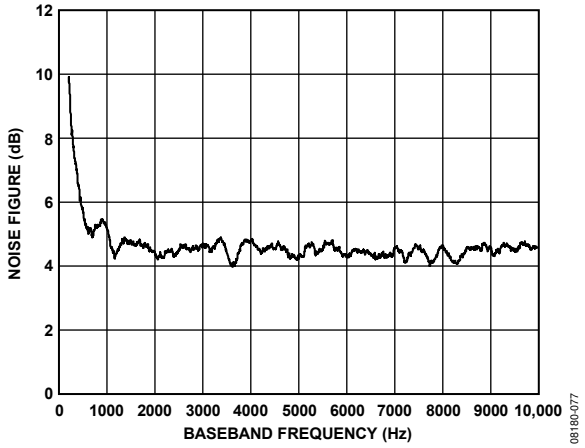


Figure 27. Noise Figure vs. Baseband Frequency

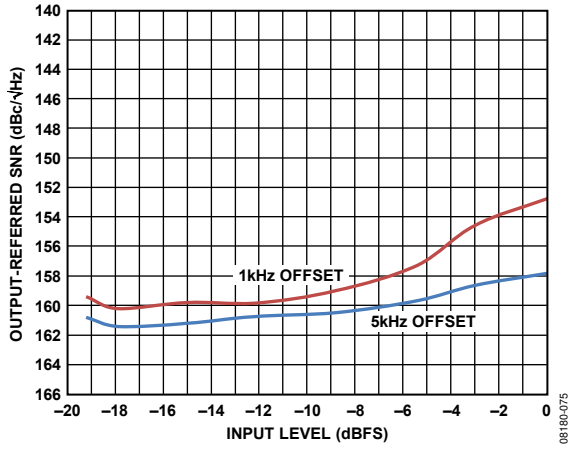


Figure 25. Output-Referred SNR vs. Input Level

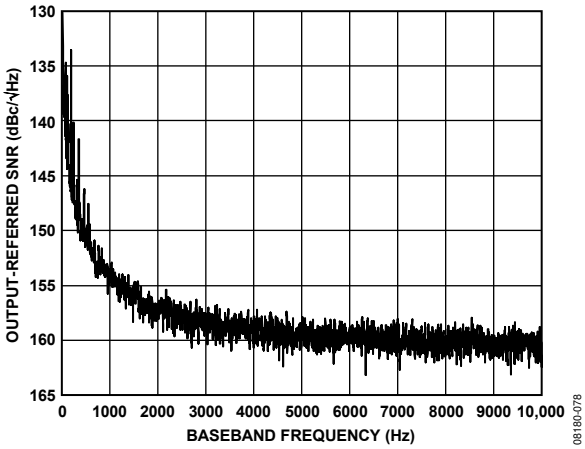


Figure 28. Output-Referred SNR vs. Baseband Frequency

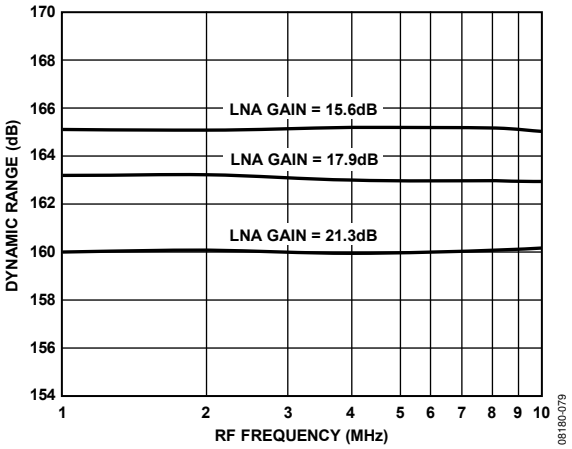


Figure 29. Small-Signal Dynamic Range vs. RF Frequency

EQUIVALENT CIRCUITS

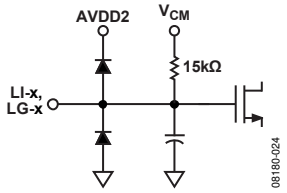


Figure 30. Equivalent LNA Input Circuit

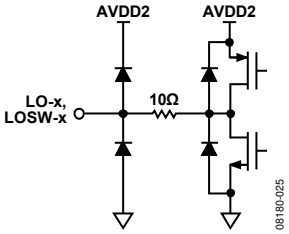


Figure 31. Equivalent LNA Output Circuit

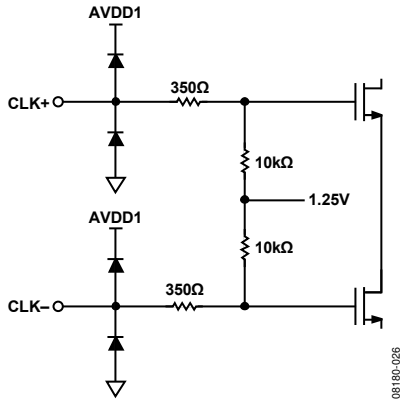


Figure 32. Equivalent Clock Input Circuit

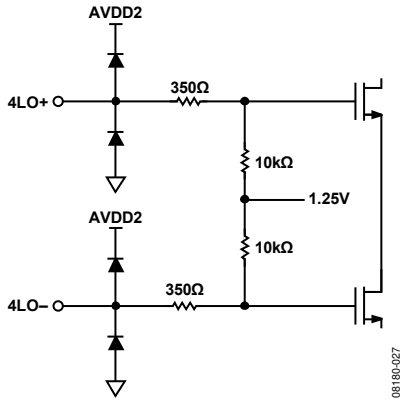


Figure 33. Equivalent 4LO Input Circuit

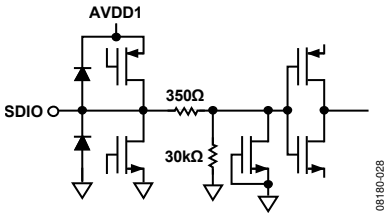


Figure 34. Equivalent SDIO Input Circuit

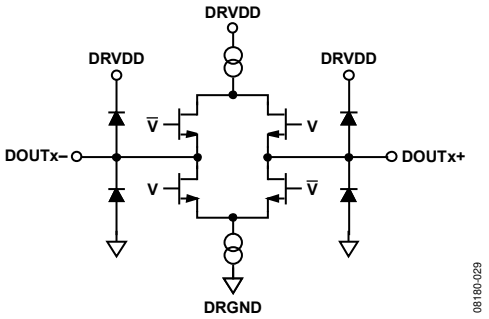


Figure 35. Equivalent Digital Output Circuit

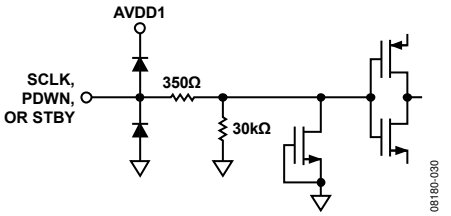


Figure 36. Equivalent SCLK, PDWN, or STBY Input Circuit

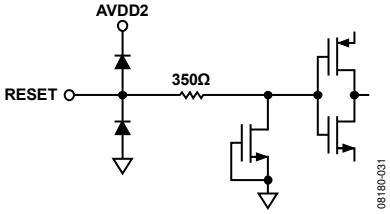


Figure 37. Equivalent RESET Input Circuit

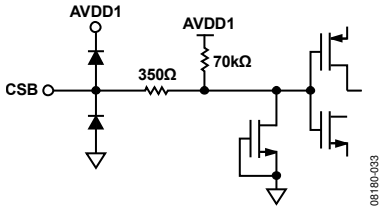


Figure 38. Equivalent CSB Input Circuit

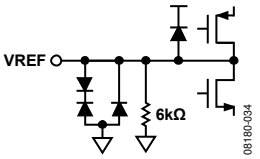


Figure 39. Equivalent VREF Circuit

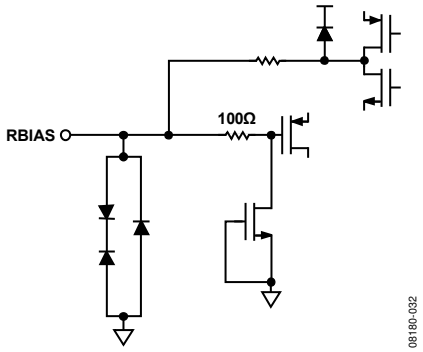


Figure 40. Equivalent RBIAS Circuit

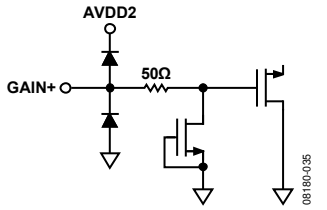


Figure 41. Equivalent GAIN+ Input Circuit

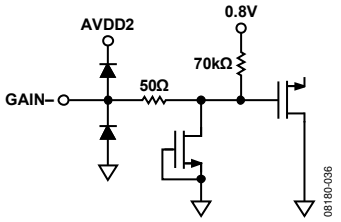


Figure 42. Equivalent GAIN– Input Circuit

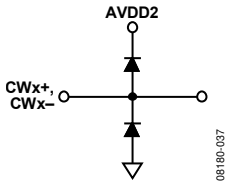


Figure 43. Equivalent CWI±, CWQ± Output Circuit

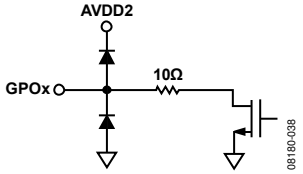


Figure 44. Equivalent GPOx Output Circuit

THEORY OF OPERATION

ULTRASOUND

The primary application for the AD9276 is medical ultrasound. Figure 45 shows a simplified block diagram of an ultrasound system. A critical function of an ultrasound system is the time gain control (TGC) compensation for physiological signal attenuation. Because the attenuation of ultrasound signals is exponential with respect to distance (time), a linear-in-dB VGA is the optimal solution.

Key requirements in an ultrasound signal chain are very low noise, active input termination, fast overload recovery, low power, and differential drive to an ADC. Because ultrasound machines use beamforming techniques requiring large binary-weighted numbers of channels (for example, 32 to 512), using the lowest power at the lowest possible noise is of chief importance.

Most modern ultrasound machines use digital beamforming. In this technique, the signal is converted to digital format immediately following the TGC amplifier, and then beamforming is accomplished digitally.

The ADC resolution of 12 bits with up to 80 MSPS sampling satisfies the requirements of both general-purpose and high end systems.

Power conservation and low cost are two of the most important factors in low end and portable ultrasound machines, and the AD9276 is designed to meet these criteria.

For additional information regarding ultrasound systems, refer to "How Ultrasound System Considerations Influence Front-End Component Choice," *Analog Dialogue*, Volume 36, Number 3, May–July 2002, and "The AD9271—A Revolutionary Solution for Portable Ultrasound," *Analog Dialogue*, Volume 41, Number 7, July 2007.

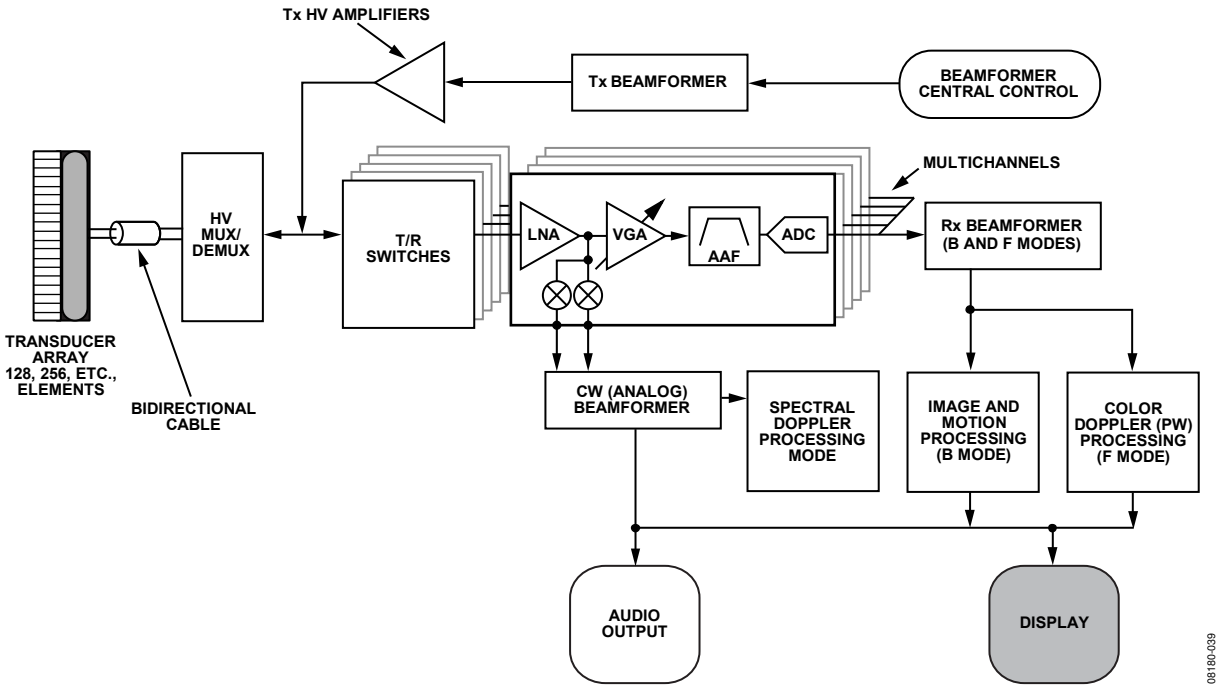


Figure 45. Simplified Ultrasound System Block Diagram

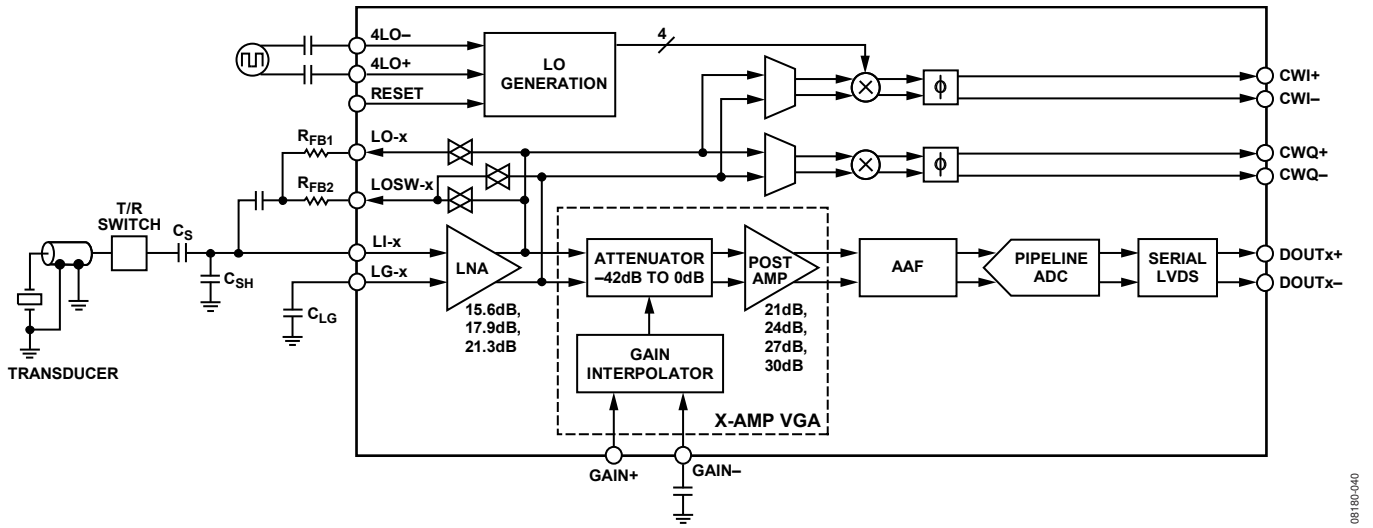


Figure 46. Simplified Block Diagram of a Single Channel

CHANNEL OVERVIEW

Each channel contains both a TGC signal path and a CW Doppler signal path. Common to both signal paths, the LNA provides user-adjustable input impedance termination. The CW Doppler path includes an I/Q demodulator. The TGC path includes a differential X-AMP® VGA, an antialiasing filter, and an ADC. Figure 46 shows a simplified block diagram with external components.

The signal path is fully differential throughout to maximize signal swing and reduce even-order distortion; however, the LNA is designed to be driven from a single-ended signal source.

Low Noise Amplifier (LNA)

Good noise performance relies on a proprietary ultralow noise LNA at the beginning of the signal chain, which minimizes the noise contribution in the following VGA. Active impedance control optimizes noise performance for applications that benefit from input impedance matching.

A simplified schematic of the LNA is shown in Figure 47. LI-x is capacitively coupled to the source. An on-chip bias generator establishes dc input bias voltages of around 0.9 V and centers the output common-mode levels at 1.5 V (AVDD2 divided by 2). A capacitor, C_{LG}, of the same value as the input coupling capacitor, C_S, is connected from the LG-x pin to ground.

It is highly recommended that the LG-x pins form a Kelvin type connection to the input or probe connection ground. Simply connecting the LG-x pin to ground near the device can allow differences in potential to be amplified through the LNA. This generally shows up as a dc offset voltage that can vary from channel to channel and part to part, depending on the application and the layout of the PCB.

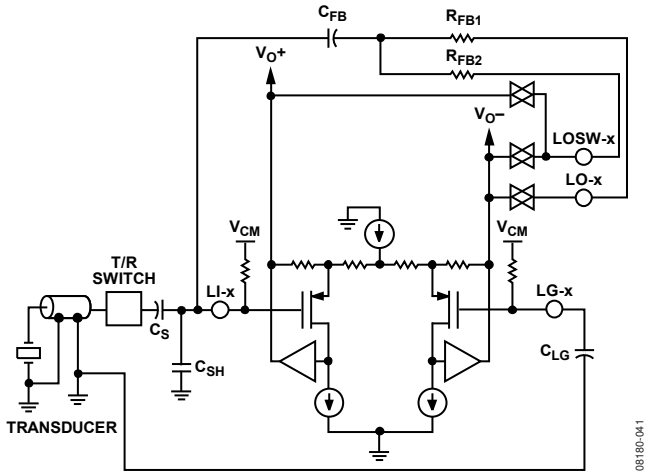


Figure 47. Simplified LNA Schematic

The LNA supports differential output voltages as high as 4.4 V p-p with positive and negative excursions of ±1.1 V from a common-mode voltage of 1.5 V. The LNA differential gain sets the maximum input signal before saturation. One of three gains is set through the SPI. The corresponding full-scale input for the gain settings of 15.6 dB, 17.9 dB, and 21.3 dB is 733 mV p-p, 550 mV p-p, and 367 mV p-p, respectively. Overload protection ensures quick recovery time from large input voltages. Because the inputs are capacitively coupled to a bias voltage near midsupply, very large inputs can be handled without interacting with the ESD protection.

Low value feedback resistors and the current-driving capability of the output stage allow the LNA to achieve a low input-referred noise voltage of 0.75 nV/√Hz (at a gain of 21.3 dB). This is achieved with a current consumption of only 27 mA per channel (80 mW). On-chip resistor matching results in precise single-ended gains, which are critical for accurate impedance control. The use of a fully differential topology and negative feedback minimizes distortion. Low second-order harmonic distortion is particularly important in second harmonic ultrasound imaging applications. Differential signaling enables smaller swings at each output, further reducing third-order harmonic distortion.

Active Impedance Matching

The LNA consists of a single-ended voltage gain amplifier with differential outputs and the negative output externally available. For example, with a fixed gain of 8× (17.9 dB), an active input termination is synthesized by connecting a feedback resistor between the negative output pin, LO-x, and the positive input pin, LI-x. This well-known technique is used for interfacing multiple probe impedances to a single system. The input resistance is shown in Equation 1.

$$R_{IN} = \frac{R_{FB}}{(1 + A/2)} \quad (1)$$

where:
$A/2$ is the single-ended gain or the gain from the LI-x inputs to the LO-x outputs.
R_{FB} is the resulting impedance of the R_{FB1} and R_{FB2} combination (see Figure 47).

Because the amplifier has a gain of 8× from its input to its differential output, it is important to note that the gain A/2 is the gain from Pin LI-x to Pin LO-x and that it is 6 dB less than the gain of the amplifier, or 11.9 dB (4×). The input resistance is reduced by an internal bias resistor of 15 kΩ in parallel with the source resistance connected to Pin LI-x, with Pin LG-x ac grounded. Equation 2 can be used to calculate the required R_{FB} for a desired R_{IN}, even for higher values of R_{IN}.

$$R_{IN} = \frac{R_{FB}}{(1+3)} \,||\, 15\ \text{k}\Omega \quad (2)$$

For example, to set R_{IN} to 200 Ω, the value of R_{FB} must be 1000 Ω. If the simplified equation (Equation 2) is used to calculate R_{IN}, the value is 188 Ω, resulting in a gain error of less than 0.6 dB. Some factors, such as the presence of a dynamic source resistance, may influence the absolute gain accuracy more significantly. At higher frequencies, the input capacitance of the LNA must be considered. The user must determine the level of matching accuracy and adjust R_{FB} accordingly.

The bandwidth (BW) of the LNA is greater than 100 MHz. Ultimately, the BW of the LNA limits the accuracy of the synthesized R_{IN}. For $R_{IN} = R_S$ up to about 200 Ω, the best match is between 100 kHz and 10 MHz, where the lower frequency limit is determined by the size of the ac coupling capacitors, and the upper limit is determined by the LNA BW. Furthermore, the input capacitance and R_S limit the BW at higher frequencies. Figure 48 shows R_{IN} vs. frequency for various values of R_{FB}.

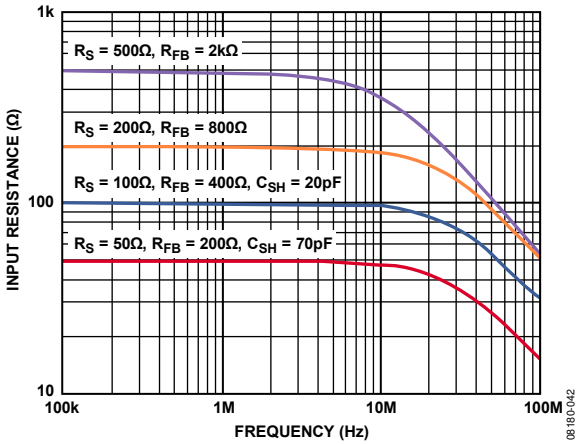


Figure 48. R_{IN} vs. Frequency for Various Values of R_{FB} (Effects of R_S and C_{SH} Are Also Shown)

Note that at the lowest value of R_{IN} (50 Ω), R_{IN} peaks at frequencies greater than 10 MHz. This is due to the BW roll-off of the LNA, as mentioned previously.

However, as can be seen for larger R_{IN} values, parasitic capacitance starts rolling off the signal BW before the LNA can produce peaking. C_{SH} further degrades the match; therefore, C_{SH} should not be used for values of R_{IN} that are greater than 100 Ω. Table 7 lists the recommended values for R_{FB} and C_{SH} in terms of R_{IN}.

C_{FB} is needed in series with R_{FB} because the dc levels at Pin LO-x and Pin LI-x are unequal.

Table 7. Active Termination External Component Values

LNA Gain (dB)	R_{IN} (Ω)	R_{FB} (Ω)	Minimum C_{SH} (pF)	BW (MHz)
15.6	50	200	90	57
17.9	50	250	70	69
21.3	50	350	50	88
15.6	100	400	30	57
17.9	100	500	20	69
21.3	100	700	10	88
15.6	200	800	N/A	72
17.9	200	1000	N/A	72
21.3	200	1400	N/A	72

LNA Noise

The short-circuit noise voltage (input-referred noise) is an important limit on system performance. The short-circuit noise voltage for the LNA is 0.75 nV/√Hz at a gain of 21.3 dB, including the VGA noise at a VGA postamp gain of 27 dB. These measurements, which were taken without a feedback resistor, provide the basis for calculating the input noise and noise figure (NF) performance of the configurations shown in Figure 49.

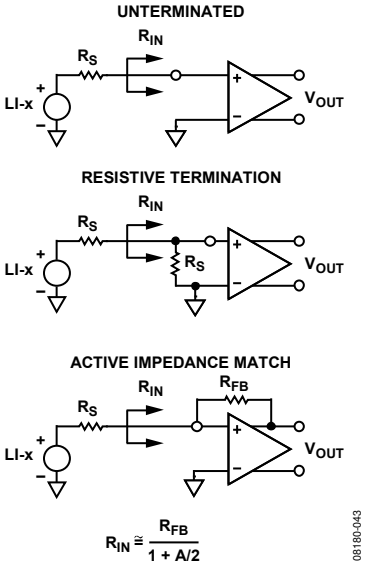


Figure 49. Input Configurations

Figure 50 and Figure 51 are simulations of noise figure vs. R_S results using these configurations and an input-referred noise voltage of 3.8 nV/√Hz for the VGA. Unterminated ($R_{FB} = \infty$) operation exhibits the lowest equivalent input noise and noise figure. Figure 51 shows the noise figure vs. source resistance rising at low R_S—where the LNA voltage noise is large compared with the source noise—and at high R_S due to the noise contribution from R_{FB}. The lowest NF is achieved when R_S matches R_{IN}.

The main purpose of input impedance matching is to improve the transient response of the system. With resistive termination, the input noise increases due to the thermal noise of the matching resistor and the increased contribution of the LNA's input voltage noise generator. With active impedance matching, however, the contributions of both are smaller (by a factor of 1/(1 + LNA gain)) than they would be for resistive termination.

Figure 50 shows the relative noise figure performance. With an LNA gain of 21.3 dB, the input impedance was swept with R_S to preserve the match at each point. The noise figures for a source impedance of 50 Ω are 7.3 dB, 4.2 dB, and 2.8 dB for the resistive termination, active termination, and unterminated configurations, respectively. The noise figures for 200 Ω are 4.5 dB, 1.7 dB, and 1.0 dB, respectively.

Figure 51 shows the noise figure as it relates to R_S for various values of R_{IN}, which is helpful for design purposes.

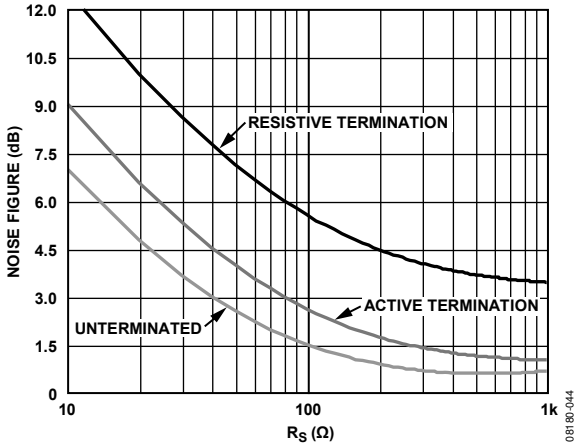


Figure 50. Noise Figure vs. R_S for Resistive Termination, Active Termination Matched, and Unterminated Inputs, V_{GAIN} = 0.8 V

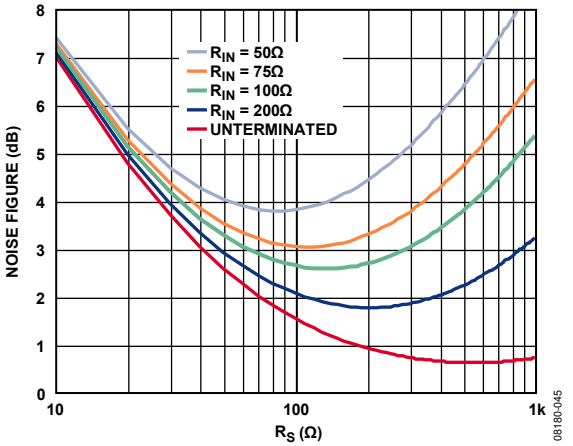


Figure 51. Noise Figure vs. R_S for Various Fixed Values of R_{IN}, Active Termination Matched Inputs, V_{GAIN} = 0.8 V