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Octal LNA/VGA/AAF/ADC and CW I/Q Demodulator

Data Sheet

AD9278

FEATURES

- 8 channels of LNA, VGA, AAF, ADC, and I/Q demodulator
  - Low power: 88 mW per channel, TGC mode, 40 MSPS; 32 mW per channel, CW mode
  - 10 mm × 10 mm, 144-ball CSP-BGA
  - TGC channel input-referred noise: 1.3 nV/√Hz, max gain
  - Flexible power-down modes
  - Fast recovery from low power standby mode: <2 µs
  - Overload recovery: <10 ns
- Low noise preamplifier (LNA)
  - Input-referred noise: 1.25 nV/√Hz, gain = 21.3 dB
  - Programmable gain: 15.6 dB/17.9 dB/21.3 dB
  - 0.1 dB compression: 1000 mV p-p/ 750 mV p-p/450 mV p-p
  - Dual-mode active input impedance matching
  - Bandwidth (BW): >50 MHz
- Variable gain amplifier (VGA)
  - Attenuator range: −45 dB to 0 dB
  - Postamp gain (PGA): 21 dB/24 dB/27 dB/30 dB
  - Linear-in-dB gain control
- Antialiasing filter (AAF)
  - Programmable second-order LPF from 8 MHz to 18 MHz
  - Programmable HPF
- Analog-to-digital converter (ADC)
  - SNR: 70 dB, 12 bits up to 65 MSPS
  - Serial LVDS (ANSI-644, low power/reduced signal)
- CW mode I/Q demodulator
  - Individual programmable phase rotation
  - Output dynamic range per channel: >158 dBc/√Hz
  - Output-referred SNR: 153 dBc/√Hz, 1 kHz offset, −3 dBFS

GENERAL DESCRIPTION

The AD9278 is designed for low cost, low power, small size, and ease of use for medical ultrasound and automotive radar. It contains eight channels of a variable gain amplifier (VGA) with a low noise preamplifier (LNA), an antialiasing filter (AAF), an analog-to-digital converter (ADC), and an I/Q demodulator with programmable phase rotation.

Each channel features a variable gain range of 45 dB, a fully differential signal path, an active input preamplifier termination, and a maximum gain of up to 51 dB. The channel is optimized for high dynamic performance and low power in applications where a small package size is critical.

The LNA has a single-ended-to-differential gain that is selectable through the SPI. Assuming a 15 MHz noise bandwidth (NBW) and a 21.3 dB LNA gain, the LNA input SNR is roughly 88 dB. In CW Doppler mode, each LNA output drives an I/Q demodulator that has independently programmable phase rotation with 16 phase settings.

Power-down of individual channels is supported to increase battery life for portable applications. Standby mode allows quick power-up for power cycling. In CW Doppler operation, the VGA, AAF, and ADC are powered down. The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable clock, data alignment, and programmable digital test pattern generation. The digital test patterns include built-in fixed patterns, built-in pseudo random patterns, and custom user-defined test patterns entered via the serial port interface.

FUNCTIONAL BLOCK DIAGRAM

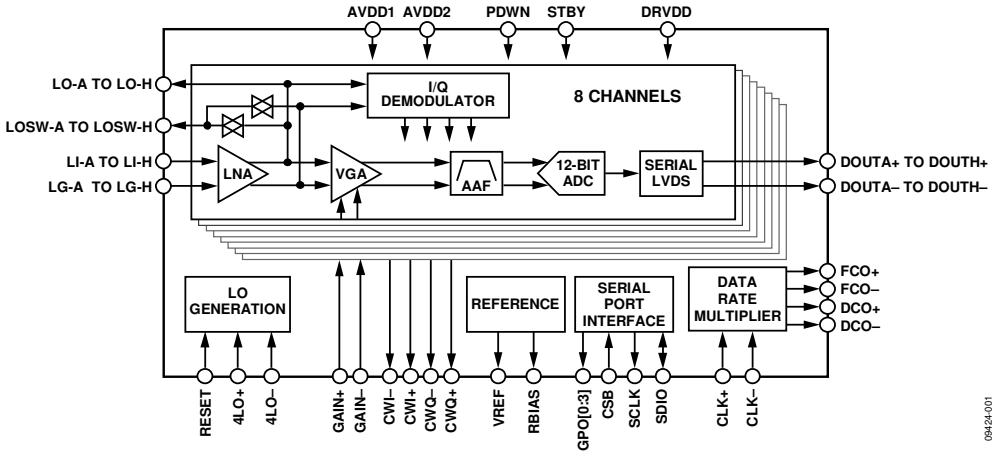

Figure 1.

Rev. A

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- AD9278 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9278: Octal LNA/VGA/AAF/ADC and CW I/Q Demodulator

TOOLS AND SIMULATIONS

- Visual Analog

REFERENCE MATERIALS

Press

- Industry's First Octal Ultrasound Receiver with Digital I/Q Demodulator and Decimation Filter Reduces Processor Overhead in Ultrasound Systems
- Low Cost, Octal Ultrasound Receiver with On-Chip RF Decimator and JESD204B Serial Interface

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

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- AD9278 Material Declaration
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10/10—Revision 0: Initial Version

SPECIFICATIONS

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, full temperature range (−40°C to +85°C), f_{IN} = 5 MHz, R_S = 50 Ω, R_{FB} = ∞ (unterminated), LNA gain = 21.3 dB, LNA bias = default, PGA gain = 24 dB, GAIN− = 0.8 V, GAIN+ = 0 V, AAF LPF cutoff = f_{SAMPLE}/3 (MODE I/II/III), AAF LPF cutoff = f_{SAMPLE}/4.5 (MODE IV), HPF cutoff = LPF cutoff/12, MODE I = f_{SAMPLE} = 40 MSPS, MODE II = f_{SAMPLE} = 25 MSPS, MODE III = f_{SAMPLE} = 50 MSPS, MODE IV = f_{SAMPLE} = 65 MSPS, low power LVDS mode, unless otherwise noted.

Table 1.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
LNA CHARACTERISTICS					
Gain	Single-ended input to differential output		15.6/17.9/21.3		dB
	Single-ended input to single-ended output		9.6/11.9/15.3		dB
0.1 dB Input Compression Point					
	LNA gain = 15.6 dB		1.00		V p-p
	LNA gain = 17.9 dB		0.75		V p-p
	LNA gain = 21.3 dB		0.45		V p-p
1 dB Input Compression Point					
	LNA gain = 15.6 dB		1.20		V p-p
	LNA gain = 17.9 dB		0.90		V p-p
	LNA gain = 21.3 dB		0.60		V p-p
Input Common Mode (LI-x, LG-x)			2.2		V
Output Common Mode (LO-x)					V
Output Common Mode (LOSW-x)	Switch off		High-Z		Ω
	Switch on		1.5		V
Input Resistance (LI-x)	R_{FB} = 350 Ω, LNA gain = 21.3 dB		50		Ω
	R_{FB} = 1400 Ω, LNA gain = 21.3 dB		200		Ω
	R_{FB} = ∞, LNA gain = 21.3 dB		15		kΩ
Input Capacitance (LI-x)			22		pF
−3 dB Bandwidth	LNA gain = 15.6 dB		100		MHz
	LNA gain = 17.9 dB		80		MHz
	LNA gain = 21.3 dB		50		MHz
Input Noise Voltage	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		1.60		nV/√Hz
	LNA gain = 17.9 dB		1.42		nV/√Hz
	LNA gain = 21.3 dB		1.27		nV/√Hz
Input Noise Current	R_{FB} = ∞		1.5		pA/√Hz
Noise Figure	R_S = 50 Ω				
Active Termination Matched	LNA gain = 15.6 dB, R_{FB} = 200 Ω		7.8		dB
	LNA gain = 17.9 dB, R_{FB} = 250 Ω		6.7		dB
	LNA gain = 21.3 dB, R_{FB} = 350 Ω		5.6		dB
Unterminated	LNA gain = 15.6 dB, R_{FB} = ∞		6.1		dB
	LNA gain = 17.9 dB, R_{FB} = ∞		5.3		dB
	LNA gain = 21.3 dB, R_{FB} = ∞		4.7		dB
FULL-CHANNEL (TGC) CHARACTERISTICS					
AAF Low-Pass Cutoff	−3 dB, programmable	8		18	MHz
In Range AAF Bandwidth Tolerance			±10		%
Group Delay Variation	f = 1 MHz to 18 MHz, GAIN+ = 0 V to 1.6 V		±0.3		ns

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Input-Referred Noise Voltage	GAIN+ = 1.6 V, R_{FB} = ∞				
	LNA gain = 15.6 dB		1.7		nV/√Hz
	LNA gain = 17.9 dB		1.5		nV/√Hz
	LNA gain = 21.3 dB		1.3		nV/√Hz
Noise Figure	GAIN+ = 1.6 V, R_S = 50 Ω				
Active Termination Matched	LNA gain = 15.6 dB, R_{FB} = 200 Ω		9.2		dB
	LNA gain = 17.9 dB, R_{FB} = 250 Ω		7.7		dB
	LNA gain = 21.3 dB, R_{FB} = 350 Ω		6.3		dB
Unterminated	LNA gain = 15.6 dB, R_{FB} = ∞		6.7		dB
	LNA gain = 17.9 dB, R_{FB} = ∞		5.7		dB
	LNA gain = 21.3 dB, R_{FB} = ∞		4.9		dB
Correlated Noise Ratio	No signal, correlated/uncorrelated		−30		dB
Output Offset		−35		+35	LSB
Signal-to-Noise Ratio (SNR)	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V,		65		dBFS
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		57		dBFS
Harmonic Distortion					
Second Harmonic	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		−70		dBc
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		−70		dBc
Third Harmonic	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		−70		dBc
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		−70		dBc
Two-Tone Intermodulation (IMD3)	f_{RF1} = 5.015 MHz, f_{RF2} = 5.020 MHz, A_{RF1} = 0 dB, A_{RF2} = −20 dB, GAIN+ = 1.6 VIMD3 relative to A_{RF2}		−70		dBc
Channel-to-Channel Crosstalk	f_{IN1} = 5.0 MHz at −1 dBFS		−60		dB
	Overrange condition[2]		−55		dB
Channel-to-Channel Delay Variation	Full TGC path, f_{IN} = 5 MHz, GAIN+ = 0 V to 1.6 V		0.3		Degrees
PGA Gain	Differential input to differential output		21/24/27/30		dB
GAIN ACCURACY	25°C				
Gain Law Conformance Error	0 < GAIN+ < 0.16 V		0.5		dB
	0.16 V < GAIN+ < 1.44 V	−1.6		+1.6	dB
	1.44 V < GAIN+ < 1.6 V		0.5		dB
Linear Gain Error	GAIN+ = 0.8 V, normalized for ideal AAF loss	−1.6		+1.6	dB
Channel-to-Channel Matching	0.16 V < GAIN+ < 1.44 V		0.1		dB
GAIN CONTROL INTERFACE					
Control Range	Differential	−0.8		+0.8	V
	Single-ended	0		1.6	V
Gain Range	GAIN+ = 0 V to 1.6 V		45		dB
Scale Factor			28		dB/V
Response Time	45 dB change		750		ns
Gain+ Impedance	Single-ended		10		MΩ
Gain− Impedance	Single-ended		70		kΩ
CW DOPPLER MODE					
LO Frequency	$f_{LO} = f_{4LO}/4$	1		10	MHz
Phase Resolution	Per channel		22.5		Degrees
Output DC Bias (Single-Ended)	CWI+, CWI−, CWQ+, CWQ−		1.5		V
Output AC Current Range	Per CWI+, CWI−, CWQ+, CWQ−, each channel enabled			±1.25	mA
Transconductance (Differential)	Demodulated I_{OUT}/V_{IN}, per CWI+, CWI−, CWQ+, CWQ−				
	LNA gain = 15.6 dB		1.8		mA/V
	LNA gain = 17.9 dB		2.4		mA/V
	LNA gain = 21.3 dB		3.5		mA/V

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Input-Referred Noise Voltage	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		2.0		nV/√Hz
	LNA gain = 17.9 dB		1.9		nV/√Hz
	LNA gain = 21.3 dB		1.8		nV/√Hz
Noise Figure	R_S = 50 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		7.8		dB
	LNA gain = 17.9 dB		7.3		dB
	LNA gain = 21.3 dB		6.9		dB
Input-Referred Dynamic Range	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		162		dBFS/√Hz
	LNA gain = 17.9 dB		160		dBFS/√Hz
	LNA gain = 21.3 dB		157		dBFS/√Hz
Output-Referred SNR	−3 dBFS input, f_{RF} = 2.5 MHz, f_{4LO} = 10 MHz, 1 kHz offset		153		dBc/√Hz
Two-Tone Intermodulation (IMD3)	f_{RF1} = 5.015 MHz, f_{RF2} = 5.020 MHz, f_{4LO} = 20 MHz, A_{RF1} = −1 dBFS, A_{RF2} = −21 dBFS, IMD3 relative to A_{RF2}		−58		dB
Quadrature Phase Error	I to Q, all phases, 1 σ		0.15		Degrees
I/Q Amplitude Imbalance	I to Q, all phases, 1 σ		0.015		dB
Channel-to-Channel Matching	Phase I to I, Q to Q, 1 σ		0.5		Degrees
	Amplitude I to I, Q to Q, 1 σ		0.25		dB
POWER SUPPLY, MODE I/II/III/IV					
AVDD1		1.7	1.8	1.9	V
AVDD2[3]		2.7	3.0	3.6	V
DRVDD		1.7	1.8	1.9	V
I_{AVDD1}	TGC mode		178/145/ 215/260		mA
	CW Doppler mode		32		mA
I_{AVDD2}	TGC mode, no signal		108		mA
	CW Doppler mode		63		mA
I_{DRVDD}	ANSI-644 mode		47/44/48/53		mA
	Low power (IEEE 1596.3 similar) mode		33/31/34/38		
Total Power Dissipation (Including Output Drivers)	TGC mode, no signal		704/640/ 772/860	815/755/ 908/996	mW
	CW Doppler mode		252		mW
Power-Down Dissipation				5	mW
Standby Power Dissipation			420		mW
Power Supply Rejection Ratio (PSRR)			1.6		mV/V
ADC RESOLUTION			12		Bits
ADC REFERENCE					
Output Voltage Error	VREF = 1 V			±50	mV
Load Regulation at 1.0 mA	VREF = 1 V		2		mV
Input Resistance			6		kΩ

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.
[2] The overrange condition is specified as 6 dB more than the full-scale input range.
[3] When the LNA gain is set to 15.6 dB, AVDD2 ≥3.0 V.

DIGITAL SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, full temperature, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
CW 4LO INPUTS (4LO+, 4LO−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
LOGIC INPUTS (PDWN, STBY, SCLK, RESET)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		70		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full	1.2		DRVDD + 0.3	V
Logic 0 Voltage (I_{OL} = 50 µA)	Full	0		0.3	V
Input Resistance	25°C		30		
Input Capacitance	25°C		2		
DIGITAL OUTPUTS (DOUTx+, DOUTx−), (ANSI-644)					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V
Output Coding (Default)			Offset binary		
DIGITAL OUTPUTS (DOUTx+, DOUTx−), (LOW POWER, REDUCED SIGNAL OPTION)					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	V
Output Coding (Default)			Offset binary		
LOGIC OUTPUT (GPO0/GPO1/GPO2/GPO3)					
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, full temperature, unless otherwise noted.

Table 3.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK[2]					
Clock Rate					
25 MSPS (Mode II)	Full	18.5		25	MHz
40 MSPS (Mode I)	Full	18.5		40	MHz
50 MSPS (Mode III)	Full	18.5		50	MHz
65 MSPS (Mode IV)	Full	18.5		65	MHz
Clock Pulse Width High (t_{EH})	Full		4.8		ns
Clock Pulse Width Low (t_{EL})	Full		4.8		ns
OUTPUT PARAMETERS[2, 3]					
Propagation Delay (t_{PD})	Full	(t_{SAMPLE}/2) + 1.5	(t_{SAMPLE}/2) + 2.3	(t_{SAMPLE}/2) + 3.1	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO Propagation Delay (t_{FCO})	Full	(t_{SAMPLE}/2) + 1.5	(t_{SAMPLE}/2) + 2.3	(t_{SAMPLE}/2) + 3.1	ns
DCO Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/24)		ns
DCO to Data Delay (t_{DATA})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
DCO to FCO Delay (t_{FRAME})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
Data-to-Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±100	±350	ps
Wake-Up Time (Standby), GAIN+ = 0.5 V	25°C		2		µs
Wake-Up Time (Power-Down)	25°C		1		ms
Pipeline Latency	Full		8		Clock cycles
APERTURE					
Aperture Uncertainty (Jitter)	25°C		<1		ps rms
LO GENERATION					
4LO Frequency	Full	4		40	MHz
LO Divider RESET Setup Time[5]	Full	5			ns
LO Divider RESET Hold Time[5]	Full	5			ns
LO Divider RESET High Pulse Width	Full	20			ns

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.
[2] Can be adjusted via the SPI.
[3] Measurements were made using a part soldered to FR-4 material.
[4] t_{SAMPLE}/24 is based on the number of bits divided by 2 because the delays are based on half duty cycles.
[5] RESET edge to rising 4LO edge.

ADC TIMING DIAGRAMS

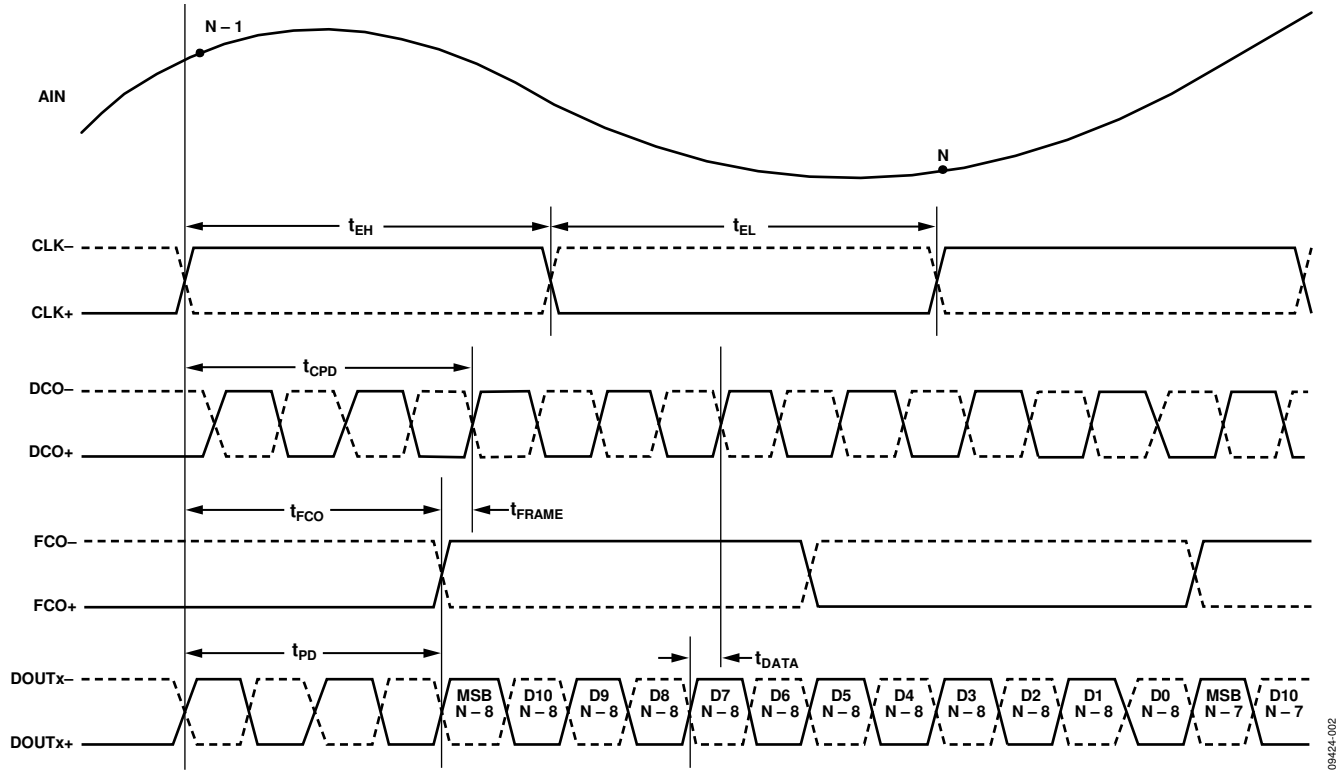

Figure 2. 12-Bit Data Serial Stream (Default)

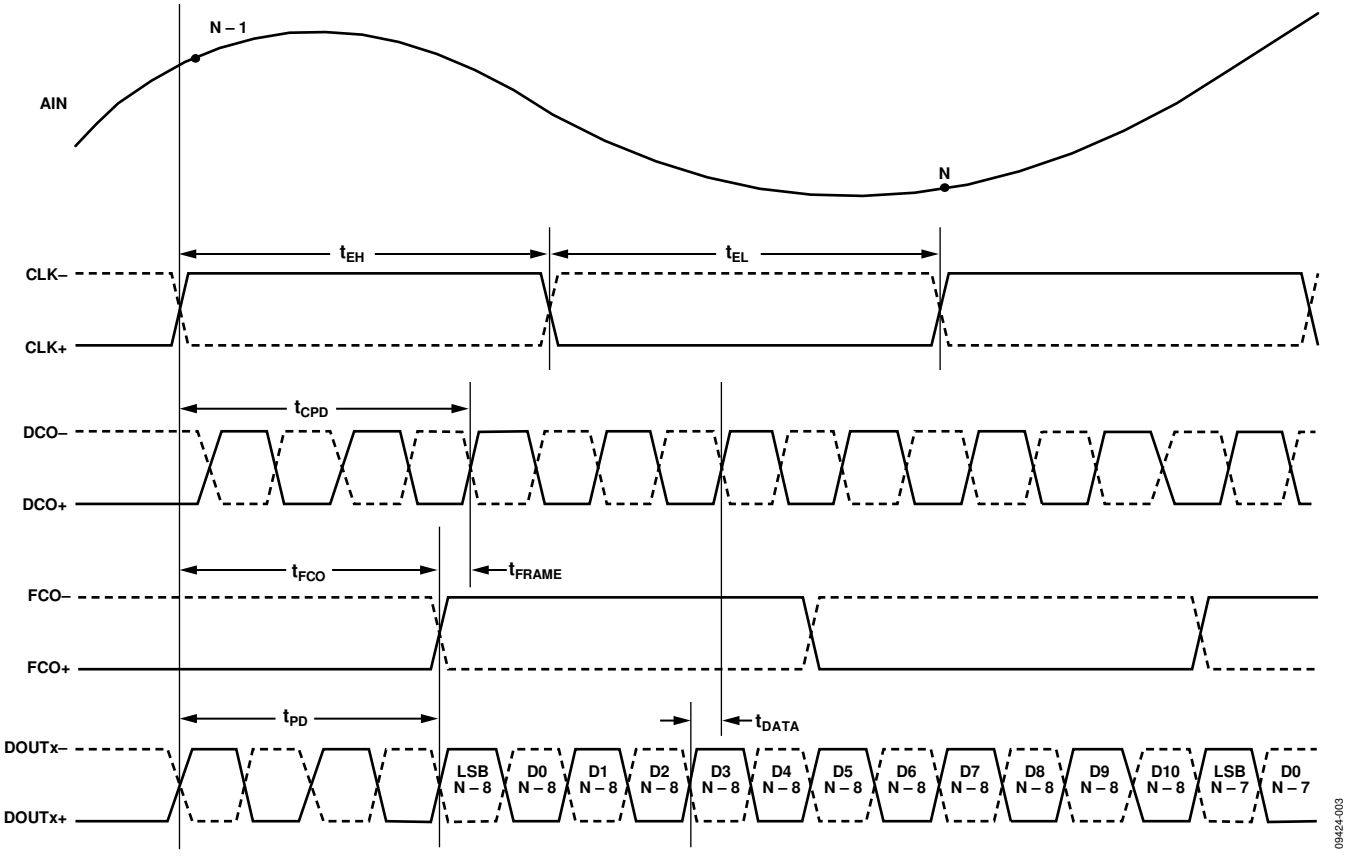

Figure 3. 12-Bit Data Serial Stream, LSB First

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD1 to GND	−0.3 V to +2.0 V
AVDD2 to GND	−0.3 V to +3.9 V
DRVDD to GND	−0.3 V to +2.0 V
GND to GND	−0.3 V to +0.3 V
AVDD2 to AVDD1	−2.0 V to +3.9 V
AVDD1 to DRVDD	−2.0 V to +2.0 V
AVDD2 to DRVDD	−2.0 V to +3.9 V
Digital Outputs (DOUTx+, DOUTx−, DCO+, DCO−, FCO+, FCO−) to GND	−0.3 V to DRVDD + 0.3 V
CLK+, CLK−, SDIO to GND	−0.3 V to AVDD1 + 0.3 V
LI-x, LO-x, LOSW-x to GND	−0.3 V to AVDD2 + 0.3 V
CWI−, CWI+, CWQ−, CWQ+ to GND	−0.3 V to AVDD2 + 0.3 V
PDWN, STBY, SCLK, CSB to GND	−0.3 V to AVDD1 + 0.3 V
GAIN+, GAIN−, RESET, 4LO+, 4LO−, GPO0, GPO1, GPO2, GPO3 to GND	−0.3 V to AVDD2 + 0.3 V
VREF to GND	−0.3 V to AVDD1 + 0.3 V
Operating Temperature Range (Ambient)	−40°C to +85°C
Storage Temperature Range (Ambient)	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE

Table 5.

Symbol	Description	Value[1]	Units
θ_{JA}	Junction-to-ambient thermal resistance, 0.0 m/s air flow per JEDEC JESD51-2 (still air)	22.0	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter, 0 m/s air flow per JEDEC JESD51-8 (still air)	9.2	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 m/s air flow per JEDEC JESD51-2 (still air)	0.12	°C/W

[1] Results are from simulations. PCB is JEDEC multilayer. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12
A	LI-E	LI-F	LI-G	LI-H	VREF	RBIAS	GAIN+	GAIN–	LI-A	LI-B	LI-C	LI-D
B	LG-E	LG-F	LG-G	LG-H	GND	GND	AVDD2	GND	LG-A	LG-B	LG-C	LG-D
C	LO-E	LO-F	LO-G	LO-H	GND	GND	GND	GND	LO-A	LO-B	LO-C	LO-D
D	LOSW-E	LOSW-F	LOSW-G	LOSW-H	GND	GND	GND	GND	LOSW-A	LOSW-B	LOSW-C	LOSW-D
E	GND	AVDD2	AVDD2	AVDD2	GND	GND	GND	GND	AVDD2	AVDD2	AVDD2	GND
F	AVDD1	GND	AVDD1	GND	AVDD1	GND	GND	AVDD1	GND	AVDD1	GND	AVDD1
G	GND	AVDD1	GND	AVDD1	GND	GND	GND	GND	AVDD1	GND	AVDD1	GND
H	CLK–	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	CSB
J	CLK+	GND	CWQ+	GND	CWI+	AVDD2	4LO+	GND	GPO3	GPO1	PDWN	SDIO
K	GND	GND	CWQ–	GND	CWI–	AVDD2	4LO–	RESET	GPO2	GPO0	STBY	SCLK
L	DRVDD	DOUTH+	DOUTG+	DOUTF+	DOUTE+	DCO+	FCO+	DOUTD+	DOUTC+	DOUTB+	DOUTA+	DRVDD
M	GND	DOUTH–	DOUTG–	DOUTF–	DOUTE–	DCO–	FCO–	DOUTD–	DOUTC–	DOUTB–	DOUTA–	GND

09424-004

Figure 4. Pin Configuration

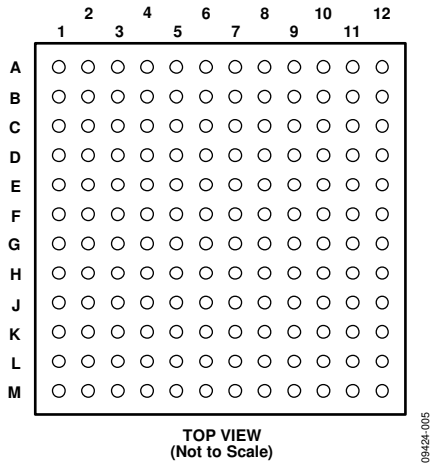

Figure 5.

Table 6. Pin Function Descriptions

Pin No.	Name	Description
B5, B6, B8, C5, C6, C7, C8, D5, D6, D7, D8, E1, E5, E6, E7, E8, E12, F2, F4, F6, F7, F9, F11, G1, G3, G5, G6, G7, G8, G10, G12, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, J2, J4, J8, K1, K2, K4, M1, M12	GND	Ground (should be tied to a quiet analog ground)
F1, F3, F5, F8, F10, F12, G2, G4, G9, G11	AVDD1	1.8 V Analog Supply
B7, E2, E3, E4, E9, E10, E11, J6, K6	AVDD2	3.0 V Analog Supply
L1, L12	DRVDD	1.8 V Digital Output Driver Supply
A1	LI-E	LNA Analog Input for Channel E
B1	LG-E	LNA Ground for Channel E
C2	LO-F	LNA Analog Inverted Output for Channel F
D2	LOSW-F	LNA Analog Switched Output for Channel F
A2	LI-F	LNA Analog Input for Channel F
B2	LG-F	LNA Ground for Channel F
C3	LO-G	LNA Analog Inverted Output for Channel G
D3	LOSW-G	LNA Analog Switched Output for Channel G
A3	LI-G	LNA Analog Input for Channel G
B3	LG-G	LNA Ground for Channel G
C4	LO-H	LNA Analog Inverted Output for Channel H
D4	LOSW-H	LNA Analog Switched Output for Channel H
A4	LI-H	LNA Analog Input for Channel H
B4	LG-H	LNA Ground for Channel H
H1	CLK–	Clock Input Complement
J1	CLK+	Clock Input True
M2	DOUTH–	ADC H Digital Output Complement
L2	DOUTH+	ADC H Digital Output True
M3	DOUTG–	ADC G Digital Output Complement
L3	DOUTG+	ADC G Digital Output True
M4	DOUTF–	ADC F Digital Output Complement
L4	DOUTF+	ADC F Digital Output True
M5	DOUTE–	ADC E Digital Output Complement
L5	DOUTE+	ADC E Digital Output True
M6	DCO–	Digital Clock Output Complement
L6	DCO+	Digital Clock Output True
M7	FCO–	Frame Clock Digital Output Complement
L7	FCO+	Frame Clock Digital Output True
M8	DOUTD–	ADC D Digital Output Complement
L8	DOUTD+	ADC D Digital Output True
M9	DOUTC–	ADC C Digital Output Complement
L9	DOUTC+	ADC C Digital Output True
M10	DOUTB–	ADC B Digital Output Complement
L10	DOUTB+	ADC B Digital Output True
M11	DOUTA–	ADC A Digital Output Complement
L11	DOUTA+	ADC A Digital Output True
K11	STBY	Standby Power-Down
J11	PDWN	Full Power-Down
K12	SCLK	Serial Clock
J12	SDIO	Serial Data Input/Output
H12	CSB	Chip Select Bar
B9	LG-A	LNA Ground for Channel A
A9	LI-A	LNA Analog Input for Channel A
D9	LOSW-A	LNA Analog Switched Output for Channel A
C9	LO-A	LNA Analog Inverted Output for Channel A

Pin No.	Name	Description
B10	LG-B	LNA Ground for Channel B
A10	LI-B	LNA Analog Input for Channel B
D10	LOSW-B	LNA Analog Switched Output for Channel B
C10	LO-B	LNA Analog Inverted Output for Channel B
B11	LG-C	LNA Ground for Channel C
A11	LI-C	LNA Analog Input for Channel C
D11	LOSW-C	LNA Analog Switched Output for Channel C
C11	LO-C	LNA Analog Inverted Output for Channel C
B12	LG-D	LNA Ground for Channel D
A12	LI-D	LNA Analog Input for Channel D
D12	LOSW-D	LNA Analog Switched Output for Channel D
C12	LO-D	LNA Analog Inverted Output for Channel D
K10	GPO0	General Purpose Open Drain Output 0
J10	GPO1	General Purpose Open Drain Output 1
K9	GPO2	General Purpose Open Drain Output 2
J9	GPO3	General Purpose Open Drain Output 3
K8	RESET	Reset for Synchronizing 4LO Divide-by-4 Counter
K7	4LO−	CW Doppler 4LO Input Complement
J7	4LO+	CW Doppler 4LO Input True
A8	GAIN−	Gain Control Voltage Input Complement
A7	GAIN+	Gain Control Voltage Input True
A6	RBIAS	External Resistor to Set the Internal ADC Core Bias Current
A5	VREF	Voltage Reference Input/Output
K5	CWI−	CW Doppler I Output Complement
J5	CWI+	CW Doppler I Output True
K3	CWQ−	CW Doppler Q Output Complement
J3	CWQ+	CW Doppler Q Output True
C1	LO-E	LNA Analog Inverted Output for Channel E
D1	LOSW-E	LNA Analog Switched Output for Channel E

TYPICAL PERFORMANCE CHARACTERISTICS

TGC MODE

f_{SAMPLE} = 40 MSPS, f_{IN} = 5 MHz, R_S = 50 Ω, LNA gain = 21.3 dB, LNA bias = mid-high, PGA gain = 24 dB, GAIN− = 0.8 V, AAF LPF cutoff = f_{SAMPLE}/3.0, HPF cutoff = LPF cutoff/12.00 (default).

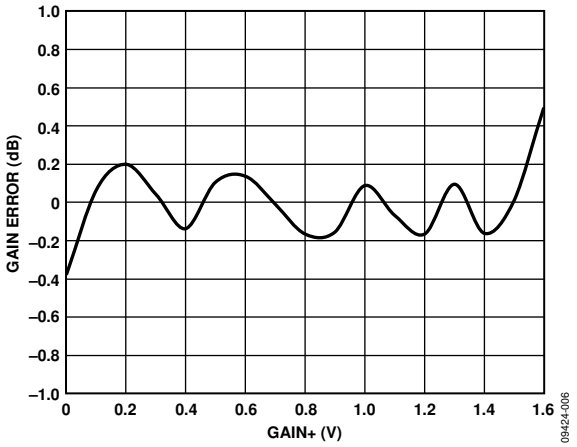

Figure 6. Gain Error vs. GAIN+

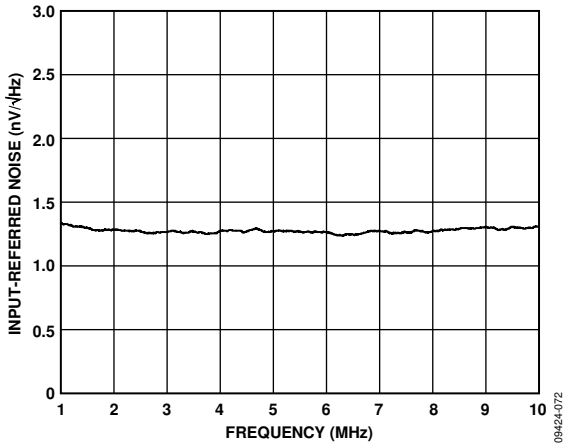

Figure 9. Short-Circuit, Input-Referred Noise vs. Frequency, LNA Gain = 21.3 dB, PGA Gain = 30 dB, GAIN+ = 1.6 V

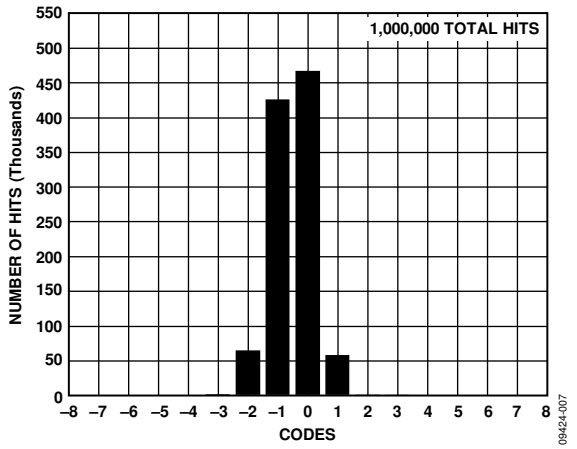

Figure 7. Output-Referred Noise Histogram, GAIN+ = 0.0 V

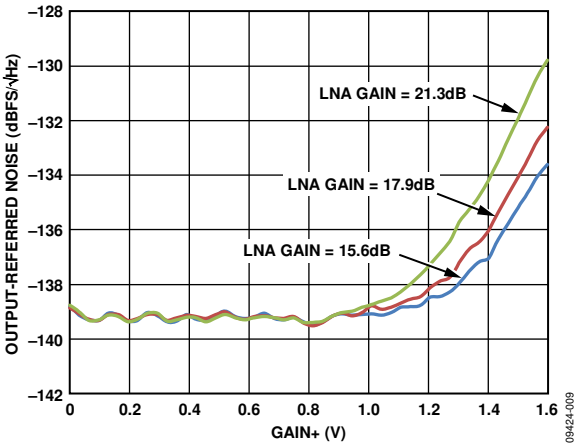

Figure 10. Short-Circuit, Output-Referred Noise vs. GAIN+

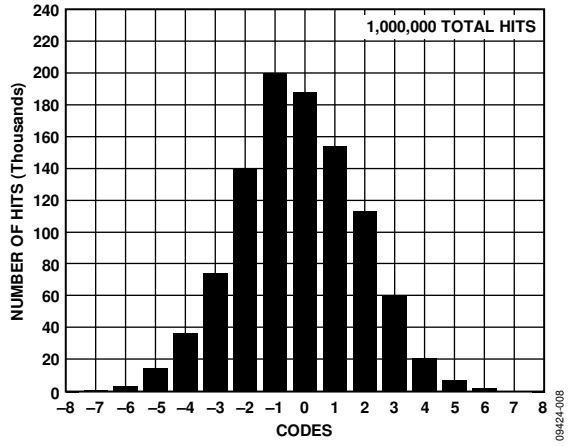

Figure 8. Output-Referred Noise Histogram, GAIN+ = 1.6 V

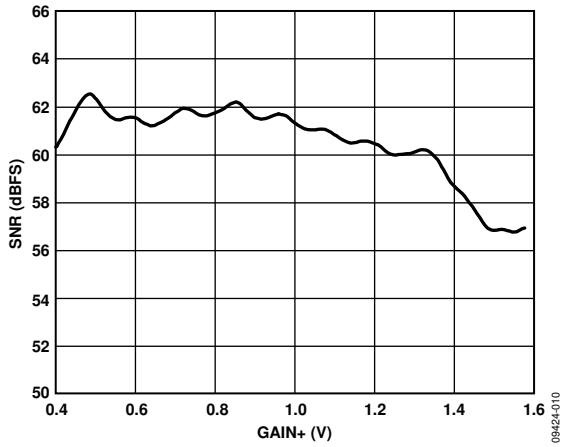

Figure 11. SNR vs. GAIN+, AOUT = −1.0 dBFS

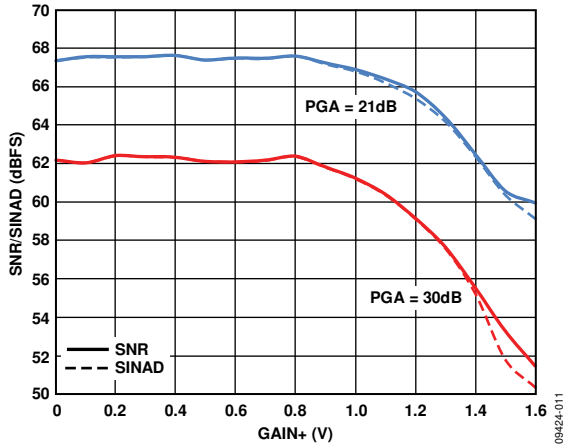

Figure 12. SNR/SINAD vs. GAIN+, AIN = −45 dBm

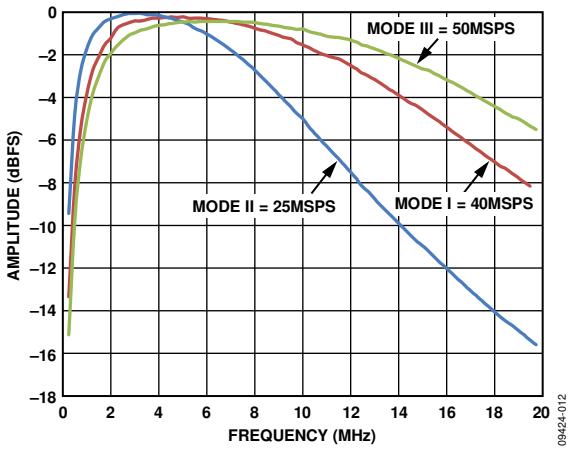

Figure 13. Antialiasing Filter (AAF) Pass-Band Response, LPF Cutoff = 1 × (1/3) × f_{SAMPLE}

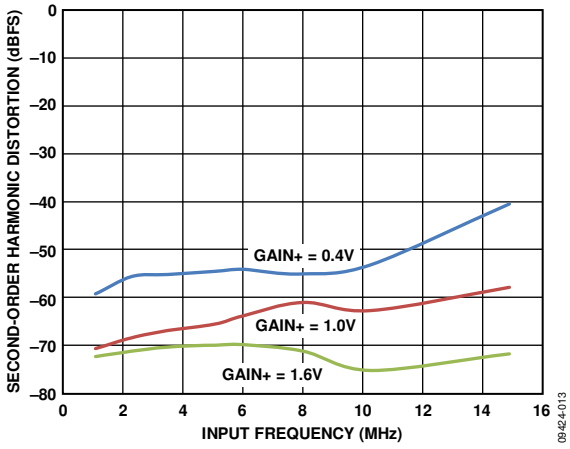

Figure 14. Second-Order Harmonic Distortion vs. Frequency, AOUT = −1.0 dBFS

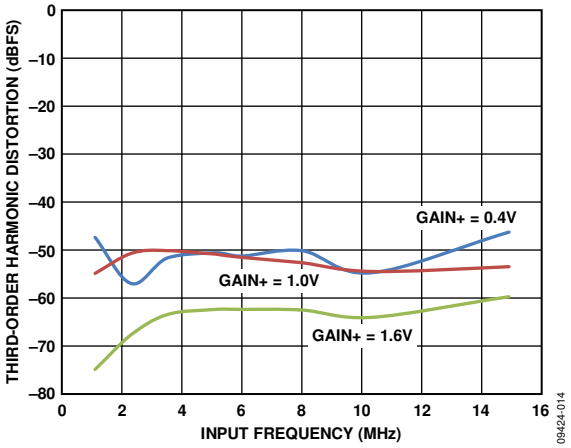

Figure 15. Third-Order Harmonic Distortion vs. Frequency, AOUT = −1.0 dBFS

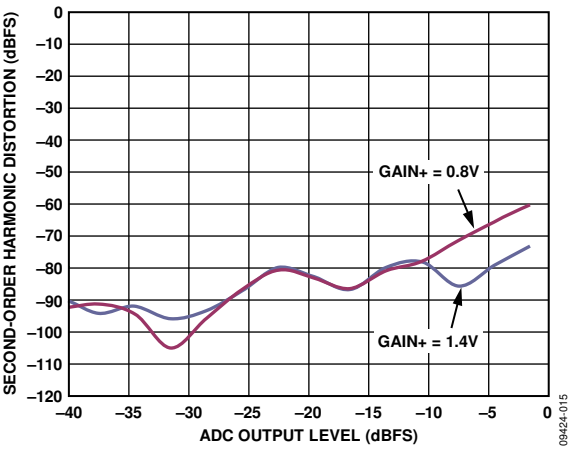

Figure 16. Second-Order Harmonic Distortion vs. ADC Output Level, AOUT

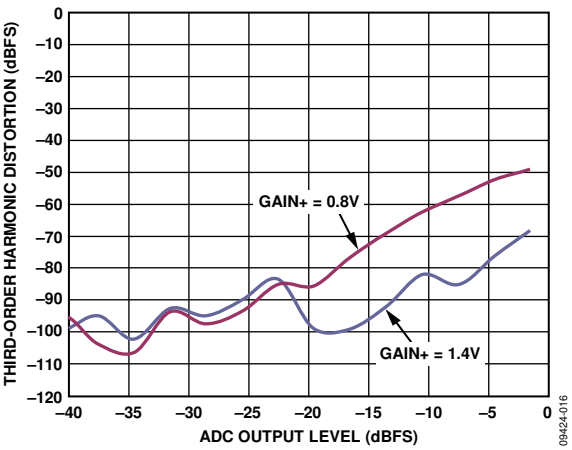

Figure 17. Third-Order Harmonic Distortion vs. ADC Output Level

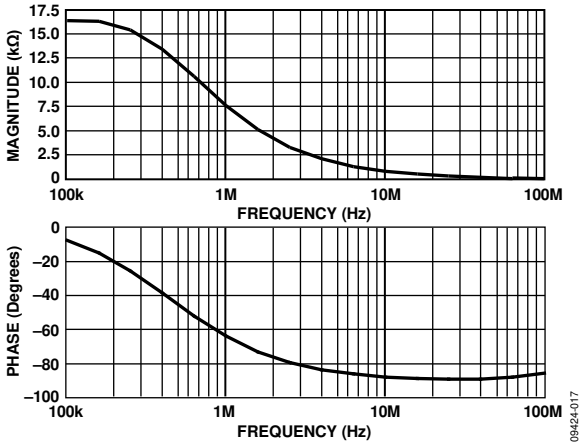

Figure 18. LNA Input Impedance Magnitude and Phase, Unterminated

CW DOPPLER MODE

f_{IN} = 5 MHz, R_S = 50 Ω, LNA gain = 21.3 dB, LNA bias = mid-high, all CW channels enabled, phase rotation 0 degrees.

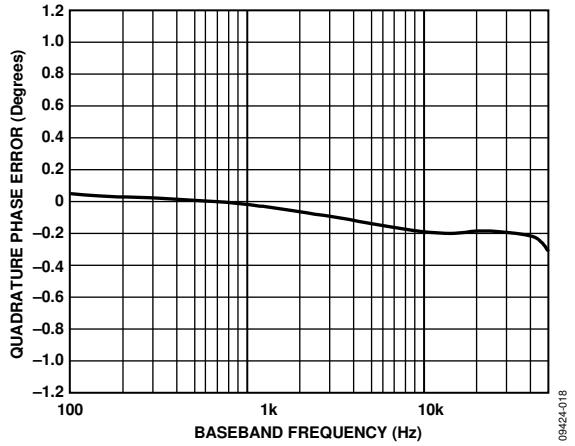

Figure 19. Quadrature (I/Q) Phase Error vs. Baseband Frequency

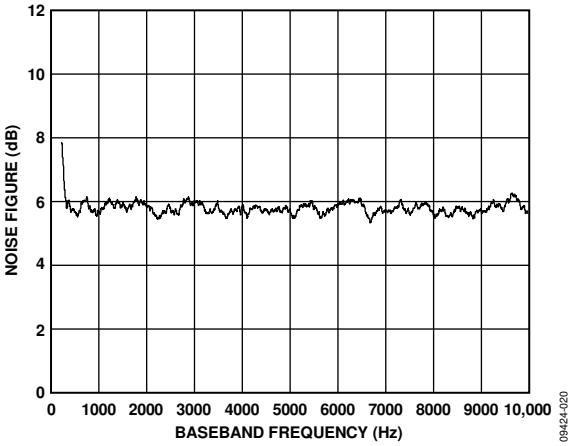

Figure 21. Noise Figure vs. Baseband Frequency

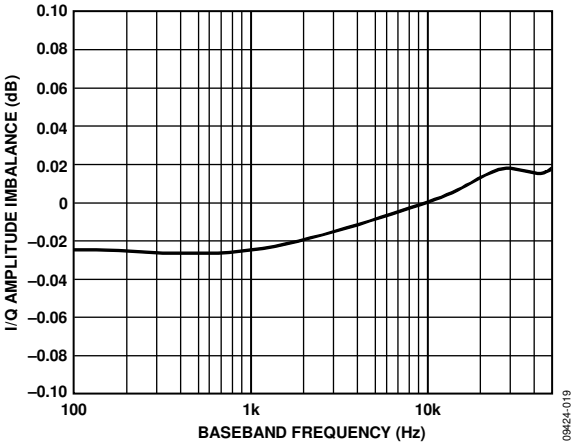

Figure 20. Quadrature (I/Q) Amplitude Error vs. Baseband Frequency

EQUIVALENT CIRCUITS

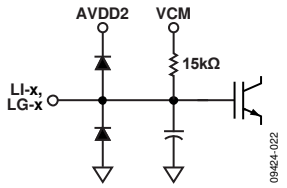

Figure 22. Equivalent LNA Input Circuit (VCM = Common-Mode Voltage)

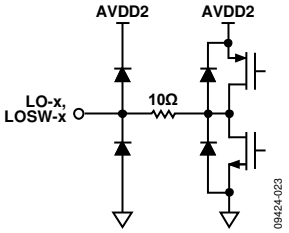

Figure 23. Equivalent LNA Output Circuit

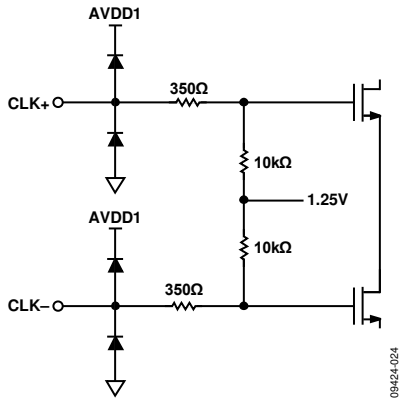

Figure 24. Equivalent Clock Input Circuit

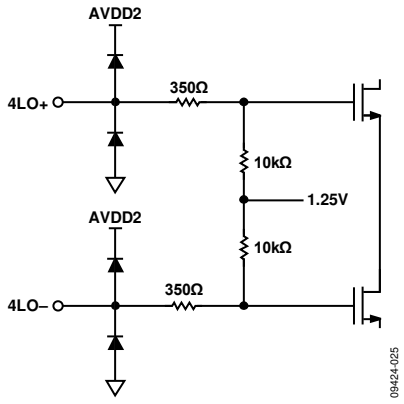

Figure 25. Equivalent 4LO Input Circuit

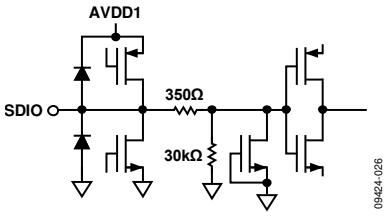

Figure 26. Equivalent SDIO Input Circuit

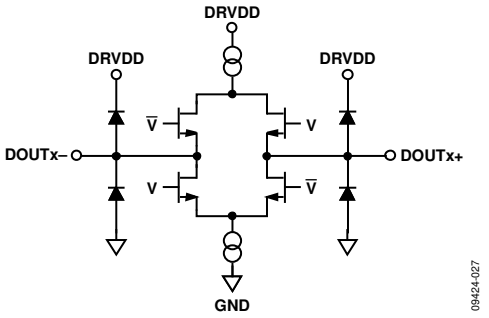

Figure 27. Equivalent Digital Output Circuit

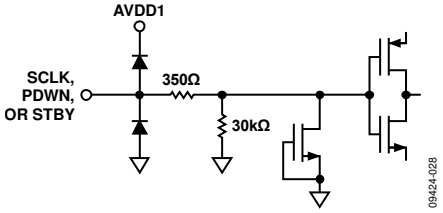

Figure 28. Equivalent SCLK, PDWN, or STBY Input Circuit

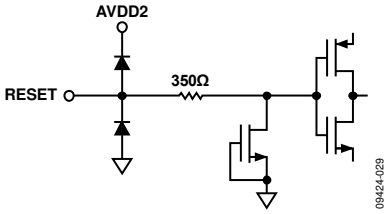

Figure 29. Equivalent RESET Input Circuit

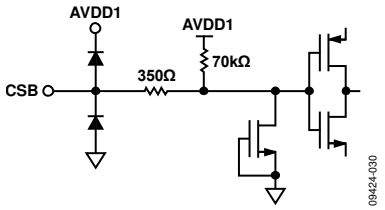

Figure 30. Equivalent CSB Input Circuit

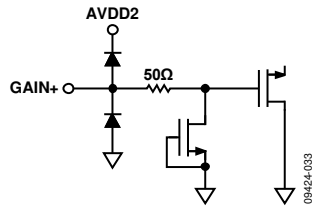

Figure 33. Equivalent GAIN+ Input Circuit

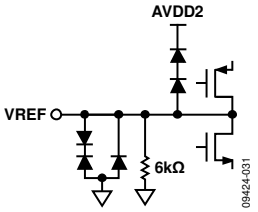

Figure 31. Equivalent VREF Circuit

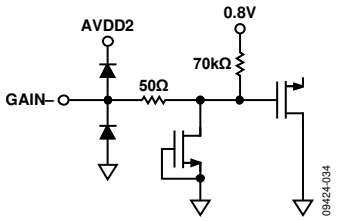

Figure 34. Equivalent GAIN– Input Circuit

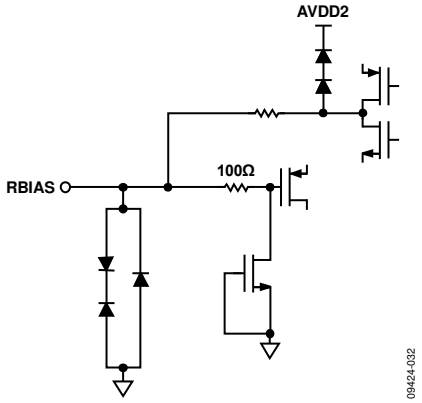

Figure 32. Equivalent RBIAS Circuit

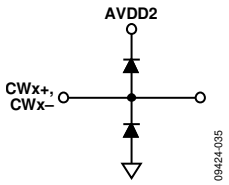

Figure 35. Equivalent CWI±, CWQ± Output Circuit

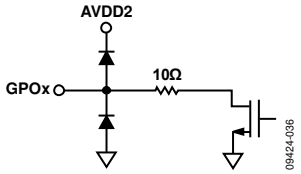

Figure 36. Equivalent GPOx Output Circuit

ULTRASOUND THEORY OF OPERATION

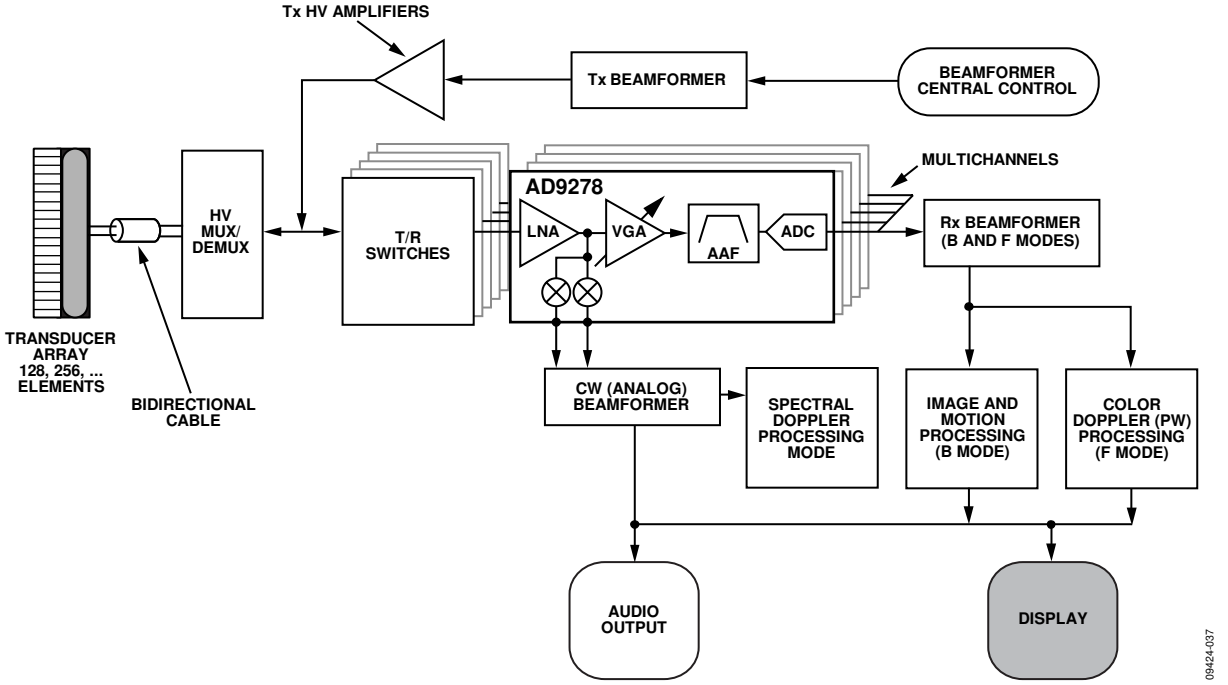

Figure 37. Simplified Ultrasound System Block Diagram

The primary application for the AD9278 is medical ultrasound. Figure 37 shows a simplified block diagram of an ultrasound system. A critical function of an ultrasound system is the time gain control (TGC) compensation for physiological signal attenuation. Because the attenuation of ultrasound signals is exponential with respect to distance (time), a linear-in-dB VGA is the optimal solution.

Key requirements in an ultrasound signal chain are very low noise, active input termination, fast overload recovery, low power, and differential drive to an ADC. Because ultrasound machines use beamforming techniques requiring large binary-weighted numbers of channels (for example, 32 to 512), using the lowest power at the lowest possible noise is of chief importance.

Most modern ultrasound machines use digital beamforming. In this technique, the signal is converted to digital format immediately following the TGC amplifier, and then beamforming is accomplished digitally.

The ADC resolution of 12 bits with up to 50 MSPS sampling satisfies the requirements of both general-purpose and high end systems. The power dissipation of the ADC scales with programmable speed modes for optimum power performance depending on system architecture.

Power conservation, high performance, and low cost are three of the most important factors in low end and portable ultrasound machines, and the AD9278 is designed to meet these criteria.

For additional information regarding ultrasound systems, see "How Ultrasound System Considerations Influence Front-End Component Choice," *Analog Dialogue*, Volume 36, Number 3, May–July 2002, and "The AD9271—A Revolutionary Solution for Portable Ultrasound," *Analog Dialogue*, Volume 41, Number 7, July 2007.

CHANNEL OVERVIEW

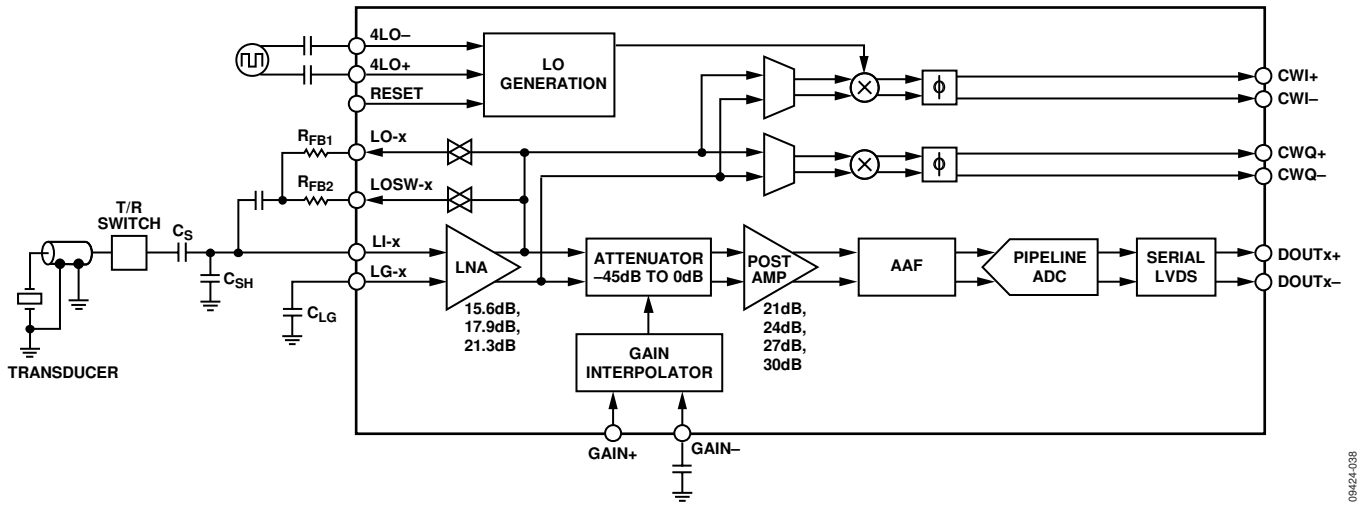

Figure 38. Simplified Block Diagram of a Single Channel

Each channel contains both a TGC signal path and a CW Doppler signal path. Common to both signal paths, the LNA provides four user-adjustable input impedance termination options for matching different probe impedances. The CW Doppler path includes an I/Q demodulator with programmable phase rotation needed for analog beamforming. The TGC path includes a differential X-AMP® VGA, an antialiasing filter, and an ADC. Figure 38 shows a simplified block diagram with external components.

TGC OPERATION

The TGC signal path is fully differential throughout to maximize signal swing and reduce even-order distortion; however, the LNAs are designed to be driven from a single-ended signal source. Gain values are referenced from the single-ended LNA input to the differential ADC input. A simple exercise in understanding the maximum and minimum gain requirements is shown in Figure 39.

The maximum gain required is determined by

(*ADC Noise Floor*/*LNA Input Noise Floor*) + *Margin* =
20 log(224/5.8) + 11 dB = 42 dB

The minimum gain required is determined by

(*ADC Input FS*/*LNA Input FS*) + *Margin* =
20 log(2/0.45) − 10 dB = 3 dB

Therefore, 42 dB of gain range for a 12-bit, 40 MSPS ADC with 15 MHz of bandwidth should suffice in achieving the dynamic range required for most of today's ultrasound systems.

The system gain is distributed as listed in Table 7.

Table 7. Channel Gain Distribution

Section	Nominal Gain (dB)
LNA	15.6/17.9/21.3
Attenuator	0 to −45
VGA Amplifier	21/24/27/30
Filter	0
ADC	0

The linear-in-dB gain (law conformance) range of the TGC path is 45 dB. The slope of the gain control interface is 28 dB/V, and the gain control range is −0.8 V to +0.8 V. Equation 3 is the expression for the differential voltage, V_{GAIN}, at the gain control interface. Equation 4 is the expression for the VGA attenuation, VGA_{ATT}, as a function of V_{GAIN}.

$$V_{GAIN}\,(\mathrm{V}) = (GAIN+) - (GAIN-) \quad (3)$$

$$VGA_{ATT}\,(\mathrm{dB}) = -28\frac{\mathrm{dB}}{\mathrm{V}}(0.8 - V_{GAIN}) \quad (4)$$

The total channel gain can then be calculated as in Equation 5.

$$ChannelGain\,(\mathrm{dB}) = LNA_{GAIN} + VGA_{ATT} + PGA_{GAIN} \quad (5)$$

In its default condition, the LNA has a gain of 21.3 dB (12×), and the VGA postamp gain is 24 dB if the voltage on the GAIN+ pin is 0 V and the voltage on the GAIN− pin is 0.8 V (42 dB attenuation). This results in a total gain (or ICPT) of 3.6 dB through the TGC path if the LNA input is unmatched or a total gain of −2.4 dB if the LNA is matched to 50 Ω (R_{FB} = 350 Ω). However, if the voltage on the GAIN+ pin is 1.6 V and the voltage on the GAIN− pin is 0.8 V (0 dB attenuation), the VGA gain is 24 dB. This results in a total gain of 45 dB through the TGC path if the LNA input is unmatched or in a total gain of 39 dB if the LNA input is matched.

Each LNA output is dc-coupled to a VGA input. The VGA consists of an attenuator with a range of −42 dB, followed by an amplifier with 21 dB/24 dB/27 dB/30 dB of gain. The X-AMP gain interpolation technique results in low gain error and uniform bandwidth, and differential signal paths minimize distortion.

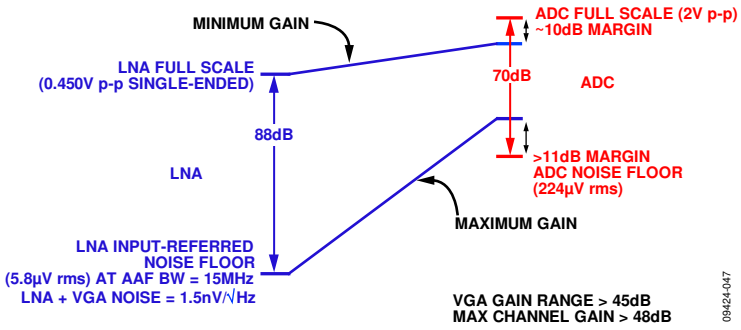

Figure 39. Gain Requirements of TGC Operation for a 12-Bit, 40 MSPS ADC

Table 8. Sensitivity and Dynamic Range of Trade-Offs[1, 2, 3]

LNA				VGA	Channel		
Gain					Typical Output Dynamic Range (dB)		
(V/V)	(dB)	Full-Scale Input (V p-p)	Input Noise (nV/√Hz)	Postamp Gain (dB)	GAIN+ = 0 V[4]	GAIN+ = 1.6 V[5]	Input-Referred Noise[6] at GAIN+ = 1.6 V (nV/√Hz)
6	15.6	0.733	1.60	21	68.6	63.6	1.863
				24	67.8	61.2	1.773
				27	66.5	58.5	1.725
				30	64.7	55.7	1.701
7.8	17.9	0.550	1.42	21	68.6	62.6	1.590
				24	67.8	60.0	1.531
				27	66.5	57.3	1.500
				30	64.7	54.4	1.485
11.6	21.3	0.367	1.27	21	68.6	60.6	1.347
				24	67.8	57.9	1.316
				27	66.5	55.0	1.301
				30	64.7	52.1	1.293

[1] LNA: output full scale = 4.4 V p-p differential.
[2] Filter: loss ~ 1 dB, NBW = 13.3 MHz, GAIN− = 0.8 V.
[3] ADC: 40 MSPS, 70 dB SNR, 2 V p-p full-scale input.
[4] Output dynamic range at minimum VGA gain (VGA dominated).
[5] Output dynamic range at maximum VGA gain (LNA dominated).
[6] Channel noise at maximum VGA gain.

Table 8 demonstrates the sensitivity and dynamic range of trade-offs that can be achieved relative to various LNA and VGA gain settings.

For example, when the VGA is set for the minimum gain voltage, the TGC path is dominated by VGA noise and achieves the maximum output SNR. However, as the postamp gain options are increased, the input-referred noise is reduced and the SNR is degraded.

If the VGA is set for the maximum gain voltage, the TGC path is dominated by LNA noise and achieves the lowest input-referred noise but with degraded output SNR. The higher the TGC (LNA + VGC) gain, the lower the output SNR. As the postamp gain is increased, the input-referred noise is reduced.

At low gains, the VGA should limit the system noise performance (SNR); at high gains, the noise is defined by the source and the LNA. The maximum voltage swing is bound by the full-scale peak-to-peak ADC input voltage (2 V p-p).

Both the LNA and VGA have full-scale limitations within each section of the TGC path. These limitations are dependent on the gain setting of each function block and on the voltage applied to the GAIN+ and GAIN− pins. The LNA has three limitations, or full-scale settings, that can be applied through the SPI. Similarly, the VGA has four postamp gain settings that can be applied through the SPI. The voltage applied to the GAIN± pins determines which amplifier (the LNA or VGA) saturates first. The maximum signal input level prior to 0.1 dB compression on the output of the LNA that can be applied as a function of voltage on the GAIN± pins for the selectable gain options of the SPI is shown in Figure 40 to Figure 42.

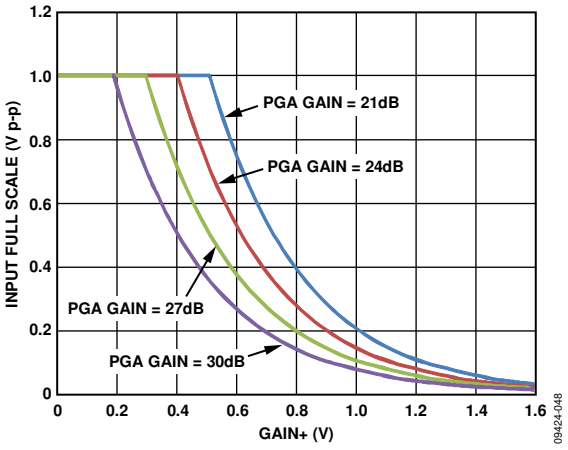

Figure 40. LNA with 15.6 dB Gain Setting/VGA Full-Scale Limitations

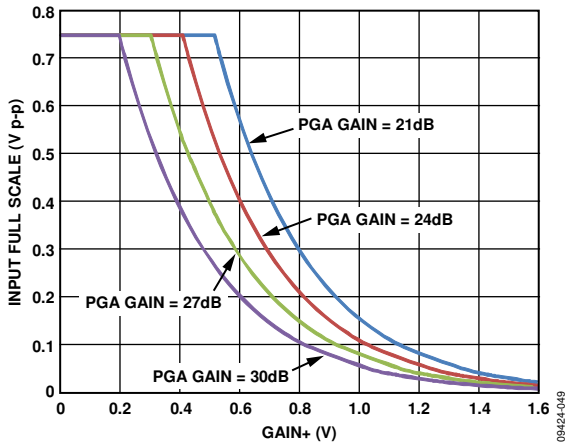

Figure 41. LNA with 17.9 dB Gain Setting/VGA Full-Scale Limitations

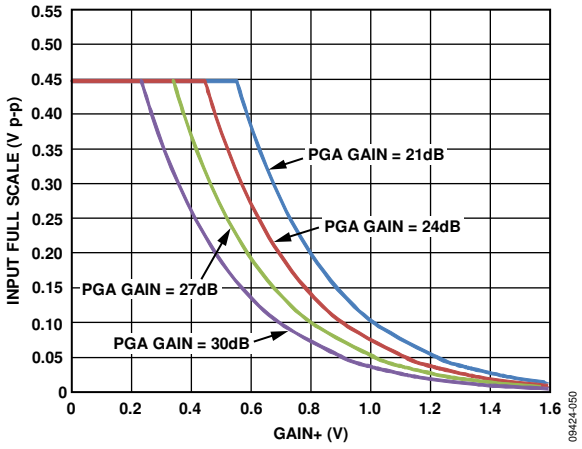

Figure 42. LNA with 21.3 dB Gain Setting/VGA Full-Scale Limitations

Low Noise Amplifier (LNA)

Good system sensitivity relies on a proprietary ultralow noise LNA at the beginning of the signal chain, which minimizes the noise contribution in the following VGA. Active impedance control optimizes noise performance for applications that benefit from input impedance matching.

The LNA input, LI-x, is capacitively coupled to the source. An on-chip bias generator establishes dc input bias voltages of approximately 2.2 V and centers the output common-mode levels at 1.5 V (AVDD2 divided by 2). A capacitor, C_{LG}, of the same value as the input coupling capacitor, C_S, is connected from the LG-x pin to ground.

It is highly recommended that the LG-x pins form a Kelvin type connection to the input or probe connection ground. Simply connecting the LG-x pin to ground near the device can allow differences in potential to be amplified through the LNA. This generally shows up as a dc offset voltage that can vary from channel to channel and part to part depending on the application and the layout of the PCB.

The LNA supports a nominal differential output voltage of 4.4 V p-p with positive and negative excursions of ±1.1 V from a common-mode voltage of 1.5 V. The LNA differential gain sets the maximum input signal before saturation. One of three gains is set through the SPI. Overload protection ensures quick recovery time from large input voltages. Because the inputs are capacitively coupled to a bias voltage near midsupply, very large inputs can be handled without interacting with the ESD protection.

Low value feedback resistors and the current-driving capability of the output stage allow the LNA to achieve a low input-referred noise voltage of 1.3 nV/√Hz (at a gain of 21.3 dB). On-chip resistor matching results in precise single-ended gains, which are critical for accurate impedance control. The use of a fully differential topology and negative feedback minimizes distortion. Low second-order harmonic distortion is particularly important in second harmonic ultrasound imaging applications. Differential signaling enables smaller swings at each output, further reducing third-order harmonic distortion.

Active Impedance Matching

The LNA consists of a single-ended voltage gain amplifier with differential outputs and the negative output externally available. For example, with a fixed gain of 8× (17.9 dB), an active input termination is synthesized by connecting a feedback resistor between the negative output pin, LO-x, and the positive input pin, LI-x. This well-known technique is used for interfacing multiple probe impedances to a single system. The input resistance is shown in Equation 1.

$$R_{IN} = \frac{R_{FB}}{(1 + A/2)} \quad (1)$$

where:
$A/2$ is the single-ended gain or the gain from the LI-x inputs to the LO-x outputs.

Because the amplifier has a gain of 8× from its input to its differential output, it is important to note that the gain, A/2, is the gain from Pin LI-x to Pin LO-x and that it is 6 dB less than the gain of the amplifier, or 12.1 dB (4×). The input resistance is reduced by an internal bias resistor of 15 kΩ in parallel with the source resistance connected to Pin LI-x, with Pin LG-x ac grounded. Equation 2 can be used to calculate the required R_{FB} for a desired R_{IN}, even for higher values of R_{IN}.

$$R_{IN} = \frac{R_{FB}}{(1+4)} || 15\,k\Omega \quad (2)$$

For example, to set R_{IN} to 200 Ω, the value of R_{FB} must be 1000 Ω. If the simplified equation (Equation 2) is used to calculate R_{IN}, the value is 197 Ω, resulting in a gain error of less than 0.11 dB. Some factors, such as the presence of a dynamic source resistance, may influence the absolute gain accuracy more significantly. At higher frequencies, the input capacitance of the LNA must be considered. The user must determine the level of matching accuracy and adjust R_{FB} accordingly.

R_{FB} is the resulting impedance of the R_{FB1} and R_{FB2} combination (see Figure 38). Using Register 0x2C in the SPI memory, the AD9278 can be programmed for four impedance matching options: three active terminations and unterminated. Table 9 shows an example of how to select R_{FB1} and R_{FB2} for 66 Ω, 100 Ω, and 200 Ω input impedance for LNA gain = 21.3 dB (12×).

Table 9. Active Termination Example for LNA Gain = 21.3 dB, R_{FB1} = 700 Ω, R_{FB2} = 1400 Ω

Register 0x2C Value	R_S (Ω)	LO-x Switch	LOSW-x Switch	R_{FB} (Ω)	R_{IN} (Ω) (Eq. 1)
00 (default)	100	On	Off	R_{FB1}	100
01	50	On	On	$R_{FB1}\|\|R_{FB2}$	66
10	200	Off	On	R_{FB2}	200
11	N/A	Off	Off	∞	∞

The bandwidth (BW) of the LNA is greater than 100 MHz. Ultimately, the BW of the LNA limits the accuracy of the synthesized R_{IN}. For $R_{IN} = R_S$ up to about 200 Ω, the best match is between 100 kHz and 10 MHz, where the lower frequency limit is determined by the size of the ac coupling capacitors, and the upper limit is determined by the LNA BW. Furthermore, the input capacitance and R_S limit the BW at higher frequencies. Figure 43 shows R_{IN} vs. frequency for various values of R_{FB}.

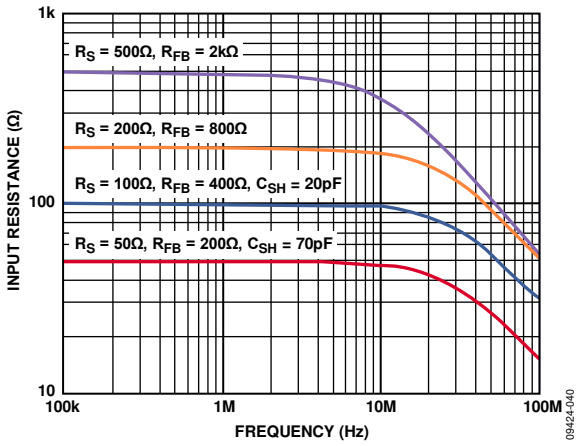

Figure 43. R_{IN} vs. Frequency for Various Values of R_{FB} (Effects of R_{SH} and C_{SH} Are Also Shown)

Note that, at the lowest value of R_{IN} (50 Ω), R_{IN} peaks at frequencies greater than 10 MHz. This is due to the BW roll-off of the LNA.

However, as can be seen for larger R_{IN} values, parasitic capacitance starts rolling off the signal BW before the LNA can produce peaking. C_{SH} further degrades the match; therefore, C_{SH} should not be used for values of R_{IN} that are greater than 100 Ω.

Table 10 lists the recommended values for R_{FB} and C_{SH} in terms of R_{IN}.

C_{FB} is needed in series with R_{FB} because the dc levels at Pin LO-x and Pin LI-x are unequal.

Table 10. Active Termination External Component Values

LNA Gain (dB)	R_{IN} (Ω)	R_{FB} (Ω)	Minimum C_{SH} (pF)	BW (MHz)
15.6	50	200	90	57
17.9	50	250	70	69
21.3	50	350	50	88
15.6	100	400	30	57
17.9	100	500	20	69
21.3	100	700	10	88
15.6	200	800	N/A	72
17.9	200	1000	N/A	72
21.3	200	1400	N/A	72

LNA Noise

The short-circuit noise voltage (input-referred noise) is an important limit on system performance. The short-circuit noise voltage for the LNA is 1.3 nV/√Hz at a gain of 21.3 dB, including the VGA noise at a VGA postamp gain of 27 dB. These measurements, which were taken without a feedback resistor, provide the basis for calculating the input noise and noise figure (NF) performance of the configurations shown in Figure 44.

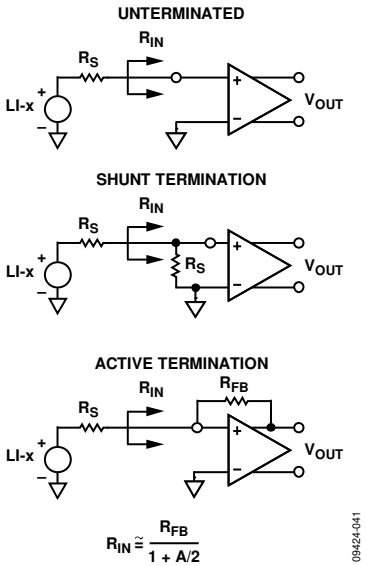

Figure 44. Input Configurations

Figure 45 and Figure 46 are simulations of noise figure vs. R_S results using these configurations and an input-referred noise voltage of 3.5 nV/√Hz for the VGA. Unterminated (R_{FB} = ∞) operation exhibits the lowest equivalent input noise and noise figure. Figure 46 shows the noise figure vs. source resistance rising at low R_S—where the LNA voltage noise is large compared with the source noise—and at high R_S due to the noise contribution from R_{FB}. The lowest NF is achieved when R_S matches R_{IN}.