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Integrated, Dual RF Transceiver with Observation Path

Data Sheet

AD9375

FEATURES

Dual differential Tx
Dual differential Rx
Observation receiver with 2 inputs
Fully integrated, ultralow power DPD actuator and adaptation engine for PA linearization
Sniffer receiver with 3 inputs
Tunable range: 300 MHz to 6000 MHz
Linearization signal BW to 40 MHz
Tx synthesis BW to 250 MHz
Rx BW: 8 MHz to 100 MHz
Supports FDD and TDD operation
Fully integrated independent fractional-N RF synthesizers for Tx, Rx, ORx, and clock generation
JESD204B digital interface

APPLICATIONS

3G/4G small cell base transceiver station (BTS)
3G/4G massive MIMO/active antenna systems

GENERAL DESCRIPTION

The AD9375 is a highly integrated, wideband radio frequency (RF) transceiver offering dual-channel transmitters (Tx) and receivers (Rx), integrated synthesizers, a fully integrated digital predistortion (DPD) actuator and adaptation engine, and digital signal processing functions. The IC delivers a versatile combination of high performance and low power consumption required by 3G/4G small cell and massive multiple input, multiple output (MIMO) equipment in both frequency division duplex (FDD) and time division duplex (TDD) applications. The AD9375 operates from 300 MHz to 6000 MHz, covering most of the licensed and unlicensed cellular bands. The DPD algorithm supports linearization on signal bandwidths up to 40 MHz depending on the power amplifier (PA) characteristics (for example, two adjacent 20 MHz carriers). The IC supports Rx bandwidths up to 100 MHz. It also supports observation receiver (ORx) and Tx synthesis bandwidths up to 250 MHz to accommodate digital correction algorithms.

The transceiver consists of wideband direct conversion signal paths with state-of-the-art noise figure and linearity. Each complete Rx and Tx subsystem includes dc offset correction, quadrature error correction (QEC), and programmable digital filters, eliminating the need for these functions in the digital baseband. Several auxiliary functions such as an auxiliary analog-to-digital converter (ADC), auxiliary digital-to-analog converters (DACs), and general-purpose input/outputs (GPIOs) are integrated to provide additional monitoring and control capability.

An ORx channel with two inputs is included to monitor each Tx output and implement calibration applications. This channel also connects to three sniffer receiver (SnRx) inputs that can monitor radio activity in different bands.

The high speed JESD204B interface supports lane rates up to 6144 Mbps. Four lanes are dedicated to the transmitters and four lanes are dedicated to the receiver and observation receiver channels.

The fully integrated phase-locked loops (PLLs) provide high performance, low power, fractional-N frequency synthesis for the Tx, the Rx, the ORx, and the clock sections. Careful design and layout techniques provide the isolation demanded in high performance base station applications. All voltage controlled oscillator (VCO) and loop filter components are integrated to minimize the external component count.

The device contains a fully integrated, low power DPD actuator and adaptation engine for use in PA linearization. The DPD feature enables use of high efficiency PAs, significantly reducing the power consumption of small cell base station radios while also reducing the number of JESD204B lanes necessary to interface with baseband processors.

A 1.3 V supply is required to power the AD9375 core, and a standard 4-wire serial port controls it. Other voltage supplies provide proper digital interface levels and optimize transmitter and auxiliary converter performance. The AD9375 is packaged in a 12 mm × 12 mm, 196-ball chip scale ball grid array (CSP_BGA).

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REVISION HISTORY

3/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

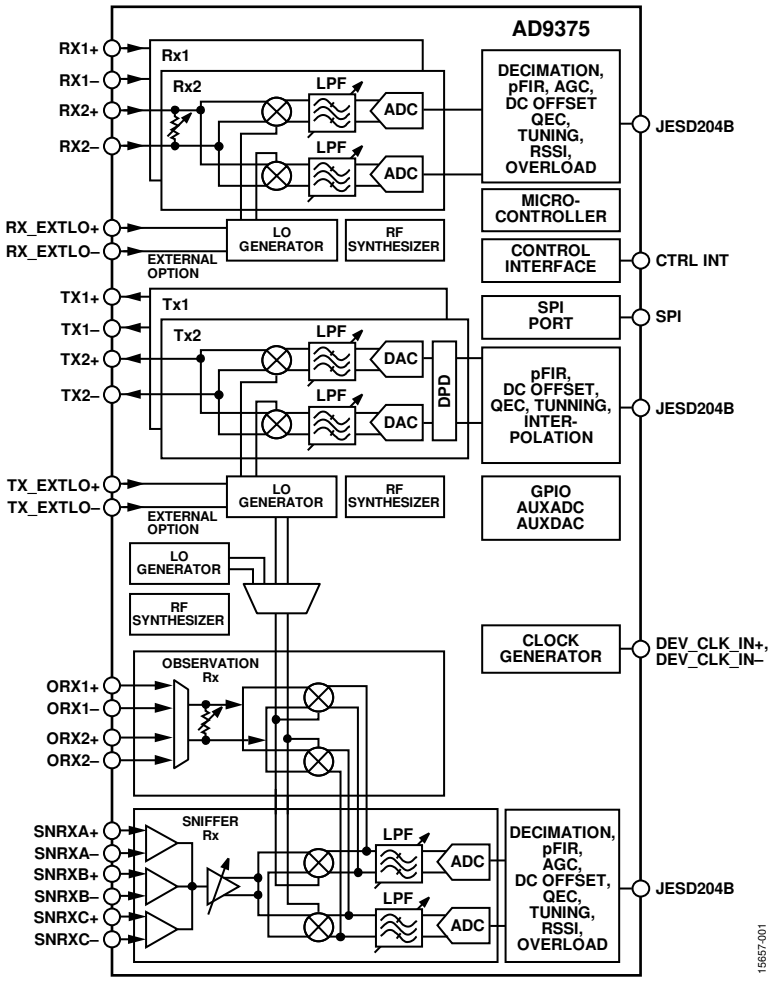

Figure 1.

SPECIFICATIONS

Electrical characteristics at ambient temperature range, VDDA_SER = 1.3 V, VDDA_DES = 1.3 V, JESD_VTT_DES = 1.3 V, VDDA_1P3[1] = 1.3 V, VDIG = 1.3 V, VDDA_1P8 = 1.8 V, VDD_IF = 2.5 V, and VDDA_3P3 = 3.3 V; all RF specifications based on measurements that include printed circuit board (PCB) and matching circuit losses, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSMITTERS (Tx)						
Center Frequency		300		6000	MHz	
Tx Large Signal Bandwidth (BW)						
Normal Operation				100	MHz	
DPD Activated				40	MHz	
Tx Synthesis BW[2]				250	MHz	Wider bandwidth for use in digital processing algorithms
BW Flatness			±0.5		dB	250 MHz BW, compensated by programmable finite impulse response (pFIR) filter
			±0.15		dB	Any 20 MHz BW span, compensated by pFIR filter
Deviation from Linear Phase			10		Degrees	250 MHz BW
Power Control Range		0		42	dB	Increased calibration time, reduced QEC[3], LOL[4] performance beyond 20 dB
Power Control Resolution			0.05		dB	
ACLR[5] (Four Universal Mobile Telecommunications System (UMTS) Carriers)						−11.2 dBFS rms, 0 dB RF attenuation
700 MHz Local Oscillator (LO)			−64		dB	
2600 MHz LO			−64		dB	
3500 MHz LO			−63		dB	
5500 MHz LO			−61		dB	
In Band Noise			−155		dBFS[6]/Hz	
Tx to Tx Isolation						
700 MHz LO			70		dB	
2600 MHz LO			65		dB	
3500 MHz LO			65		dB	
5500 MHz LO			50		dB	
Image Rejection						Up to 20 dB RF attenuation, within large signal BW, QEC[3] active
700 MHz LO			65		dB	
2600 MHz LO			65		dB	
3500 MHz LO			65		dB	
5500 MHz LO			50		dB	
Maximum Output Power						0 dBFS, 1 MHz signal input, 50 Ω load, 0 dB RF attenuation
700 MHz LO			7		dBm	
2600 MHz LO			7		dBm	
3500 MHz LO			6		dBm	
5500 MHz LO			4		dBm	
Output Third-Order Intercept Point	OIP3					−5 dBFS rms, 0 dB RF attenuation
700 MHz LO			27		dBm	
2600 MHz LO			27		dBm	
3500 MHz LO			25		dBm	
5500 MHz LO			25		dBm	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Carrier Leakage						After calibration, LOL correction active, CW[7] input signal, 3 dB RF and 3 dB digital attenuation, 40 kHz measurement BW
700 MHz LO			−81		dBFS[6]	
2600 MHz LO			−81		dBFS[6]	
3500 MHz LO			−81		dBFS[6]	
5500 MHz LO			−75		dBFS[6]	
Error Vector Magnitude (3GPP Test Signals)	EVM					Long-term evolution (LTE) 20 MHz downlink, 5 dB RF attenuation
700 MHz LO			−45		dB	
2600 MHz LO			−39		dB	
3500 MHz LO			−38.5		dB	
5500 MHz LO			−37.5		dB	
Output Impedance			50		Ω	Differential
RECEIVERS (Rx)						
Center Frequency		300		6000	MHz	
Gain Range		0		30	dB	
Analog Gain Step			0.5		dB	
BW Ripple			±0.5		dB	100 MHz BW, compensated by programmable FIR filter
			±0.2		dB	Any 20 MHz span, compensated by programmable FIR filter
Rx Bandwidth		8		100	MHz	Analog low-pass filter (LPF) BW is 20 MHz minimum, programmable FIR BW configurable over the entire range
Rx Alias Band Rejection		75			dB	Due to digital filters
Maximum Recommended Input Power[8]			−14		dBm	Input is a CW[7] signal at a 0 dB attenuation setting; this level increases decibel for decibel with attenuation
Noise Figure	NF					Maximum Rx gain, at Rx port, matching losses de-embedded
700 MHz LO			12		dB	
2600 MHz LO			13.5		dB	
3500 MHz LO			14		dB	
5500 MHz LO			18		dB	
Input Third-Order Intercept Point	IIP3					Maximum Rx gain, third-order intermodulation (IM3) 1 MHz offset from LO
700 MHz LO			22		dBm	
2600 MHz LO			22		dBm	
3500 MHz LO			20		dBm	
5500 MHz LO			20		dBm	
Input Second-Order Intercept Point	IIP2					Maximum Rx gain, second-order intermodulation (IM2) 1 MHz offset from LO
700 MHz LO			65		dBm	
2600 MHz LO			65		dBm	
3500 MHz LO			65		dBm	
5500 MHz LO			57		dBm	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Image Rejection						QEC[3] active, within Rx BW
700 MHz LO			75		dB	
2600 MHz LO			75		dB	
3500 MHz LO			75		dB	
5500 MHz LO			75		dB	
Input Impedance			200		Ω	Differential
Tx1 to Rx1 Signal Isolation and Tx2 to Rx2 Signal Isolation						
700 MHz LO			68		dB	
2600 MHz LO			68		dB	
3500 MHz LO			62		dB	
5500 MHz LO			60		dB	
Tx1 to Rx2 Signal Isolation and Tx2 to Rx1 Signal Isolation						
700 MHz LO			70		dB	
2600 MHz LO			70		dB	
3500 MHz LO			62		dB	
5500 MHz LO			60		dB	
Rx1 to Rx2 Signal Isolation						
700 MHz LO			60		dB	
2600 MHz LO			60		dB	
3500 MHz LO			60		dB	
5500 MHz LO			60		dB	
Rx Band Spurs Referenced to RF Input at Maximum Gain			−95		dBm	No more than one spur at this level per 10 MHz of Rx BW; excludes harmonics of the reference clock
Rx LO Leakage at Rx Input at Maximum Gain						Leakage decreases decibel for decibel with attenuation for first 12 dB
700 MHz LO			−65		dBm	
2600 MHz LO			−65		dBm	
3500 MHz LO			−62		dBm	
5500 MHz LO			−62		dBm	
OBSERVATION RECEIVER (ORx)						
Center Frequency		300		6000	MHz	
Gain Range		0		18	dB	
Analog Gain Step			1		dB	
BW Ripple			±0.5		dB	250 MHz RF BW, compensated by programmable FIR filter
Deviation from Linear Phase			10		Degrees	250 MHz RF BW
ORx Bandwidth				250	MHz	
ORx Alias Band Rejection		60			dB	Due to digital filters
Maximum Recommended Input Power[8]			−13		dBm	Input is a CW[7] signal at 0 dB attenuation setting; this level increases decibel for decibel with attenuation
Signal-to-Noise Ratio[9]	SNR					Maximum gain at ORx port
700 MHz LO			60		dB	
2600 MHz LO			60		dB	
3500 MHz LO			60		dB	
5500 MHz LO			59		dB	200 MHz BW, 245.76 MSPS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Third-Order Intercept Point	IIP3					Maximum ORx gain, IM3 1 MHz offset from LO
700 MHz LO			22		dBm	
2600 MHz LO			22		dBm	
3500 MHz LO			18		dBm	
5500 MHz LO			18		dBm	
Input Second-Order Intercept Point	IIP2					Maximum ORx gain, IM2 1 MHz offset from LO
700 MHz LO			65		dBm	
2600 MHz LO			65		dBm	
3500 MHz LO			65		dBm	
5500 MHz LO			60		dBm	
Image Rejection						After online tone calibration
700 MHz LO			65		dB	
2600 MHz LO			65		dB	
3500 MHz LO			65		dB	
5500 MHz LO			65		dB	
Input Impedance			200		Ω	Differential
Tx1 to ORx1 Signal and Tx2 to ORx2 Signal Isolation						
700 MHz LO			70		dB	
2600 MHz LO			70		dB	
3500 MHz LO			70		dB	
5500 MHz LO			70		dB	
Tx1 to ORx2 Signal and Tx2 to ORx1 Signal Isolation						
700 MHz LO			70		dB	
2600 MHz LO			70		dB	
3500 MHz LO			70		dB	
5500 MHz LO			70		dB	
SNIFFER RECEIVER (SnRx)						
Center Frequency		300		6000	MHz	
Gain Range		0		52	dB	
Analog Gain Step			1		dB	
BW Ripple			±0.5		dB	20 MHz RF BW, compensated by programmable FIR filter
Rx Bandwidth				20	MHz	
Rx Alias Band Rejection		60			dB	Due to digital filters
Maximum Recommended Input Power[8]			−26		dBm	Input is a CW[7] signal at 0 dB attenuation setting
Noise Figure	NF					Maximum gain at SnRx port, matching losses de-embedded
700 MHz LO			5		dB	
2600 MHz LO			5		dB	
3500 MHz LO			7		dB	
Input Third-Order Intercept Point	IIP3					Maximum gain, IM3 1 MHz offset from LO, gain control limited to the first 20 steps
700 MHz LO			1		dBm	
2600 MHz LO			1		dBm	
3500 MHz LO			1		dBm	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Second-Order Intercept Point	IIP2					Maximum gain, IM2 1 MHz offset from LO, gain control limited to the first 20 steps
700 MHz LO			45		dBm	
2600 MHz LO			45		dBm	
3500 MHz LO			45		dBm	
Image Rejection						After online tone calibration
700 MHz LO			75		dB	
2600 MHz LO			75		dB	
3500 MHz LO			75		dB	
Input Impedance			400		Ω	Differential
Tx1 to SnRx Signal and Tx2 to SnRx Signal Isolation						Applies to each SnRx input
700 MHz LO			60		dB	
2600 MHz LO			60		dB	
3500 MHz LO			60		dB	
LO SYNTHESIZER						
LO Frequency Step			2.3		Hz	1.5 GHz to 3 GHz, 76.8 MHz phase frequency detector (PFD) frequency
LO Spur			−80		dBc	Excludes integer boundary spurs 1 kHz to 100 MHz
Spot Phase Noise						
700 MHz LO						
10 kHz			−104		dBc	
100 kHz			−107		dBc	
1 MHz			−133		dBc	
2600 MHz LO						
10 kHz			−93		dBc	
100 kHz			−97		dBc	
1 MHz			−123		dBc	
3500 MHz LO						
10 kHz			−91		dBc	
100 kHz			−97		dBc	
1 MHz			−123		dBc	
5500 MHz LO						
10 kHz			−98		dBc	
100 kHz			−100		dBc	
1 MHz			−110		dBc	
Integrated Phase Noise						Integrated from 1 kHz to 100 MHz
700 MHz LO			0.20		°rms	
2600 MHz LO			0.49		°rms	
3500 MHz LO			0.55		°rms	
5500 MHz LO			0.75		°rms	
EXTERNAL LO INPUT						
Input Frequency	f_{EXTLO}	600		8000	MHz	Input frequency must be 2× the desired LO frequency
Input Signal Power		0	3	6	dBm	50 Ω matching at the source

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE CLOCK (DEV_CLK_IN SIGNAL)						
Frequency Range		10		320	MHz	
Signal Level		0.3		2.0	V p-p	AC-coupled, common-mode voltage (V_{CM}) = 618 mV; for best spurious performance, use a <1 V p-p input clock
AUXILIARY CONVERTERS						
ADC						
ADC Resolution			12		Bits	
Input Voltage						
Minimum			0.25		V	
Maximum			3.05		V	
DAC						
DAC Resolution			10		Bits	Includes four offset levels
Output Voltage						
Minimum			0.5		V	Reference voltage (V_{REF}) = 1 V
Maximum			3.0		V	V_{REF} = 2.5 V
Drive Capability			10		mA	
DIGITAL SPECIFICATIONS (CMOS), GPIO_x, RX1_ENABLE, RX2_ENABLE, TX1_ENABLE, TX2 ENABLE, SYNCINBx+, SYNCOUTB0+, GP_INTERRUPT, SDIO, SDO, SCLK, CSB, $\overline{\text{RESET}}$						
Logic Inputs						
Input Voltage						
High Level		VDD_IF × 0.8		VDD_IF	V	
Low Level		0		VDD_IF × 0.2	V	
Input Current						
High Level		−10		+10	µA	
Low Level		−10		+10	µA	
Logic Outputs						
Output Voltage						
High Level		VDD_IF × 0.8			V	
Low Level				VDD_IF × 0.2	V	
Drive Capability			3		mA	
DIGITAL SPECIFICATIONS (LVDS), SYSREF_INx±, SYNCOUTB0±, SYNCINBx± PAIRS						
Logic Inputs						
Input Voltage Range		825		1675	mV	Each differential input in the pair
Input Differential Voltage Threshold		−100		+100	mV	
Receiver Differential Input Impedance			100		Ω	Internal termination enabled
Logic Outputs						
Output Voltage						
High				1375	mV	
Low		1025			mV	
Differential			225		mV	
Offset			1200		mV	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL SPECIFICATIONS (CMOS), GPIO_3P3_x SIGNALS						
Logic Inputs						
Input Voltage						
High Level		VDDA_3P3 × 0.8		VDDA_3P3	V	
Low Level		0		VDDA_3P3 × 0.2	V	
Input Current						
High Level		−10		+10	µA	
Low Level		−10		+10	µA	
Logic Outputs						
Output Voltage						
High Level		VDDA_3P3 × 0.8			V	
Low Level				VDDA_3P3 × 0.2	V	
Drive Capability			4		mA	

[1] VDDA_1P3 refers to all analog 1.3 V supplies including the following: VDDA_BB, VDDA_CLKSYNTH, VDDA_TXLO, VDDA_RXRF, VDDA_RXSYNTH, VDDA_RXVCO, VDDA_RXTX, VDDA_TXSYNTH, VDDA_TXVCO, VDDA_CALPLL, VDDA_SNRXSYNTH, VDDA_SNRXVCO, VDDA_CLK, and VDDA_RXLO.
[2] Synthesis BW) is the extended bandwidth used by digital correction algorithms to measure conditions and generate compensation.
[3] Quadrature error correction (QEC) is the system for minimizing quadrature images of a desired signal.
[4] Local oscillator leakage (LOL) is a measure of the amount of the LO signal that is passed from a mixer with the desired signal.
[5] Adjacent channel level reduction (ACLR) is a measure of the amount of power from the desired signal leaking into an adjacent channel.
[6] dBFS represents the ratio of the actual output signal to the maximum possible output level for a continuous wave output signal at the given RF attenuation setting.
[7] Continuous wave (CW) is a single frequency signal.
[8] Note that the input signal power limit does not correspond to 0 dBFS at the digital output because of the nature of the continuous time Σ-Δ ADCs. Unlike the hard clipping characteristic of pipeline ADCs, these converters exhibit a soft overload behavior when the input approaches the maximum level.
[9] Signal-to-noise ratio is limited by the baseband quantization noise.

CURRENT AND POWER CONSUMPTION SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
SUPPLY CHARACTERISTICS					
VDDA_1P3 Analog Supplies[1]	1.267	1.3	1.33	V	
VDIG Supply	1.267	1.3	1.33	V	
VDDA_1P8 Supply	1.71	1.8	1.89	V	
VDD_IF Supply	1.71	1.8	2.625	V	CMOS and LVDS supply, 1.8 V to 2.5 V nominal range
VDDA_3P3 Supply	3.135	3.3	3.465	V	
VDDA_SER, VDDA_DES, JESD_VTT_DES Supplies	1.14	1.3	1.365	V	
POSITIVE SUPPLY CURRENT (Rx MODE)					Two Rx channels enabled, Tx upconverter disabled, 100 MHz Rx BW, 122.88 MSPS data rate
VDDA_1P3 Analog Supplies[1]		1055		mA	
VDIG Supply		625		mA	Rx QEC[2] enabled, QEC[2] engine active
VDD_IF Supply (CMOS and LVDS)		8		mA	
VDDA_3P3 Supply		1		mA	No auxiliary DACs or auxiliary ADCs enabled; if enabled, the auxiliary ADC adds 2.7 mA, and each auxiliary ADC adds 1.5 mA
VDDA_SER, VDDA_DES, JESD_VTT_DES Supplies		375		mA	
Total Power Dissipation		2.70		W	

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
POSITIVE SUPPLY CURRENT (Tx MODE)					Two Tx channels enabled, Rx downconverter disabled, 200 MHz Tx BW, 245.76 MSPS data rate (ORx disabled)
VDDA_1P3 Analog Supplies[1]		1000		mA	
VDIG Supply		410		mA	Tx QEC[2] active
VDDA_1P8 Supply					Full-scale CW[3]
		405		mA	Tx RF attenuation = 0 dB,
		80		mA	Tx RF attenuation = 15 dB
VDD_IF Supply		8		mA	
VDDA_3P3 Supply		1		mA	No auxiliary DACs or auxiliary ADCs enabled; if enabled, the auxiliary ADC adds 2.7 mA, and each auxiliary ADC adds 1.5 mA
VDDA_SER, VDDA_DES, JESD_VTT_DES Supplies		375		mA	
Total Power Dissipation					Typical supply voltages, Tx QEC[2] active
		3.70		W	Tx RF attenuation = 0 dB
		3.11		W	Tx RF attenuation = 15 dB
POSITIVE SUPPLY CURRENT (FDD MODE), 2× Rx, 2× Tx, ORx ACTIVE					100 MHz Rx BW, 122.88 MSPS data rate; 200 MHz Tx BW, 245.76 MSPS data rate; 200 MHz ORx BW, 245.76 MSPS data rate
VDDA_1P3 Analog Supplies[1]		1700		mA	
VDIG Supply		1080		mA	Tx QEC[2] active
VDDA_1P8 Supply					Full scale CW[3]
		405		mA	Tx RF attenuation = 0 dB
		80		mA	Tx RF attenuation = 15 dB
VDD_IF Supply		8		mA	
VDDA_3P3 Supply		2		mA	No auxiliary DACs or auxiliary ADCs enabled; if enabled, the auxiliary ADC adds 2.7 mA, and each auxiliary ADC adds 1.5 mA
VDDA_SER, VDDA_DES, JESD_VTT_DES Supplies		375		mA	
Total Power Dissipation					Typical supply voltages, Tx QEC[2] active
		4.86		W	Tx RF attenuation = 0 dB
		4.27		W	Tx RF attenuation = 15 dB
MAXIMUM OPERATING JUNCTION TEMPERATURE			110	°C	Device designed for 10-year lifetime when operating at maximum junction temperature

[1] VDDA_1P3 refers to all analog 1.3 V supplies including the following: VDDA_BB, VDDA_CLKSYNTH, VDDA_TXLO, VDDA_RXRF, VDDA_RXSYNTH, VDDA_RXVCO, VDDA_RXTX, VDDA_TXSYNTH, VDDA_TXVCO, VDDA_CALPLL, VDDA_SNRXSYNTH, VDDA_SNRXVCO, VDDA_CLK, and VDDA_RXLO.
[2] QEC is the system for minimizing quadrature images of a desired signal.
[3] CW is a single frequency signal.

TIMING SPECIFICATIONS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL PERIPHERAL INTERFACE (SPI) TIMING						
SCLK Period	t_{CP}	20			ns	
SCLK Pulse Width	t_{MP}	10			ns	
CSB Setup to First SCLK Rising Edge	t_{SC}	3			ns	
Last SCLK Falling Edge to CSB Hold	t_{HC}	0			ns	
SDIO Data Input Setup to SCLK	t_S	2			ns	
SDIO Data Input Hold to SCLK	t_H	0			ns	
SCLK Falling Edge to Output Data Delay (3- or 4-Wire Mode)	t_{CO}	3		8	ns	
Bus Turnaround Time After Baseband Processor (BBP) Drives Last Address Bit	t_{HZM}	t_H		t_{CO}	ns	
Bus Turnaround Time After AD9375 Drives Last Address Bit	t_{HZS}	0		t_{CO}	ns	
DIGITAL TIMING						
TXx_ENABLE Pulse Width		10			µs	
RXx_ENABLE Pulse Width		10			µs	
JESD204B DATA OUTPUT TIMING						
Unit Interval	UI	162.76		1627.6	ps	
Data Rate per Channel (Nonreturn to Zero (NRZ))		614.4		6144	Mbps	
Rise Time	t_R	24	35		ps	20% to 80% in 100 Ω load
Fall Time	t_F	24	35		ps	20% to 80% in 100 Ω load
Output Common-Mode Voltage	V_{CM}	0		1.8	V	AC-coupled
Termination Voltage (V_{TT}) = 1.2 V		735		1135	mV	DC-coupled
Differential Output Voltage	V_{DIFF}	360	466	770	mV	
Short-Circuit Current	I_{DSHORT}	−100		+100	mA	
Differential Termination Impedance	Z_{RDIFF}	80	100	120	Ω	
Total Jitter			17	48.8	ps	Bit error rate (BER) = 10^{-15}
Uncorrelated Bounded High Probability Jitter	UBHPJ		1.2	24.4	ps	
Duty Cycle Distortion	DCD		3	8.1	ps	
SYSREF_IN Signal Setup Time to DEV_CLK_IN Signal	t_S	2.5			ns	See Figure 2 and Figure 3
SYSREF_IN Signal Hold Time to DEV_CLK_IN Signal	t_H	−1.5			ns	See Figure 2 and Figure 3
JESD204B DATA INPUT TIMING						
Unit Interval	UI	162.76		1627.6	ps	
Data Rate per Channel (NRZ)		614.4		6144	Mbps	
Input Common-Mode Voltage	V_{CM}	0.05		1.85	V	AC-coupled
V_{TT} = 1.2 V		720		1200	mV	DC-coupled
Differential Input Voltage	V_{DIFF}	125		750	mV	
V_{TT} Source Impedance	Z_{TT}		1.2	30	Ω	
Differential Termination Impedance	Z_{RDIFF}	80	106	120	Ω	
V_{TT}						
AC-Coupled		1.27		1.33	V	
DC-Coupled		1.14		1.26	V	

Timing Diagrams

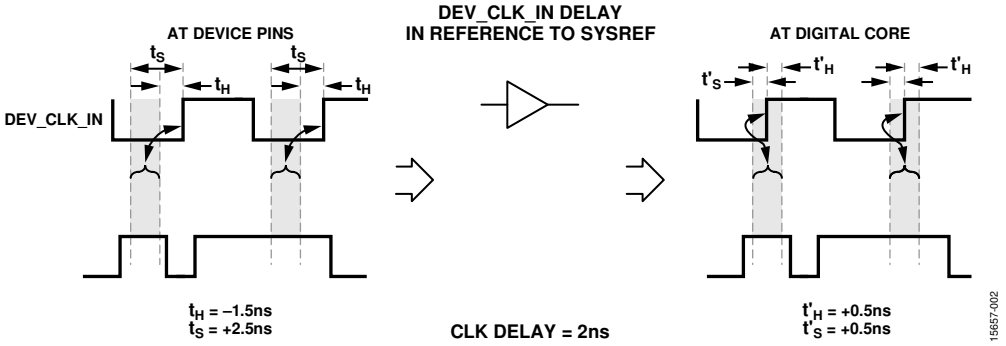

Figure 2. SYSREF_IN Signal Setup and Hold Timing

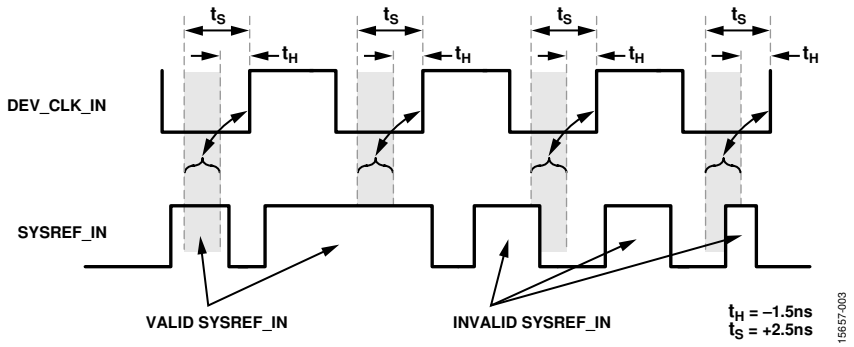

Figure 3. SYSREF_IN Signal Setup and Hold Timing Examples Relative to DEV_CLK_IN Signal

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VDDA_1P3[1] to VSSA	−0.3 V to +1.4 V
VDDA_SER, VDDA_DES, and JESD_VTT_DES to VSSA	−0.3 V to +1.4 V
VDIG to VSSD	−0.3 V to +1.4 V
VDDA_1P8 to VSSA	−0.3 V to +2.0 V
VDD_IF to VSSA	−0.3 V to +3.0 V
VDDA_3P3 to VSSA	−0.3 V to +3.9 V
Logic Inputs and Outputs to VSSD	−0.3 V to VDD_IF + 0.3 V
JESD204B Logic Outputs to VSSA	−0.3 V to VDDA_SER
JESD204B Logic Inputs to VSSA	−0.3 V to VDDA_DES
Input Current to Any Pin Except Supplies	±10 mA
Maximum Input Power into RF Ports (Excluding Sniffer Receiver Inputs)	23 dBm (peak)
Maximum Input Power into SNRXA±, SNRXB±, and SNRXC±	2 dBm (peak)
Maximum Junction Temperature ($T_{J\ MAX}$)	110°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] VDDA_1P3 refers to all analog 1.3 V supplies: VDDA_BB, VDDA_CLKSYNTH, VDDA_TXLO, VDDA_RXSYNTH, VDDA_RXVCO, VDDA_RXTX, VDDA_RXRF, VDDA_TXSYNTH, VDDA_TXVCO, VDDA_CALPLL, VDDA_SNRXSYNTH, VDDA_SNRXVCO, VDDA_CLK, and VDDA_RXLO.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The AD9375 reflow profile is in accordance with the JEDEC JESD20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction-to-case thermal resistance.

Table 5. Thermal Resistance

Package	Airflow Velocity[1] (m/sec)	θ_{JA}[2,3] (°C/W)	θ_{JC}[2,4] (°C/W)
BC-196-12			
JEDEC[5]	0.0	20.5	0.05
	1.0	18.5	N/A[6]
	2.5	17.2	N/A[6]
10-Layer PCB	0.0	14.1	0.05
	1.0	12.4	N/A[6]
	2.5	11.6	N/A[6]

[1] Power dissipation is 3.0 W for all test cases.
[2] Per JEDEC JESD51-7 for JEDEC JESD51-5 2S2P test board.
[3] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[4] Per MIL-STD 883, Method 1012.1.
[5] JEDEC entries refer to the JEDEC JESD51-9 (high-K thermal test board).
[6] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

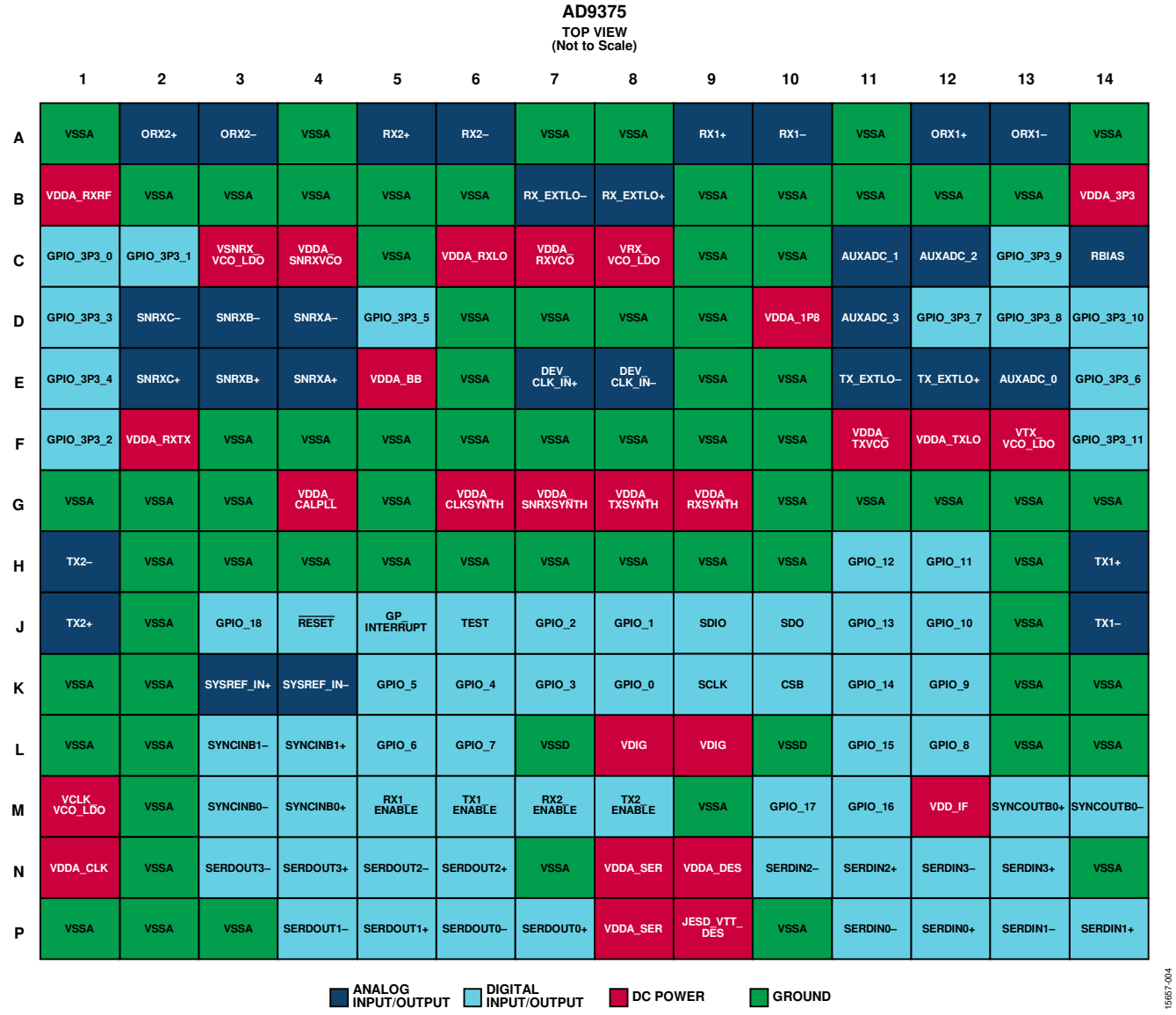

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Type[1]	Mnemonic	Description
A1, A4, A7, A8, A11, A14, B2 to B6, B9 to B13, C5, C9, C10, D6 to D9, E6, E9, E10, F3 to F10, G1 to G3, G5, G10 to G14, H2 to H10, H13, J2, J13, K1, K2, K13, K14, L1, L2, L13, L14, M2, M9, N2, N7, N14, P1, P2, P3, P10	I	VSSA	Analog ground.
A2, A3	I	ORX2+, ORX2–	Differential Input for Observation Receiver 2. Do not connect if these pins are unused.
A5, A6	I	RX2+, RX2–	Differential Input for Receiver 2. Do not connect if these pins are unused.
A9, A10	I	RX1+, RX1–	Differential Input for Receiver 1. Do not connect if these pins are unused.
A12, A13	I	ORX1+, ORX1–	Differential Input for Observation Receiver 1. Do not connect if these pins are unused.
B1	I	VDDA_RXRF	1.3 V Supply Input.

Pin No.	Type[1]	Mnemonic	Description
B7, B8	I/O	RX_EXTLO−, RX_EXTLO+	Differential Rx External LO Input/Output. If used for the external LO, the input frequency must be 2× the desired carrier frequency. Do not connect if these pins are unused.
B14	I	VDDA_3P3	Supply Voltage for GPIO_3P3_x.
C1, C2, C13, D1, D5, D12 to D14, E1, E14, F1, F14	I/O	GPIO_3P3_0 to GPIO_3P3_11	General-Purpose Inputs and Outputs Referenced to 3.3 V Supply. See Figure 4 to match the ball location to the GPIO_3P3_x signal name. Some GPIO_3P3_x pins can also function as auxiliary DAC outputs.
C3	O	VSNRX_VCO_LDO	Sniffer VCO LDO 1.1 V Output. Bypass this pin with a 1 µF capacitor.
C4	I	VDDA_SNRXVCO	1.3 V Supply Input for Sniffer VCO Low Dropout (LDO) Regulator.
C6	I	VDDA_RXLO	1.3 V Supply for the Rx Synthesizer LO Generator. This pin is sensitive to aggressors.
C7	I	VDDA_RXVCO	1.3 V Supply Input for Receiver VCO LDO Regulator.
C8	O	VRX_VCO_LDO	Receiver VCO LDO 1.1 V Output. Bypass this pin with a 1 µF capacitor.
C11	I	AUXADC_1	Auxiliary ADC 1 Input.
C12	I	AUXADC_2	Auxiliary ADC 2 Input.
C14	N/A	RBIAS	Bias Resistor Connection. This pin generates an internal current based on an external 1% resistor. Connect a 14.3 kΩ resistor between this pin and ground (VSSA).
D2, E2	I	SNRXC−, SNRXC+	Differential Input for Sniffer Receiver Input C. If these pins are unused, connect to VSSA with a short or with a 1 kΩ resistor.
D3, E3	I	SNRXB−, SNRXB+	Differential Input for Sniffer Receiver Input B. If these pins are unused, connect to VSSA with a short or with a 1 kΩ resistor.
D4, E4	I	SNRXA−, SNRXA+	Differential Input for Sniffer Receiver Input A. If these pins are unused, connect to VSSA with a short or with a 1 kΩ resistor.
D10	I	VDDA_1P8	1.8 V Tx Supply.
D11	I	AUXADC_3	Auxiliary ADC 3 Input.
E5	I	VDDA_BB	1.3 V Supply Input for ADCs, DACs, and Auxiliary ADCs.
E7, E8	I	DEV_CLK_IN+, DEV_CLK_IN−	Device Clock Differential Input.
E11, E12	I/O	TX_EXTLO−, TX_EXTLO+	Differential Tx External LO Input/Output. If these pins are used for the external LO, the input frequency must be 2× the desired carrier frequency. Do not connect if these pins are unused.
E13	I	AUXADC_0	Auxiliary ADC 0 Input.
F2	I	VDDA_RXTX	1.3 V Supply Input for Tx/Rx Baseband Circuits, Transimpedance Amplifier (TIA), Tx Transconductance (G_m), Baseband Filters, and Auxiliary DACs.
F11	I	VDDA_TXVCO	1.3 V Supply Input for Transmitter VCO LDO Regulator.
F12	I	VDDA_TXLO	1.3 V Supply for the Tx Synthesizer LO Generator. This pin is sensitive to aggressors.
F13	O	VTX_VCO_LDO	Transmitter VCO LDO 1.1 V Output. Bypass this pin with a 1 µF capacitor.
G4	I	VDDA_CALPLL	1.3 V Supply Input for Calibration PLL Circuits. Use a separate trace on the PCB back to a common supply point.
G6	I	VDDA_CLKSYNTH	1.3 V Clock Synthesizer Supply Input. This pin is sensitive to aggressors.
G7	I	VDDA_SNRXSYNTH	1.3 V Sniffer Rx Synthesizer Supply Input. This pin is sensitive to aggressors.
G8	I	VDDA_TXSYNTH	1.3 V Tx Synthesizer Supply Input. This pin is sensitive to aggressors.
G9	I	VDDA_RXSYNTH	1.3 V Rx Synthesizer Supply Input. This pin is sensitive to aggressors.
H1, J1	O	TX2−, TX2+	Differential Output for Transmitter 2.

Pin No.	Type[1]	Mnemonic	Description
H11, H12, J3, J7, J8, J11, J12, K5 to K8, K11, K12, L5, L6, L11, L12, M10, M11	I/O	GPIO_0 to GPIO_18	General-Purpose Inputs and Outputs Referenced to VDD_IF. See Figure 4 to match the ball location to the GPIO_x signal name.
H14, J14	O	TX1+, TX1−	Differential Output for Transmitter 1.
J4	I	$\overline{\text{RESET}}$	Active Low Chip Reset.
J5	O	GP_INTERRUPT	General-Purpose Interrupt Signal.
J6	I	TEST	Test Pin Used for JTAG Boundary Scan. Ground this pin if unused.
J9	I/O	SDIO	Serial Data Input in 4-Wire Mode or Input/Output in 3-Wire Mode.
J10	O	SDO	Serial Data Output.
K3, K4	I	SYSREF_IN+, SYSREF_IN−	LVDS System Reference Clock Inputs for the JESD204B Interface.
K9	I	SCLK	Serial Data Bus Clock.
K10	I	CSB	Serial Data Bus Chip Select. Active low.
L3, L4	I	SYNCINB1−, SYNCINB1+	LVDS Sync Signal Associated with ORx/Sniffer Channel Data on the JESD204B Interface. Alternatively, these pins can be set to a CMOS input using SYNCINB1+ as the input and connecting SYNCINB1− with a 1 kΩ resistor to GND.
L7, L10	I	VSSD	Digital Ground.
L8, L9	I	VDIG	1.3 V Digital Core Supply. Use a separate trace on the PCB back to a common supply point.
M1	O	VCLK_VCO_LDO	Clock VCO LDO 1.1 V Output. Bypass this pin with a 1 µF capacitor.
M3, M4	I	SYNCINB0−, SYNCINB0+	LVDS Sync Signal Associated with Rx Channel Data on the JESD204B Interface. Alternatively, these pins can be set to a CMOS input using SYNCINB0+ as the input and connecting SYNCINB0− with a 1 kΩ resistor to GND.
M5	I	RX1_ENABLE	Enables Rx Channel 1 Signal Path.
M6	I	TX1_ENABLE	Enables Tx Channel 1 Signal Path.
M7	I	RX2_ENABLE	Enables Rx Channel 2 Signal Path.
M8	I	TX2_ENABLE	Enables Tx Channel 2 Signal Path.
M12	I	VDD_IF	CMOS/LVDS Interface Supply.
M13, M14	O	SYNCOUTB0+, SYNCOUTB0−	LVDS Sync Signal Associated with Transmitter Channel Data on the JESD204B Interface. Alternatively, these pins can be set to a CMOS output using SYNCOUTB0+ as the output while leaving SYNCOUTB0− floating.
N1	I	VDDA_CLK	1.3 V Clock Supply Input.
N3, N4	O	SERDOUT3−, SERDOUT3+	RF Current Mode Logic (CML) Differential Output 3. This JESD204B lane can be used by the receiver data or by the sniffer/observation receiver data.
N5, N6	O	SERDOUT2−, SERDOUT2+	RF CML Differential Output 2. This lane can be used by the receiver data or by the sniffer/observation receiver data.
N8, P8	I	VDDA_SER	JESD204B 1.3 V Serializer Supply Input.
N9	I	VDDA_DES	JESD204B 1.3 V Deserializer Supply Input.
N10, N11	I	SERDIN2−, SERDIN2+	RF CML Differential Input 2.
N12, N13	I	SERDIN3−, SERDIN3+	RF CML Differential Input 3.
P4, P5	O	SERDOUT1−, SERDOUT1+	RF CML Differential Output 1. This JESD204B lane can be used by receiver data or by sniffer/observation receiver data.
P6, P7	O	SERDOUT0−, SERDOUT0+	RF CML Differential Output 0. This JESD204B lane can be used by receiver data or by sniffer/observation receiver data.
P9	I	JESD_VTT_DES	JESD204B Deserializer Termination Supply Input.
P11, P12	I	SERDIN0−, SERDIN0+	RF CML Differential Input 0.
P13, P14	I	SERDIN1−, SERDIN1+	RF CML Differential Input 1.

[1] I is input, I/O is input/output, O is output, and N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

Temperature settings refer to the die temperature. The die temperature is 40°C for single-trace plots.

700 MHz BAND

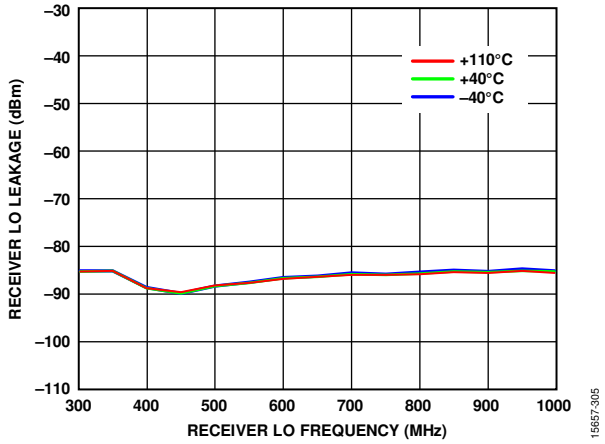

Figure 5. Receiver Local Oscillator (LO) Leakage vs. Receiver LO Frequency, 0 dB Receiver Attenuation, 20 MHz RF Bandwidth, 30.72 MSPS Sample Rate

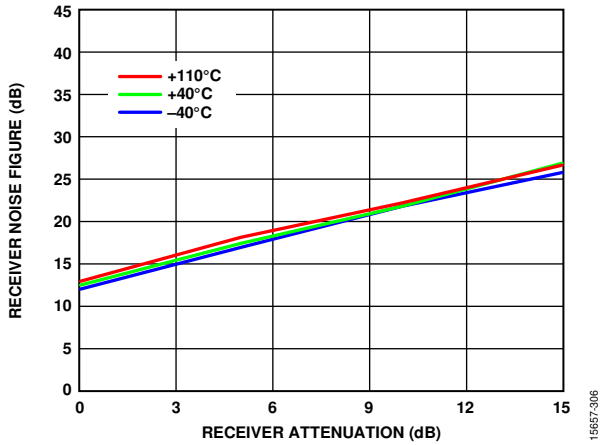

Figure 6. Receiver Noise Figure vs. Receiver Attenuation, 700 MHz LO, 20 MHz Bandwidth, 30.72 MSPS Sample Rate, 20 MHz Integration Bandwidth (Includes 1 dB Matching Circuit Loss)

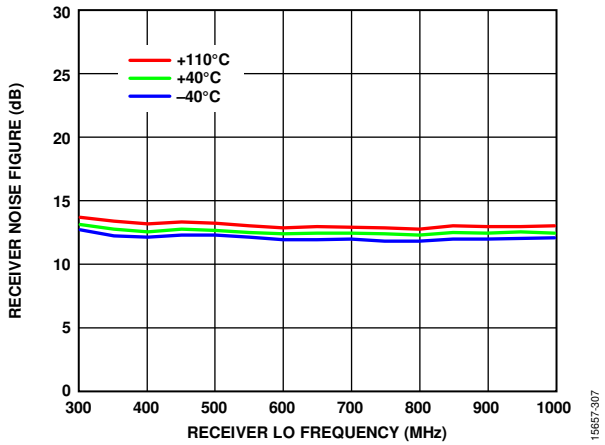

Figure 7. Receiver Noise Figure vs. Receiver LO Frequency, 0 dB Receiver Attenuation, 20 MHz RF Bandwidth, 30.72 MSPS Sample Rate, 20 MHz Integration Bandwidth (Includes 1 dB Matching Circuit Loss)

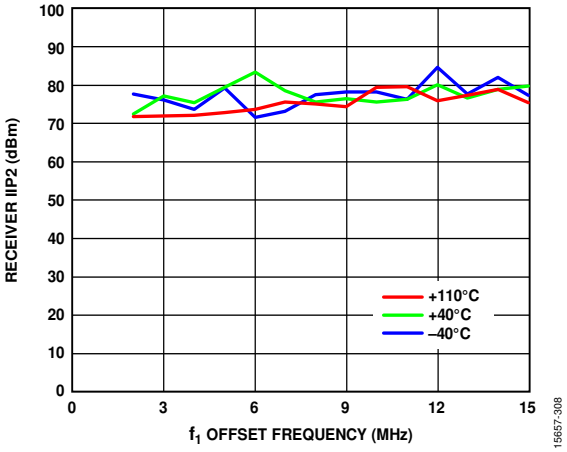

Figure 8. Receiver IIP2 vs. f_1 Offset Frequency, 900 MHz LO, 0 dB Attenuation, 20 MHz RF Bandwidth, $f_2 = f_1 + 1$ MHz, 30.72 MSPS Sample Rate

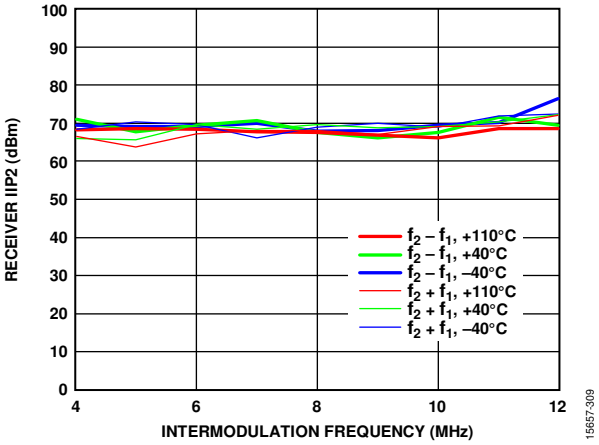

Figure 9. Receiver IIP2 vs. Intermodulation Frequency, 900 MHz LO, 0 dB Attenuation, 20 MHz RF Bandwidth, 30.72 MSPS Sample Rate

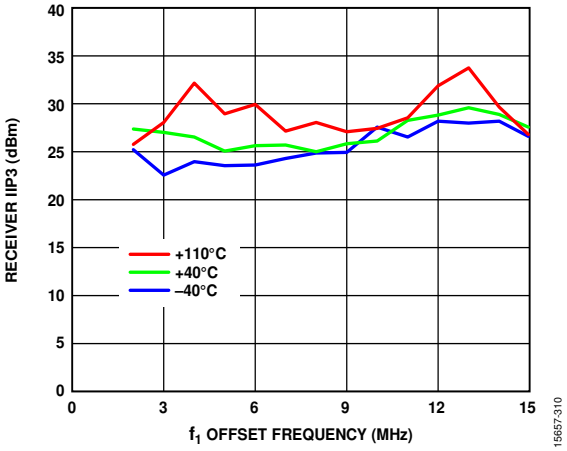

Figure 10. Receiver IIP3 vs. f_1 Offset Frequency, 900 MHz LO, 0 dB Attenuation, 20 MHz RF Bandwidth, $f_2 = 2f_1 + 1$ MHz, 30.72 MSPS Sample Rate

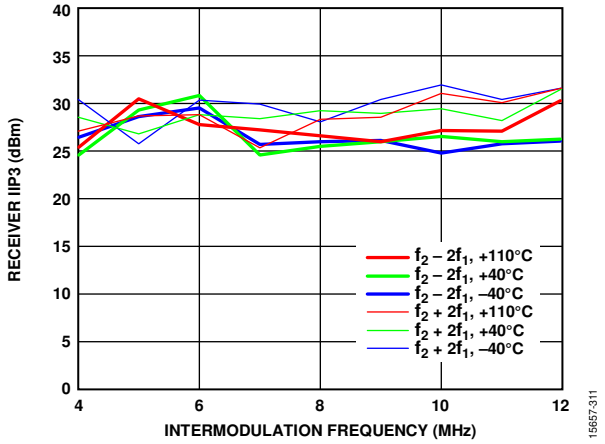

Figure 11. Receiver IIP3 vs. Intermodulation Frequency, 900 MHz LO, 0 dB Attenuation, 20 MHz RF Bandwidth, 30.72 MSPS Sample Rate

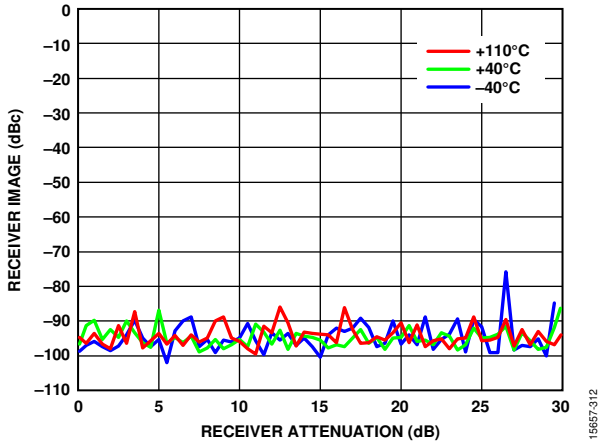

Figure 12. Receiver Image vs. Receiver Attenuation, 800 MHz LO, Continuous Wave (CW) Signal 3 MHz Offset, 20 MHz RF Bandwidth, Background Tracking Calibration (BTC) Active, 30.72 MSPS Sample Rate

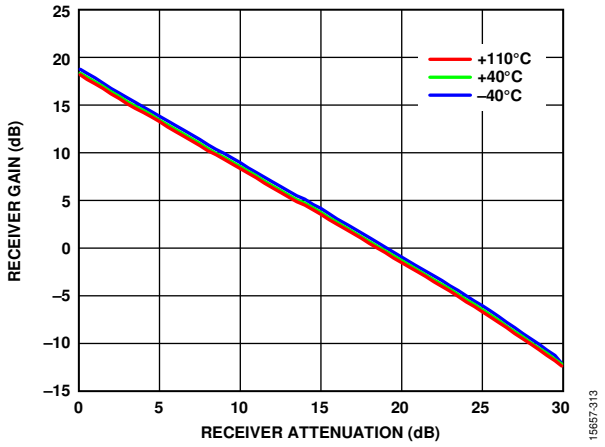

Figure 13. Receiver Gain vs. Receiver Attenuation, 800 MHz LO, CW Signal 3 MHz Offset, 20 MHz RF Bandwidth, 30.72 MSPS Sample Rate

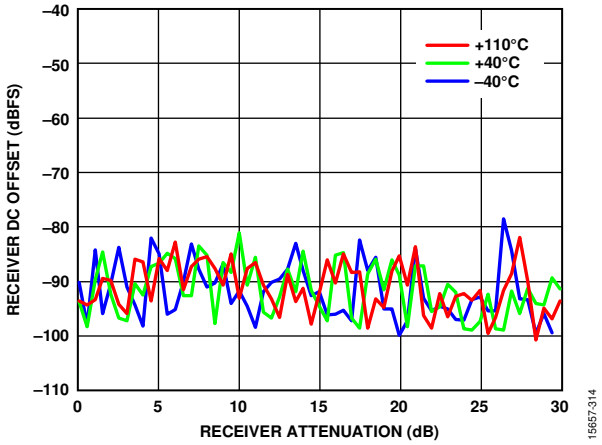

Figure 14. Receiver DC Offset vs. Receiver Attenuation, 800 MHz LO, 20 MHz RF Bandwidth, 30.72 MSPS Sample Rate

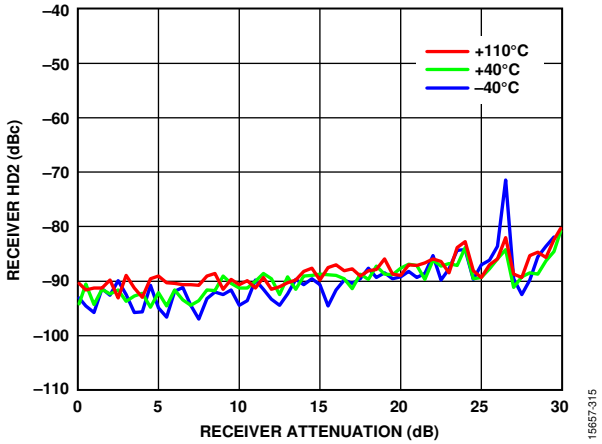

Figure 15. Receiver HD2 vs. Receiver Attenuation, 800 MHz LO, CW Signal 3 MHz Offset, –20 dBm at 0 dB Attenuation, Input Power Increasing Decibel for Decibel with Attenuation, 20 MHz RF Bandwidth, 30.72 MSPS Sample Rate

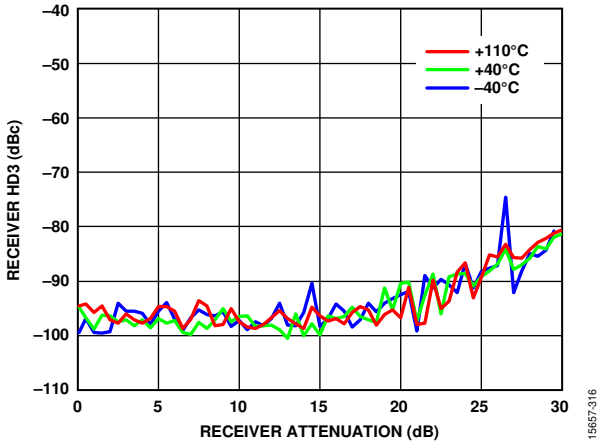

Figure 16. Receiver HD3 vs. Receiver Attenuation, 800 MHz LO, CW Signal 3 MHz Offset, –20 dBm at 0 dB Attenuation, Input Power Increasing Decibel for Decibel with Attenuation, 20 MHz RF Bandwidth, 30.72 MSPS Sample Rate

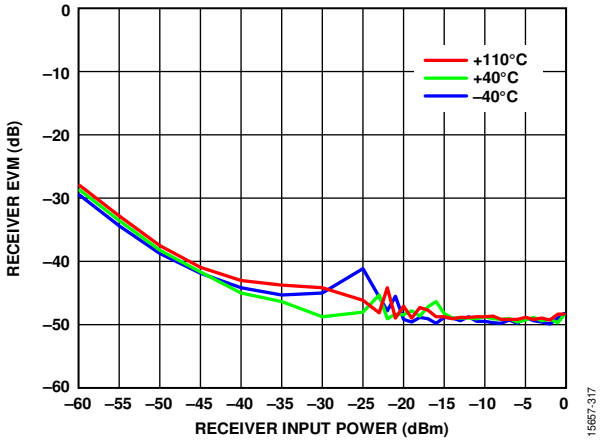

Figure 17. Receiver Error Vector Magnitude (EVM) vs. Receiver Input Power, 900 MHz LO, 20 MHz RF Bandwidth, LTE 20 MHz Uplink Centered at DC, BTC Active, 30.72 MSPS Sample Rate

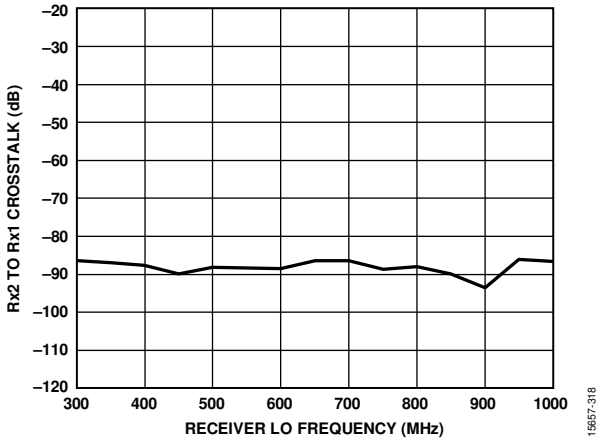

Figure 18. Rx2 to Rx1 Crosstalk vs. Receiver LO Frequency, 100 MHz RF Bandwidth, CW Tone 3 MHz Offset from LO

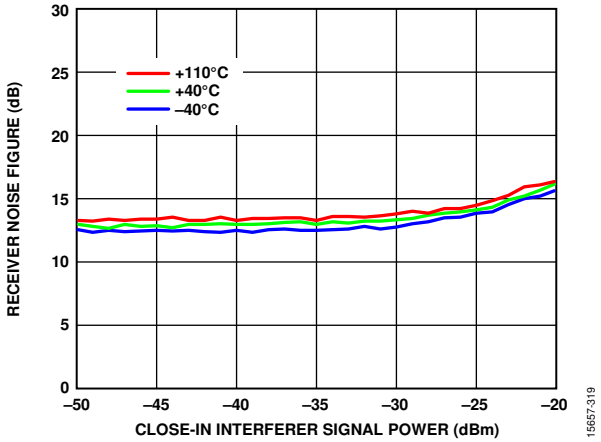

Figure 19. Receiver Noise Figure vs. Close-In Interferer Signal Power, 703 MHz LO, 709 MHz CW Interferer, NF Integrated over 7 MHz to 10 MHz, 20 MHz RF Bandwidth

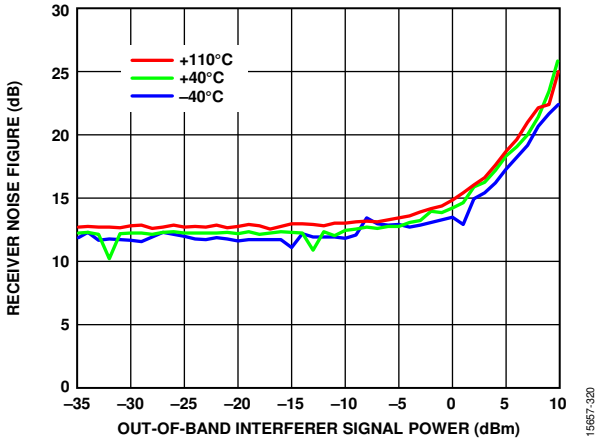

Figure 20. Receiver Noise Figure vs. Out-of-Band Interferer Signal Power, 703 MHz LO, 901 MHz CW Interferer, NF Integrated over 7 MHz to 10 MHz, 20 MHz RF Bandwidth

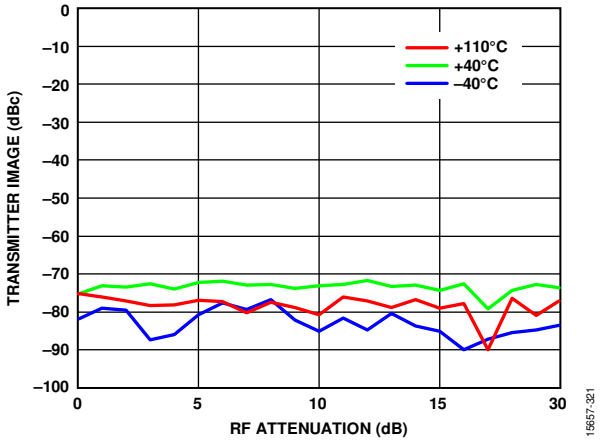

Figure 21. Transmitter Image vs. RF Attenuation, 20 MHz RF Bandwidth, 900 MHz LO, Transmitter Quadrature Error Correction (QEC) Tracking Run with Two 20 MHz LTE Downlink Carriers, Then Image Measured with CW 10 MHz Offset from LO, 3 dB Digital Backoff, 122.88 MSPS Sample Rate

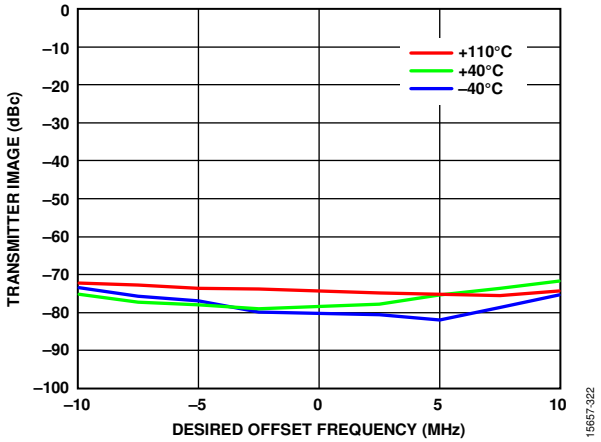

Figure 22. Transmitter Image vs. Desired Offset Frequency, 20 MHz RF Bandwidth, 900 MHz LO, 0 dB RF Attenuation, Transmitter QEC Tracking Run with Two 20 MHz LTE Downlink Carriers, Then Image Measured with CW Signal, 3 dB Digital Backoff, 122.88 MSPS Sample Rate

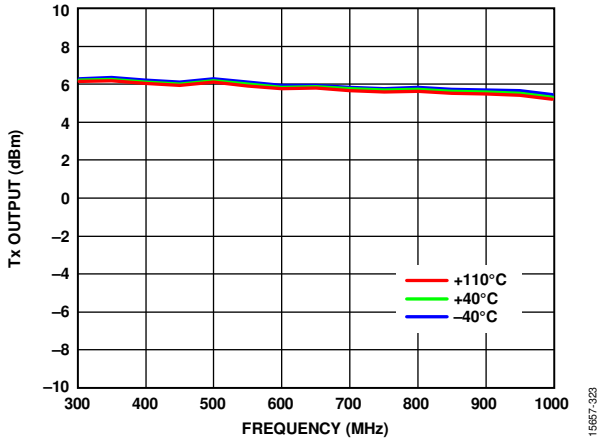

Figure 23. Tx Output Power, Transmitter QEC, and External LO Leakage Tracking Active, 10 MHz CW Offset Signal, 1 MHz Resolution Bandwidth, 122.88 MSPS Sample Rate

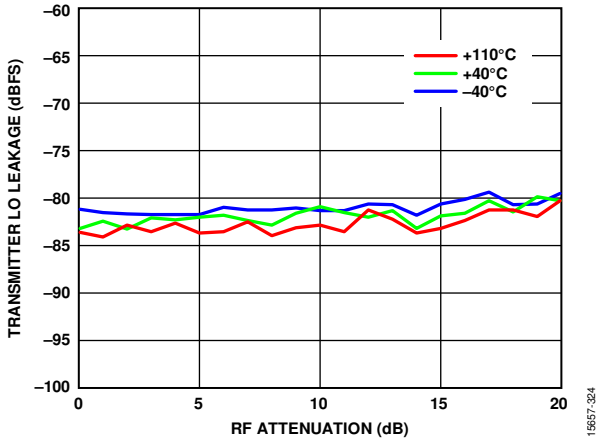

Figure 24. Transmitter LO Leakage vs. RF Attenuation, 900 MHz LO, Transmitter QEC and External LO Leakage Tracking Active, CW Signal 5 MHz Offset from LO, 6 dB Digital Backoff, 1 MHz Measurement Bandwidth (If Input Power to ORx Channel Is Not Held Constant, Performance Degrades As Shown in This Plot)

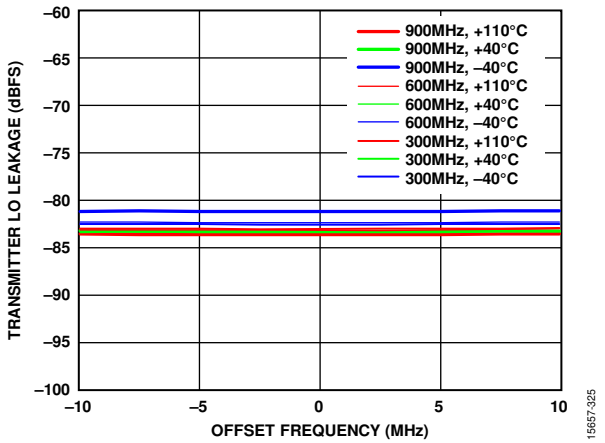

Figure 25. Transmitter LO Leakage vs. Offset Frequency, Transmitter QEC and External LO Leakage Tracking Active, 5 dB Digital Backoff, 1 MHz Measurement Bandwidth

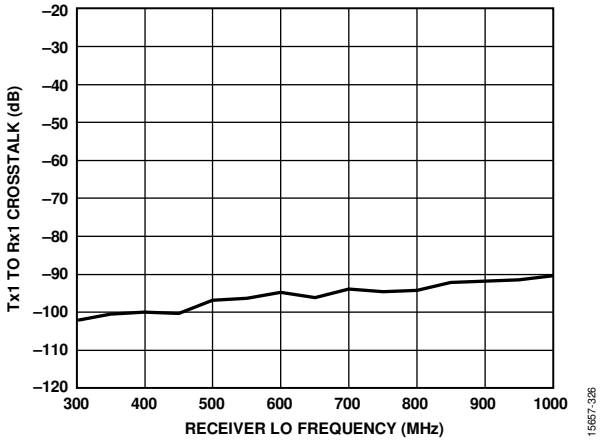

Figure 26. Tx1 to Rx1 Crosstalk vs. Receiver LO Frequency, 20 MHz Receiver RF Bandwidth, 20 MHz Transmitter RF Bandwidth, CW Signal 3 MHz Offset from LO

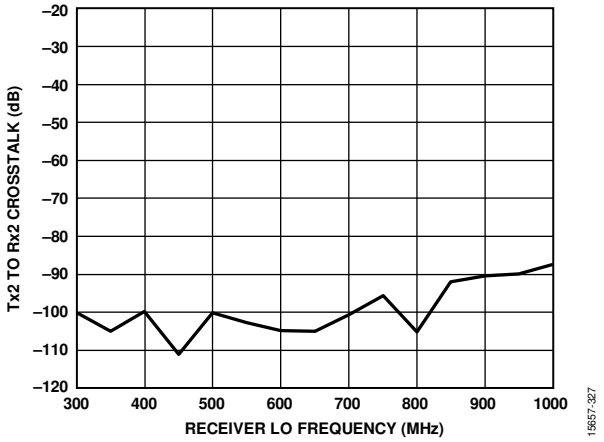

Figure 27. Tx2 to Rx2 Crosstalk vs. Receiver LO Frequency, 20 MHz Receiver RF Bandwidth, 20 MHz Transmitter RF Bandwidth, CW Signal 3 MHz Offset from LO

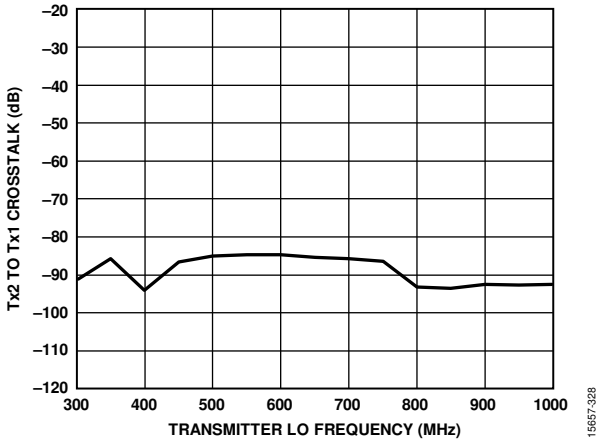

Figure 28. Tx2 to Tx1 Crosstalk vs. Transmitter LO Frequency, 20 MHz RF Bandwidth, CW Signal 3 MHz Offset from LO

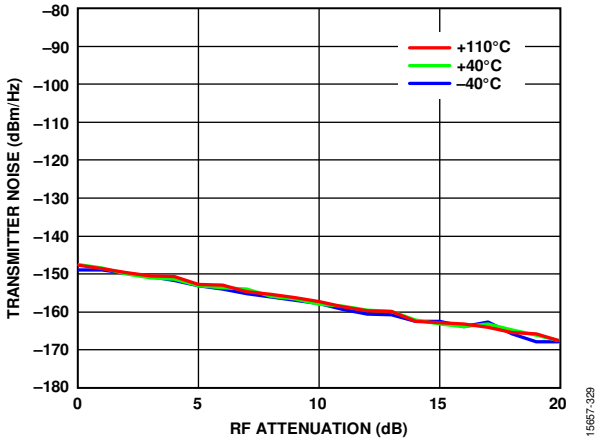

Figure 29. Transmitter Noise vs. RF Attenuation, 800 MHz LO, 20 MHz Offset Frequency

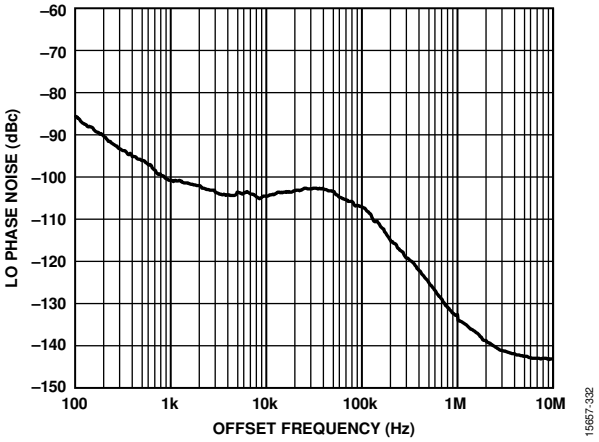

Figure 32. LO Phase Noise vs. Offset Frequency, 3 dB Digital Backoff, 710 MHz LO

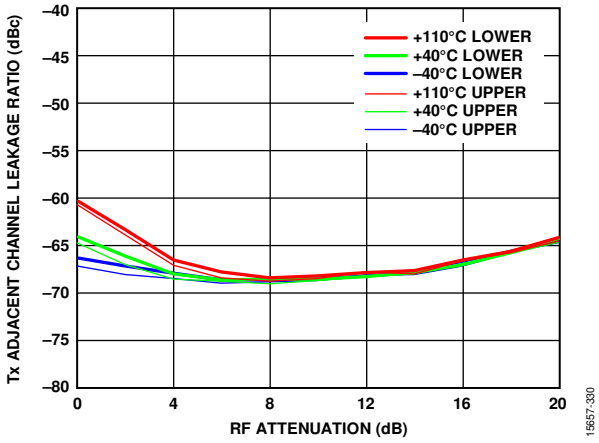

Figure 30. Tx Adjacent Channel Leakage Ratio vs. RF Attenuation, 900 MHz LO, 20 MHz RF Bandwidth, Four-Carrier W-CDMA Desired Signal, Transmitter QEC and LO Leakage Tracking Active

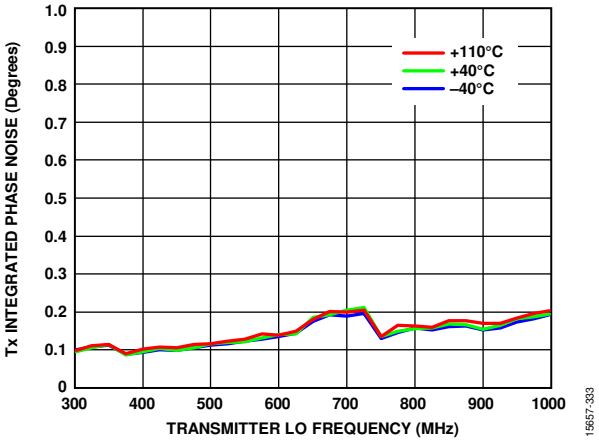

Figure 33. Tx Integrated Phase Noise vs. Transmitter LO Frequency, 20 MHz RF Bandwidth, CW 20 MHz Offset from LO, 3 dB Digital Backoff

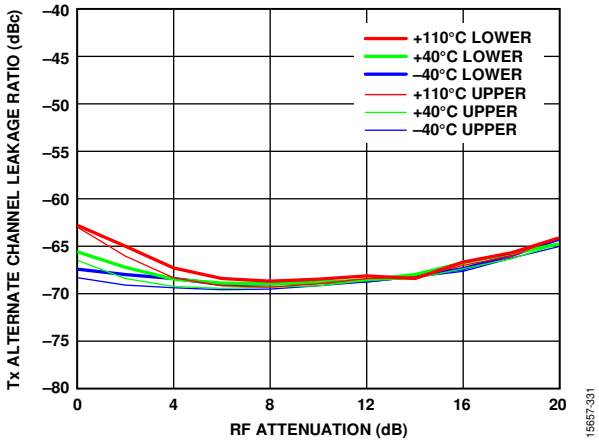

Figure 31. Tx Alternate Channel Leakage Ratio vs. RF Attenuation, 900 MHz LO, 20 MHz RF Bandwidth, Four-Carrier W-CDMA Desired Signal, 2 dB Digital Backoff, Transmitter QEC and LO Leakage Tracking Active

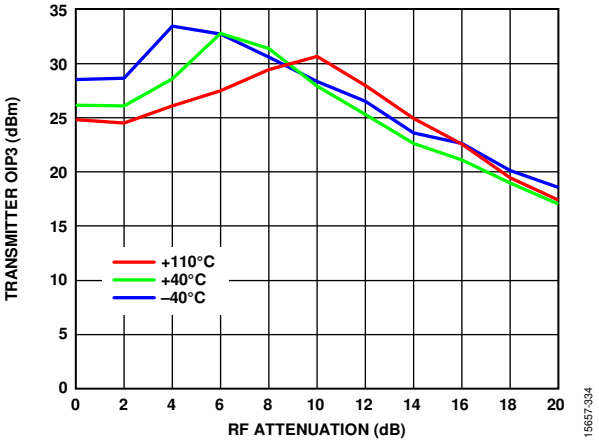

Figure 34. Transmitter OIP3 vs. RF Attenuation, 800 MHz LO, 20 MHz RF Bandwidth, f_1 = 10 MHz, f_2 = 11 MHz, 3 dB Digital Backoff, 122.88 MSPS Sample Rate

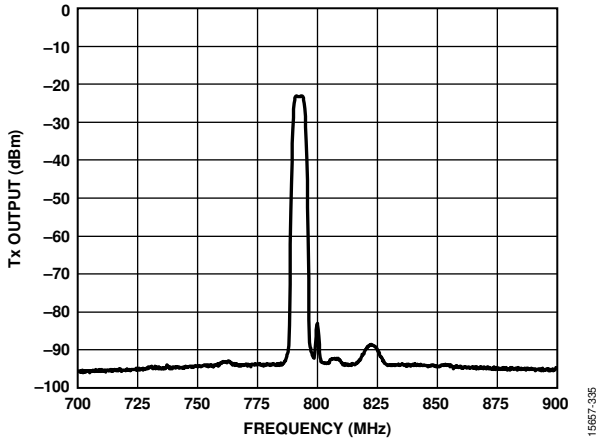

Figure 35. Tx Output Power Spectrum, 2 dB Digital and 3 dB RF Backoff, 20 MHz RF Bandwidth, Transmitter QEC, and Internal LO Leakage Active, LTE 10 MHz Signal, 800 MHz LO, 1 MHz Resolution Bandwidth, 122.88 MSPS Sample Rate, Test Equipment Noise Floor De-Embedded

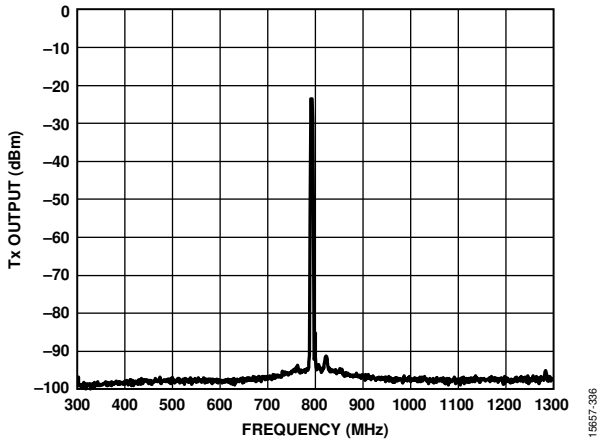

Figure 36. Tx Output Power Spectrum, 2 dB Digital and 3 dB RF Backoff, 20 MHz RF Bandwidth, Transmitter QEC, and Internal LO Leakage Active, LTE 10 MHz Signal, 800 MHz LO, 1 MHz Resolution Bandwidth, 122.88 MSPS Sample Rate, Expanded Frequency View, Test Equipment Noise Floor De-Embedded

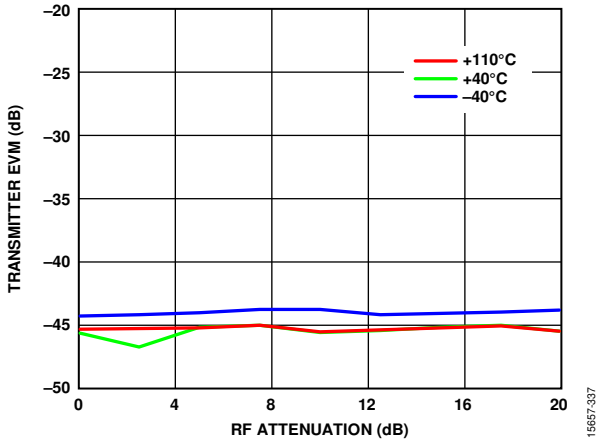

Figure 37. Transmitter EVM vs. RF Attenuation, 900 MHz LO, Transmitter LO Leakage and Transmitter QEC Tracking Active, 20 MHz RF Bandwidth, LTE 20 MHz Downlink Signal, 122.88 MSPS Sample Rate

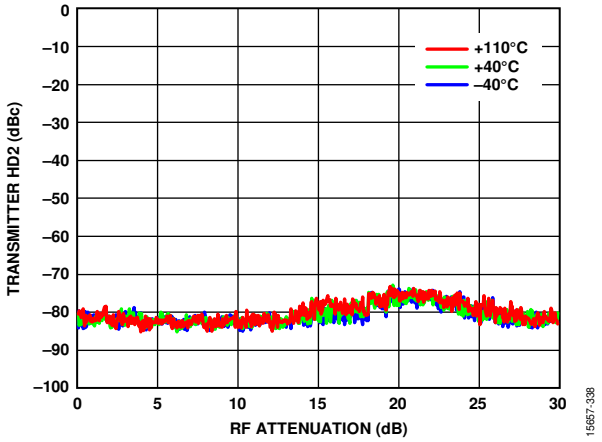

Figure 38. Transmitter HD2 vs. RF Attenuation, 800 MHz LO, 810 MHz CW Desired Signal, 20 MHz RF Bandwidth, 122.88 MSPS Sample Rate

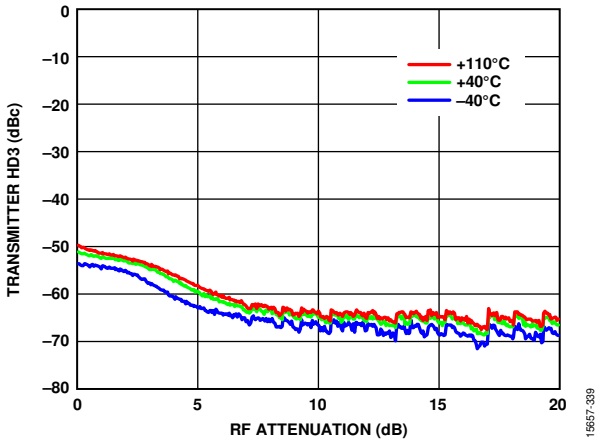

Figure 39. Transmitter HD3 vs. RF Attenuation, 800 MHz LO, 810 MHz CW Desired Signal, 20 MHz RF Bandwidth, 122.88 MSPS Sample Rate

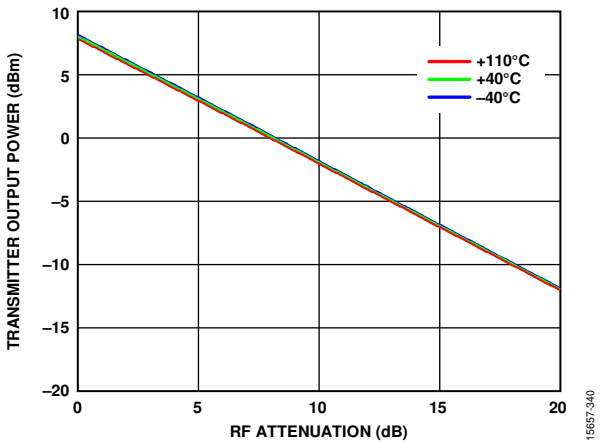

Figure 40. Transmitter Output Power vs. RF Attenuation, 800 MHz LO, 810 MHz CW Desired Signal, 20 MHz RF Bandwidth, 122.88 MSPS Sample Rate

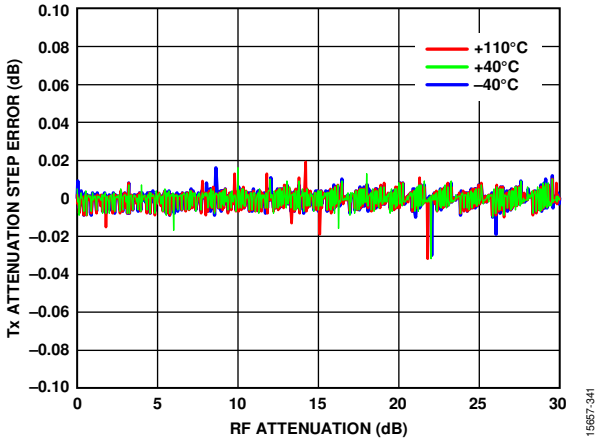

Figure 41. Tx Attenuation Step Error vs. RF Attenuation, 800 MHz LO, 810 MHz CW Desired Signal, 20 MHz RF Bandwidth, 122.88 MSPS Sample Rate

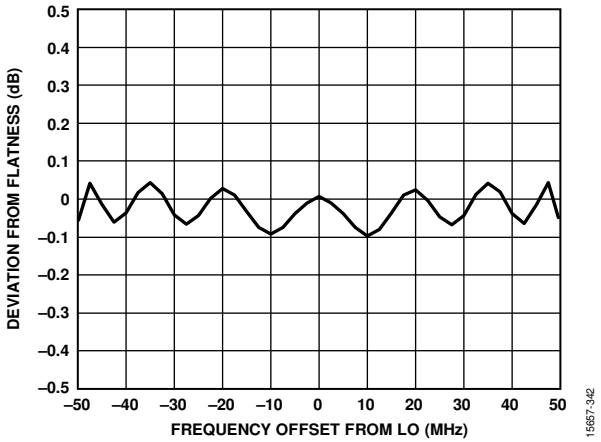

Figure 42. Transmitter Frequency Response Deviation from Flatness vs. Frequency Offset from LO, 800 MHz LO, 20 MHz RF Bandwidth, 6 dB Digital Backoff, 122.88 MSPS Sample Rate

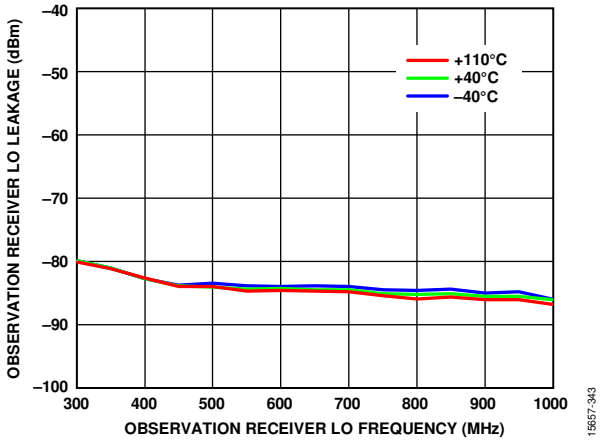

Figure 43. Observation Receiver LO Leakage vs. Observation Receiver LO Frequency, 0 dB Receiver Attenuation, 100 MHz RF Bandwidth, 122.88 MSPS Sample Rate

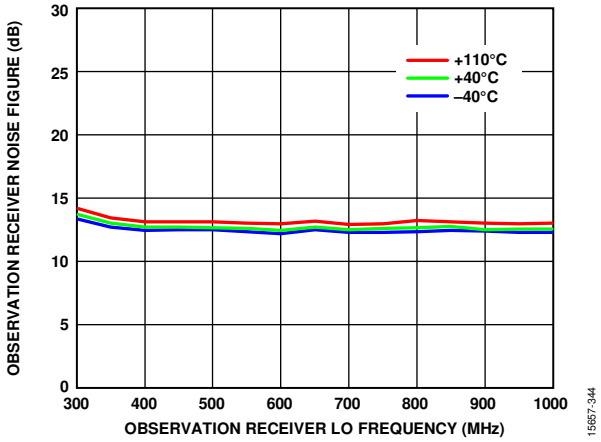

Figure 44. Observation Receiver Noise Figure vs. Observation Receiver LO Frequency, 0 dB Receiver Attenuation, 100 MHz RF Bandwidth, 122.88 MSPS Sample Rate, 100 MHz Integration Bandwidth

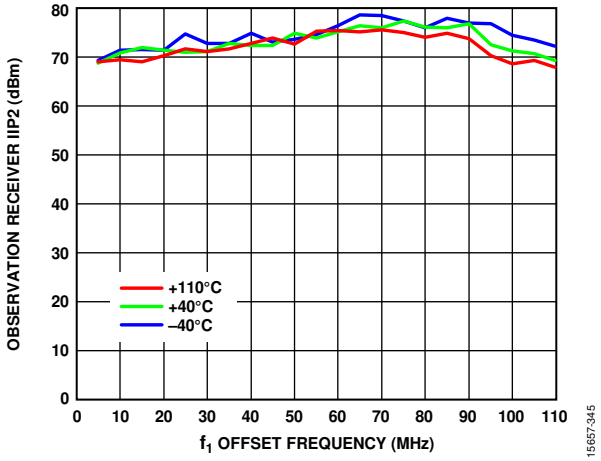

Figure 45. Observation Receiver IIP2 vs. f_1 Offset Frequency, 900 MHz LO, 0 dB Attenuation, 100 MHz RF Bandwidth, $f_2 = f_1 + 1$ MHz, 122.88 MSPS Sample Rate

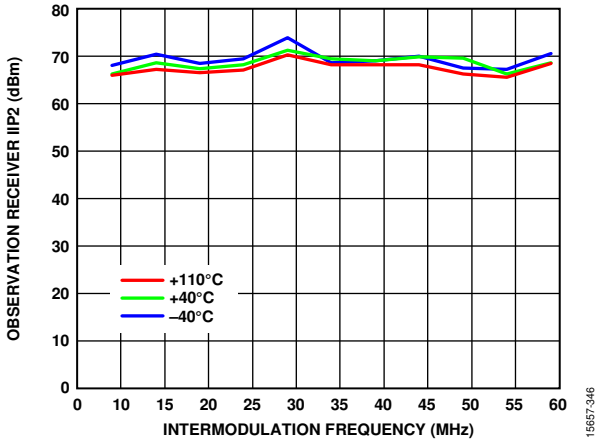

Figure 46. Observation Receiver IIP2 vs. Intermodulation Frequency ($f_2 - f_1$), 900 MHz LO, 0 dB Attenuation, 100 MHz RF Bandwidth, 122.88 MSPS Sample Rate

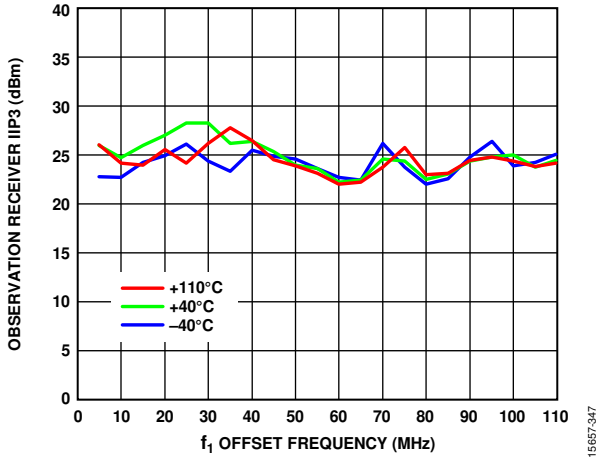

Figure 47. Observation Receiver IIP3 vs. f_1 Offset Frequency, 900 MHz LO, 0 dB Attenuation, 100 MHz RF Bandwidth, $f_2 = 2f_1 + 1$ MHz, 122.88 MSPS Sample Rate

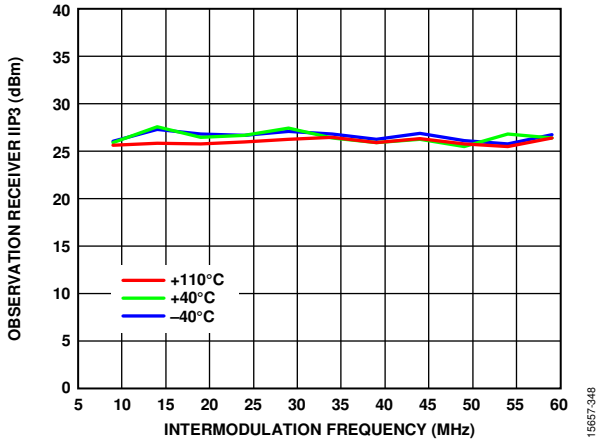

Figure 48. Observation Receiver IIP3 vs. Intermodulation Frequency ($2f_2 - f_1$), 900 MHz LO, 0 dB Attenuation, 100 MHz RF Bandwidth, 122.88 MSPS Sample Rate

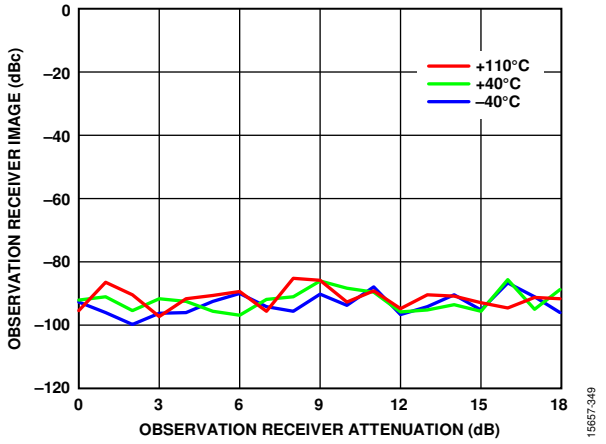

Figure 49. Observation Receiver Image vs. Observation Receiver Attenuation, 800 MHz LO, CW Signal 16 MHz Offset, 100 MHz RF Bandwidth, BTC Active, 122.88 MSPS Sample Rate

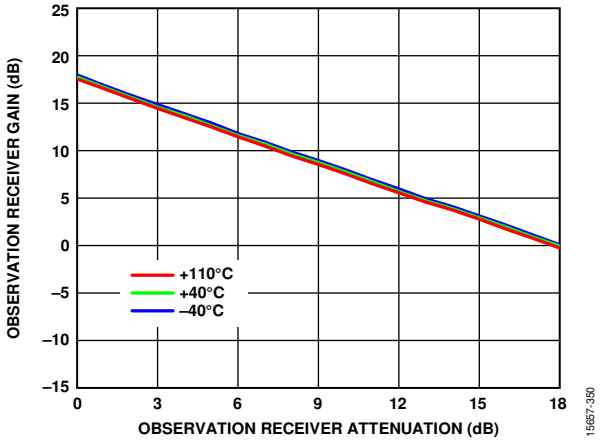

Figure 50. Observation Receiver Gain vs. Observation Receiver Attenuation, 800 MHz LO, CW Signal 16 MHz Offset, 100 MHz RF Bandwidth, 122.88 MSPS Sample Rate

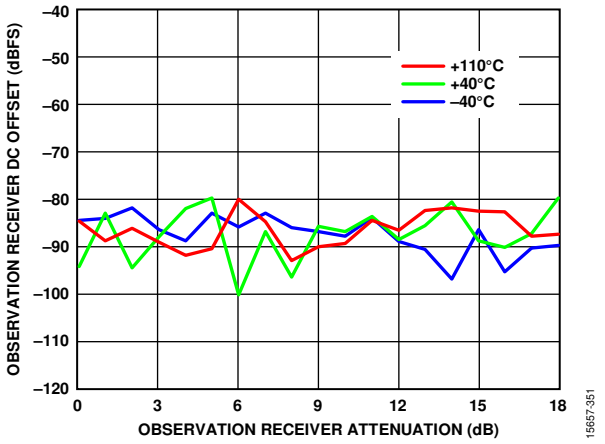

Figure 51. Observation Receiver DC Offset vs. Observation Receiver Attenuation, 800 MHz LO, 100 MHz RF Bandwidth, 122.88 MSPS Sample Rate

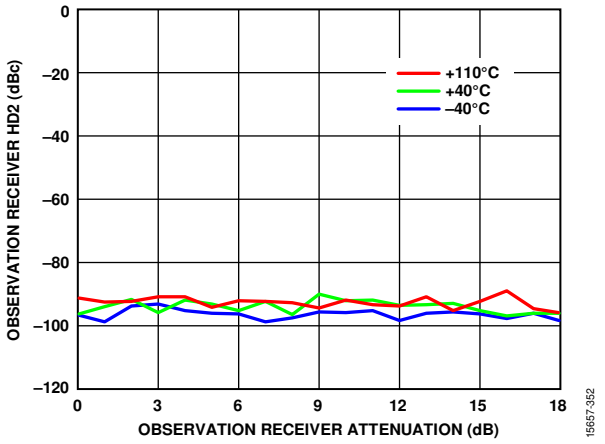

Figure 52. Observation Receiver HD2 vs. Observation Receiver Attenuation, 800 MHz LO, CW Signal 16 MHz Offset, –20 dBm at 0 dB Attenuation, Input Power Increasing Decibel for Decibel with Attenuation, 100 MHz RF Bandwidth, 122.88 MSPS Sample Rate