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16-Bit, 80 MSPS/105 MSPS ADC

AD9460

FEATURES

- 105 MSPS guaranteed sampling rate (AD9460-105)
- 79.4 dBFS SNR/91 dBc SFDR with 10 MHz input (3.4 V p-p input, 80 MSPS)
- 78.3 dBFS SNR/ with 170 MHz input (4.0 V p-p input, 80 MSPS)
- 77.8 dBFS SNR/87 dBc SFDR with 170 MHz input (3.4 V p-p input, 80 MSPS)
- 77.2 dBFS SNR/84 dBc SFDR with 170 MHz input (3.4 V p-p input, 105 MSPS)
- 90 dBFS two-tone SFDR with 139 MHz/140 MHz input (3.4 V p-p input, 105 MSPS)
- 60 fsec rms jitter
- Excellent linearity
  - DNL = ±0.5 LSB typical
  - INL = ±3.0 LSB typical
- 2.0 V p-p to 4.0 V p-p differential full-scale input
- Buffered analog inputs
- LVDS outputs (ANSI-644 compatible) or CMOS outputs
- Data format select (offset binary or twos complement)
- Output data capture clock available
- 3.3 V and 5 V supply operation

APPLICATIONS

- MRI receivers
- Multicarrier, multimode, cellular receivers
- Antenna array positioning
- Power amplifier linearization
- Broadband wireless
- Radar
- Infrared imaging
- Communications instrumentation

GENERAL DESCRIPTION

The AD9460 is a 16-bit, monolithic, sampling, analog-to-digital converter (ADC) with an on-chip track-and-hold circuit. It is optimized for performance, small size, and ease of use. The AD9460 operates up to 105 MSPS, providing a superior signal-to-noise ratio (SNR) for instrumentation, medical imaging, and radar receivers using baseband (<100 MHz) and IF frequencies.

The ADC requires 3.3 V and 5.0 V power supplies and a low voltage differential input clock for full performance operation. No external reference or driver components are required for many applications. Data outputs are CMOS or LVDS compatible (ANSI-644 compatible) and include the means to reduce the overall current needed for short trace distances.

FUNCTIONAL BLOCK DIAGRAM

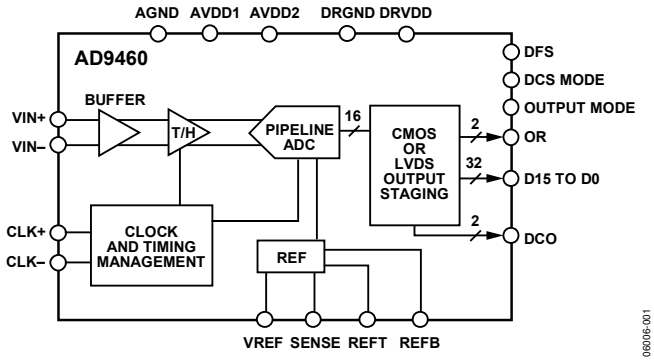

Figure 1.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data mode.

The AD9460 is available in a Pb-free, 100-lead, surface-mount, plastic package (TQFP_EP) specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. True 16-bit linearity.
2. High performance: outstanding SNR performance for baseband IFs in data acquisition, instrumentation, magnetic resonance imaging, and radar receivers.
3. Ease of use: on-chip reference and high input impedance, track-and-hold with adjustable analog input range, and an output clock simplifies data capture.
4. Packaged in a Pb-free, 100-lead TQFP/EP.
5. Clock duty cycle stabilizer (DCS) maintains overall ADC performance over a wide range of clock pulse widths.
6. Out-of-range (OR) outputs indicate when the signal is beyond the selected input range.

Rev. 0

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Tel: 781.329.4700 **www.analog.com**
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AD9460* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9460 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9460: 16-Bit, 80/105 MSPS ADC Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog
- AD9460 IBIS Models

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9460 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9460 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

7/06—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD = 3.3 V, LVDS mode, specified minimum sampling rate, 3.4 V p-p differential input, internal trimmed reference (1.0 V mode), analog input amplitude = −1.0 dBFS, DCS = AGND (on), SFDR = AGND, unless otherwise noted.

Table 1.

		AD9460BSVZ-80			AD9460BSVZ-105			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full		16			16		Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full	−5.0	±0.1	+5.0	−5.0	±0.1	+5.0	mV
Gain Error	25°C	−3	±0.5	+3	−3	±0.5	+3	% FSR
	Full	−3.4		+3.4	−3.4		+3.4	% FSR
Differential Nonlinearity (DNL)[1]	25°C	−0.8	±0.5	+0.8	−0.85	±0.5	+0.85	LSB
	Full	−0.9		+0.9	−1		+1.2	
Integral Nonlinearity (INL)[1]	25°C	−6	±3	+6	−6	±3	+6	LSB
VOLTAGE REFERENCE								
Output Voltage VREF = 1.7 V	Full		1.7			1.7		V
Load Regulation @ 1.0 mA	Full		±2			±2		mV
Reference Input Current (External VREF = 1.7 V)	Full		350			350		µA
INPUT REFERRED NOISE	25°C		2.4			2.5		LSB rms
ANALOG INPUT								
Input Span								
VREF = 1.7 V	Full		3.4			3.4		V p-p
VREF = 1.0 V	Full		2.0			2.0		V p-p
Internal Input Common-Mode Voltage	Full		3.5			3.5		V
External Input Common-Mode Voltage	Full	3.2		3.9	3.2		3.9	V
Input Resistance[2]	Full		1			1		kΩ
Input Capacitance[2]	Full		6			6		pF
POWER SUPPLIES								
Supply Voltages								
AVDD1	Full	3.14	3.3	3.46	3.14	3.3	3.46	V
AVDD2	Full	4.75	5.0	5.25	4.75	5.0	5.25	V
DRVDD—LVDS Outputs	Full	3.0	3.3	3.6	3.0	3.3	3.6	V
DRVDD—CMOS Outputs	Full	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Currents[1]								
AVDD1	Full		290	310		337	373	mA
AVDD2[1, 3]	Full		101	110		116	133	mA
I_{DRVDD}[1]—LVDS Outputs	Full		70	78.5		71	81	mA
I_{DRVDD}[1]—CMOS Outputs	Full		14			14		mA
PSRR								
Offset	Full		1			1		mV/V
Gain	Full		0.2			0.2		%/V
POWER CONSUMPTION[3]								
LVDS Outputs	Full		1.7	1.8		1.9	2.2	W
CMOS Outputs (DC Input)	Full		1.5			1.7		W

[1] Measured at the maximum clock rate, f_{IN} = 15 MHz, full-scale sine wave, with a 100 Ω differential termination on each pair of output bits for LVDS output mode and approximately 5 pF loading on each output bit for CMOS output mode.
[2] Input capacitance or resistance refers to the effective impedance between one differential input pin and AGND. Refer to Figure 6 for the equivalent analog input structure.
[3] For SFDR = AVDD1, I_{AVDD2} power increases by ~70 mW for the AD9460BSVZ-80 and ~20 mW for the AD9460BSVZ-105.

AC SPECIFICATIONS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD = 3.3 V, LVDS mode, specified minimum sample rate, 3.4 V p-p differential input, internal trimmed reference (1.7 V mode), A_{IN} = −1.0 dBFS, DCS = AGND (on), SFDR = AGND, unless otherwise noted.

Table 2.

		AD9460BSVZ-80			AD9460BSVZ-105			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 10 MHz	25°C	77.6	78.4		77.2	78.1		dB
	Full	77.4			76.9			
f_{IN} = 170 MHz	25°C	76.1	76.8		75.0	76.2		dB
	Full	75.0			74.5			
f_{IN} = 225 MHz	25°C		75.7			75.2		dB
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 10 MHz	25°C	76.1	78.0		75.2	77.4		dB
	Full	74.4			74.5			
f_{IN} = 170 MHz	25°C	74.0	76.1		72.0	75.1		dB
	Full	72.1			71.2			
f_{IN} = 225 MHz	25°C		74.6			73.6		dB
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 10 MHz	25°C		12.8			12.7		bits
f_{IN} = 170 MHz	25°C		12.5			12.4		bits
f_{IN} = 225 MHz	25°C		12.3			12.1		bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR, SECOND OR THIRD HARMONIC)								
f_{IN} = 10 MHz	25°C	80	91		80	88		dBc
	Full	78			76			
f_{IN} = 170 MHz	25°C	80	87		78	84		dBc
	Full	78			74			
f_{IN} = 225 MHz	25°C		82			81		dBc
WORST SPUR EXCLUDING SECOND OR THIRD HARMONICS								
f_{IN} = 10 MHz	25°C	94	100		92	98		dBc
	Full	91			91			
f_{IN} = 170 MHz	25°C	90	98		89	98		dBc
	Full	88			85			
f_{IN} = 225 MHz	25°C		97			92		dBc
TWO-TONE SFDR								
f_{IN} = 139.6 MHz @ −7 dBFS, 140.6 MHz @ −7 dBFS	25°C		89			90		dBFS
ANALOG BANDWIDTH	Full		615			615		MHz

DIGITAL SPECIFICATIONS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD = 3.3 V, R_{LVDS_BIAS} = 3.74 kΩ, unless otherwise noted.

Table 3.

		AD9460BSVZ-80/105			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Unit**
CMOS LOGIC INPUTS (DFS, DCS MODE, OUTPUT MODE)					
High Level Input Voltage	Full	2.0			V
Low Level Input Voltage	Full			0.8	V
High Level Input Current	Full			200	µA
Low Level Input Current	Full	−10		+10	µA
Input Capacitance	Full		2		pF
DIGITAL OUTPUT BITS—CMOS MODE (D0 to D15, OTR)[1]					
DRVDD = 3.3 V					
High Level Output Voltage	Full	3.25			V
Low Level Output Voltage	Full			0.2	V
DIGITAL OUTPUT BITS—LVDS MODE (D0 to D15, OTR)					
V_{OD} Differential Output Voltage[2]	Full	247		545	mV
V_{OS} Output Offset Voltage	Full	1.125		1.375	V
CLOCK INPUTS (CLK+, CLK−)					
Differential Input Voltage	Full	0.2			V
Common-Mode Voltage	Full	1.3	1.5	1.6	V
Input Resistance	Full	1.1	1.4	1.7	kΩ
Input Capacitance	Full		2		pF

[1] Output voltage levels measured with 5 pF load on each output.
[2] LVDS R_{TERM} = 100 Ω.

SWITCHING SPECIFICATIONS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD = 3.3 V, unless otherwise noted.

Table 4.

		AD9460BSVZ-80			AD9460BSVZ-105			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS								
Maximum Conversion Rate	Full	80			105			MSPS
Minimum Conversion Rate	Full			1			1	MSPS
CLK Period	Full	12.5			9.5			ns
CLK Pulse Width High[1] (t_{CLKH})	Full	5.0			3.8			ns
CLK Pulse Width Low[1] (t_{CLKL})	Full	5.0			3.8			ns
DATA OUTPUT PARAMETERS								
Output Propagation Delay—CMOS (t_{PD})[2] (Dx, DCO+)	Full		3.35			3.35		ns
Output Propagation Delay—LVDS (t_{PD})[3] (Dx+), (t_{CPD})[3] (DCO+)	Full	2.3	3.6	4.8	2.3	3.6	4.8	ns
Pipeline Delay (Latency)	Full		13			13		cycles
Aperture Delay (t_A)	Full							ns
Aperture Uncertainty (Jitter, t_J)	Full		60			60		fs, rms

[1] With duty cycle stabilizer (DCS) enabled.
[2] Output propagation delay is measured from clock 50% transition to data 50% transition with 5 pF load.
[3] LVDS R_{TERM} = 100 Ω. Measured from the 50% point of the rising edge of CLK+ to the 50% point of the data transition.

TIMING DIAGRAMS

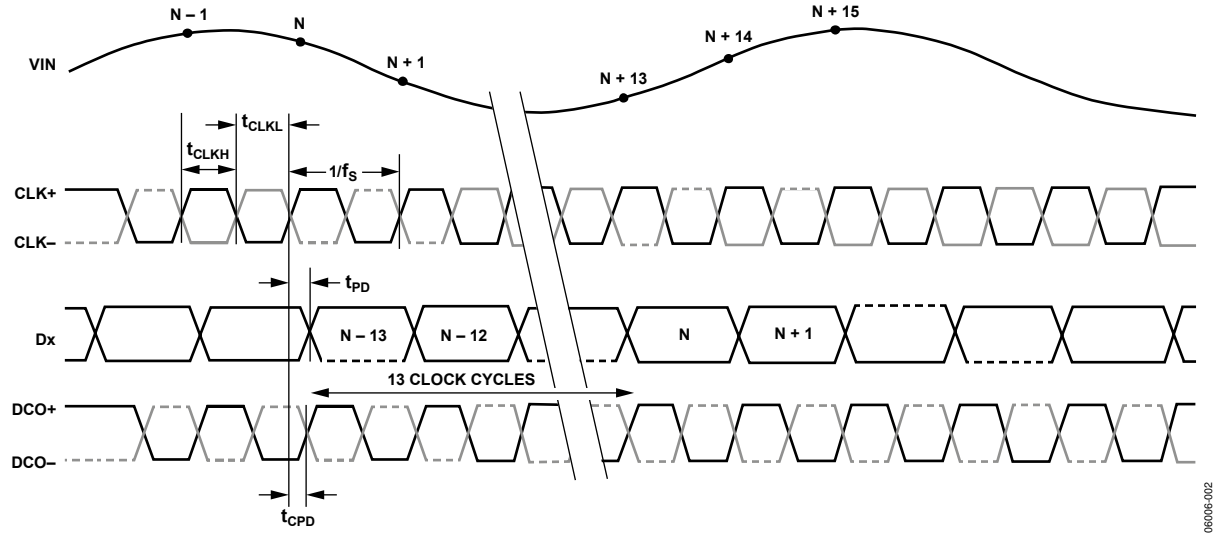

Figure 2. LVDS Mode Timing Diagram

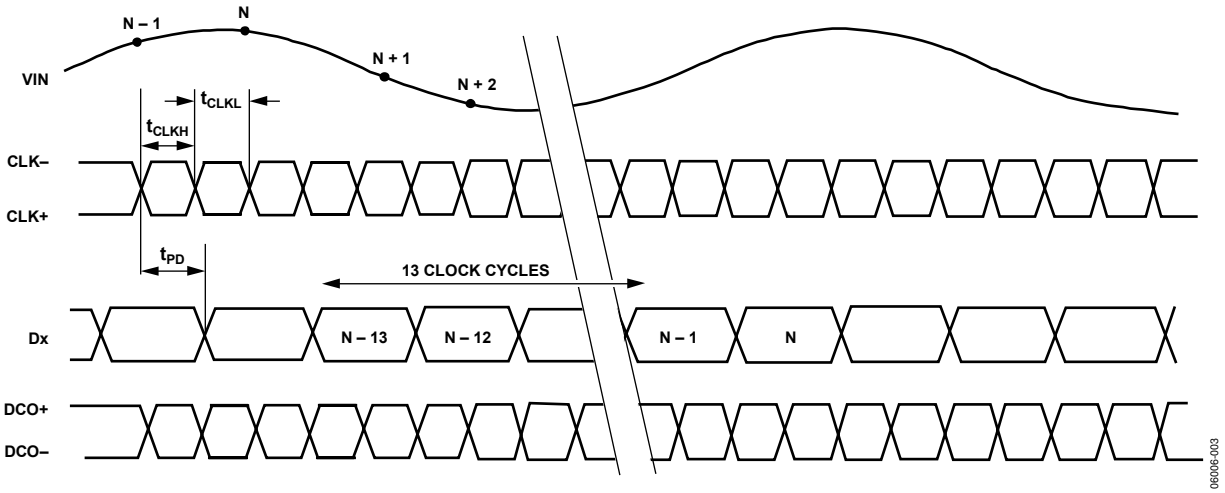

Figure 3. CMOS Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
ELECTRICAL	
AVDD1 to AGND	−0.3 V to +4 V
AVDD2 to AGND	−0.3 V to +6 V
DRVDD to DGND	−0.3 V to +4 V
AGND to DGND	−0.3 V to +0.3 V
AVDD1 to DRVDD	−4 V to +4 V
AVDD2 to DRVDD	−4 V to +6 V
AVDD2 to AVDD1	−4 V to +6 V
D0± Through D15± to DGND	−0.3 V to DRVDD + 0.3 V
CLK+/CLK− to AGND	−0.3 V to AVDD1 + 0.3 V
OUTPUT MODE, DCS MODE, and DFS to AGND	−0.3 V to AVDD1 + 0.3 V
VIN+, VIN− to AGND	−0.3 V to AVDD2 + 0.3 V
VREF to AGND	−0.3 V to AVDD1 + 0.3 V
SENSE to AGND	−0.3 V to AVDD1 + 0.3 V
REFT, REFB to AGND	−0.3 V to AVDD1 + 0.3 V
ENVIRONMENTAL	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The heat sink of the AD9460 package must be soldered to ground.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces through holes, ground, and power planes reduces the θ_{JA}. It is required that the exposed heat sink be soldered to the ground plane.

Table 6.

Package Type	θ_{JA}[1]	θ_{JB}[2]	θ_{JC}[3]	Unit
100-Lead TQFP_EP	19.8	8.3	2	°C/W

[1] Typical θ_{JA} = 19.8°C/W (heat sink soldered) for a multilayer board in still air.
[2] Typical θ_{JB} = 8.3°C/W (heat sink soldered) for a multilayer board in still air.
[3] Typical θ_{JC} = 2°C/W (junction to exposed heat sink) represents the thermal resistance through heat sink path

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

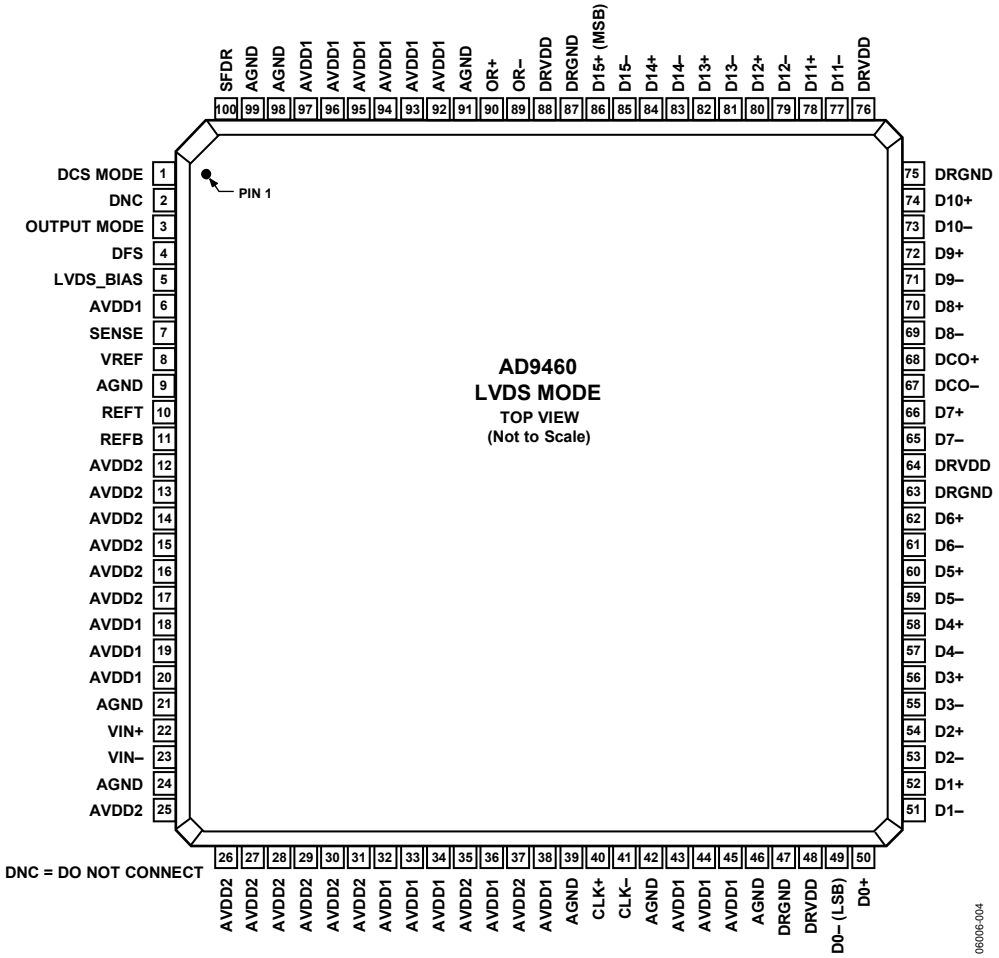

Figure 4. 100-Lead TQFP_EP Pin Configuration in LVDS Mode

Table 7. Pin Function Descriptions—100-Lead TQFP_EP in LVDS Mode

Pin No.	Mnemonic	Description
1	DCS MODE	Clock Duty Cycle Stabilizer (DCS) Control Pin. CMOS compatible. DCS = low (AGND) to enable DCS (recommended). DCS = high (AVDD1) to disable DCS.
2	DNC	Do Not Connect. This pin should float.
3	OUTPUT MODE	CMOS-Compatible Output Logic Mode Control Pin. OUTPUT MODE = 0 for CMOS mode. OUTPUT MODE = 1 (AVDD1) for LVDS outputs.
4	DFS	Data Format Select Pin. CMOS control pin that determines the format of the output data. DFS = high (AVDD1) for twos complement DFS = low (ground) for offset binary format.
5	LVDS_BIAS	Set Pin for LVDS Output Current. Place a 3.7 kΩ resistor terminated to DRGND.
6, 18 to 20, 32 to 34, 36, 38, 43 to 45, 92 to 97	AVDD1	3.3 V (±5%) Analog Supply.
7	SENSE	Reference Mode Selection. Connect to AGND for internal 1.7 V reference (3.4 V p-p analog input range); connect to AVDD1 for external reference.
8	VREF	1.7 V Reference I/O. The function is dependent on the SENSE pin and external programming resistors. Decouple to ground with 0.1 µF and 10 µF capacitors.
9, 21, 24, 39, 42, 46, 91, 98, 99, Exposed Heat Sink	AGND	Analog Ground. The exposed heat sink on the bottom of the package must be connected to AGND.

Pin No.	Mnemonic	Description
10	REFT	Differential Reference Output. Decoupled to ground with 0.1 µF capacitor and to REFB (Pin 11) with 0.1 µF and 10 µF capacitors.
11	REFB	Differential Reference Output. Decoupled to ground with a 0.1 µF capacitor and to REFT (Pin 10) with 0.1 µF and 10 µF capacitors.
12 to 17, 25 to 31, 35, 37	AVDD2	5.0 V Analog Supply (±5%).
22	VIN+	Analog Input—True.
23	VIN−	Analog Input—Complement.
40	CLK+	Clock Input—True.
41	CLK−	Clock Input—Complement.
47, 63, 75, 87	DRGND	Digital Output Ground.
48, 64, 76, 88	DRVDD	3.3 V Digital Output Supply (3.0 V to 3.6 V).
49	D0− (LSB)	D0 Complement Output Bit (LVDS Levels).
50	D0+	D0 True Output Bit.
51	D1−	D1 Complement Output Bit.
52	D1+	D1 True Output Bit.
53	D2−	D2 Complement Output Bit.
54	D2+	D2 True Output Bit.
55	D3−	D3 Complement Output Bit.
56	D3+	D3 True Output Bit.
57	D4−	D4 Complement Output Bit.
58	D4+	D4 True Output Bit.
59	D5−	D5 Complement Output Bit.
60	D5+	D5 True Output Bit.
61	D6−	D6 Complement Output Bit.
62	D6+	D6 True Output Bit.
65	D7−	D7 Complement Output Bit.
66	D7+	D7 True Output Bit.
67	DCO−	Data Clock Output—Complement.
68	DCO+	Data Clock Output—True.
69	D8−	D8 Complement Output Bit.
70	D8+	D8 True Output Bit.
71	D9−	D9 Complement Output Bit.
72	D9+	D9 True Output Bit.
73	D10−	D10 Complement Output Bit.
74	D10+	D10 True Output Bit.
77	D11−	D11 Complement Output Bit.
78	D11+	D11 True Output Bit.
79	D12−	D12 Complement Output Bit.
80	D12+	D12 True Output Bit.
81	D13−	D13 Complement Output Bit.
82	D13+	D13 True Output Bit.
83	D14−	D14 Complement Output Bit.
84	D14+	D14 True Output Bit.
85	D15−	D15 Complement Output Bit.
86	D15+ (MSB)	D15 True Output Bit.
89	OR−	Out-of-Range Complement Output Bit.
90	OR+	Out-of-Range True Output Bit.
100	SFDR	SFDR Control Pin. CMOS-compatible control pin for optimizing the configuration of the AD9460 analog front end. Connecting SFDR to AGND optimizes SFDR performance for applications with analog input frequencies <200 MHz for 80 MSPS and 105 MSPS speed grades. For applications with analog inputs >200 MHz, connect this pin to AVDD1 for optimum SFDR performance; power dissipation from AVDD2 increases by ~70 mW for the AD9460BSVZ-80 and ~20 mW for the AD9460BSVZ-105.

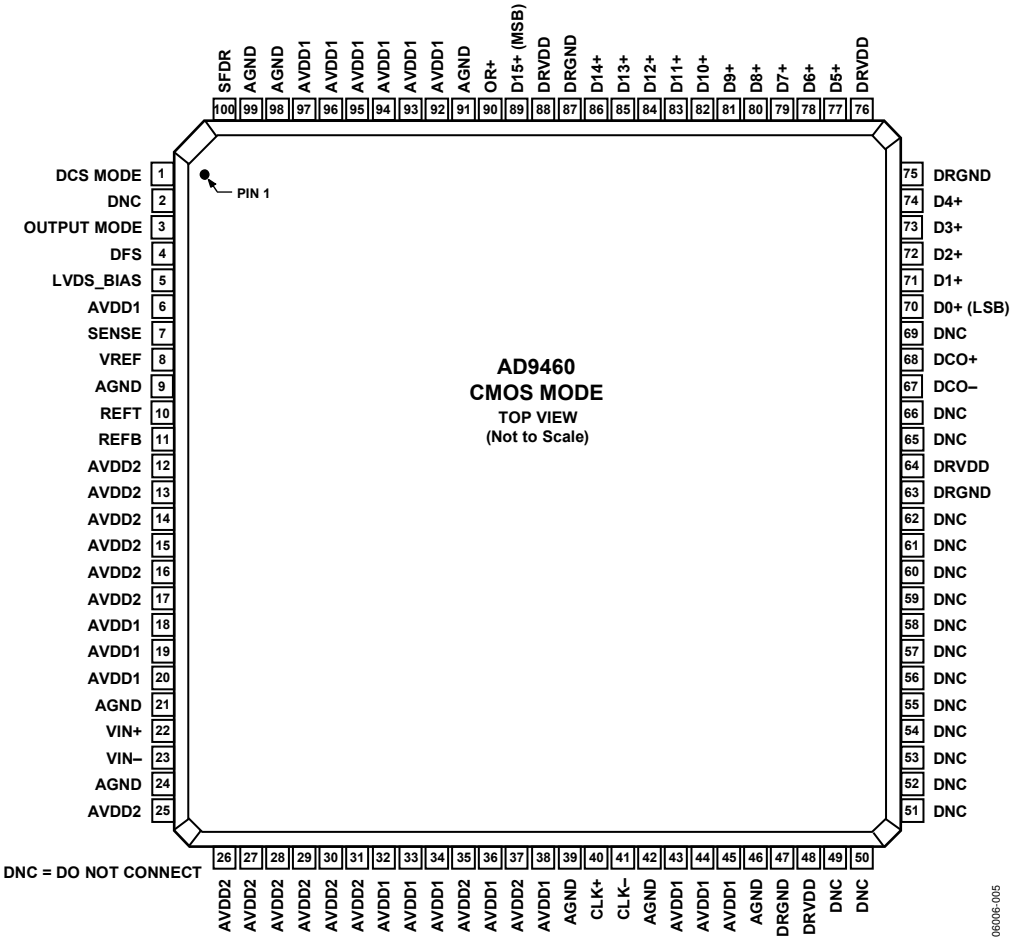

Figure 5. 100-Lead TQFP_EP Pin Configuration in CMOS Mode

Table 8. Pin Function Descriptions—100-Lead TQFP_EP in CMOS Mode

Pin No.	Mnemonic	Description
1	DCS MODE	Clock Duty Cycle Stabilizer (DCS) Control Pin. CMOS compatible. DCS = low (AGND) to enable DCS (recommended). DCS = high (AVDD1) to disable DCS.
2, 49 to 62, 65 to 66, 69	DNC	Do Not Connect. These pins should float.
3	OUTPUT MODE	CMOS-Compatible Output Logic Mode Control Pin. OUTPUT MODE = 0 for CMOS mode. OUTPUT MODE = 1 (AVDD1) for LVDS outputs.
4	DFS	Data Format Select Pin. CMOS control pin that determines the format of the output data. DFS = high (AVDD1) for twos complement. DFS = low (ground) for offset binary format.
5	LVDS_BIAS	Set Pin for LVDS Output Current. Place a 3.7 kΩ resistor terminated to DRGND.
6, 18 to 20, 32 to 34, 36, 38, 43 to 45, 92 to 97	AVDD1	3.3 V (±5%) Analog Supply.
7	SENSE	Reference Mode Selection. Connect to AGND for internal 1.7 V reference (3.4 V p-p analog input range); connect to AVDD1 for external reference.
8	VREF	1.7 V Reference I/O. The function is dependent on the SENSE pin and external programming resistors. Decouple to ground with 0.1 µF and 10 µF capacitors.
9, 21, 24, 39, 42, 46, 91, 98, 99, Exposed Heat Sink	AGND	Analog Ground. The exposed heat sink on the bottom of the package must be connected to AGND.
10	REFT	Differential Reference Output. Decoupled to ground with 0.1 µF capacitor and to REFB (Pin 11) with 0.1 µF and 10 µF capacitors.

Pin No.	Mnemonic	Description
11	REFB	Differential Reference Output. Decoupled to ground with a 0.1 µF capacitor and to REFT (Pin 10) with 0.1 µF and 10 µF capacitors.
12 to 17, 25 to 31, 35, 37	AVDD2	5.0 V Analog Supply (±5%).
22	VIN+	Analog Input—True.
23	VIN−	Analog Input—Complement.
40	CLK+	Clock Input—True.
41	CLK−	Clock Input—Complement.
47, 63, 75, 87	DRGND	Digital Output Ground.
48, 64, 76, 88	DRVDD	3.3 V Digital Output Supply (3.0 V to 3.6 V).
67	DCO−	Data Clock Output—Complement.
68	DCO+	Data Clock Output—True.
70	D0+ (LSB)	D0 True Output Bit (CMOS Levels).
71	D1+	D1 True Output Bit.
72	D2+	D2 True Output Bit.
73	D3+	D3 True Output Bit.
74	D4+	D4 True Output Bit.
77	D5+	D5 True Output Bit.
78	D6+	D6 True Output Bit.
79	D7+	D7 True Output Bit.
80	D8+	D8 True Output Bit.
81	D9+	D9 True Output Bit.
82	D10+	D10 True Output Bit.
83	D11+	D11 True Output Bit.
84	D12+	D12 True Output Bit.
85	D13+	D13 True Output Bit.
86	D14+	D14 True Output Bit.
89	D15+ (MSB)	D15 True Output Bit.
90	OR+	Out-of-Range True Output Bit.
100	SFDR	SFDR Control Pin. CMOS-compatible control pin for optimizing the configuration of the AD9460 analog front end. Connecting SFDR to AGND optimizes SFDR performance for applications with analog input frequencies <200 MHz for 80 MSPS and 105 MSPS speed grades. For applications with analog inputs >200 MHz, connect this pin to AVDD1 for optimum SFDR performance; power dissipation from AVDD2 increases by ~70 mW for the AD9460BSVZ-80 and ~20 mW for the AD9460BSVZ-105.

EQUIVALENT CIRCUITS

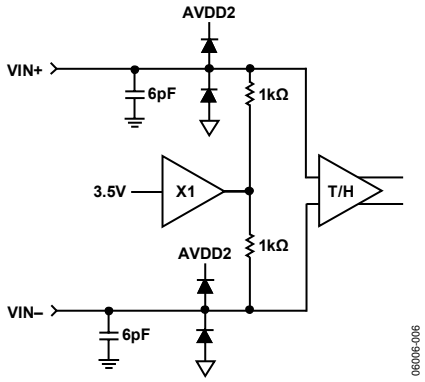

Figure 6. Equivalent Analog Input Circuit

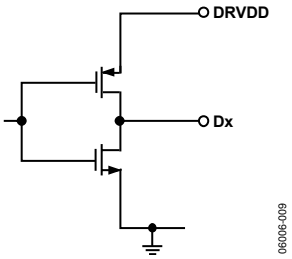

Figure 9. Equivalent CMOS Digital Output Circuit

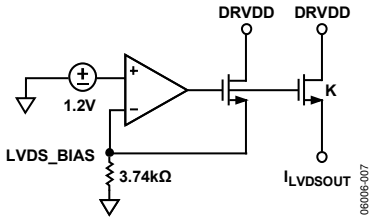

Figure 7. Equivalent LVDS_BIAS Circuit

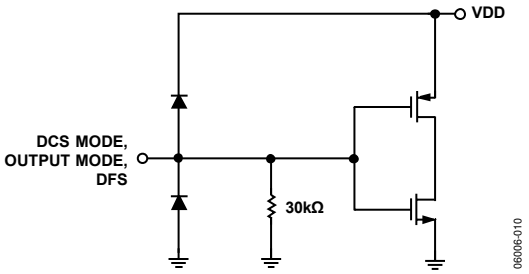

Figure 10. Equivalent Digital Input Circuit, DFS, DCS MODE, OUTPUT MODE

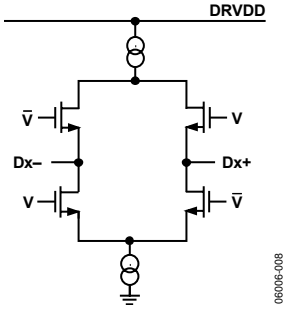

Figure 8. Equivalent LVDS Digital Output Circuit

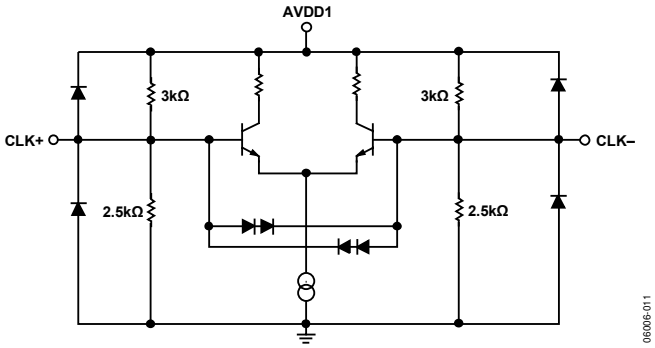

Figure 11. Equivalent Sample Clock Input Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD = 3.3 V, rated sample rate, LVDS mode, DCS enabled, T_A = 25°C, 3.4 V p-p differential input, AIN = −1 dBFS, internal trimmed reference (nominal VREF = 1.7 V), unless otherwise noted.

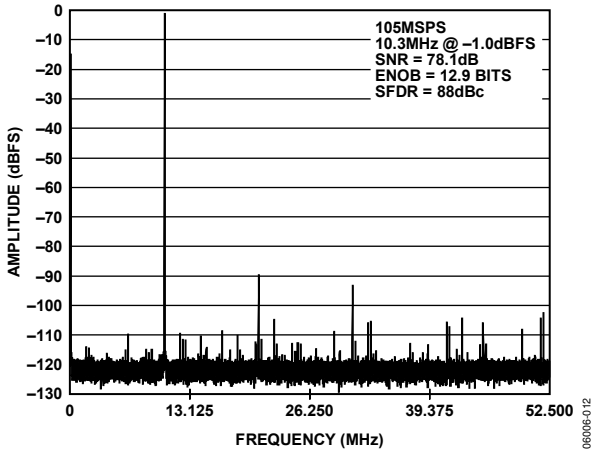

Figure 12. 105 MSPS, 64k Point, Single-Tone FFT, 10.3 MHz

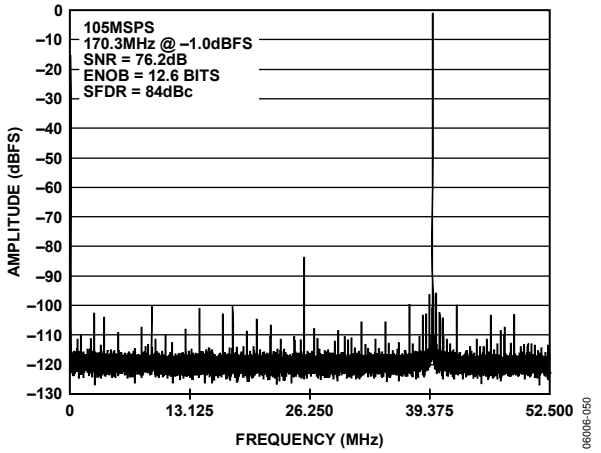

Figure 13. 105 MSPS, 64k Point, Single-Tone FFT, 170.3 MHz

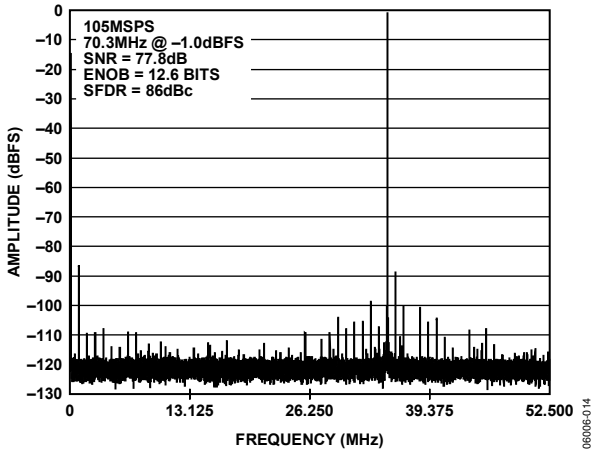

Figure 14. 105 MSPS, 64k Point, Single-Tone FFT, 70.3 MHz

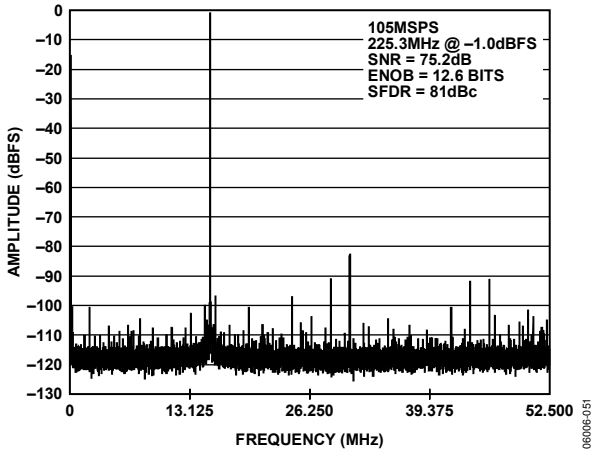

Figure 15. 105 MSPS, 64k Point, Single-Tone FFT, 225.3 MHz

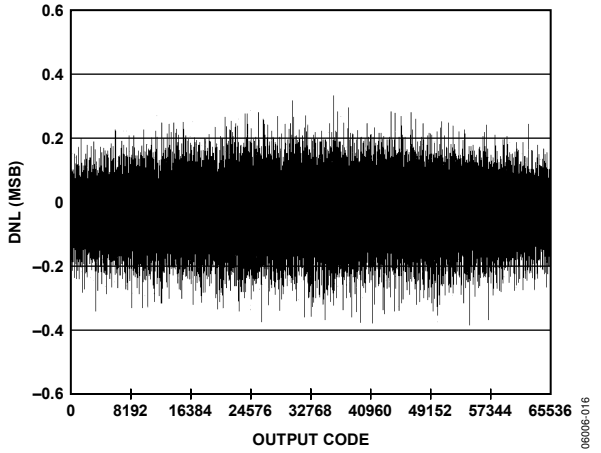

Figure 16. 105 MSPS, DNL Error vs. Output Code, 10.3 MHz

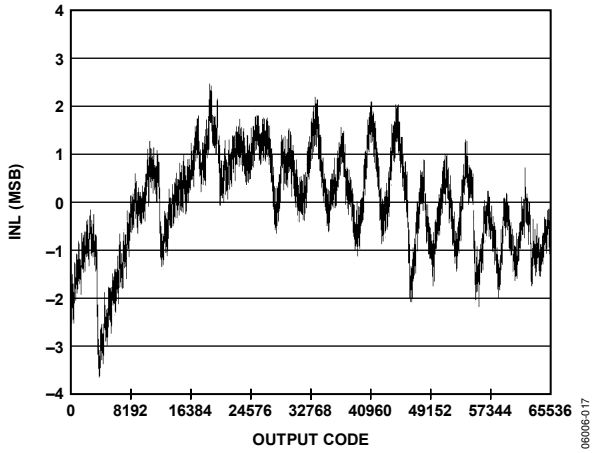

Figure 17. 105 MSPS, INL Error vs. Output Code, 10.3 MHz

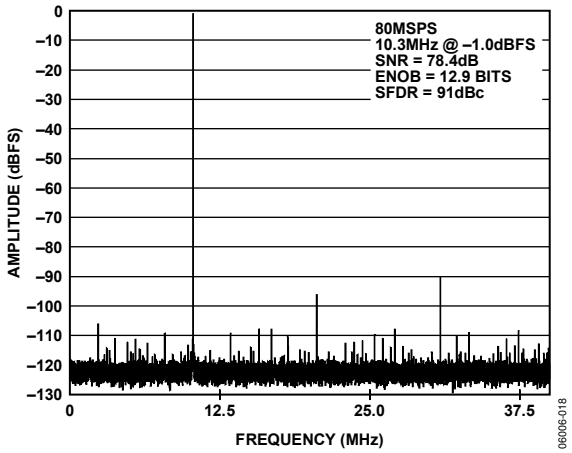

Figure 18. 80 MSPS, 64k Point Single-Tone FFT, 10.3 MHz

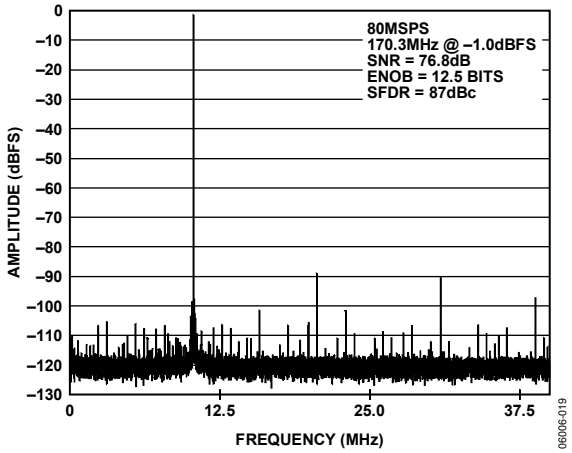

Figure 19. 80 MSPS, 64k Point, Single-Tone FFT, 170.3 MHz

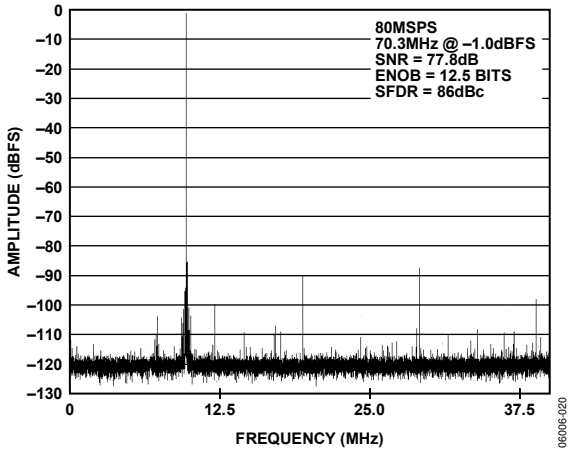

Figure 20. 80 MSPS, 64k Point, Single-Tone FFT, 70.3 MHz

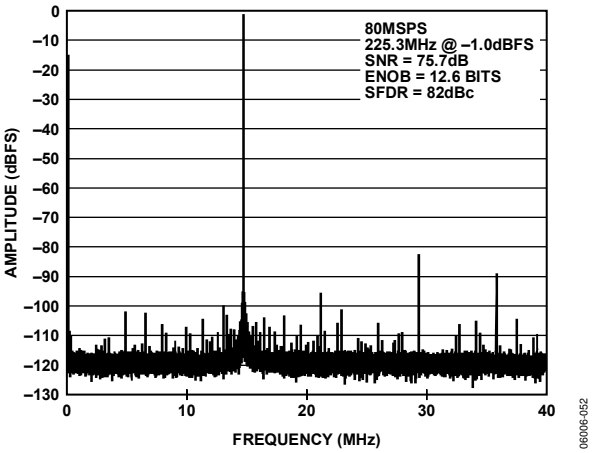

Figure 21. 80 MSPS, 64k Point Single-Tone FFT, 225.3 MHz

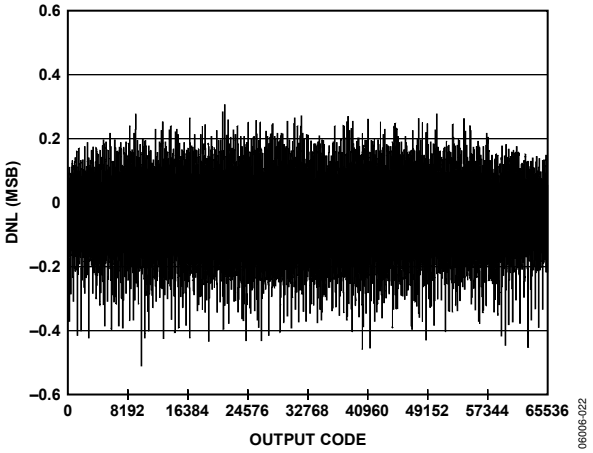

Figure 22. 80 MSPS, DNL Error vs. Output Code, 10.3 MHz

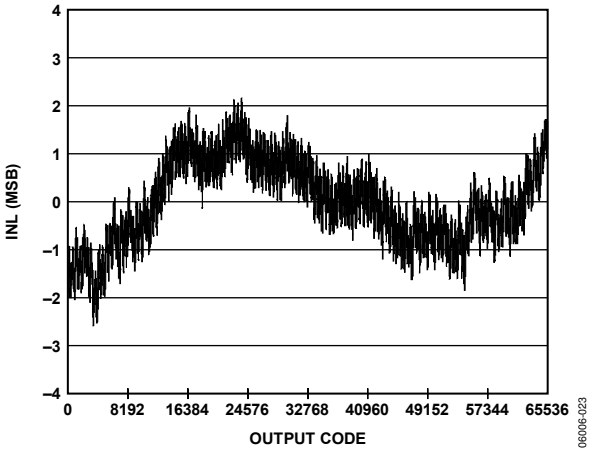

Figure 23. 80 MSPS, INL Error vs. Output Code, 10.3 MHz

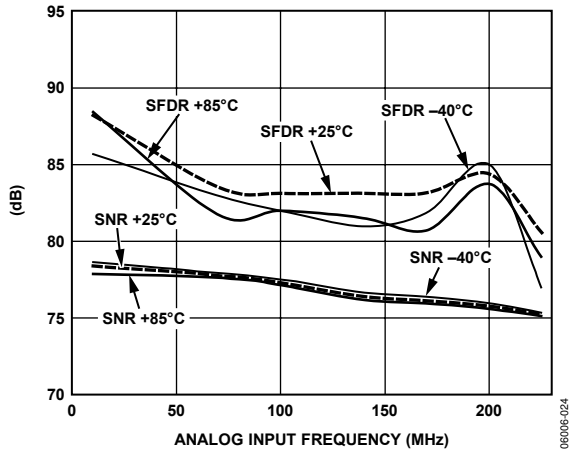

Figure 24. 105 MSPS, SNR/SFDR vs. Analog Input Frequency, 3.4 V p-p

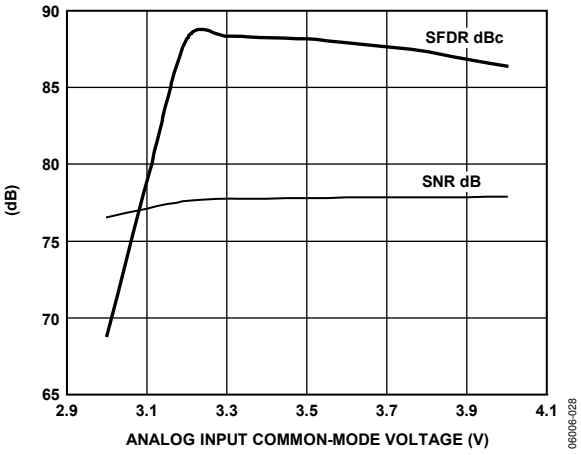

Figure 27. 105 MSPS, SNR/SFDR vs. Analog Input Common Mode

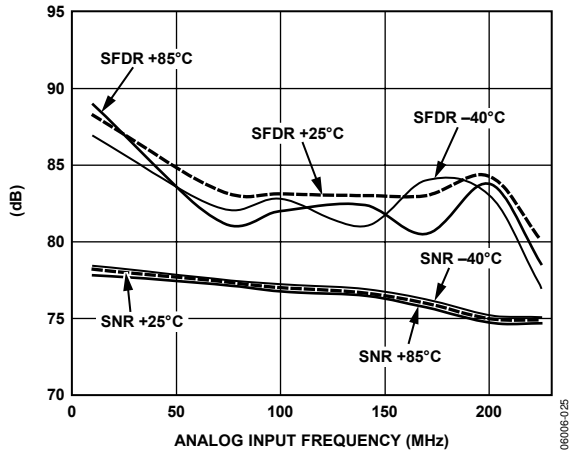

Figure 25. 105 MSPS, SNR/SFDR vs. Analog Input Frequency, 3.4 V p-p, CMOS Mode

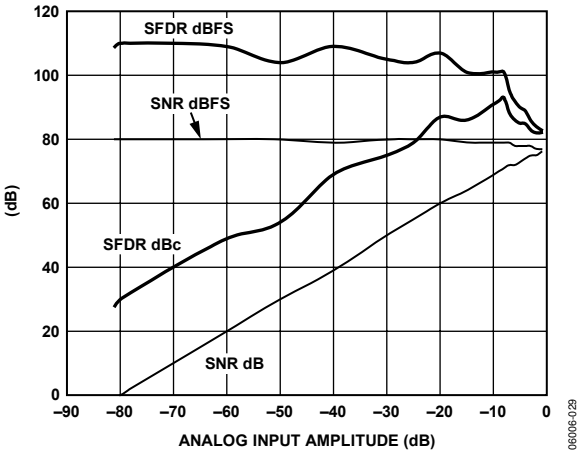

Figure 28. 105 MSPS, 170.3 MHz SNR/SFDR vs. Analog Input Level, CMOS Output Mode

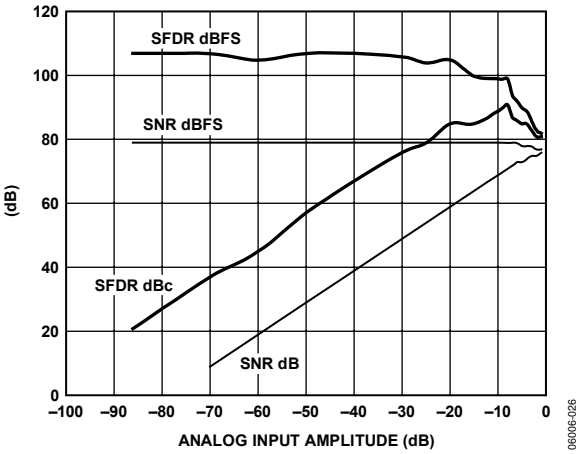

Figure 26. 105 MSPS, 170.3 MHz SNR/SFDR vs. Analog Input Level

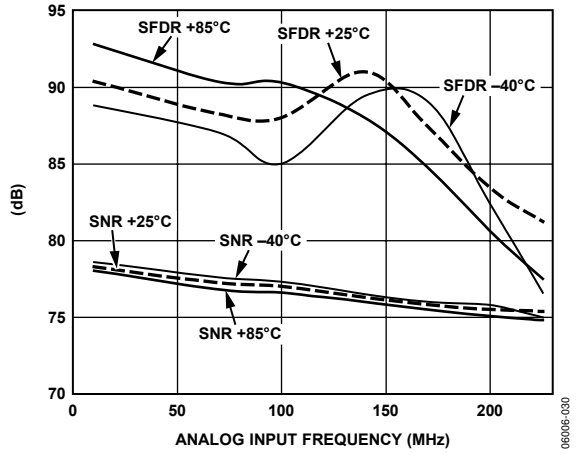

Figure 29. 80 MSPS, SNR/SFDR vs. Analog Input Frequency, 3.4 V p-p, CMOS Mode

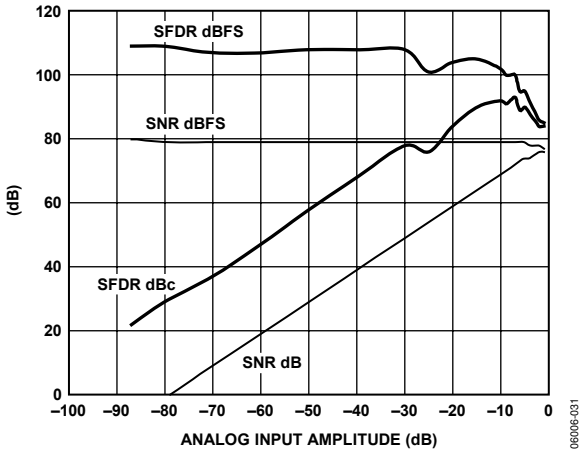

Figure 30. 80 MSPS, 170.3 MHz SNR/SFDR vs. Analog Input Level

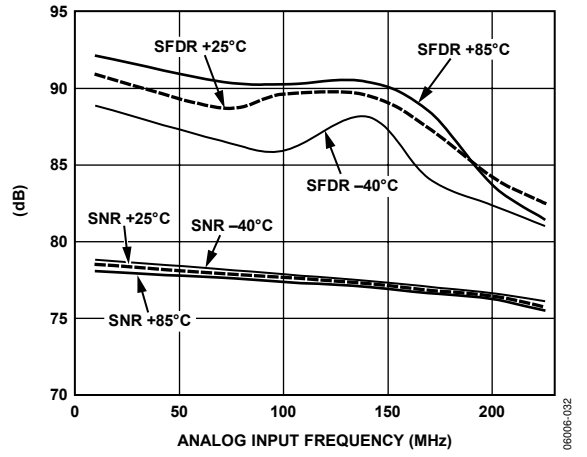

Figure 31. 80 MSPS, SNR/SFDR vs. Analog Input Frequency, 3.4 V p-p

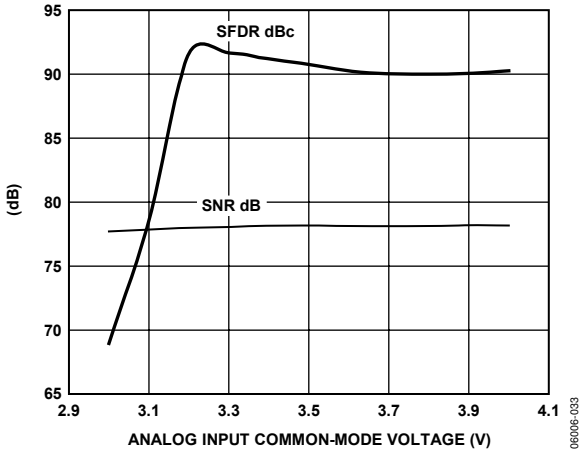

Figure 32. 80 MSPS, SNR/SFDR vs. Analog Input Common Mode

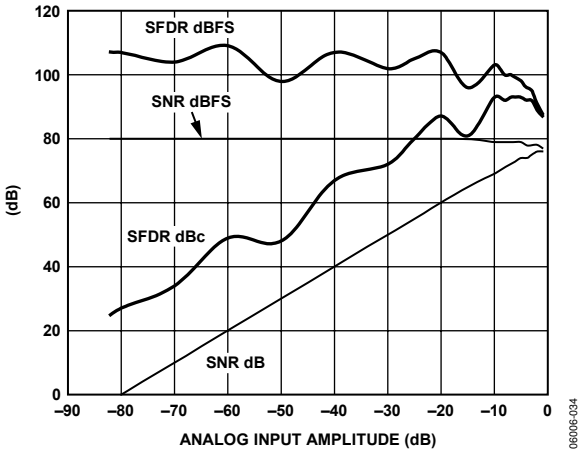

Figure 33. 80 MSPS, 170.3 MHz SNR/SFDR vs. Analog Input Level, CMOS Output Mode

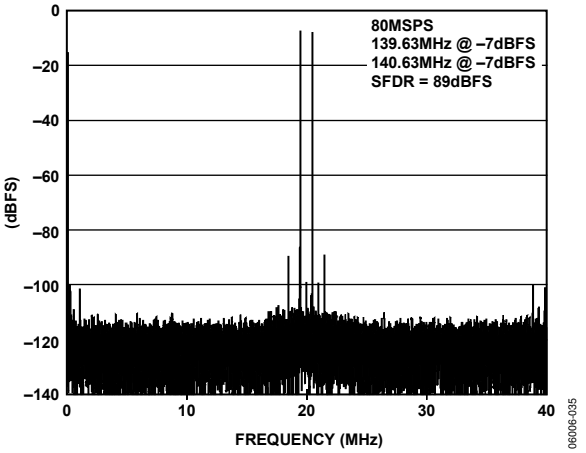

Figure 34. 80 MSPS, 64k Point Two-Tone FFT, 139.6 MHz, 140.6 MHz

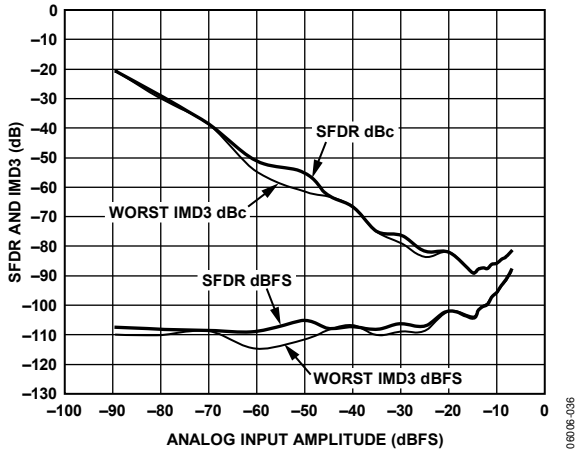

Figure 35. 80 MSPS, 64k Point Two-Tone FFT, 139.6 MHz, 140.6 MHz

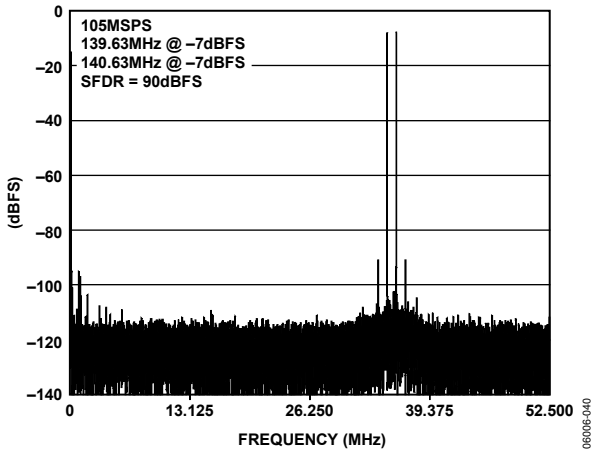

Figure 36. 105 MSPS, 64k Point Two-Tone FFT, 139.6 MHz, 140.6 MHz

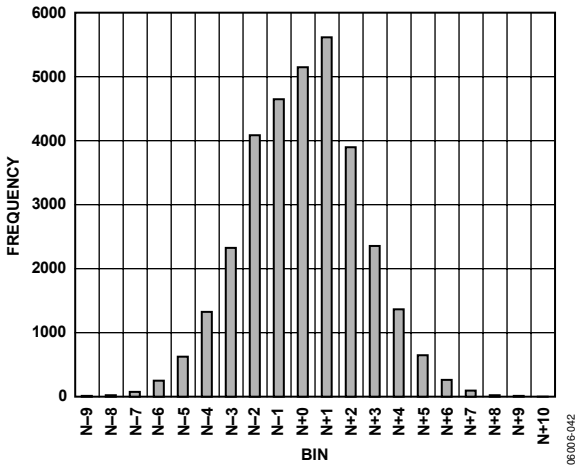

Figure 38. 80 MSPS, Grounded Input Histogram

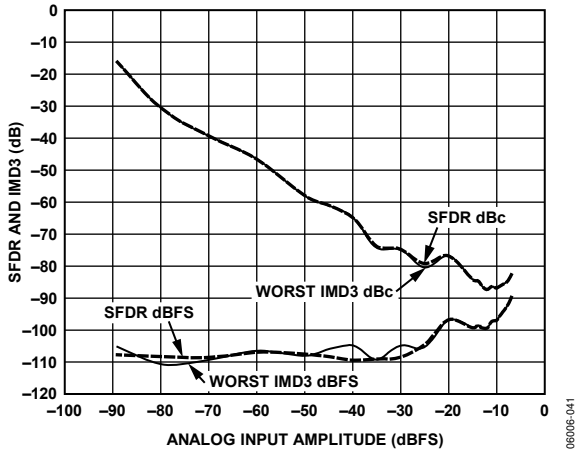

Figure 37. 105 MSPS, Two-Tone SFDR vs. Analog Input Level, 139.6 MHz, 140.6 MHz

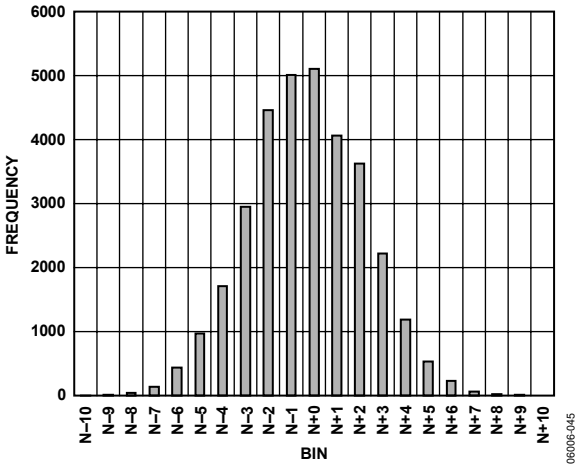

Figure 39 105 MSPS, Grounded Input Histogram

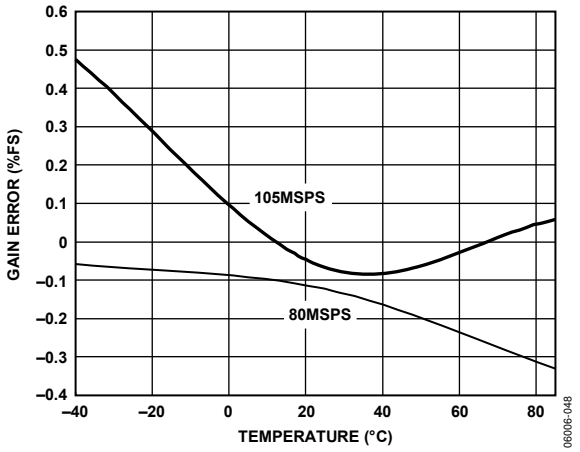

Figure 40. Gain vs. Temperature

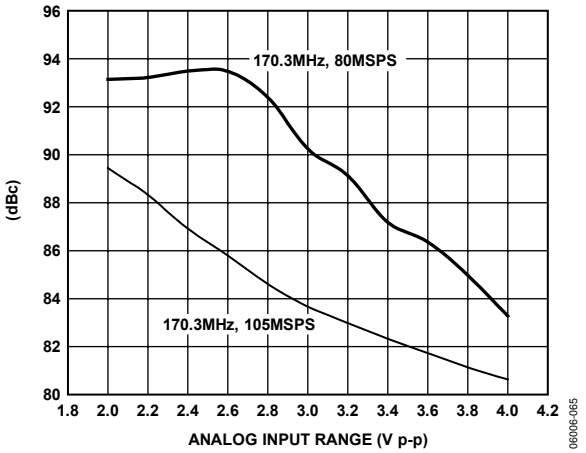

Figure 42. SFDR vs. Analog Input Range

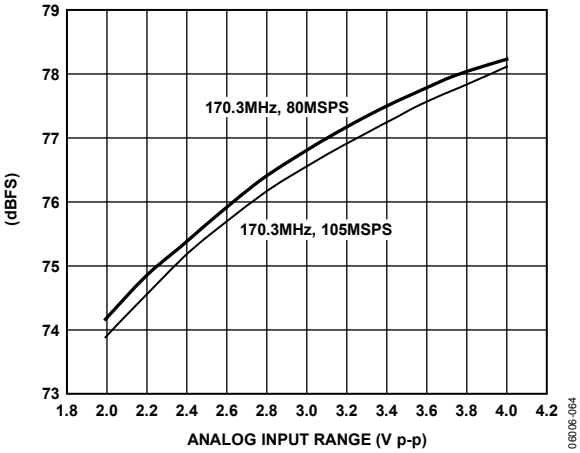

Figure 41. SNR vs. Analog Input Range

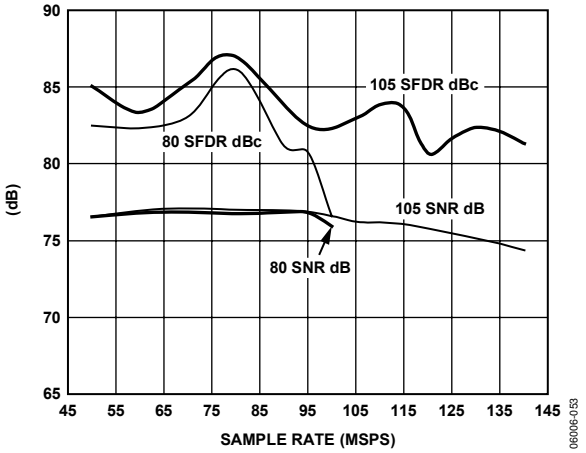

Figure 43. Single-Tone SNR/SFDR vs. Sample Rate, 170.3 MHz

TERMINOLOGY

Analog Bandwidth (Full Power Bandwidth)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay (t_A)
The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter, t_J)
The sample-to-sample variation in aperture delay.

Clock Pulse Width and Duty Cycle
Pulse width high is the minimum amount of time that the clock pulse should be left in the Logic 1 state to achieve rated performance. Pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 16-bit resolution indicates that all 65,536 codes must be present over all operating ranges.

Integral Nonlinearity (INL)
INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Signal-to-Noise and Distortion (SINAD)
SINAD is the ratio of the rms input signal amplitude to the rms value of the sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms input signal amplitude to the rms value of the sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
SFDR is the ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may be a harmonic. SFDR can be reported in dBc (that is, degrades as signal level is lowered) or dBFS (always related back to converter full scale).

Total Harmonic Distortion (THD)
The ratio of the rms input signal amplitude to the rms value of the sum of the first six harmonic components.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product.

Effective Number of Bits (ENOB)
The effective number of bits for a sine wave input at a given input frequency can be calculated directly from its measured SINAD using the following formula:

$$ENOB = \frac{(SINAD - 1.76)}{6.02}$$

Gain Error
The first code transition should occur at an analog value of ½ LSB above negative full scale. The last transition should occur at an analog value of 1½ LSB below the positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Maximum Conversion Rate
The clock rate at which parametric testing is performed.

Minimum Conversion Rate
The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Offset Error
The major carry transition should occur for an analog value of ½ LSB below VIN+ = VIN−. Offset error is defined as the deviation of the actual transition from that point.

Out-of-Range Recovery Time
The time it takes for the ADC to reacquire the analog input after a transition from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Output Propagation Delay (t_{PD})
The delay between the clock rising edge and the time when all bits are within valid logic levels.

Power-Supply Rejection Ratio
The change in full scale from the value with the supply at the minimum limit to the value with the supply at the maximum limit.

Temperature Drift
The temperature drift for offset error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

THEORY OF OPERATION

The AD9460 architecture is optimized for high speed and ease of use. The analog inputs drive an integrated, high bandwidth track-and-hold circuit that samples the signal prior to quantization by the 16-bit pipeline ADC core. The device includes an on-board reference and input logic that accepts TTL, CMOS, or LVPECL levels. The digital output logic levels are user selectable as standard 3 V CMOS or LVDS (ANSI-644 compatible) via the OUTPUT MODE pin.

ANALOG INPUT AND REFERENCE OVERVIEW

A stable and accurate 0.5 V band gap voltage reference is built into the AD9460. The input range can be adjusted by varying the reference voltage applied to the AD9460, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly.

Internal Reference Connection

A comparator within the AD9460 detects the potential at the SENSE pin and configures the reference into three possible states, summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 44), setting VREF to ~1.7 V. If a resistor divider is connected as shown in Figure 45, the switch again sets to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$VREF = 0.5\ \text{V} \times \left(1 + \frac{R2}{R1}\right)$$

In all reference configurations, REFT and REFB drive the analog-to-digital conversion core and establish its input span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

Internal Reference Trim

The internal reference voltage is trimmed during the production test; therefore, there is little advantage to the user supplying an external voltage reference to the AD9460. The gain trim is performed with the AD9460 input range set to 3.4 V p-p nominal (SENSE connected to AGND). Because of this trim, and the maximum ac performance provided by the 3.4 V p-p analog input range, there is little benefit to using analog input ranges <2 V p-p. However, reducing the range can improve SFDR performance in some applications. Likewise, increasing the range up to 3.4 V p-p can improve SNR. Users are cautioned that the differential nonlinearity of the ADC varies with the reference voltage. Configurations that use <2.0 V p-p can exhibit missing codes and, therefore, degraded noise and distortion performance.

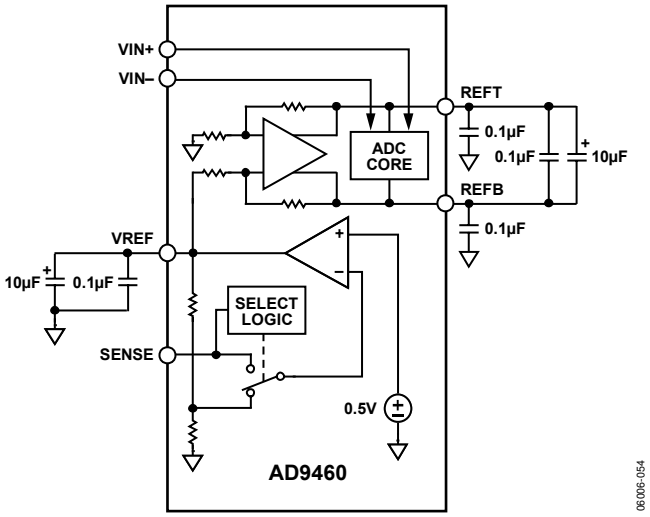

Figure 44. Internal Reference Configuration

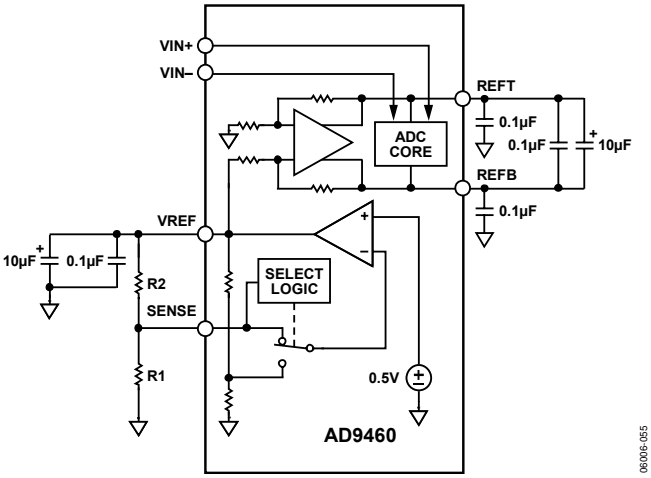

Figure 45. Programmable Reference Configuration

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × external reference
Programmable Reference	0.2 V to VREF	$0.5 \times 1+\frac{R2}{R1}$ (See Figure 45)	2 × VREF
Programmable Reference (Set for 2 V p-p)	0.2 V to VREF	$0.5 \times \left(1+\frac{R2}{R1}\right)$, R1 = R2 = 1 kΩ	2.0
Internal Fixed Reference	AGND to 0.2 V	1.7	3.4

External Reference Operation

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7 kΩ load. The internal buffer continues to generate the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span is always twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 2.0 V. See Figure 40 for gain variation vs. temperature.

Analog Inputs

As with most new high speed, high dynamic range ADCs, the analog input to the AD9460 is differential. Differential inputs improve on-chip performance because signals are processed through attenuation and gain stages. Most of the improvement is a result of differential analog stages having high rejection of even-order harmonics. There are also benefits at the PCB level. First, differential inputs have high common-mode rejection of stray signals, such as ground and power noise. Second, they provide good rejection of common-mode signals, such as local oscillator feedthrough. The specified noise and distortion of the AD9460 cannot be realized with a single-ended analog input; therefore, such configurations are discouraged. Contact sales for recommendations of other 16-bit ADCs that support single-ended analog input configurations.

With the 1.7 V reference, which is the nominal value (see the Internal Reference Trim section), the differential input range of the AD9460 analog input is nominally 3.4 V p-p or 1.7 V p-p on each input (VIN+ or VIN−).

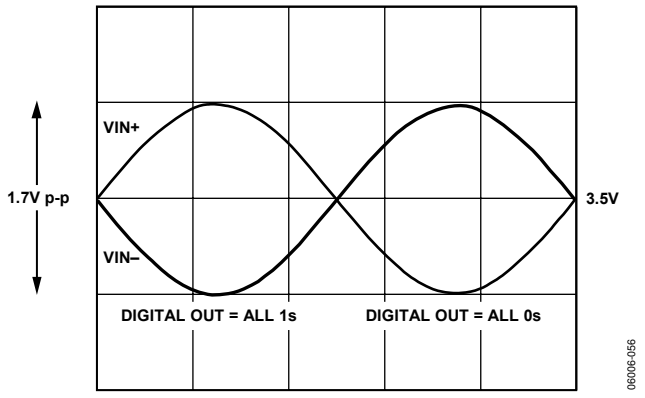

Figure 46. Differential Analog Input Range for VREF = 1.7 V

The AD9460 analog input voltage range is offset from ground by 3.5 V. Each analog input connects through a 1 kΩ resistor to the 3.5 V bias voltage and to the input of a differential buffer. The internal bias network on the input properly biases the buffer for maximum linearity and range (see the Equivalent Circuits section). Therefore, the analog source driving the AD9460 should be ac-coupled to the input pins. The recommended method for driving the analog input of the AD9460 is to use an RF transformer to convert single-ended signals to differential signals (see Figure 47).

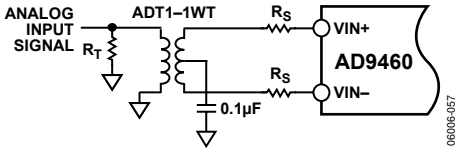

Figure 47. Transformer-Coupled Analog Input Circuit

Series resistors between the output of the transformer and the AD9460 analog inputs help isolate the analog input source from switching transients caused by the internal sample-and-hold circuit. The series resistors, along with the 1 kΩ resisters connected to the internal 3.5 V bias, must be considered in impedance matching the transformer input. For example, if R_T is set to 51 Ω, R_S is set to 33 Ω, and there is a 1:1 impedance ratio transformer, then the input matches a 50 Ω source with a full-scale drive of 16.0 dBm. The 50 Ω impedance matching can also be incorporated on the secondary side of the transformer, as shown in the evaluation board schematic (see Figure 50).

CLOCK INPUT CONSIDERATIONS

Any high speed ADC is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock combines with the desired signal at the analog-to-digital output. For that reason, considerable care was taken in the design of the clock inputs of the AD9460, and the user is advised to give careful thought to the clock source.

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, can be sensitive to the clock duty cycle. Commonly a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9460 contains a clock duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock

signal with a nominal ~50% duty cycle. Noise and distortion performance are nearly flat for a 30% to 70% duty cycle with the DCS enabled. The DCS circuit locks to the rising edge of CLK+ and optimizes timing internally. This allows for a wide range of input duty cycles at the input without degrading performance. Jitter in the rising edge of the input is still of paramount concern and is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 30 MHz nominally. The loop is associated with a time constant that should be considered in applications where the clock rate can change dynamically, requiring a wait time of 1.5 µs to 5 µs after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time that the loop is not locked, the DCS loop is bypassed, and the internal device timing is dependent on the duty cycle of the input clock signal. In such an application, it can be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

The DCS circuit is controlled by the DCS MODE pin; a CMOS logic low (AGND) on DCS MODE enables the duty cycle stabilizer, and logic high (AVDD1 = 3.3 V) disables the controller.

The AD9460 input sample clock signal must be a high quality, extremely low phase noise source to prevent degradation of performance. Maintaining 16-bit accuracy places a premium on the encode clock phase noise. SNR performance can easily degrade by 3 dB to 4 dB with 70 MHz analog input signals when using a high jitter clock source. See the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance,* for more information. For optimum performance, the AD9460 must be clocked differentially. The sample clock inputs are internally biased to ~1.5 V, and the input signal is usually ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. Figure 48 shows one preferred method for clocking the AD9460. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary of the transformer limit clock excursions into the AD9460 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9460 and limits the noise presented to the sample clock inputs.

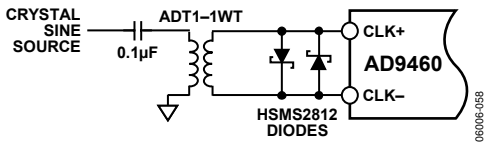

Figure 48. Crystal Clock Oscillator, Differential Encode

If a low jitter clock is available, it helps to band-pass filter the clock reference before driving the ADC clock inputs. Another option is to ac couple a differential ECL/PECL signal to the encode input pins, as shown in Figure 49.

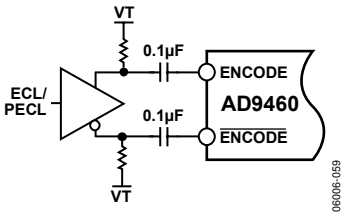

Figure 49. Differential ECL for Encode

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{INPUT}) and rms amplitude due only to aperture jitter (t_J) can be calculated using the following equation:

$$SNR = 20 \log[2\pi f_{INPUT} \times t_J]$$

In the equation, the rms aperture jitter represents the root-mean-square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter.

The clock input should be treated as an analog signal in cases where aperture jitter can affect the dynamic range of the AD9460. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be synchronized by the original clock during the last step.

POWER CONSIDERATIONS

Care should be taken when selecting a power source. The use of linear dc supplies is highly recommended. Switching supplies tend to have radiated components that can be received by the AD9460. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1 µF chip capacitors.

The AD9460 has separate digital and analog power supply pins. The analog supplies are denoted AVDD1 (3.3 V) and AVDD2 (5 V), and the digital supply pins are denoted DRVDD. Although the AVDD1 and DRVDD supplies can be tied together, best performance is achieved when the supplies are separate. This is because the fast digital output swings can couple switching current back into the analog supplies. Note that both AVDD1 and AVDD2 must be held within 5% of the specified voltage.

The DRVDD supply of the AD9460 is a dedicated supply for the digital outputs in either LVDS or CMOS output modes. When in LVDS mode, the DRVDD should be set to 3.3 V. In CMOS mode, the DRVDD supply can be connected from 2.5 V to 3.6 V for compatibility with the receiving logic.

DIGITAL OUTPUTS

LVDS Mode

The off-chip drivers on the chip can be configured to provide LVDS-compatible output levels via Pin 3 (OUTPUT MODE). LVDS outputs are available when OUTPUT MODE is CMOS logic high (or AVDD1 for convenience) and a 3.74 kΩ R_{SET} resistor is placed at Pin 5 (LVDS_BIAS) to ground. Dynamic performance, including both SFDR and SNR, maximizes when using the AD9460 in LVDS mode; designers are encouraged to take advantage of this mode. The AD9460 outputs include complementary LVDS outputs for each data bit (Dx+/Dx−), the overrange output (OR+/OR−), and the output data clock output (DCO+/DCO−). The R_{SET} resistor current is multiplied on-chip, setting the output current at each output equal to a nominal 3.5 mA ($11 \times I_{RSET}$). A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver. LVDS mode facilitates interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended, with a 100 Ω termination resistor located as close to the receiver as possible. It is recommended to keep the trace length less than two inches and to keep differential output trace lengths as equal as possible.

CMOS Mode

In applications that can tolerate a slight degradation in dynamic performance, the AD9460 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. CMOS outputs are available when OUTPUT MODE is CMOS logic low (or AGND for convenience). In this mode, the output data bits, Dx, are single-ended CMOS, as is the overrange output, OR+. The output clock serves as a differential CMOS signal, DCO+/DCO−. Lower supply voltages are recommended to avoid coupling switching transients back to the sensitive analog sections of the ADC. Minimize the capacitive load to the CMOS outputs and connect each output to a single gate through a series resistor (220 Ω) to minimize switching transients caused by the capacitive loading.

TIMING

The AD9460 provides latched data outputs with a pipeline delay of 13 clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of CLK+. Refer to Figure 2 and Figure 3 for detailed timing diagrams.

OPERATIONAL MODE SELECTION

Data Format Select

The data format select (DFS) pin of the AD9460 determines the coding format of the output data. This pin is 3.3 V CMOS compatible, with logic high (or AVDD1, 3.3 V) selecting twos complement and DFS logic low (AGND) selecting offset binary format. Table 10 summarizes the output coding.

Output Mode Select

The OUPUT MODE pin controls the logic compatibility, as well as the pinout of the digital outputs. This pin is a CMOS-compatible input. With OUTPUT MODE = 0 (AGND), the AD9460 outputs are CMOS compatible, and the pin assignment for the device is as defined in Table 8. With OUTPUT MODE = 1 (AVDD1, 3.3 V), the AD9460 outputs are LVDS compatible, and the pin assignment for the device is as defined in Table 7.

Duty Cycle Stabilizer

The DCS circuit is controlled by the DCS MODE pin; a CMOS logic low (AGND) on DCS MODE enables the DCS, and logic high (AVDD1, 3.3 V) disables the controller.

SFDR Enhancement

Under certain conditions, the SFDR performance of the AD9460 improves by adding some additional power to the core of the ADC. The SFDR control pin (Pin 100) is a CMOS-compatible control pin to optimize the configuration of the AD9460 analog front end. Connecting SFDR to AGND optimizes SFDR performance for applications with analog input frequencies <200 MHz for 80 MSPS and 105 MSPS speed grades. For applications with analog inputs >200 MHz, this pin should be connected to AVDD1 for optimum SFDR performance; power dissipation from AVDD2 increases by ~70 mW for the AD9460BSVZ-80 and ~20 mW for the AD9460BSVZ-105.

Table 10. Digital Output Coding

Code	VIN+ – VIN− Input Span = 3.4 V p-p (V)	VIN+ – VIN− Input Span = 2 V p-p (V)	Digital Output Offset Binary (D15…D0)	Digital Output Twos Complement (D15…D0)
65,536	+1.700	+1.000	1111 1111 1111 1111	0111 1111 1111 1111
32,768	0	0	1000 0000 0000 0000	0000 0000 0000 0000
32,767	−0.000052	−0.000031	0111 1111 1111 1111	1111 1111 1111 1111
0	−1.70	−1.00	0000 0000 0000 0000	1000 0000 0000 0000

EVALUATION BOARD

Evaluation boards are offered to configure the AD9460 in either CMOS mode or LVDS mode only. This design represents a recommended configuration for using the device over a wide range of sampling rates and analog input frequencies. These evaluation boards provide all the support circuitry required to operate the ADC in its various modes and configurations. Complete schematics are shown in Figure 50 through Figure 53. Gerber files are available from engineering applications demonstrating the proper routing and grounding techniques that should be applied at the system level.

It is critical that signal sources with very low phase noise (<60 fsec rms jitter) are used to realize the ultimate performance of the converter. Proper filtering of the input signal to remove harmonics and lower the integrated noise at the input is also necessary to achieve the specified noise performance.

The evaluation boards are shipped with a 115 V ac to 6 V dc power supply. The evaluation boards include low dropout regulators to generate the various dc supplies required by the AD9460 and its support circuitry. Separate power supplies are provided to isolate the DUT from the support circuitry. Each input configuration can be selected by proper connection of various jumpers (see Figure 50).

The LVDS mode evaluation boards include an LVDS-to-CMOS translator, making them compatible with the high speed ADC FIFO evaluation kit (HSC-ADC-EVALA-SC, www.analog.com/FIFO). The kit includes a high speed data capture board that provides a hardware solution for capturing up to 32 kB samples of high speed ADC output data in a FIFO memory chip (user upgradeable to 256 kB samples). Software is provided to enable the user to download the captured data to a PC via the USB port. This software also includes a behavioral model of the AD9460 and many other high speed ADCs.

Behavioral modeling of the AD9460 using ADIsimADC™ software is also available at www.analog.com/ADIsimADC. The ADIsimADC software supports virtual ADC evaluation using ADI proprietary behavioral modeling technology. This allows rapid comparison between the AD9460 and other high speed ADCs with or without hardware evaluation boards.

The user can choose to remove the translator and terminations to access the LVDS outputs directly.