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1.65 GHz Clock Fanout Buffer with Output Dividers and Delay Adjust

Data Sheet **AD9508**

FEATURES

- 1.65 GHz differential clock inputs/outputs
- 10-bit programmable dividers, 1 to 1024, all integers
- Up to 4 differential outputs or 8 CMOS outputs
- Pin strapping capability for hardwired programming at power-up
- <115 fs rms broadband random jitter (see Figure 25)
- Additive output jitter: 41 fs rms typical (12 kHz to 20 MHz)
- Excellent output-to-output isolation
- Automatic synchronization of all outputs
- Single 2.5 V/3.3 V power supply
- Internal LDO (low drop-out) voltage regulator for enhanced power supply immunity
- Phase offset select for output-to-output coarse delay adjust
- 3 programmable output logic levels, LVDS, HSTL, and CMOS
- Serial control port (SPI/I²C) or pin-programmable mode
- Space-saving 24-lead LFCSP

APPLICATIONS

- Low jitter, low phase noise clock distribution
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- High performance wireless transceivers
- High performance instrumentation
- Broadband infrastructure

FUNCTIONAL BLOCK DIAGRAM

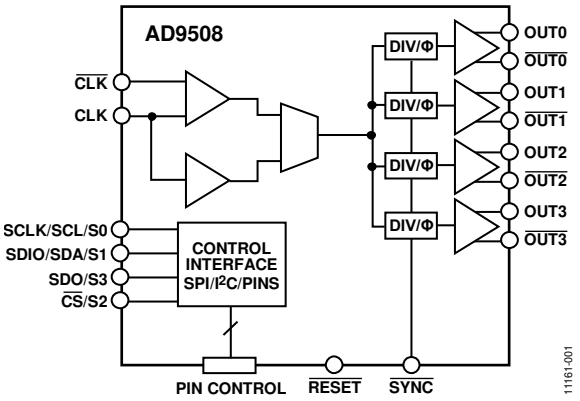

Figure 1.

GENERAL DESCRIPTION

The AD9508 provides clock fanout capability in a design that emphasizes low jitter to maximize system performance. This device benefits applications like clocking data converters with demanding phase noise and low jitter requirements.

There are four independent differential clock outputs, each with various types of logic levels available. Available logic types include LVDS (1.65 GHz), HSTL (1.65 GHz), and 1.8 V CMOS (250 MHz). In 1.8 V CMOS output mode, the differential output becomes two CMOS single-ended signals. The CMOS outputs are 1.8 V logic levels, regardless of the operating supply voltage.

Each output has a programmable divider that can be bypassed or be set to divide by any integer up to 1024. In addition, the AD9508 supports a coarse output phase adjustment between the outputs.

The device can also be pin programmed for various fixed configurations at power-up without the need for SPI or I²C programming.

The AD9508 is available in a 24-lead LFCSP and operates from a either a single 2.5 V or 3.3 V supply. The temperature range is −40°C to +85°C.

Rev. F

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9508 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9508-DSCC: Military Data Sheet
- AD9508-EP: Enhanced Product Data Sheet
- AD9508: 1.65 GHz Clock Fanout Buffer with Output Dividers and Delay Adjust Data Sheet

TOOLS AND SIMULATIONS

- AD9508 IBIS Model

REFERENCE MATERIALS

Press

- Multi-output, 1.65-GHz Clock Buffer and Divider Delivers Low Jitter to Optimize Noise Performance in Ultra-high-speed Data Converters

DESIGN RESOURCES

- AD9508 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Typical values are given for V_S = 3.3 V and 2.5 V and T_A = 25°C; minimum and maximum values are given over the full V_{DD} = 3.3 V + 5% down to 2.5 V − 5% and T_A = −40°C to +85°C variation; and input slew rate > 1 V/ns, unless otherwise noted.

POWER SUPPLY CURRENT AND TEMPERATURE CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE	2.375	2.5	3.465	V	Use supply voltage setting (2.5 V or 3.3 V) and appropriate current consumption configuration (see Current Consumption parameters in Table 1) to calculate total power dissipation
CURRENT CONSUMPTION					
LVDS Configuration		165	182	mA	Input clock: 1500 MHz in differential mode, all LVDS output drivers at 1500 MHz
		122	134	mA	Input clock: 800 MHz in differential mode, all LVDS output drivers at 200 MHz
HSTL Configuration		194	213	mA	Input clock: 1500 MHz in differential mode, all HSTL output drivers at 1500 MHz
		131	144	mA	Input clock: 491.52 MHz in differential mode, all output drivers at 491.52 MHz
		92	101	mA	Input clock: 122.88 MHz in differential mode, all output drivers at 122.88 MHz
CMOS Configuration		141	185	mA	Input clock: 1500 MHz in differential mode, all CMOS output drivers at 250 MHz, 10 pF load
		122	134	mA	Input clock: 800 MHz in differential mode, all CMOS outputs drivers at 200 MHz, 10 pF load
		85	94	mA	Input clock: 100 MHz in differential mode, all CMOS outputs drivers at 100 MHz, 10 pF load
Full Power-Down		6	10	mA	
TEMPERATURE					
Ambient Temperature Range, T_A	−40	+25	+85	°C	
Junction Temperature, T_J			115	°C	Junction temperatures above 115°C can degrade performance but no damage should occur, unless the absolute temperature is exceeded

CLOCK INPUTS AND OUTPUT DC SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUTS						
Differential Mode						
Input Frequency		0		1650	MHz	Differential input
Input Sensitivity		360		2200	mV p-p	As measured with a differential probe; jitter performance improves with higher slew rates (greater voltage swing)
Input Common-Mode Voltage	V_{ICM}	0.95	1.05	1.15	V	Input pins are internally self biased, which enables ac coupling
Input Voltage Offset			30		mV	
DC-Coupled Input Common-Mode Range	V_{CMR}	0.58		1.67	V	This is the allowable common-mode voltage range when dc-coupled
Pulse Width						
Low		303			ps	
High		303			ps	
Input Resistance (Single-Ended)		5.0	7	9	kΩ	
Input Capacitance	C_{IN}		2		pF	
Input Bias Current (Each Pin)		100		400	µA	Full input swing
CMOS CLOCK MODE (SINGLE-ENDED)						2.5 V or 3.3 V CMOS only; for 1.8 V CMOS, use (ac-coupled) differential input mode
Input Frequency				250	MHz	
Input Voltage						
High	V_{IH}	VDD/2 + 0.15			V	
Low	V_{IL}			VDD/2 − 0.15	V	
Input Current						
High	I_{INH}		1		µA	
Low	I_{INL}		−142		µA	
Input Capacitance	C_{IN}		2		pF	
LVDS CLOCK OUTPUTS						Termination = 100 Ω differential (OUTx, $\overline{OUTx}$)
Output Frequency				1650	MHz	
Output Voltage Differential	V_{OD}	247	375	454	mV	$V_{OH} - V_{OL}$ measurement across a differential pair at the default amplitude setting with output driver not toggling; see Figure 6 for variation over frequency
Delta V_{OD}	ΔV_{OD}			50	mV	This is the absolute value of the difference between V_{OD} when the normal output is high vs. when the complementary output is high
Offset Voltage	V_{OS}	1.125	1.18	1.375	V	$(V_{OH} + V_{OL})/2$ across a differential pair
Delta V_{OS}	ΔV_{OS}			50	mV	This is the absolute value of the difference between V_{OS} when the normal output is high vs. when the complementary output is high
Short-Circuit Current	I_SA, I_SB		13.6	24	mA	Each pin (output shorted to GND)
LVDS Duty Cycle		45		55	%	Up to 750 MHz input
		39		61	%	750 MHz to1500 MHz input
			50.1		%	1650 MHz input
HSTL CLOCK OUTPUTS						100 Ω across differential pair; default amplitude setting
Output Frequency				1650	MHz	
Differential Output Voltage	V_O	859	925	978	mV	$V_{OH} - V_{OL}$ with output driver static
Common-Mode Output Voltage	V_{OCM}	905	940	971	mV	$(V_{OH} + V_{OL})/2$ with output driver static
HSTL Duty Cycle		45		55	%	Up to 750 MHz input
		40		60	%	750 MHz to 1500 MHz input
			50.9		%	1650 MHz input

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CMOS CLOCK OUTPUTS						Single-ended; termination = open; OUTx and $\overline{\text{OUTx}}$ in phase
Output Frequency				250	MHz	With 10 pF load per output, see Figure 14 for swing vs. frequency
Output Voltage						
At 1 mA Load						
High	V_{OH}	1.7			V	
Low	V_{OL}			0.1	V	
At 10 mA load						
High	V_{OH}	1.2			V	
Low	V_{OL}			0.6	V	
At 10 mA Load (2 × CMOS Mode)						
High	V_{OH}	1.45			V	
Low	V_{OL}			0.35	V	
CMOS Duty Cycle		45		55	%	Up to 250 MHz

OUTPUT DRIVER TIMING CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUTS						Termination = 100 Ω differential, 1 × LVDS
Output Rise/Fall Time	t_R, t_F		152	177	ps	20% to 80% measured differentially
Propagation Delay, Clock-to-LVDS Output	t_{PD}	1.56	2.01	2.43	ns	
Temperature Coefficient			2.8		ps/°C	
Output Skew[1]						
All LVDS Outputs						
On the Same Part				48	ps	
Across Multiple Parts				781	ps	Assumes same temperature and supply; takes into account worst-case propagation delay delta due to worst-case process variation
HSTL OUTPUTS						Termination = 100 Ω differential, 1 × HSTL
Output Rise/Fall Time	t_R, t_F		118	143	ps	20% to 80% measured differentially
Propagation Delay, Clock-to-HSTL Output	t_{PD}	1.59	2.05	2.5	ns	
Temperature Coefficient			2.9		ps/°C	
Output Skew[1]						
All HSTL Outputs						
On the Same Part				59	ps	
Across Multiple Parts				825	ps	Assumes same temperature and supply; takes into account worst-case propagation delay delta due to worst-case process variation
CMOS OUTPUTS						
Output Rise/Fall Time	t_R, t_F		1.18	1.45	ns	20% to 80%; C_{LOAD} = 10 pF
Propagation Delay, Clock-to-CMOS Output	t_{PD}	2.04	2.56	3.07	ns	10 pF load
Temperature Coefficient			3.3		ps/°C	
Output Skew[1]						
All CMOS Outputs						
On the Same Part				112	ps	
Across Multiple Parts				965	ps	Assumes same temperature and supply; takes into account worst-case propagation delay delta due to worst-case process variation

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT LOGIC SKEW[1]						CMOS load = 10 pF and LVDS load = 100 Ω
LVDS Output(s) and HSTL Output(s)			77	119	ps	Outputs on the same device; assumes worst-case output combination
LVDS Output(s) and CMOS Output(s)			497	700	ps	Outputs on the same device; assumes worst-case output combination
HSTL Output(s) and CMOS Output(s)			424	622	ps	Outputs on the same device; assumes worst-case output combination

[1] Output skew is the difference between any two similar delay paths while operating at the same voltage and temperature.

LOGIC INPUTS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS $\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, IN_SEL						
Input Voltage						
High	V_{IH}	1.7			V	2.5 V supply voltage operation
		2.0			V	3.3 V supply voltage operation
Low	V_{IL}			0.7	V	2.5 V supply voltage operation
				0.8	V	3.3 V supply voltage operation
Input Current	I_{INH}, I_{INL}	−300		+100	µA	
Input Capacitance	C_{IN}		2		pF	

SERIAL PORT SPECIFICATIONS—SPI MODE

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{\text{CS}}$					SCLK has a 200 kΩ internal pull-down resistor
Input Voltage					
Logic 1	VDD − 0.4			V	
Logic 0			0.4	V	
Input Current					
Logic 1		−4		µA	
Logic 0		−85		µA	
Input Capacitance		2		µA	
SCLK					
Input Voltage					
Logic 1	VDD − 0.4			V	
Logic 0			0.4	V	
Input Current					
Logic 1		70		µA	
Logic 0		13		µA	
Input Capacitance		2		pF	
SDIO					
As Input					
Input Voltage					
Logic 1	VDD − 0.4			V	
Logic 0			0.4	V	
Input Current					
Logic 1		−1		µA	
Logic 0		−1		µA	
Input Capacitance		2		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
As Output					
Output Voltage					
Logic 1	VDD – 0.4			V	1 mA load current
Logic 0			0.4	V	1 mA load current
SDO					
Output Voltage					
Logic 1	VDD – 0.4			V	1 mA load current
Logic 0			0.4	V	1 mA load current
TIMING					
SCLK					
Clock Rate, $1/t_{CLK}$			30	MHz	
Pulse Width High, t_{HIGH}	4.6			ns	
Pulse Width Low, t_{LOW}	3.5			ns	
SDIO to SCLK Setup, t_{DS}	2.9			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			15	ns	
$\overline{CS}$ to SCLK Setup (t_S)	3.4			ns	
$\overline{CS}$ to SCLK Hold (t_C)	0			ns	
$\overline{CS}$ to Minimum Pulse Width High	3.4			ns	

SERIAL PORT SPECIFICATIONS—I²C MODE

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (AS INPUT)					
Input Voltage					
Logic 1	VDD – 0.4			V	
Logic 0			0.4	V	
Input Current	–40		0	µA	For V_{IN} = 10% to 90% DVDD3
Hysteresis of Schmitt Trigger Inputs	150			mV	
SDA (AS OUTPUT)					
Output Logic 0 Voltage			0.4	V	I_O = 3 mA
Output Fall Time from $V_{IH\ (MIN)}$ to $V_{IL\ (MAX)}$			250	ns	10 pF ≤ C_b ≤ 400 pF
TIMING					
SCL Clock Rate			400	kHz	
Bus-Free Time Between a Stop and Start Condition, t_{BUF}	1.3			µs	
Repeated Start Condition Setup Time, $t_{SU;\ STA}$			0.6	µs	
Repeated Hold Time Start Condition, $t_{HD;\ STA}$	0.6			µs	After this period, the first clock pulse is generated
Stop Condition Setup Time, $t_{SU;\ STO}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
Data Setup Time, $t_{SU;\ DAT}$	100			ns	
Data Hold Time, $t_{HD;\ DAT}$	0		0.9	µs	

EXTERNAL RESISTOR VALUES FOR PIN STRAPPING MODE

Table 7.

Parameter	Resistor Polarity	Min	Typ	Max	Unit	Test Conditions/Comments
EXTERNAL RESISTORS						Using 10% tolerance resistor
Voltage Level 0	Pull down to ground		820		Ω	
Voltage Level 1	Pull down to ground		1.8		kΩ	
Voltage Level 2	Pull down to ground		3.9		kΩ	
Voltage Level 3	Pull down to ground		8.2		kΩ	
Voltage Level 4	Pull up to VDD		820		Ω	
Voltage Level 5	Pull up to VDD		1.8		kΩ	
Voltage Level 6	Pull up to VDD		3.9		kΩ	
Voltage Level 7	Pull up to VDD		8.2		kΩ	

CLOCK OUTPUT ADDITIVE PHASE NOISE

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-HSTL OR LVDS ADDITIVE PHASE NOISE					
CLK = 1474.56 MHz, OUTx = 1474.56 MHz					Input slew rate > 1 V/ns
Divide Ratio = 1					
At 10 Hz Offset		−88		dBc/Hz	
At 100 Hz Offset		−100		dBc/Hz	
At 1 kHz Offset		−109		dBc/Hz	
At 10 kHz Offset		−116		dBc/Hz	
At 100 kHz Offset		−135		dBc/Hz	
At 1 MHz Offset		−144		dBc/Hz	
At 10 MHz Offset		−148		dBc/Hz	
At 100 MHz Offset		−149		dBc/Hz	
CLK-TO-HSTL OR LVDS or CMOS ADDITIVE PHASE NOISE					
CLK = 625 MHz, OUTx = 125 MHz					Input slew rate > 1 V/ns
Divide Ratio = 5					
At 10 Hz Offset		−114		dBc/Hz	
At 100 Hz Offset		−125		dBc/Hz	
At 1 kHz Offset		−133		dBc/Hz	
At 10 kHz Offset		−141		dBc/Hz	
At 100 kHz Offset		−159		dBc/Hz	
At 1 MHz Offset		−162		dBc/Hz	
At 10 MHz Offset		−163		dBc/Hz	
At 20 MHz Offset		−163		dBc/Hz	
CLK-TO-HSTL OR LVDS ADDITIVE PHASE NOISE					
CLK = 491.52 MHz, OUTx = 491.52 MHz					Input slew rate > 1 V/ns
Divide Ratio = 1					
At 10 Hz Offset		−100		dBc/Hz	
At 100 Hz Offset		−111		dBc/Hz	
At 1 kHz Offset		−120		dBc/Hz	
At 10 kHz Offset		−127		dBc/Hz	
At 100 kHz Offset		−146		dBc/Hz	
At 1 MHz Offset		−153		dBc/Hz	
At 10 MHz Offset		−153		dBc/Hz	
At 20 MHz Offset		−153		dBc/Hz	

CLOCK OUTPUT ADDITIVE TIME JITTER

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUT ADDITIVE TIME JITTER					
CLK = 622.08 MHz, Outputs = 622.08 MHz		41		fs rms	BW = 12 kHz to 20 MHz
		70		fs rms	BW = 20 kHz to 80 MHz
		69		fs rms	BW = 50 kHz to 80 MHz
CLK = 622.08 MHz, Outputs = 155.52 MHz		93		fs rms	BW = 12 kHz to 20 MHz
		144		fs rms	BW = 20 kHz to 80 MHz
		142		fs rms	BW = 50 kHz to 80 MHz
CLK = 125 MHz, Outputs = 125 MHz		105		fs rms	BW = 12 kHz to 20 MHz
		209		fs rms	BW = 20 kHz to 80 MHz
		206		fs rms	BW = 50 kHz to 80 MHz
CLK = 400 MHz, Outputs = 50 MHz		184		fs rms	BW = 12 kHz to 20 MHz
HSTL OUTPUT ADDITIVE TIME JITTER					
CLK = 622.08 MHz, Outputs = 622.08 MHz		41		fs rms	BW = 12 kHz to 20 MHz
		56		fs rms	BW = 100 Hz to 20 MHz
		72		fs rms	BW = 20 kHz to 80 MHz
		70		fs rms	BW = 50 kHz to 80 MHz
CLK = 622.08 MHz, Outputs = 155.52 MHz		76		fs rms	BW = 12 kHz to 20 MHz
		87		fs rms	BW = 100 Hz to 20 MHz
		158		fs rms	BW = 20 kHz to 80 MHz
		156		fs rms	BW = 50 kHz to 80 MHz
CMOS OUTPUT ADDITIVE TIME JITTER					
CLK = 100 MHz, Outputs = 100 MHz		91		fs rms	BW = 12 kHz to 20 MHz

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
Supply Voltage (VDD)	3.6 V
Maximum Digital Input Voltage	−0.5 V to VDD + 0.5 V
CLK and $\overline{\text{CLK}}$	−0.5 V to VDD + 0.5 V
Maximum Digital Output Voltage	−0.5 V to VDD + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

The following equation determines the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the customer at the top center of the package.
Ψ_{JT} is the value as indicated in Table 11.
P_D is the power dissipation.

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations.

THERMAL CHARACTERISTICS

Thermal characteristics established using JEDEC51-7 and JEDEC51-5 2S2P test boards.

Table 11. Thermal Characteristics, 24-Lead LFCSP

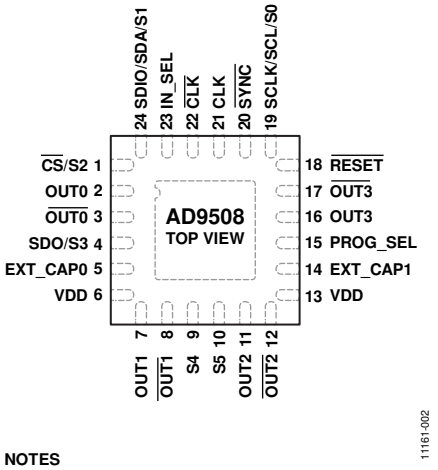
Symbol	Thermal Characteristic (JEDEC51-7 and JEDEC51-5 2S2P Test Boards[1])	Value[2]	Unit
θ_{JA}	Junction-to-ambient thermal resistance per JEDEC JESD51-2 (still air)	43.5	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air)	40	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 2.5 m/sec airflow per JEDEC JESD51-6 (moving air)	38.5	°C/W
θ_{JB}	Junction-to-board thermal resistance per JEDEC JESD51-8 (still air)	16.2	°C/W
θ_{JC}	Junction-to-case thermal resistance (die-to-heat sink) per MIL-STD-883, Method 1012.1	7.1	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter per JEDEC JESD51-2 (still air)	0.33	°C/W

[1] The exposed pad on the bottom of the package must be soldered to ground (VSS) to achieve the specified thermal performance.
[2] Results are from simulations. The PCB is a JEDEC multilayer type. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED DIE PAD MUST BE CONNECTED TO GROUND (VSS).

Figure 2. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{CS}$/S2	Chip Select/Pin Programming. Multipurpose pin. This pin is controlled by the PROG_SEL pin. Chip Select ($\overline{CS}$) is an active logic low CMOS input used in the SPI operation mode. When programming a device via SPI mode, $\overline{CS}$ must be held low. In systems where more than one AD9508 is present, this pin enables individual programming of each AD9508. In pin programming mode, this pin becomes S2. In this mode, S2 is hard wired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the output divider value for the outputs on Pin 11 and Pin 12. See the Pin Strapping to Program on Power-Up section for more details.
2	OUT0	LVDS/HSTL Differential Output or Single-Ended CMOS Output.
3	$\overline{OUT0}$	Complementary LVDS/HSTL Differential Output or Single-Ended CMOS Output.
4	SDO/S3	Serial Data Output/Pin Programming. Multipurpose pin. This pin is controlled by the PROG_SEL pin. SDO is configured as an output to read back the internal register settings in SPI mode operation. In pin programming mode, this pin becomes S3, which is hard wired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the output divider value for the outputs on Pin 16 and Pin 17. See the Pin Strapping to Program on Power-Up section for more details.
5	EXT_CAP0	Node for External Decoupling Capacitor for LDO. Tie this pin to a 0.47 µF capacitor to ground.
6	VDD	Power Supply (2.5 V or 3.3 V Operation).
7	OUT1	LVDS/HSTL Differential Output or Single-Ended CMOS Output.
8	$\overline{OUT1}$	Complementary LVDS/HSTL Differential Output or Single-Ended CMOS Output.
9	S4	Pin Programming. Use this pin in pin programming mode only. The PROG_SEL pin determines which programming mode is used. In pin programming mode, S4 is hardwired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the output logic levels used for the outputs on Pin 2, Pin 3, Pin 7, and Pin 8. See the Pin Strapping to Program on Power-Up section for more details.
10	S5	Pin Programming. Use this pin in pin programming mode only. The PROG_SEL pin determines which programming mode is used. In pin programming mode, S5 is hardwired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the output logic levels used for the outputs on Pin 11, Pin 12, Pin 16, and Pin 17. See the Pin Strapping to Program on Power-Up section for more details.
11	OUT2	LVDS/HSTL Differential Output or Single-Ended CMOS Output.
12	$\overline{OUT2}$	Complementary LVDS/HSTL Differential Output or Single-Ended CMOS Output.
13	VDD	Power Supply (2.5 V or 3.3 V Operation).
14	EXT_CAP1	Node for External Decoupling Capacitor for LDO. Tie this pin to a 0.47 µF capacitor to ground.
15	PROG_SEL	Three-State CMOS Input. Pin 15 selects the type of device programming interface to be used (SPI, I^2C, or pin programming).
16	OUT3	LVDS/HSTL Differential Output or Single-Ended CMOS Output.
17	$\overline{OUT3}$	Complementary LVDS/HSTL Differential Output or Single-Ended CMOS Output.

Pin No.	Mnemonic	Description
18	$\overline{\text{RESET}}$	CMOS Input. Device Reset. When this active low pin is asserted, the internal register settings enter their default state after the $\overline{\text{RESET}}$ is released. Note that $\overline{\text{RESET}}$ also serves as a power-down of the device while an active low signal is applied to the pin. The $\overline{\text{RESET}}$ pin has an internal 24 kΩ pull-up resistor.
19	SCLK/SCL/S0	Serial Programming Clock/Data Clock/Programming Pin. Multipurpose pin controlled by the PROG_SEL pin used for serial programming clock (SCLK) in SPI mode or data clock (SCL) for serial programming in I^2C Mode. The PROG_SEL pin determines which programming mode is used. In pin programming mode, this pin becomes S0. In this mode, S0 is hardwired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the output divider values for the outputs on Pin 2 and Pin 3. See the Pin Strapping to Program on Power-Up section for more details.
20	$\overline{\text{SYNC}}$	Clock Synchronization. When this pin is active low, the output drivers are held static and then synchronized on a low-to-high transition of this pin. The $\overline{\text{SYNC}}$ pin has an internal 24 kΩ pull-up resistor.
21	CLK	Differential Clock Input or Single-Ended CMOS Input. Whether this pin serves as the differential clock input or the single-ended CMOS input depends on the logic state of the IN_SEL pin.
22	$\overline{\text{CLK}}$	Complementary Differential Clock Input.
23	IN_SEL	CMOS Input. A logic high configures the CLK and $\overline{\text{CLK}}$ inputs for a differential input signal. A logic low configures the input for single-ended CMOS applied to the CLK pin. AC-couple the unused $\overline{\text{CLK}}$ to ground with a 0.1 µF capacitor.
24	SDIO/SDA/S1	Serial Data Input and Output (SPI)/Serial Data (I^2C)/Pin Programming. Pin 24 is a multipurpose input controlled by the PROG_SEL pin used for SPI (SDIO), I^2C (SDA), and pin strapping modes (S1). When the device is in 4-wire SPI mode, data is written via SDIO. In 3-wire mode, both data reads and writes occur on this pin. There is no internal pull-up/pull-down resistor on this pin. In I^2C mode, SDA serves as the serial data pin. The PROG_SEL pin determines which programming mode is used. In pin programming mode, this pin becomes S1. In this mode, S1 is hardwired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the output divider values for the outputs on Pin 7 and Pin 8. See the Pin Strapping to Program on Power-Up section for more details.
	EP	Exposed Pad. The exposed die pad must be connected to ground (VSS).

TYPICAL PERFORMANCE CHARACTERISTICS

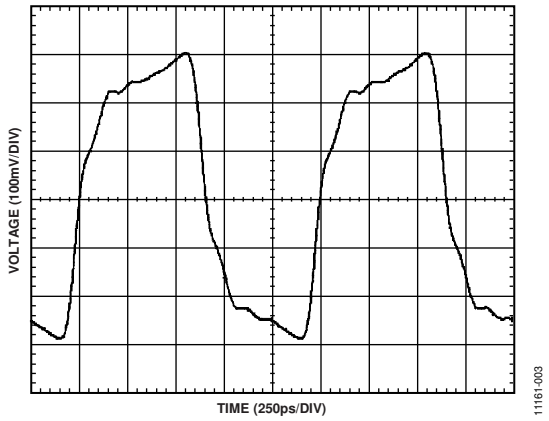


Figure 3. LVDS Differential Output Waveform at 800 MHz

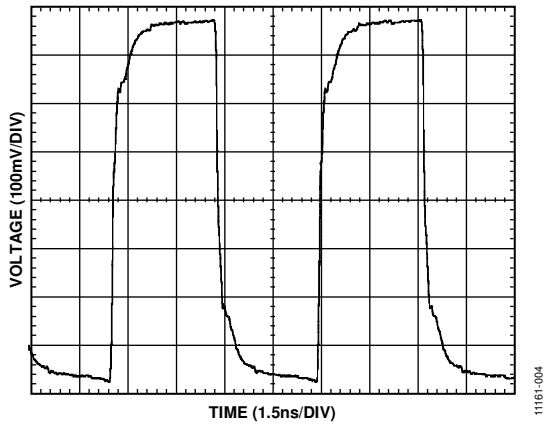


Figure 4. LVDS Differential Output Waveform at 156.25 MHz

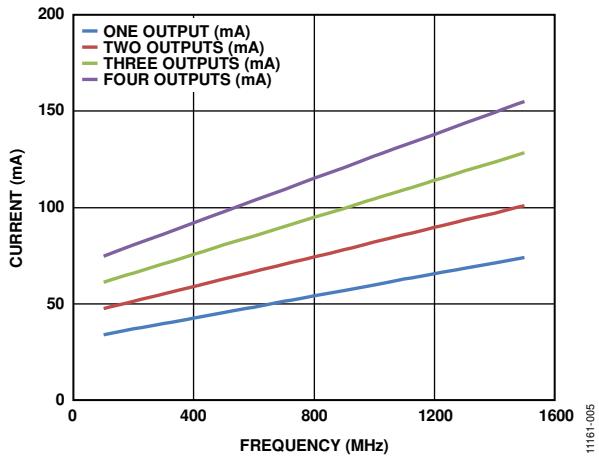


Figure 5. Power Supply Current vs. Input Frequency and Number of Outputs Used, LVDS

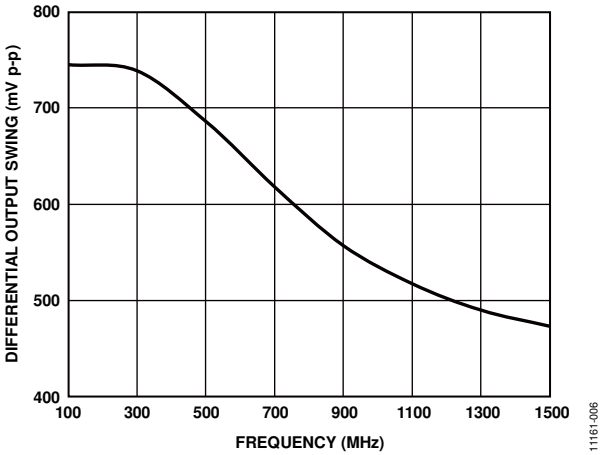


Figure 6. LVDS Differential Output Swing vs. Frequency

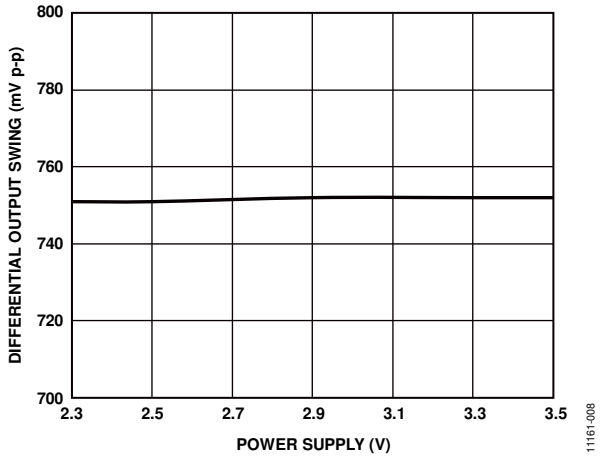


Figure 7. LVDS Differential Output Swing vs. Power Supply Voltage

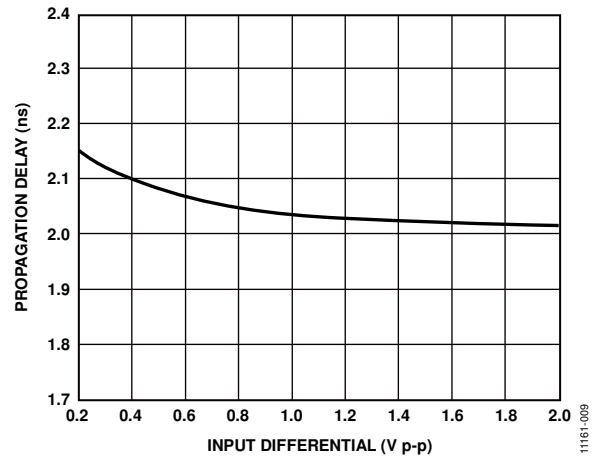


Figure 8. LVDS Propagation Delay vs. Input Differential Voltage

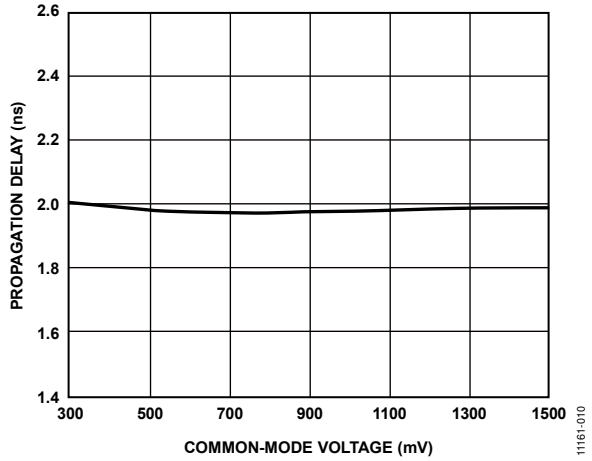


Figure 9. LVDS Propagation Delay vs. Input Common-Mode Voltage

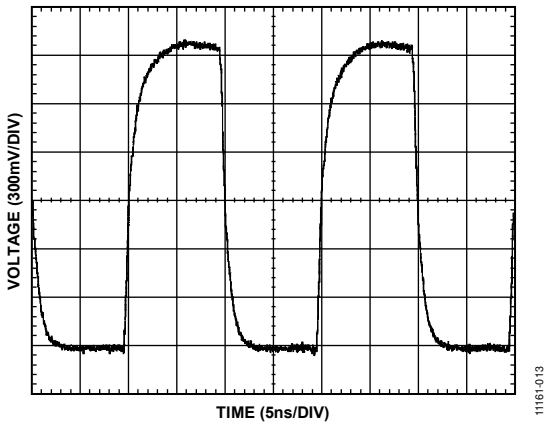


Figure 12. CMOS Output Waveform at 50 MHz with 10 pF Load

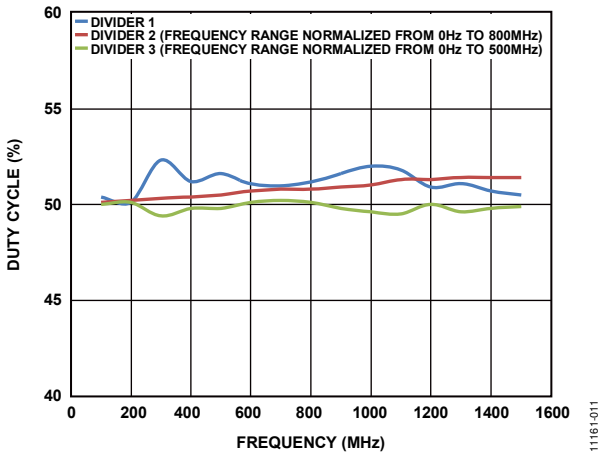


Figure 10. LVDS Output Duty Cycle vs. Output Frequency

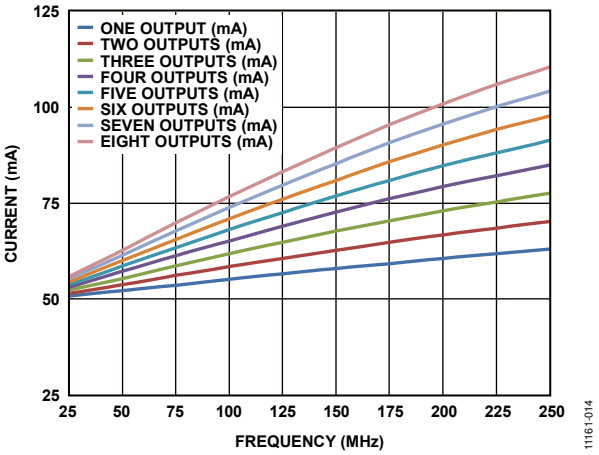


Figure 13. Power Supply Current vs. Input Frequency vs. Number of Outputs Used, CMOS

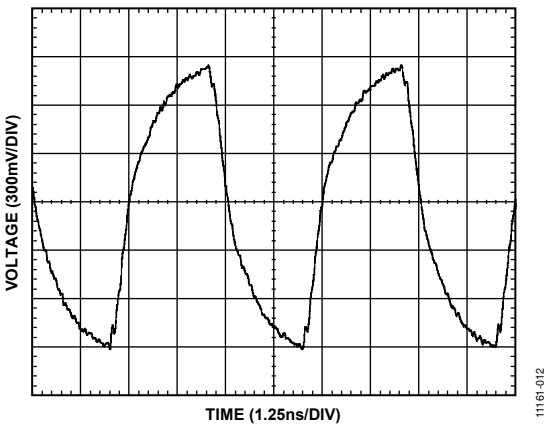


Figure 11. CMOS Output Waveform at 200 MHz with 10 pF Load

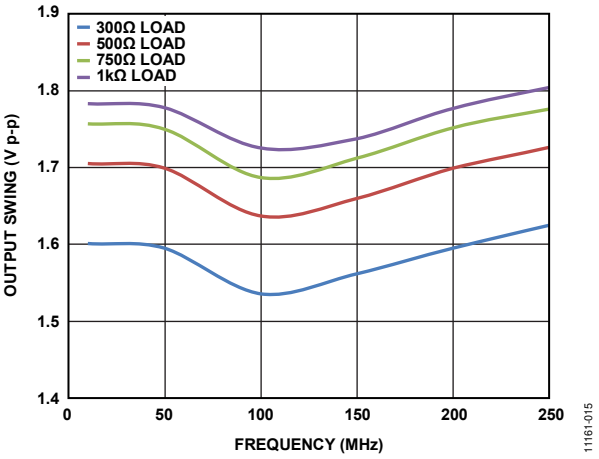


Figure 14. CMOS Output Swing vs. Frequency and Resistive Load

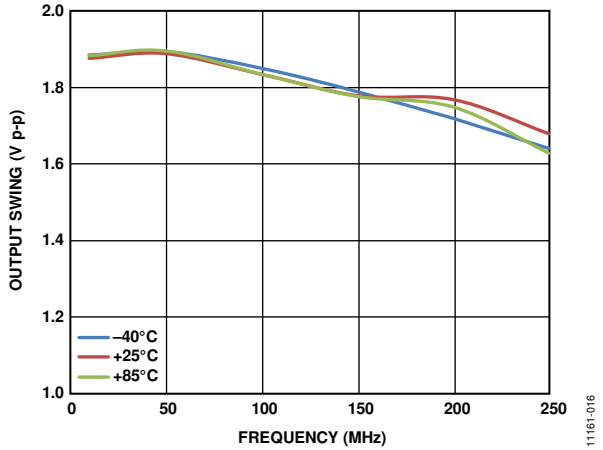


Figure 15. CMOS Output Swing vs. Frequency and Temperature (10 pF Load)

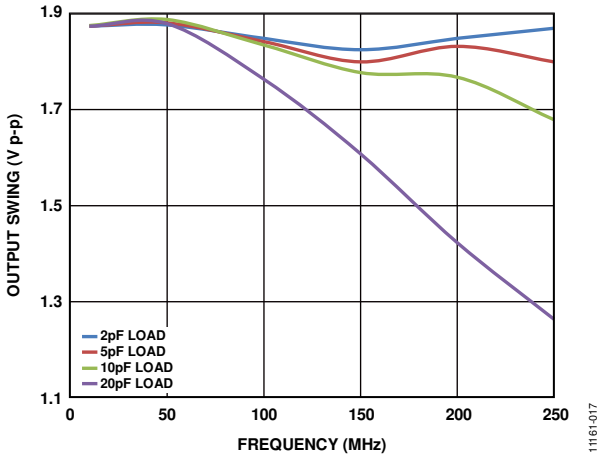


Figure 16. CMOS Output Swing vs. Frequency and Capacitive Load (2 pF, 5 pF, 10 pF, 20 pF)

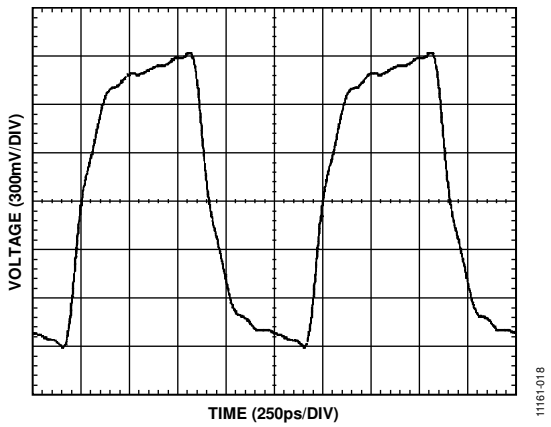


Figure 17. HSTL Differential Output Waveform at 800 MHz

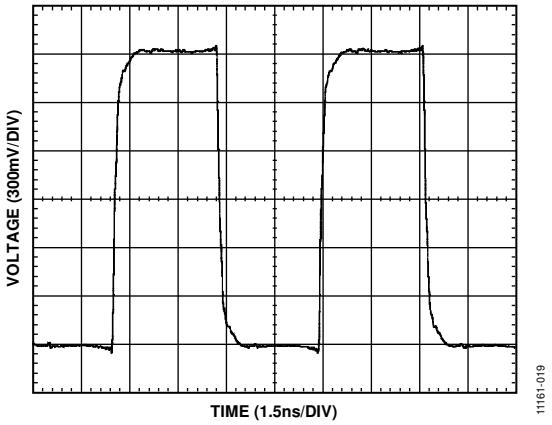


Figure 18. HSTL Differential Output Waveform at 156.25 MHz

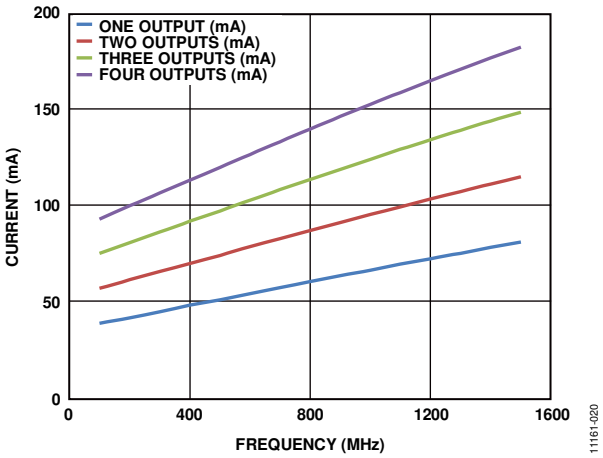


Figure 19. Power Supply Current vs. Input Frequency and Number of Outputs Used, HSTL

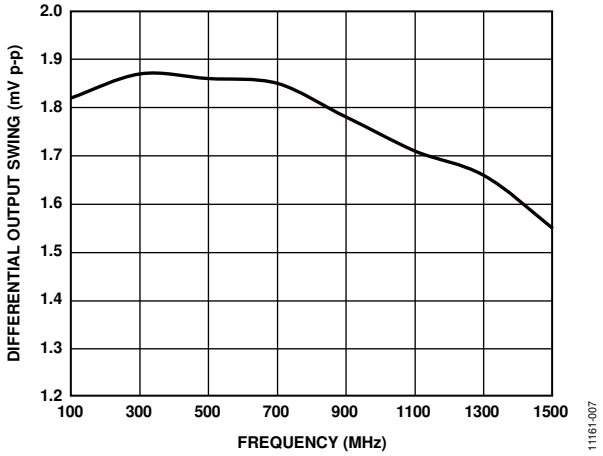


Figure 20. HSTL Differential Output Swing vs. Frequency

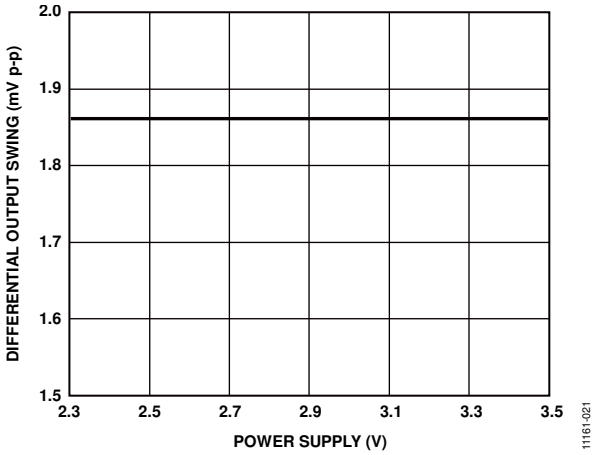


Figure 21. HSTL Differential Output Swing vs. Power Supply Voltage

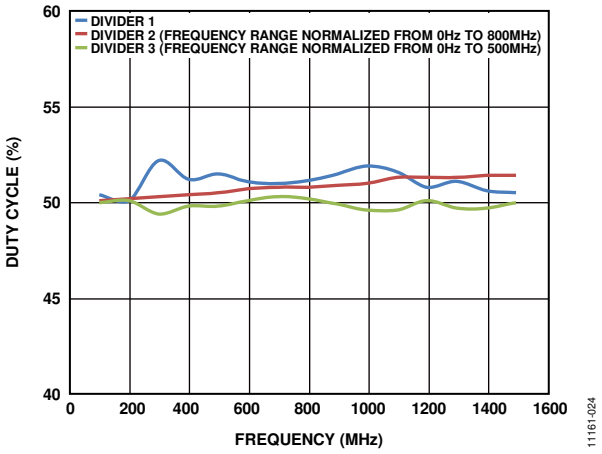


Figure 24. HSTL Output Duty Cycle vs. Output Frequency

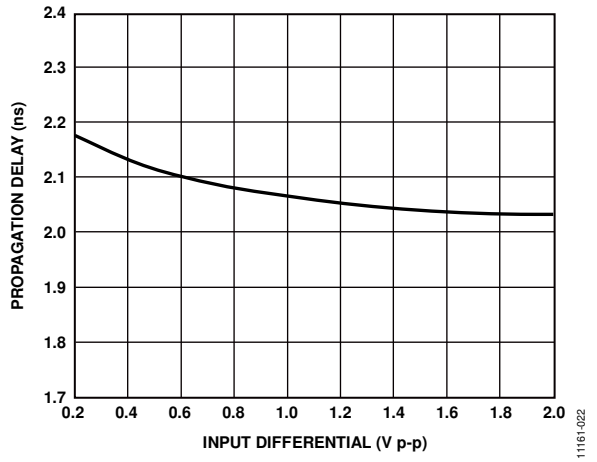


Figure 22. HSTL Propagation Delay vs. Input Differential Voltage

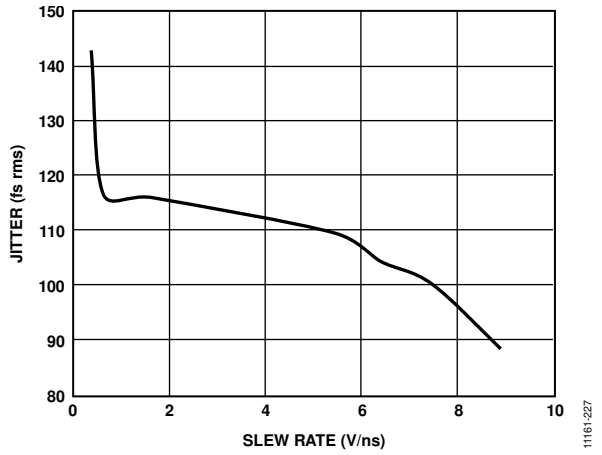


Figure 25. Additive Broadband Jitter vs. Input Slew Rate, LVDS, HSTL (Calculated from SNR of ADC Method)

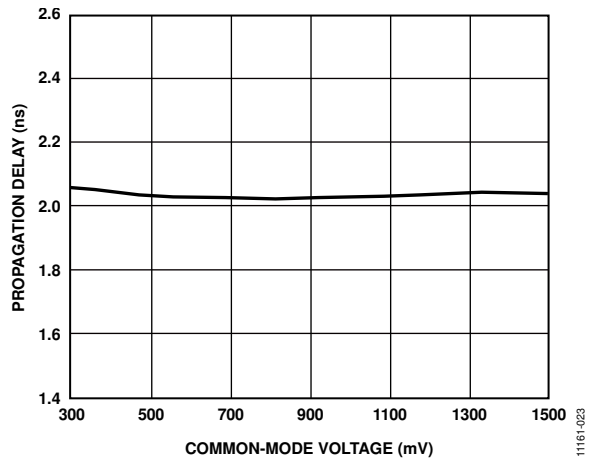


Figure 23. HSTL Propagation Delay vs. Input Common-Mode Voltage

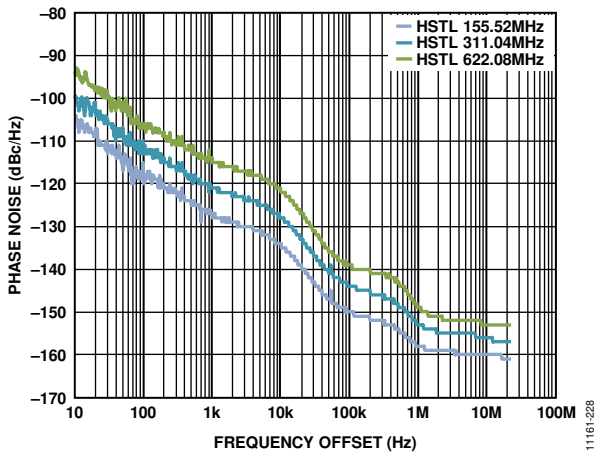


Figure 26. Absolute Phase Noise in HSTL Mode with Clock Input at 622.08 MHz and Outputs = 622.08 MHz, 311.04 MHz, 155.52 MHz

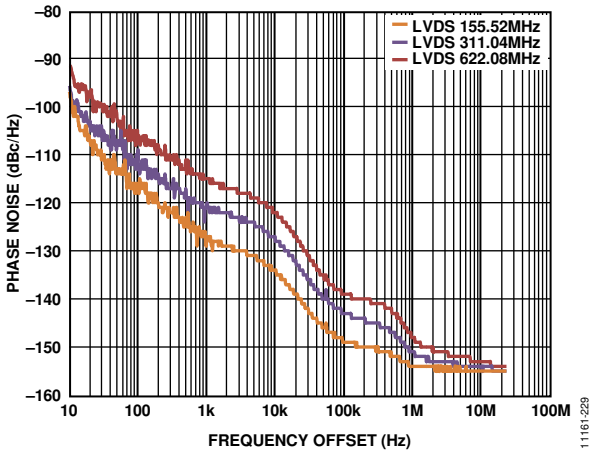


Figure 27. Absolute Phase Noise in LVDS Mode with Clock Input at 622.08 MHz and Outputs = 622.08 MHz, 311.04 MHz, 155.52 MHz

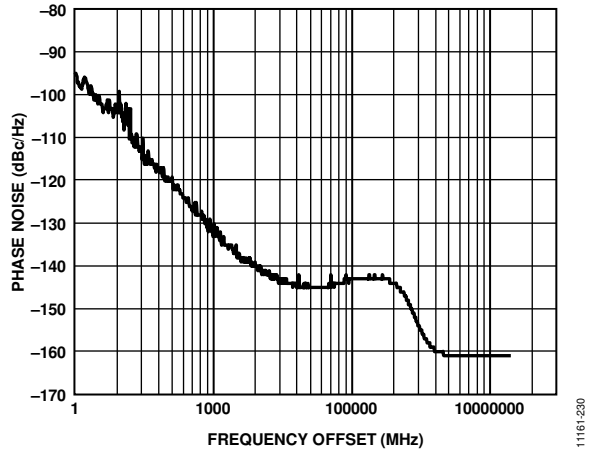


Figure 28. Absolute Phase Noise of Clock Source at 622.08 MHz

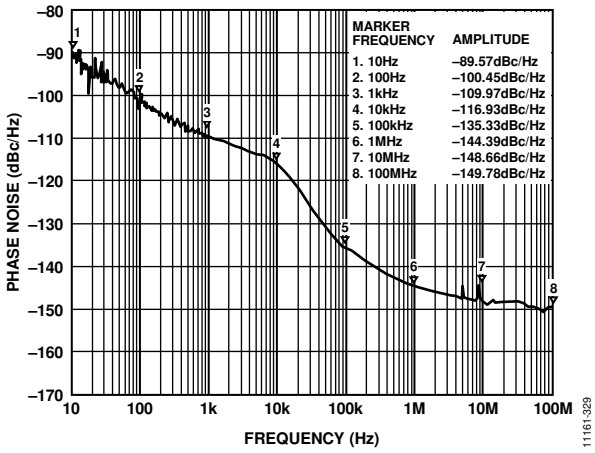


Figure 29. Additive Phase Noise with Clock Input = 1474.56 MHz with HSTL Outputs = 1474.76 MHz

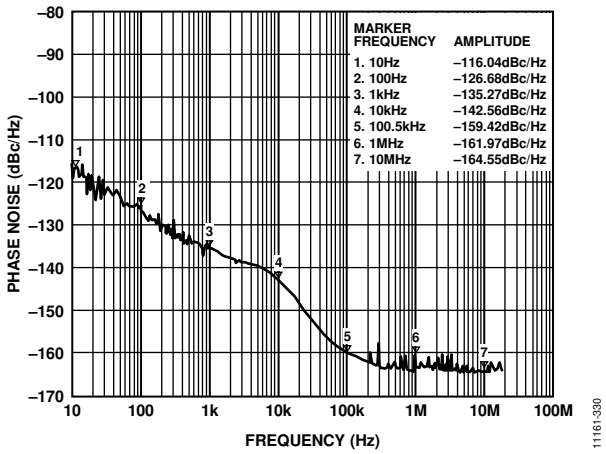


Figure 30. Additive Phase Noise with Clock Input = 1500 MHz with HSTL Outputs = 100 MHz

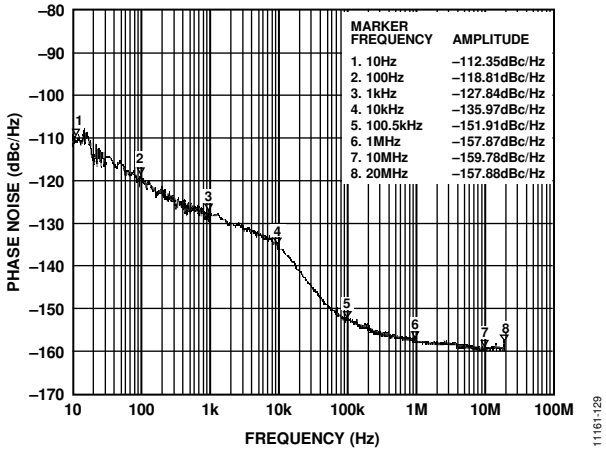


Figure 31. Additive Phase Noise with Clock Input = 622.08 MHz with HSTL Outputs = 155.52 MHz

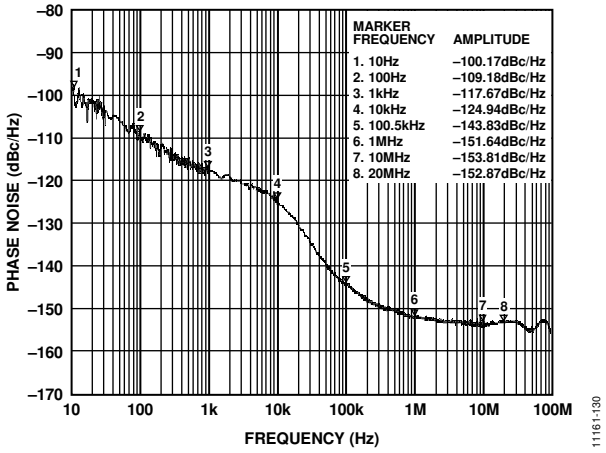


Figure 32. Additive Phase Noise with Clock Input = 622.08 MHz with LVDS Outputs = 622.08 MHz

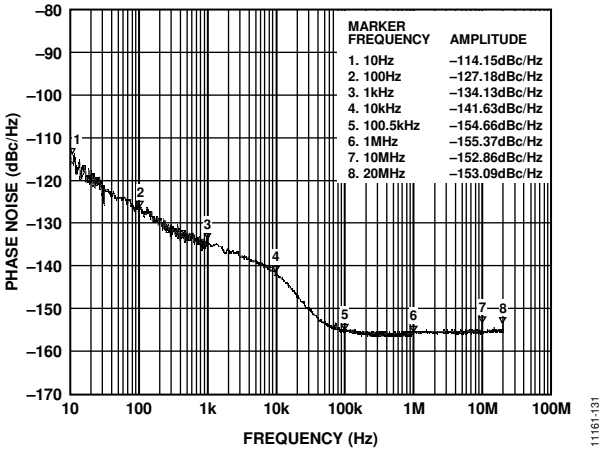


Figure 33. Additive Phase Noise with Clock Input = 100 MHz with CMOS Outputs = 100 MHz

TEST CIRCUITS

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

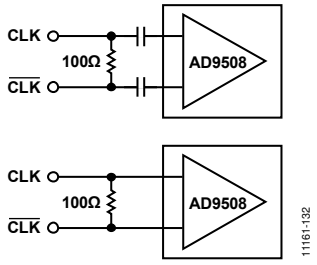


Figure 34. Typical AC-Coupled or DC-Coupled LVDS or HSTL Configurations

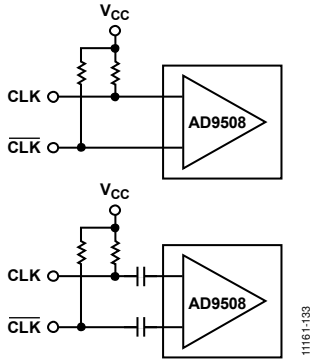


Figure 35. Typical AC-Coupled or DC-Coupled CML Configurations

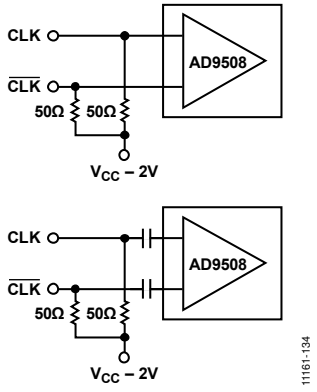


Figure 36. Typical AC-Coupled or DC-Coupled LVPECL Configurations

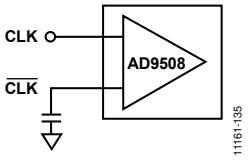


Figure 37. Typical 2.5 V or 3.3 V CMOS Configurations for Short Trace Lengths

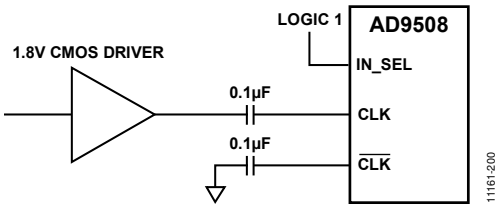


Figure 38. 1.8 V CMOS Logic Configuration for Input Clock Using Differential Mode

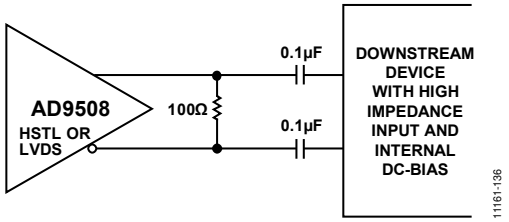


Figure 39. AC-Coupled LVDS or HSTL Output Driver (100 Ω Resistor Can Go on Either Side of Decoupling Capacitors Placed As Close As Possible To The Destination Receiver)

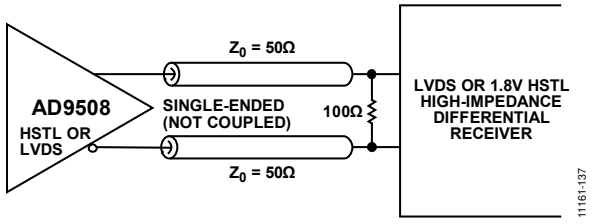


Figure 40. DC-Coupled LVDS or HSTL Output Driver

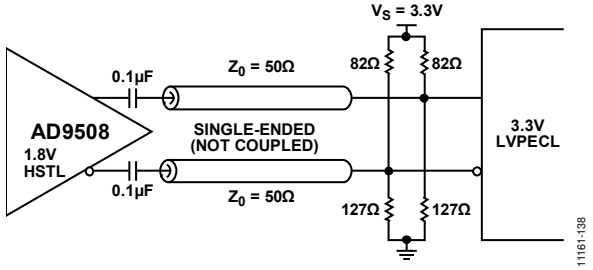


Figure 41. Interfacing the HSTL Driver to a 3.3 V LVPECL Input (This Method Incorporates Impedance Matching and DC Biasing for Bipolar LVPECL Receivers. If the Receiver Is Self-Biased, the Termination Scheme Shown in Figure 39 Is Recommended.)

TERMINOLOGY

Phase Jitter and Phase Noise
An ideal sine wave can be thought of as having a continuous and an even progression phase with time from 0 degrees to 360 degrees for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, characterized statistically as being Gaussian (normal) in distribution.

Phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in dB) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise contained within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter
Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as with time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) or one sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the SNR and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise
Additive phase noise is the amount of phase noise that is attributable only to the device or subsystem being measured. The residual phase noise system makes use of two devices operating in perfect quadrature. The correlated noise of any external components common to both devices (such as clock sources) is not present. This makes it possible to predict the degree to which the device is going to affect the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contribute their own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise.

Additive Time Jitter
Additive time jitter refers to the amount of time jitter that is attributable to the device or subsystem being measured. It is calculated by integrating the additive phase noise over a specific range. This makes it possible to predict the degree to which the device is going to impact the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contribute their own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

DETAILED BLOCK DIAGRAM

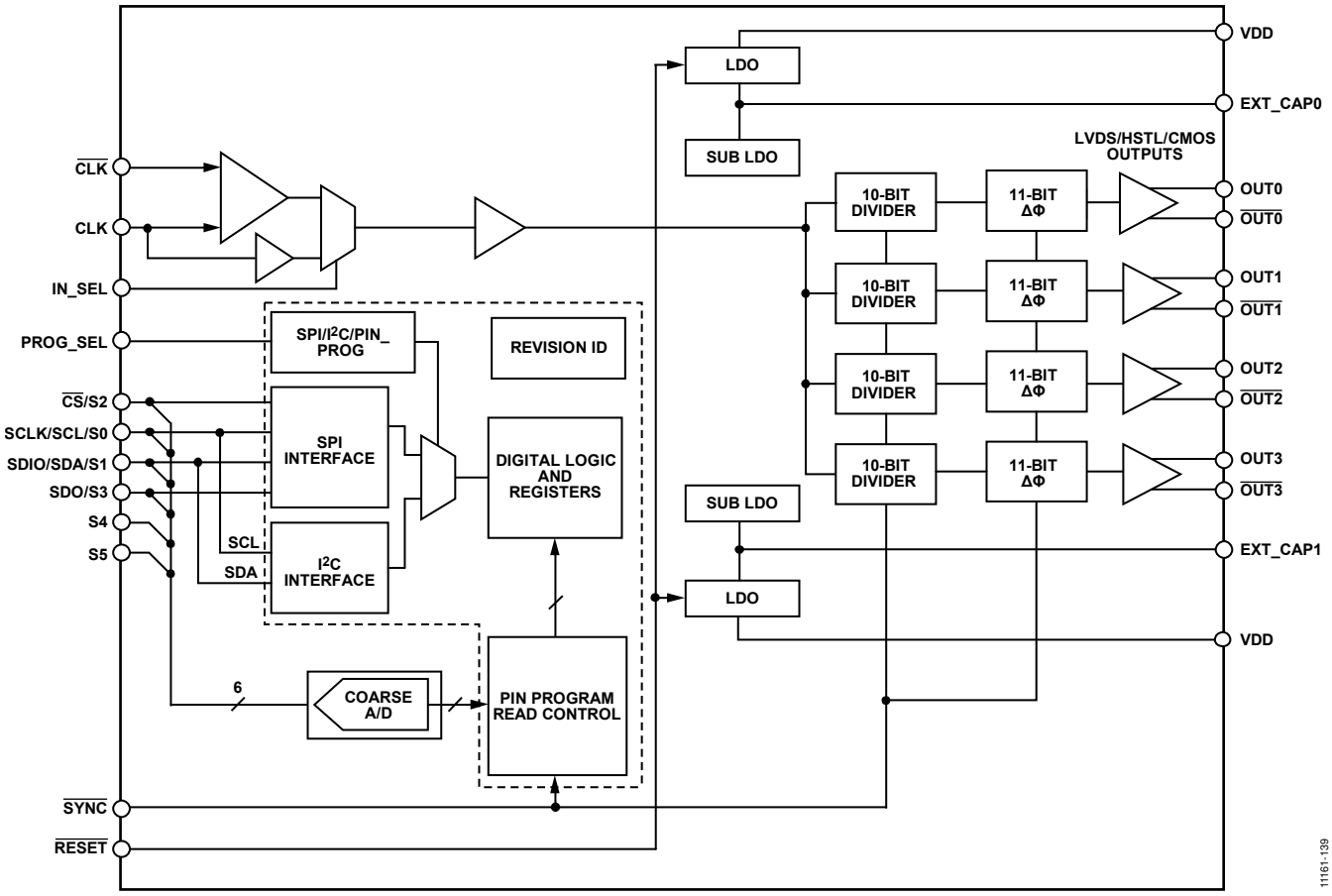


Figure 42. Detailed Block Diagram

The AD9508 accepts either a differential input clock applied to the CLK and $\overline{\text{CLK}}$ pins or a single-ended 1.8 V (if ac-coupled) 2.5 V or 3.3 V CMOS clock applied to the CLK pin. The input clock signal is sent to the clock distribution section, which has programmable dividers and phase offset adjustment. The clock distribution section operates at speeds of up to 1650 MHz.

The divider range under SPI or I²C control ranges from 1 to divide-by-1024 and the phase offset adjustment is equipped with 11 bits of resolution. However, in pin programming mode, the divider range is limited to a maximum divide-by-16 and there is no phase offset adjustment available.

The outputs can be configured to as many as four LVDS/HSTL differential outputs or as many as eight 1.8 V CMOS single-ended outputs. In addition, the output current for the different outputs is adjustable for output drive strength.

The device can be powered with either a 3.3 V or 2.5 V external supply; however, the internal supply on the chip runs off an internal 1.8 V LDO, delivering high performance with minimal power consumption.

PROGRAMMING MODE SELECTION

The AD9508 supports both SPI and I²C protocols, and a pin strapping option to program the device. The active interface depends on the logic state of the PROG_SEL pin. See Table 13 for programming mode selections. See the Serial Control Port and Pin Strapping to Program on Power-Up sections for more detailed information.

Table 13. SPI/I²C/Pin Serial Port Setup

PROG_SEL	SPI/I²C/Pin
Float	SPI
Logic 0	I²C
Logic 1	Pin programming control

CLOCK INPUT

The IN_SEL pin controls the desired input clock configuration. When the IN_SEL pin is set for single-ended operation, the device expects 1.8 V (if ac-coupled), 2.5 V, or 3.3 V CMOS-compatible logic levels on the CLK input pin. Bypass the unused $\overline{\text{CLK}}$ pin to ground with a 0.1 µF capacitor.

Note that if 2.5 V CMOS logic is used for single-ended input clock mode, the 2.5 V power supply option is recommended instead of 3.3 V operation to avoid possible duty cycle distortion. Duty cycle distortion can occur when the switching threshold level (VDD/2 or 1.65 V for 3.3 V operation) is increased and slow rise and falls times exist at the clock input.

1.8 V CMOS logic levels are not recommended in a single-ended CMOS configuration due to V_{IH} being too close to the input threshold voltage. However, the differential input clock mode can be used for a 1.8 V CMOS input, and Figure 38 shows the recommended configuration for a 1.8 V CMOS input clock.

When the IN_SEL pin is set for differential input clock mode, the inputs of the AD9508 are internally self biased. The internal inputs have a resistor divider, which sets the common-mode level. The complementary input is biased about 30 mV lower than the true input to avoid oscillations in the event that the input signal ceases. See Figure 43 for the equivalent differential input circuit.

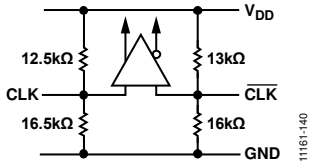


Figure 43. AD9508 Differential Input Stage

The inputs can be ac-coupled or dc-coupled in differential mode. See Table 14 for input logic compatibility. The user can supply a single-ended input with the input in differential mode by ac or dc coupling to one side of the differential input and bypassing the other input to ground by a capacitor.

Note that jitter performance degrades with low input slew rate, as shown in Figure 25. See Figure 34 through Figure 37 for different input clock termination schemes.

Table 14. CLK and $\overline{\text{CLK}}$ Differential Input Logic Compatibility

Input Logic Type	Input Common Mode (V)	Input Voltage Swing (per leg) (V)	AC-Coupled	DC-Coupled
3.3 V CML	2.9	0.8	Yes	Not allowed
2.5 V CML	2.1	0.8	Yes	Not allowed
1.8 V CML	1.4	0.8	Yes	Yes
3.3 V CMOS[1]	1.65	3.3	Not allowed	Yes
2.5 V CMOS[1, 2]	1.25	2.5	Not allowed	Yes
1.8 V CMOS[3]	0.9	1.8	Yes	Not recommended
1.5 V HSTL	0.75	0.75	Yes	Yes
LVDS	1.25	0.4	Yes	Yes
3.3 V LVPECL	2.0	0.8	Yes	Not allowed
2.5 V LVPECL	1.2	0.8	Yes	Yes

[1] IN_SEL is set for single-ended CMOS mode.
[2] VDD = 2.5 V operation recommended vs. VDD = 3.3 V operation.
[3] Refer to Figure 38 for configuration.

CLOCK OUTPUTS

Each output driver can be configured for either a differential LVDS/HSTL output or two single-ended CMOS outputs. When the LVDS/HSTL driver is enabled, the corresponding CMOS driver is in tristate. When the CMOS driver is enabled, the corresponding LVDS/HSTL driver is powered down and tristated. See Figure 44 and Figure 45 for the equivalent output stages.

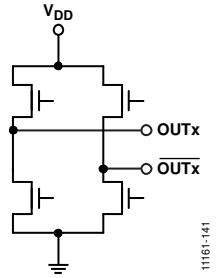


Figure 44. LVDS/HSTL Output Simplified Equivalent Circuit

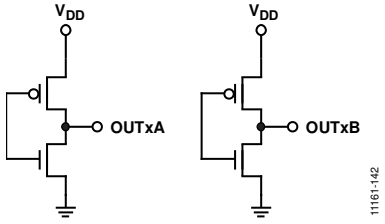


Figure 45. CMOS Equivalent Output Circuit

In LVDS or HSTL modes, there are register settings to control the output logic type and current drive strength. The LVDS output current can be set to the nominal 3.5 mA, additional settings include 0.5, 0.75, 1.0 (default), and 1.25 multiplied by 3.5 mA. The HSTL output current can be set to 8 mA (nominal) or 16 mA (boost mode). For pin programming mode, see the Pin Strapping to Program on Power-Up section for details and limitations of the device. Under pin programming mode, the nominal current is the default setting and is nonadjustable.

When routing single-ended CMOS signals, avoid driving multiple input receivers with one output. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver. The value of the series resistor is dependent on the board design and timing requirements (typically 10 Ω to 100 Ω). CMOS outputs are also limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 3 inches are recommended to preserve signal rise/fall times and signal integrity.

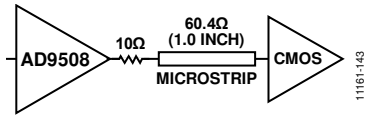


Figure 46. Series Termination of CMOS Output

CLOCK DIVIDERS

The four independent output dividers are 10-bit integer dividers with a divide range of 1 to 1024 in SPI and I²C modes. The output divider block contains duty cycle correction that guarantees 50% duty cycle for both even and odd divide ratios. In pin programming mode, divide values of 1 to 8 and 16 are supported.

PHASE DELAY CONTROL

The AD9508 provides a coarse output phase delay adjustment between outputs but with a wide delay range that is beneficial for some applications. The minimum delay step is equivalent to half the period of the input clock rate. This minimum delay step can be multiplied from 1 to 2047 times the minimum delay step to cover a wide delay range. The multiplication of the minimum delay step is provided for each output via the appropriate internal programming register. Phase delay is not supported in pin programming mode.

Note that the phase delay adjustment requires the use of the $\overline{\text{SYNC}}$ function pin. Phase adjustment and output synchronization occurs on the rising edge of the $\overline{\text{SYNC}}$ pin. Therefore, the $\overline{\text{SYNC}}$ pin must be pulled low and released to produce the desired phase relationship between outputs. If the $\overline{\text{SYNC}}$ is not active low prior to a phase delay change, the desired output phase delay between outputs is not guaranteed to occur; instead, a random phase delay can occur between outputs. However, a future $\overline{\text{SYNC}}$ pulse corrects to the desired phase relationship, if initiated. During the active low $\overline{\text{SYNC}}$ period, the outputs are forced to a static state.

Figure 47 shows three independent outputs, each set for DIV = 4 of the input clock rate. By incrementing the phase offset value in the programming registers from 0 to 2, each output is offset from the initial edge by a multiple of ½ t_{CLK}. Note that the $\overline{\text{SYNC}}$ signal is not shown in this timing diagram.

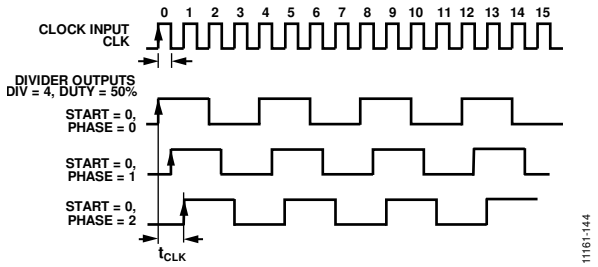


Figure 47. Phase Offset—All Dividers Set for DIV = 4, Phase Set from 0 to 2