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1.2 GHz Clock Distribution IC, PLL Core, Dividers, Delay Adjust, Five Outputs

AD9511

FEATURES

- Low phase noise phase-locked loop core
  - Reference input frequencies to 250 MHz
  - Programmable dual-modulus prescaler
  - Programmable charge pump (CP) current
  - Separate CP supply (VCP_S) extends tuning range
- Two 1.6 GHz, differential clock inputs
- 5 programmable dividers, 1 to 32, all integers
- Phase select for output-to-output coarse delay adjust
- 3 independent 1.2 GHz LVPECL outputs
  - Additive output jitter 225 fs rms
- 2 independent 800 MHz/250 MHz LVDS/CMOS clock outputs
  - Additive output jitter 275 fs rms
  - Fine delay adjust on 1 LVDS/CMOS output
- Serial control port
- Space-saving 48-lead LFCSP

APPLICATIONS

- Low jitter, low phase noise clock distribution
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- High performance wireless transceivers
- High performance instrumentation
- Broadband infrastructure

GENERAL DESCRIPTION

The AD9511 provides a multi-output clock distribution function along with an on-chip PLL core. The design emphasizes low jitter and phase noise to maximize data converter performance. Other applications with demanding phase noise and jitter requirements also benefit from this part.

The PLL section consists of a programmable reference divider (R); a low noise phase frequency detector (PFD); a precision charge pump (CP); and a programmable feedback divider (N). By connecting an external VCXO or VCO to the CLK2/CLK2B pins, frequencies up to 1.6 GHz may be synchronized to the input reference.

There are five independent clock outputs. Three outputs are LVPECL (1.2 GHz), and two are selectable as either LVDS (800 MHz) or CMOS (250 MHz) levels.

FUNCTIONAL BLOCK DIAGRAM

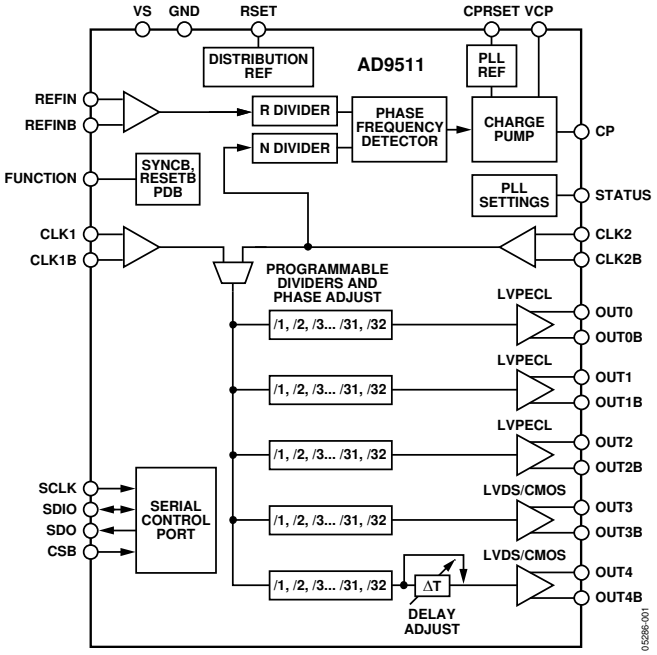

Figure 1.

Each output has a programmable divider that may be bypassed or set to divide by any integer up to 32. The phase of one clock output relative to another clock output may be varied by means of a divider phase select function that serves as a coarse timing adjustment. One of the LVDS/CMOS outputs features a programmable delay element with full-scale ranges up to 10 ns of delay. This fine tuning delay block has 5-bit resolution, giving 32 possible delays from which to choose for each full-scale setting.

The AD9511 is ideally suited for data converter clocking applications where maximum converter performance is achieved by encode signals with subpicosecond jitter.

The AD9511 is available in a 48-lead LFCSP and can be operated from a single 3.3 V supply. An external VCO, which requires an extended voltage range, can be accommodated by connecting the charge pump supply (VCP) to 5.5 V. The temperature range is −40°C to +85°C.

Rev. A

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AD9511* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9511 Evaluation Board

DOCUMENTATION

Application Notes

- AN-0974: Multicarrier TD-SCMA Feasibility
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal

Data Sheet

- AD9511: 1.2 GHz Clock Distribution IC, PLL Core, Dividers, Delay Adjust, Five Outputs Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD9511 Evaluation Tools

TOOLS AND SIMULATIONS

- ADIsimCLK Design and Evaluation Software
- AD9511 IBIS Models

REFERENCE MATERIALS

Press

- Analog Devices' Dual 14-bit A/D Converter Reduces Power and Size in Communications, Instrumentation, Test and Measurement Applications

Product Selection Guide

- RF Source Booklet

Technical Articles

- ADI Buys Korean Mobile TV Chip Maker
- Design A Clock-Distribution Strategy With Confidence
- Improved DDS Devices Enable Advanced Comm Systems
- Low-power direct digital synthesizer cores enable high level of integration
- Speedy A/Ds Demand Stable Clocks
- Understand the Effects of Clock Jitter and Phase Noise on Sampled Systems

DESIGN RESOURCES

- AD9511 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9511 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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4/05—Revision 0: Initial Version

SPECIFICATIONS

Typical (typ) is given for V_S = 3.3 V ± 5%; $V_S \le VCP_S \le 5.5$ V, T_A = 25°C, R_{SET} = 4.12 kΩ, CPR_{SET} = 5.1 kΩ, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

PLL CHARACTERISTICS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUTS (REFIN)					
Input Frequency	0		250	MHz	
Input Sensitivity		150		mV p-p	
Self-Bias Voltage, REFIN	1.45	1.60	1.75	V	Self-bias voltage of REFIN[1].
Self-Bias Voltage, REFINB	1.40	1.50	1.60	V	Self-bias voltage of REFINB[1].
Input Resistance, REFIN	4.0	4.9	5.8	kΩ	Self-biased[1].
Input Resistance, REFINB	4.5	5.4	6.3	kΩ	Self-biased[1].
Input Capacitance		2		pF	
PHASE/FREQUENCY DETECTOR (PFD)					
PFD Input Frequency			100	MHz	Antibacklash pulse width 0Dh<1:0> = 00b.
PFD Input Frequency			100	MHz	Antibacklash pulse width 0Dh<1:0> = 01b.
PFD Input Frequency			45	MHz	Antibacklash pulse width 0Dh<1:0> = 10b.
Antibacklash Pulse Width		1.3		ns	0Dh<1:0> = 00b. (This is the default setting.)
Antibacklash Pulse Width		2.9		ns	0Dh<1:0> = 01b.
Antibacklash Pulse Width		6.0		ns	0Dh<1:0> = 10b.
CHARGE PUMP (CP)					
I_{CP} Sink/Source					Programmable.
High Value		4.8		mA	With CPR_{SET} = 5.1 kΩ.
Low Value		0.60		mA	
Absolute Accuracy		2.5		%	$V_{CP} = VCP_S/2$.
CPR_{SET} Range		2.7/10		kΩ	
I_{CP} Three-State Leakage		1		nA	
Sink-and-Source Current Matching		2		%	$0.5 < V_{CP} < VCP_S - 0.5$ V.
I_{CP} vs. V_{CP}		1.5		%	$0.5 < V_{CP} < VCP_S - 0.5$ V.
I_{CP} vs. Temperature		2		%	$V_{CP} = VCP_S/2$ V.
RF CHARACTERISTICS (CLK2)[2]					
Input Frequency			1.6	GHz	Frequencies > 1200 MHz (LVPECL) or 800 MHz (LVDS) require a minimum divide-by-2 (see the Distribution Section).
Input Sensitivity		150		mV p-p	
Input Common-Mode Voltage, V_{CM}	1.5	1.6	1.7	V	Self-biased; enables ac coupling.
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied.
Input Sensitivity, Single-Ended		150		mV p-p	CLK2 ac-coupled; CLK2B capacitively bypassed to RF ground.
Input Resistance	4.0	4.8	5.6	kΩ	Self-biased.
Input Capacitance		2		pF	
CLK2 VS. REFIN DELAY		500		ps	Difference at PFD.
PRESCALER (PART OF N DIVIDER)					See the VCO/VCXO Feedback Divider—N (P, A, B) section.
Prescaler Input Frequency					
P = 2 DM (2/3)			600	MHz	
P = 4 DM (4/5)			1000	MHz	
P = 8 DM (8/9)			1600	MHz	
P = 16 DM (16/17)			1600	MHz	
P = 32 DM (32/33)			1600	MHz	
CLK2 Input Frequency for PLL			300	MHz	A, B counter input frequency.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS					
In-Band Noise of the Charge Pump/ Phase Frequency Detector (In-Band Means Within the LBW of the PLL)					The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where *N* is the N divider value).
@ 50 kHz PFD Frequency		−172		dBc/Hz	
@ 2 MHz PFD Frequency		−156		dBc/Hz	
@ 10 MHz PFD Frequency		−149		dBc/Hz	
@ 50 MHz PFD Frequency		−142		dBc/Hz	
PLL Figure of Merit		−218 + 10 × log (f_{PFD})		dBc/Hz	Approximation of the PFD/CP phase noise floor (in the flat region) inside the PLL loop bandwidth. When running closed loop this phase noise is gained up by 20 × log(N)[3].
PLL DIGITAL LOCK DETECT WINDOW[4]					Signal available at STATUS pin when selected by 08h<5:2>.
Required to Lock (Coincidence of Edges)					Selected by Register ODh.
Low Range (ABP 1.3 ns, 2.9 ns Only)		3.5		ns	<5> = 1b.
High Range (ABP 1.3 ns, 2.9 ns)		7.5		ns	<5> = 0b.
High Range (ABP 6 ns)		3.5		ns	<5> = 0b.
To Unlock After Lock (Hysteresis)[4]					Selected by Register 0Dh.
Low Range (ABP 1.3 ns, 2.9 ns Only)		7		ns	<5> = 1b.
High Range (ABP 1.3 ns, 2.9 ns)		15		ns	<5> = 0b.
High Range (ABP 6 ns)		11		ns	<5> = 0b.

[1] REFIN and REFINB self-bias points are offset slightly to avoid chatter on an open input condition.
[2] CLK2 is electrically identical to CLK1; the distribution only input can be used as differential or single-ended input (see the Clock Inputs section).
[3] Example: −218 + 10 × log(f_{PFD}) + 20 × log(N) should give the values for the in-band noise at the VCO output.
[4] For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the unlock-after-lock time.

CLOCK INPUTS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUTS (CLK1, CLK2)[1]					
Input Frequency	0		1.6	GHz	
Input Sensitivity		150[2]		mV p-p	Jitter performance can be improved with higher slew rates (greater swing).
Input Level			2[3]	V p-p	Larger swings turn on the protection diodes and can degrade jitter performance.
Input Common-Mode Voltage, V_{CM}	1.5	1.6	1.7	V	Self-biased; enables ac coupling.
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled.
Input Sensitivity, Single-Ended		150		mV p-p	CLK2 ac-coupled; CLK2B ac bypassed to RF ground.
Input Resistance	4.0	4.8	5.6	kΩ	Self-biased.
Input Capacitance		2		pF	

[1] CLK1 and CLK2 are electrically identical; each can be used as either differential or single-ended input.
[2] With a 50 Ω termination, this is −12.5 dBm.
[3] With a 50 Ω termination, this is +10 dBm.

CLOCK OUTPUTS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					Termination = 50 Ω to V_S − 2 V
OUT0, OUT1, OUT2; Differential					Output level 3Dh (3Eh) (3Fh)<3:2> = 10b
Output Frequency			1200	MHz	See Figure 21
Output High Voltage (V_{OH})	V_S − 1.22	V_S − 0.98	V_S − 0.93	V	
Output Low Voltage (V_{OL})	V_S − 2.10	V_S − 1.80	V_S − 1.67	V	
Output Differential Voltage (V_{OD})	660	810	965	mV	
LVDS CLOCK OUTPUTS					Termination = 100 Ω differential; default
OUT3, OUT4; Differential					Output level 40h (41h)<2:1> = 01b 3.5 mA termination current
Output Frequency			800	MHz	See Figure 22
Differential Output Voltage (V_{OD})	250	360	450	mV	
Delta V_{OD}			25	mV	
Output Offset Voltage (V_{OS})	1.125	1.23	1.375	V	
Delta V_{OS}			25	mV	
Short-Circuit Current (I_{SA}, I_{SB})		14	24	mA	Output shorted to GND
CMOS CLOCK OUTPUTS					
OUT3, OUT4					Single-ended measurements; B outputs: inverted, termination open
Output Frequency			250	MHz	With 5 pF load each output; see Figure 23
Output Voltage High (V_{OH})	V_S-0.1			V	@ 1 mA load
Output Voltage Low (V_{OL})			0.1	V	@ 1 mA load

TIMING CHARACTERISTICS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL					Termination = 50 Ω to V_S − 2 V Output level 3Dh (3Eh) (3Fh)<3:2> = 10b
Output Rise Time, t_{RP}		130	180	ps	20% to 80%, measured differentially
Output Fall Time, t_{FP}		130	180	ps	80% to 20%, measured differentially
PROPAGATION DELAY, t_{PECL}, CLK-TO-LVPECL OUT[1]					
Divide = Bypass	335	490	635	ps	
Divide = 2 − 32	375	545	695	ps	
Variation with Temperature		0.5		ps/°C	
OUTPUT SKEW, LVPECL OUTPUTS					
OUT1 to OUT0 on Same Part, t_{SKP}[2]	70	100	140	ps	
OUT1 to OUT2 on Same Part, t_{SKP}[2]	15	45	80	ps	
OUT0 to OUT2 on Same Part, t_{SKP}[2]	45	65	90	Ps	
All LVPECL OUT Across Multiple Parts, t_{SKP_AB}[3]			275	ps	
Same LVPECL OUT Across Multiple Parts, t_{SKP_AB}[3]			130	ps	
LVDS					Termination = 100 Ω differential Output level 40h (41h) <2:1> = 01b 3.5 mA termination current
Output Rise Time, t_{RL}		200	350	ps	20% to 80%, measured differentially
Output Fall Time, t_{FL}		210	350	ps	80% to 20%, measured differentially
PROPAGATION DELAY, t_{LVDS}, CLK-TO-LVDS OUT[1]					Delay off on OUT4
OUT3 to OUT4					
Divide = Bypass	0.99	1.33	1.59	ns	
Divide = 2 − 32	1.04	1.38	1.64	ns	
Variation with Temperature		0.9		ps/°C	
OUTPUT SKEW, LVDS OUTPUTS					Delay off on OUT4
OUT3 to OUT4 on Same Part, t_{SKV}[2]	−85		+270	ps	
All LVDS OUTs Across Multiple Parts, t_{SKV_AB}[3]			450	ps	
Same LVDS OUT Across Multiple Parts, t_{SKV_AB}[3]			325	ps	
CMOS					B outputs are inverted; termination = open
Output Rise Time, t_{RC}		681	865	ps	20% to 80%; C_{LOAD} = 3 pF
Output Fall Time, t_{FC}		646	992	ps	80% to 20%; C_{LOAD} = 3 pF
PROPAGATION DELAY, t_{CMOS}, CLK-TO-CMOS OUT[1]					Delay off on OUT4
Divide = Bypass	1.02	1.39	1.71	ns	
Divide = 2 − 32	1.07	1.44	1.76	ns	
Variation with Temperature		1		ps/°C	
OUTPUT SKEW, CMOS OUTPUTS					Delay off on OUT4
OUT3 to OUT4 on Same Part, t_{SKC}[2]	−140	+145	+300		
All CMOS OUT Across Multiple Parts, t_{SKC_AB}[3]			650	ps	
Same CMOS OUT Across Multiple Parts, t_{SKC_AB}[3]			500	ps	
LVPECL-TO-LVDS OUT					Everything the same; different logic type
Output Skew, t_{SKP_V}	0.74	0.92	1.14	ns	LVPECL to LVDS on same part
LVPECL-TO-CMOS OUT					Everything the same; different logic type
Output Skew, t_{SKP_C}	0.88	1.14	1.43	ns	LVPECL to CMOS on same part
LVDS-TO-CMOS OUT					Everything the same; different logic type
Output Skew, t_{SKV_C}	158	353	506	ps	LVDS to CMOS on same part

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DELAY ADJUST					OUT4; LVDS and CMOS
Shortest Delay Range[4]					35h <5:1> 11111b
Zero Scale	0.05	0.36	0.68	ns	36h <5:1> 00000b
Full Scale	0.72	1.12	1.51	ns	36h <5:1> 11111b
Linearity, DNL		0.5		LSB	
Linearity, INL		0.8		LSB	
Longest Delay Range[4]					35h <5:1> 00000b
Zero Scale	0.20	0.57	0.95	ns	36h <5:1> 00000b
Full Scale	9.0	10.2	11.6	ns	36h <5:1> 11111b
Linearity, DNL		0.3		LSB	
Linearity, INL		0.6		LSB	
Delay Variation with Temperature					
Long Delay Range, 10 ns[5]					
Zero Scale		0.35		ps/°C	
Full Scale		−0.14		ps/°C	
Short Delay Range, 1 ns[5]					
Zero Scale		0.51		ps/°C	
Full Scale		0.67		ps/°C	

[1] The measurements are for CLK1. For CLK2, add approximately 25 ps.
[2] This is the difference between any two similar delay paths within a single device operating at the same voltage and temperature.
[3] This is the difference between any two similar delay paths across multiple devices operating at the same voltage and temperature.
[4] Incremental delay; does not include propagation delay.
[5] All delays between zero scale and full scale can be estimated by linear interpolation.

CLOCK OUTPUT PHASE NOISE

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK1-TO-LVPECL ADDITIVE PHASE NOISE					Distribution Section only; does not include PLL or external VCO/VCXO
CLK1 = 622.08 MHz, OUT = 622.08 MHz					Input slew rate > 1 V/ns
Divide Ratio = 1					
@ 10 Hz Offset		−125		dBc/Hz	
@ 100 Hz Offset		−132		dBc/Hz	
@ 1 kHz Offset		−140		dBc/Hz	
@ 10 kHz Offset		−148		dBc/Hz	
@ 100 kHz Offset		−153		dBc/Hz	
>1 MHz Offset		−154		dBc/Hz	
CLK1 = 622.08 MHz, OUT = 155.52 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−128		dBc/Hz	
@ 100 Hz Offset		−140		dBc/Hz	
@ 1 kHz Offset		−148		dBc/Hz	
@ 10 kHz Offset		−155		dBc/Hz	
@ 100 kHz Offset		−161		dBc/Hz	
>1 MHz Offset		−161		dBc/Hz	
CLK1 = 622.08 MHz, OUT = 38.88 MHz					
Divide Ratio = 16					
@ 10 Hz Offset		−135		dBc/Hz	
@ 100 Hz Offset		−145		dBc/Hz	
@ 1 kHz Offset		−158		dBc/Hz	
@ 10 kHz Offset		−165		dBc/Hz	
@ 100 kHz Offset		−165		dBc/Hz	
>1 MHz Offset		−166		dBc/Hz	
CLK1 = 491.52 MHz, OUT = 61.44 MHz					
Divide Ratio = 8					
@ 10 Hz Offset		−131		dBc/Hz	
@ 100 Hz Offset		−142		dBc/Hz	
@ 1 kHz Offset		−153		dBc/Hz	
@ 10 kHz Offset		−160		dBc/Hz	
@ 100 kHz Offset		−165		dBc/Hz	
>1 MHz Offset		−165		dBc/Hz	
CLK1 = 491.52 MHz, OUT = 245.76 MHz					
Divide Ratio = 2					
@ 10 Hz Offset		−125		dBc/Hz	
@ 100 Hz Offset		−132		dBc/Hz	
@ 1 kHz Offset		−140		dBc/Hz	
@ 10 kHz Offset		−151		dBc/Hz	
@ 100 kHz Offset		−157		dBc/Hz	
>1 MHz Offset		−158		dBc/Hz	
CLK1 = 245.76 MHz, OUT = 61.44 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−138		dBc/Hz	
@ 100 Hz Offset		−144		dBc/Hz	
@ 1 kHz Offset		−154		dBc/Hz	
@ 10 kHz Offset		−163		dBc/Hz	
@ 100 kHz Offset		−164		dBc/Hz	
>1 MHz Offset		−165		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK1-TO-LVDS ADDITIVE PHASE NOISE					Distribution Section only; does not include PLL or external VCO/VCXO
CLK1 = 622.08 MHz, OUT= 622.08 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−100		dBc/Hz	
@ 100 Hz Offset		−110		dBc/Hz	
@ 1 kHz Offset		−118		dBc/Hz	
@ 10 kHz Offset		−129		dBc/Hz	
@ 100 kHz Offset		−135		dBc/Hz	
@ 1 MHz Offset		−140		dBc/Hz	
>10 MHz Offset		−148		dBc/Hz	
CLK1 = 622.08 MHz, OUT = 155.52 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−112		dBc/Hz	
@ 100 Hz Offset		−122		dBc/Hz	
@ 1 kHz Offset		−132		dBc/Hz	
@ 10 kHz Offset		−142		dBc/Hz	
@ 100 kHz Offset		−148		dBc/Hz	
@ 1 MHz Offset		−152		dBc/Hz	
>10 MHz Offset		−155		dBc/Hz	
CLK1 = 491.52 MHz, OUT = 245.76 MHz					
Divide Ratio = 2					
@ 10 Hz Offset		−108		dBc/Hz	
@ 100 Hz Offset		−118		dBc/Hz	
@ 1 kHz Offset		−128		dBc/Hz	
@ 10 kHz Offset		−138		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ 1 MHz Offset		−148		dBc/Hz	
>10 MHz Offset		−154		dBc/Hz	
CLK1 = 491.52 MHz, OUT = 122.88 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−118		dBc/Hz	
@ 100 Hz Offset		−129		dBc/Hz	
@ 1 kHz Offset		−136		dBc/Hz	
@ 10 kHz Offset		−147		dBc/Hz	
@ 100 kHz Offset		−153		dBc/Hz	
@ 1 MHz Offset		−156		dBc/Hz	
>10 MHz Offset		−158		dBc/Hz	
CLK1 = 245.76 MHz, OUT = 245.76 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−108		dBc/Hz	
@ 100 Hz Offset		−118		dBc/Hz	
@ 1 kHz Offset		−128		dBc/Hz	
@ 10 kHz Offset		−138		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ 1 MHz Offset		−148		dBc/Hz	
>10 MHz Offset		−155		dBc/Hz	
CLK1 = 245.76 MHz, OUT = 122.88 MHz					
Divide Ratio = 2					
@ 10 Hz Offset		−118		dBc/Hz	
@ 100 Hz Offset		−127		dBc/Hz	
@ 1 kHz Offset		−137		dBc/Hz	
@ 10 kHz Offset		−147		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
@ 100 kHz Offset		−154		dBc/Hz	
@ 1 MHz Offset		−156		dBc/Hz	
>10 MHz Offset		−158		dBc/Hz	
CLK1-TO-CMOS ADDITIVE PHASE NOISE					Distribution Section only; does not include PLL or external VCO/VCXO
CLK1 = 245.76 MHz, OUT = 245.76 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−110		dBc/Hz	
@ 100 Hz Offset		−121		dBc/Hz	
@ 1 kHz Offset		−130		dBc/Hz	
@ 10 kHz Offset		−140		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ 1 MHz Offset		−149		dBc/Hz	
> 10 MHz Offset		−156		dBc/Hz	
CLK1 = 245.76 MHz, OUT = 61.44 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−122		dBc/Hz	
@ 100 Hz Offset		−132		dBc/Hz	
@ 1 kHz Offset		−143		dBc/Hz	
@ 10 kHz Offset		−152		dBc/Hz	
@ 100 kHz Offset		−158		dBc/Hz	
@ 1 MHz Offset		−160		dBc/Hz	
>10 MHz Offset		−162		dBc/Hz	
CLK1 = 78.6432 MHz, OUT = 78.6432 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−122		dBc/Hz	
@ 100 Hz Offset		−132		dBc/Hz	
@ 1 kHz Offset		−140		dBc/Hz	
@ 10 kHz Offset		−150		dBc/Hz	
@ 100 kHz Offset		−155		dBc/Hz	
@ 1 MHz Offset		−158		dBc/Hz	
>10 MHz Offset		−160		dBc/Hz	
CLK1 = 78.6432 MHz, OUT = 39.3216 MHz					
Divide Ratio = 2					
@ 10 Hz Offset		−128		dBc/Hz	
@ 100 Hz Offset		−136		dBc/Hz	
@ 1 kHz Offset		−146		dBc/Hz	
@ 10 kHz Offset		−155		dBc/Hz	
@ 100 kHz Offset		−161		dBc/Hz	
>1 MHz Offset		−162		dBc/Hz	

CLOCK OUTPUT ADDITIVE TIME JITTER

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution Section only; does not include PLL or external VCO/VCXO
CLK1 = 622.08 MHz Any LVPECL (OUT0 to OUT2) = 622.08 MHz Divide Ratio = 1		40		fs rms	BW = 12 kHz − 20 MHz (OC-12)
CLK1 = 622.08 MHz Any LVPECL (OUT0 to OUT2) = 155.52 MHz Divide Ratio = 4		55		fs rms	BW = 12 kHz − 20 MHz (OC-3)
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4		215		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 100 MHz Both LVDS (OUT3, OUT4) = 100 MHz		215		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 50 MHz Both LVDS (OUT3, OUT4) = 50 MHz		222		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 50 MHz Both CMOS (OUT3, OUT4) = 50 MHz (B Outputs Off)		225		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 50 MHz Both CMOS (OUT3, OUT4) = 50 MHz (B Outputs On)		225		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)
LVDS OUTPUT ADDITIVE TIME JITTER					Distribution Section only; does not include PLL or external VCO/VCXO
CLK1 = 400 MHz LVDS (OUT3) = 100 MHz Divide Ratio = 4		264		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
CLK1 = 400 MHz LVDS (OUT4) = 100 MHz Divide Ratio = 4		319		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK1 = 400 MHz		395		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
LVDS (OUT3) = 100 MHz					
Divide Ratio = 4					
LVDS (OUT4) = 50 MHz					Interferer(s)
All LVPECL = 50 MHz					Interferer(s)
CLK1 = 400 MHz		395		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
LVDS (OUT4) = 100 MHz					
Divide Ratio = 4					
LVDS (OUT3) = 50 MHz					Interferer(s)
All LVPECL = 50 MHz					Interferer(s)
CLK1 = 400 MHz		367		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
LVDS (OUT3) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT4) = 50 MHz (B Outputs Off)					Interferer(s)
All LVPECL = 50 MHz					Interferer(s)
CLK1 = 400 MHz		367		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
LVDS (OUT4) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT3) = 50 MHz (B Outputs Off)					Interferer(s)
All LVPECL = 50 MHz					Interferer(s)
CLK1 = 400 MHz		548		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
LVDS (OUT3) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT4) = 50 MHz (B Outputs On)					Interferer(s)
All LVPECL = 50 MHz					Interferer(s)
CLK1 = 400 MHz		548		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
LVDS (OUT4) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT3) = 50 MHz (B Outputs On)					Interferer(s)
All LVPECL = 50 MHz					Interferer(s)
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution Section only; does not include PLL or external VCO/VCXO
CLK1 = 400 MHz		275		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
Both CMOS (OUT3, OUT4) = 100 MHz (B Output On)					
Divide Ratio = 4					
CLK1 = 400 MHz		400		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
CMOS (OUT3) = 100 MHz (B Output On)					
Divide Ratio = 4					
All LVPECL = 50 MHz					Interferer(s)
LVDS (OUT4) = 50 MHz					Interferer(s)
CLK1 = 400 MHz		374		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
CMOS (OUT3) = 100 MHz (B Output On)					
Divide Ratio = 4					
All LVPECL = 50 MHz					Interferer(s)
CMOS (OUT4) = 50 MHz (B Output Off)					Interferer(s)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK1 = 400 MHz		555		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
CMOS (OUT3) = 100 MHz (B Output On)					
Divide Ratio = 4					
All LVPECL = 50 MHz					Interferer(s)
CMOS (OUT4) = 50 MHz (B Output On)					Interferer(s)
DELAY BLOCK ADDITIVE TIME JITTER[1]					Incremental additive jitter
100 MHz Output					
Delay FS = 1 ns (1600 µA, 1C) Fine Adj. 00000		0.61		ps	
Delay FS = 1 ns (1600 µA, 1C) Fine Adj. 11111		0.73		ps	
Delay FS = 2 ns (800 µA, 1C) Fine Adj. 00000		0.71		ps	
Delay FS = 2 ns (800 µA, 1C) Fine Adj. 11111		1.2		ps	
Delay FS = 3 ns (800 µA, 4C) Fine Adj. 00000		0.86		ps	
Delay FS = 3 ns (800 µA, 4C) Fine Adj. 11111		1.8		ps	
Delay FS = 4 ns (400 µA, 4C) Fine Adj. 00000		1.2		ps	
Delay FS = 4 ns (400 µA, 4C) Fine Adj. 11111		2.1		ps	
Delay FS = 5 ns (200 µA, 1C) Fine Adj. 00000		1.3		ps	
Delay FS = 5 ns (200 µA, 1C) Fine Adj. 11111		2.7		ps	
Delay FS = 11 ns (200 µA, 4C) Fine Adj. 00000		2.0		ps	
Delay FS = 11 ns (200 µA, 4C) Fine Adj. 00100		2.8		ps	

[1] This value is incremental. That is, it is in addition to the jitter of the LVDS or CMOS output without the delay. To estimate the total jitter, the LVDS or CMOS output jitter should be added to this value using the root sum of the squares (RSS) method.

PLL AND DISTRIBUTION PHASE NOISE AND SPURIOUS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE NOISE AND SPURIOUS					Depends on VCO/VCXO selection. Measured at LVPECL clock outputs; ABP = 6 ns; I_{CP} = 5 mA; Ref = 30.72 MHz.
VCXO = 245.76 MHz, F_{PFD} = 1.2288 MHz; R = 25, N = 200					VCXO is Toyocom TCO-2112 245.76.
245.76 MHz Output					Divide by 1.
Phase Noise @100 kHz Offset		<−145		dBc/Hz	Dominated by VCXO phase noise.
Spurious		<−97		dBc	First and second harmonics of F_{PFD}. Below measurement floor.
61.44 MHz Output					Divide by 4.
Phase Noise @100 kHz Offset		<−155		dBc/Hz	Dominated by VCXO phase noise.
Spurious		<−97		dBc	First and second harmonics of F_{PFD}. Below measurement floor.

SERIAL CONTROL PORT

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CSB, SCLK (INPUTS)					CSB and SCLK have 30 kΩ internal pull-down resistors
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		110		μA	
Input Logic 0 Current			1	μA	
Input Capacitance		2		pF	
SDIO (WHEN INPUT)					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		10		nA	
Input Logic 0 Current		10		nA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, $1/t_{SCLK}$)			25	MHz	
Pulse Width High, t_{PWH}	16			ns	
Pulse Width Low, t_{PWL}	16			ns	
SDIO to SCLK Setup, t_{DS}	2			ns	
SCLK to SDIO Hold, t_{DH}	1			ns	
SCLK to Valid SDIO and SDO, t_{DV}	6			ns	
CSB to SCLK Setup and Hold, t_S, t_H	2			ns	
CSB Minimum Pulse Width High, t_{PWH}	3			ns	

FUNCTION PIN

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					The FUNCTION pin has a 30 kΩ internal pull-down resistor. This pin should normally be held high. Do not leave NC.
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current		110		μA	
Logic 0 Current			1	μA	
Capacitance		2		pF	
RESET TIMING					
Pulse Width Low	50			ns	
SYNC TIMING					
Pulse Width Low	1.5			High speed clock cycles	High speed clock is CLK1 or CLK2, whichever is used for distribution.

STATUS PIN

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					When selected as a digital output (CMOS); there are other modes in which the STATUS pin is not CMOS digital output. See Figure 37.
Output Voltage High (V_{OH})	2.7			V	
Output Voltage Low (V_{OL})			0.4	V	
MAXIMUM TOGGLE RATE		100		MHz	Applies when PLL mux is set to any divider or counter output, or PFD up/down pulse. Also applies in analog lock detect mode. Usually debug mode only. Beware that spurs may couple to output when this pin is toggling.
ANALOG LOCK DETECT					
Capacitance		3		pF	On-chip capacitance; used to calculate RC time constant for analog lock detect readback. Use a pull-up resistor.

POWER

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-UP DEFAULT MODE POWER DISSIPATION		550	600	mW	Power-up default state; does not include power dissipated in output load resistors. No clock.
POWER DISSIPATION			800	mW	All outputs on. Three LVPECL outputs @ 800 MHz, two CMOS out @ 62 MHz (5 pF load). Does not include power dissipated in external resistors.
			850	mW	All outputs on. Three LVPECL outputs @ 800 MHz, two CMOS out @ 125 MHz (5 pF load). Does not include power dissipated in external resistors.
Full Sleep Power-Down		35	60	mW	Maximum sleep is entered by setting 0Ah<1:0> = 01b and 58h<4> = 1b. This powers off the PLL BG and the distribution BG references. Does not include power dissipated in terminations.
Power-Down (PDB)		60	80	mW	Set FUNCTION pin for PDB operation by setting 58h<6:5> = 11b. Pull PDB low. Does not include power dissipated in terminations.
POWER DELTA					
CLK1, CLK2 Power-Down	10	15	25	mW	
Divider, DIV 2 – 32 to Bypass	23	27	33	mW	For each divider.
LVPECL Output Power-Down (PD2, PD3)	50	65	75	mW	For each output. Does not include dissipation in termination (PD2 only).
LVDS Output Power-Down	80	92	110	mW	For each output.
CMOS Output Power-Down (Static)	56	70	85	mW	For each output. Static (no clock).
CMOS Output Power-Down (Dynamic)	115	150	190	mW	For each CMOS output, single-ended. Clocking at 62 MHz with 5 pF load.
CMOS Output Power-Down (Dynamic)	125	165	210	mW	For each CMOS output, single-ended. Clocking at 125 MHz with 5 pF load.
Delay Block Bypass	20	24	60	mW	Vs. delay block operation at 1 ns fs with maximum delay; output clocking at 25 MHz.
PLL Section Power-Down	5	15	40	mW	

TIMING DIAGRAMS

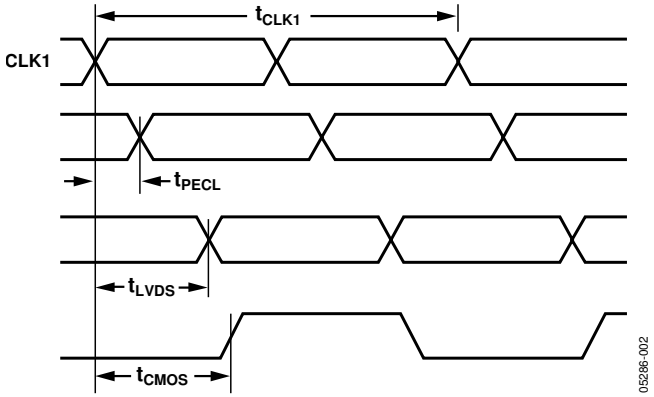

Figure 2. CLK1/CLK1B to Clock Output Timing, DIV = 1 Mode

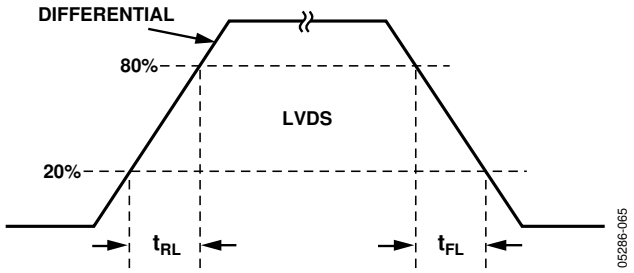

Figure 4. LVDS Timing, Differential

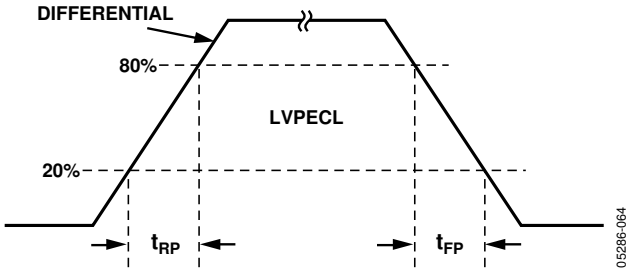

Figure 3. LVPECL Timing, Differential

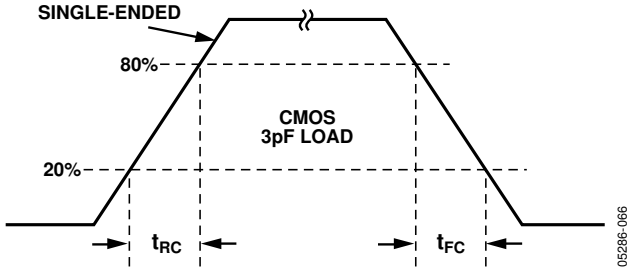

Figure 5. CMOS Timing, Single-Ended, 3 pF Load

ABSOLUTE MAXIMUM RATINGS

Table 12.

Parameter or Pin	With Respect to	Min	Max	Unit
VS	GND	−0.3	+3.6	V
VCP	GND	−0.3	+5.8	V
VCP	V_S	−0.3	+5.8	V
REFIN, REFINB	GND	−0.3	V_S + 0.3	V
RSET	GND	−0.3	V_S + 0.3	V
CPRSET	GND	−0.3	V_S + 0.3	V
CLK1, CLK1B, CLK2, CLK2B	GND	−0.3	V_S + 0.3	V
CLK1	CLK1B	−1.2	+1.2	V
CLK2	CLK2B	−1.2	+1.2	V
SCLK, SDIO, SDO, CSB	GND	−0.3	V_S + 0.3	V
OUT0, OUT1, OUT2, OUT3, OUT4	GND	−0.3	V_S + 0.3	V
FUNCTION	GND	−0.3	V_S + 0.3	V
STATUS	GND	−0.3	V_S + 0.3	V
Junction Temperature			150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			300	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance[1]

48-Lead LFCSP
θ_{JA} = 28.5°C/W

[1] Thermal impedance measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-7.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

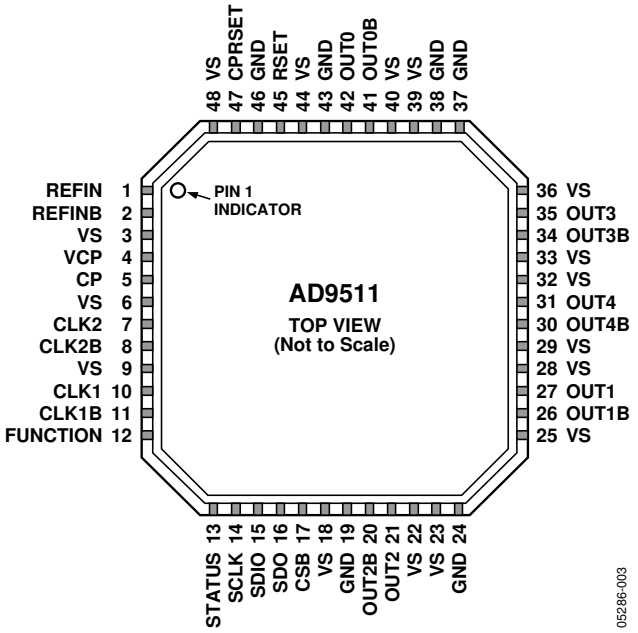

Figure 6. 48-Lead LFCSP Pin Configuration

Note that the exposed paddle on this package is an electrical connection as well as a thermal enhancement. For the device to function properly, the paddle must be attached to ground, GND.

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	REFIN	PLL Reference Input.
2	REFINB	Complementary PLL Reference Input.
3, 6, 9, 18, 22, 23, 25, 28, 29, 32, 33, 36, 39, 40, 44, 48	VS	Power Supply (3.3 V).
4	VCP	Charge Pump Power Supply. It should be greater than or equal to VS. VCP can be set as high as 5.5 V for VCOs, requiring extended tuning range.
5	CP	Charge Pump Output.
7	CLK2	Clock Input. Used to connect external VCO/VCXO to feedback divider, N. CLK2 also drives the distribution section of the chip and may be used as a generic clock input when PLL is not used.
8	CLK2B	Complementary Clock Input. Used in conjunction with CLK2.
10	CLK1	Clock Input. Drives distribution section of the chip.
11	CLK1B	Complementary Clock Input. Used in conjunction with CLK1.
12	FUNCTION	Multipurpose Input. May be programmed as a reset (RESETB), sync (SYNCB), or power-down (PDB) pin. This pin is internally pulled down by a 30 kΩ resistor. If this pin is left NC, the part is in reset by default. To avoid this, connect this pin to V_S with a 1 kΩ resistor.
13	STATUS	Output Used to Monitor PLL Status and Sync Status.
14	SCLK	Serial Data Clock.
15	SDIO	Serial Data I/O.
16	SDO	Serial Data Output.
17	CSB	Serial Port Chip Select.
19, 24, 37, 38, 43, 46	GND	Ground.
20	OUT2B	Complementary LVPECL Output.
21	OUT2	LVPECL Output.
26	OUT1B	Complementary LVPECL Output.
27	OUT1	LVPECL Output.
30	OUT4B	Complementary LVDS/Inverted CMOS Output. OUT4 includes a delay block.
31	OUT4	LVDS/CMOS Output. OUT4 includes a delay block.
34	OUT3B	Complementary LVDS/Inverted CMOS Output.
35	OUT3	LVDS/CMOS Output.
41	OUT0B	Complementary LVPECL Output.
42	OUT0	LVPECL Output.
45	RSET	Current Set Resistor to Ground. Nominal value = 4.12 kΩ.
47	CPRSET	Charge Pump Current Set Resistor to Ground. Nominal value = 5.1 kΩ.

Note that the exposed paddle on this package is an electrical connection as well as a thermal enhancement. For the device to function properly, the paddle must be attached to ground, GND.

TERMINOLOGY

Phase Jitter and Phase Noise
An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0 degrees to 360 degrees for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in dB) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter
Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings is seen to vary. In a square wave, the time jitter is seen as a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Since these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the SNR and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise
It is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources has been subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contribute their own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise.

Additive Time Jitter
It is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources has been subtracted. This makes it possible to predict the degree to which the device will impact the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contribute their own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

TYPICAL PERFORMANCE CHARACTERISTICS

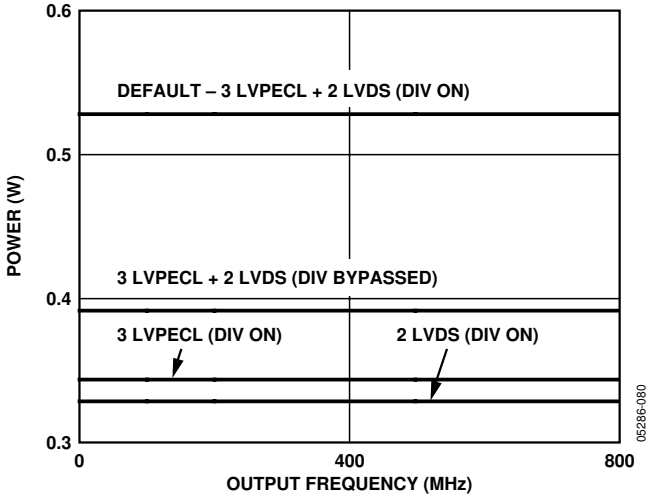

Figure 7. Power vs. Frequency—LVPECL, LVDS (PLL Off)

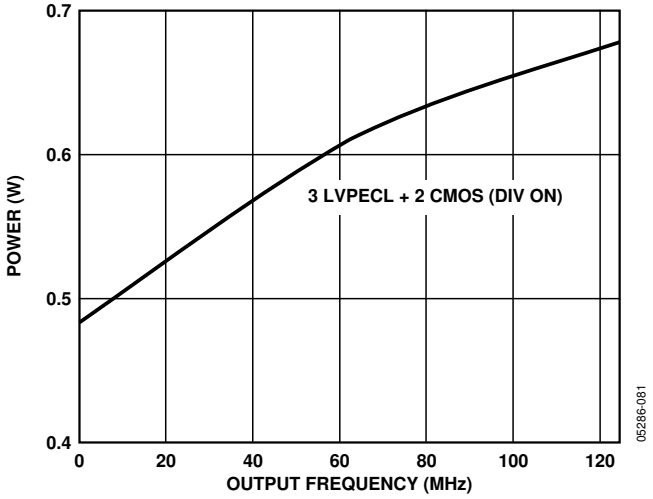

Figure 10. Power vs. Frequency—LVPECL, CMOS (PLL Off)

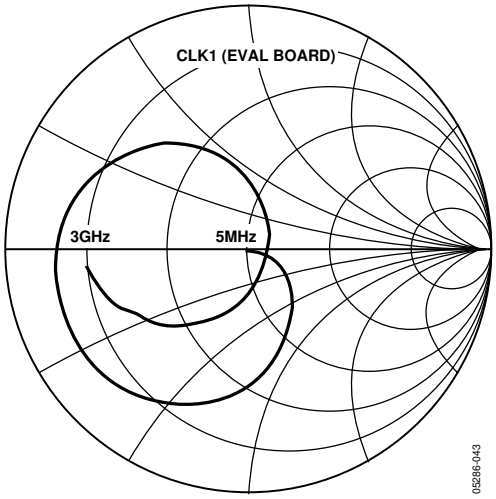

Figure 8. CLK1 Smith Chart (Evaluation Board)

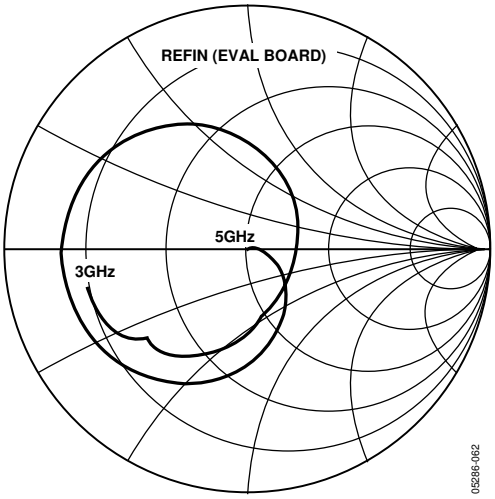

Figure 11. REFIN Smith Chart (Evaluation Board)

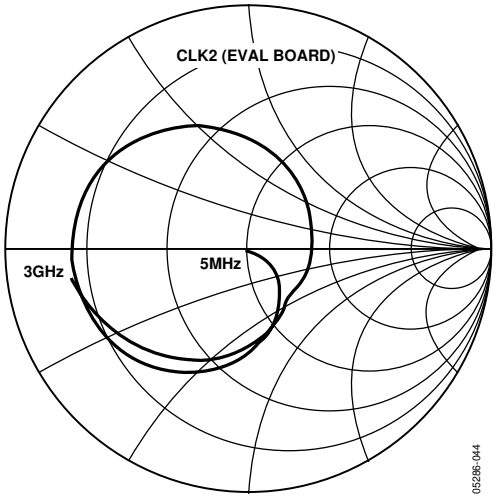

Figure 9. CLK2 Smith Chart (Evaluation Board)

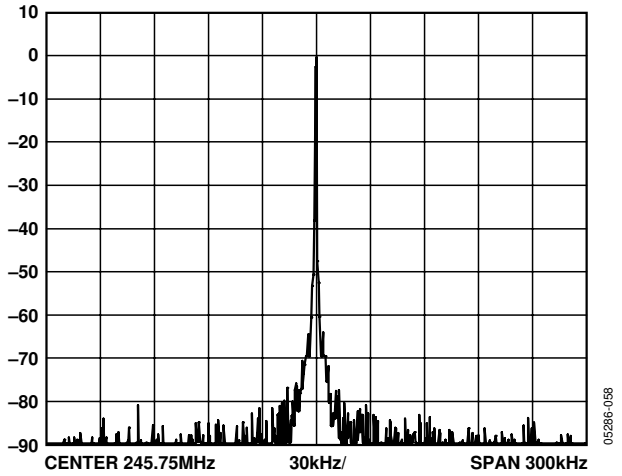

Figure 12. Phase Noise, LVPECL, DIV 1, FVCXO = 245.76 MHz, FOUT = 245.76 MHz, FPFD = 1.2288 MHz, R = 25, N = 200

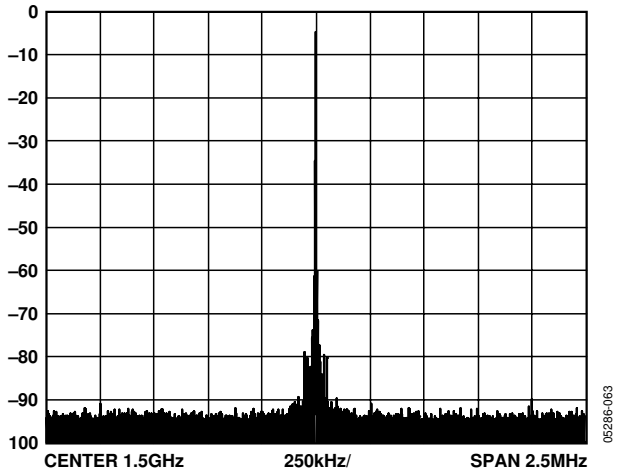

Figure 13. PLL Reference Spurs: VCO 1.5 GHz, FPFD = 1 MHz

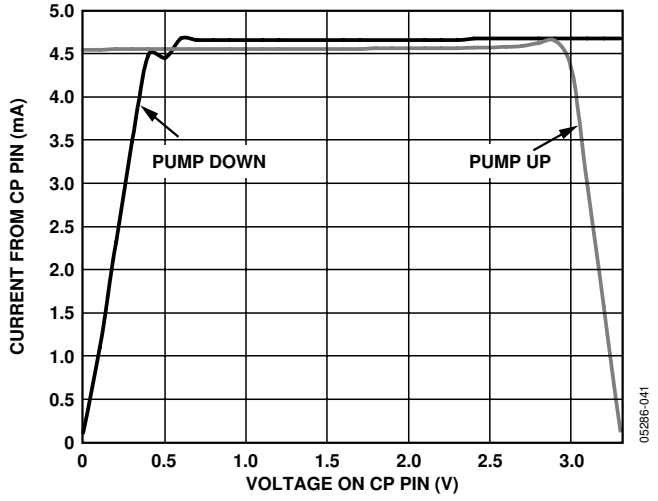

Figure 14. Charge Pump Output Characteristics @ VCP_S = 3.3 V

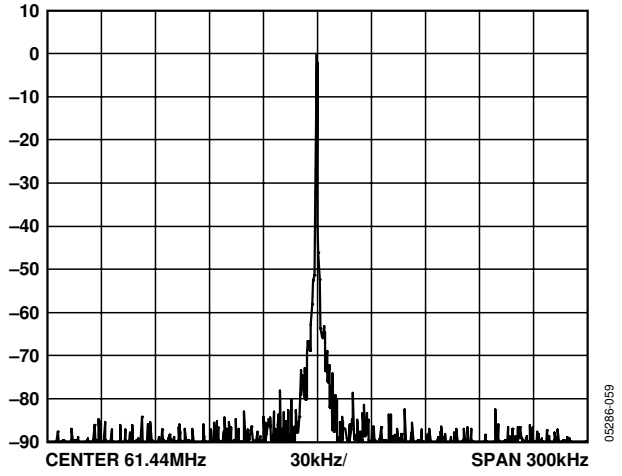

Figure 15. Phase Noise, LVPECL, DIV 4, FVCXO = 245.76 MHz, FOUT = 61.44 MHz, FPFD = 1.2288 MHz, R = 25, N = 200

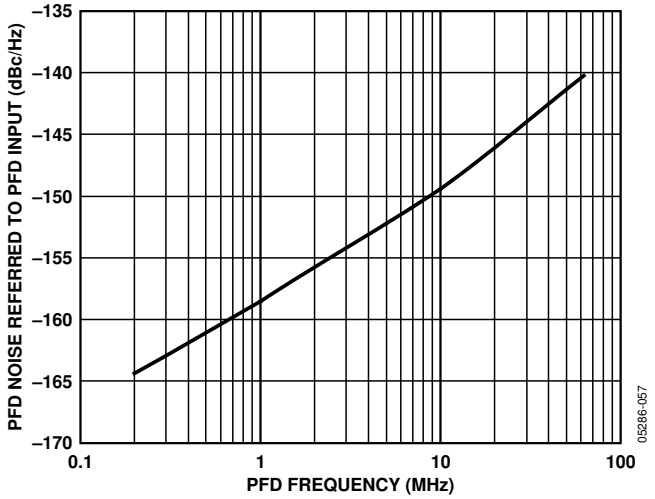

Figure 16. Phase Noise (Referred to CP Output) vs. PFD Frequency

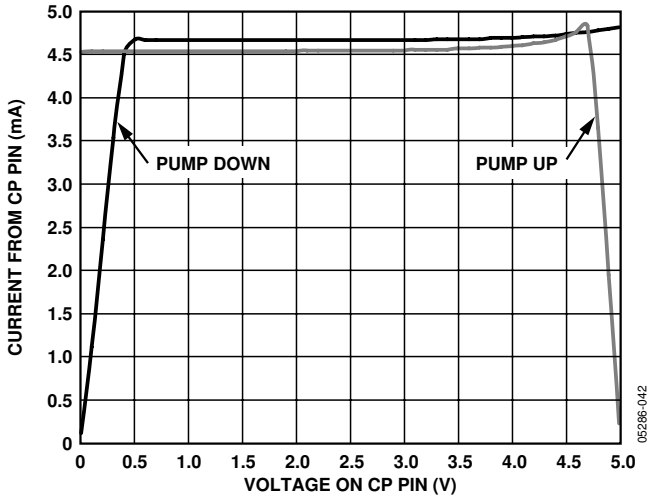

Figure 17. Charge Pump Output Characteristics @ VCP_S = 5.0 V

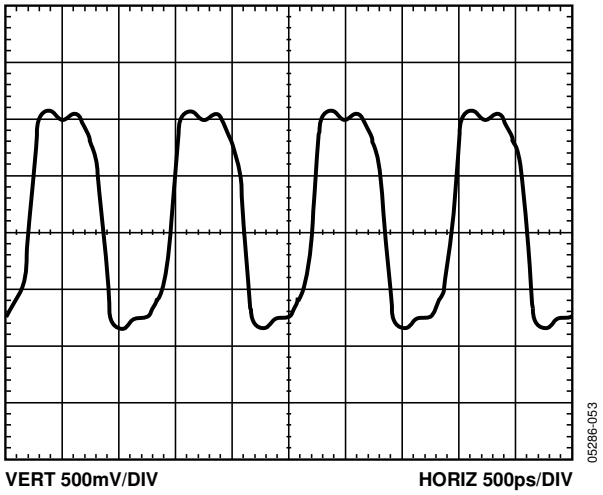

Figure 18. LVPECL Differential Output @ 800 MHz

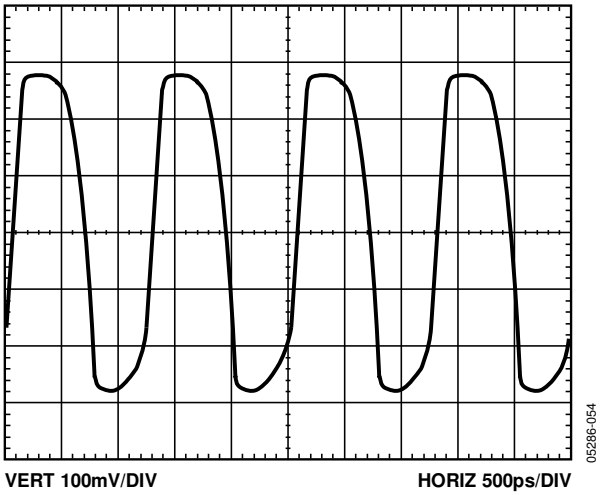

Figure 19. LVDS Differential Output @ 800 MHz

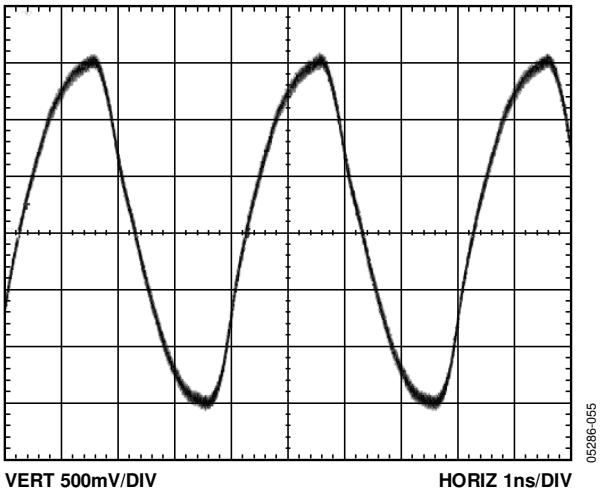

Figure 20. CMOS Single-Ended Output @ 250 MHz with 10 pF Load

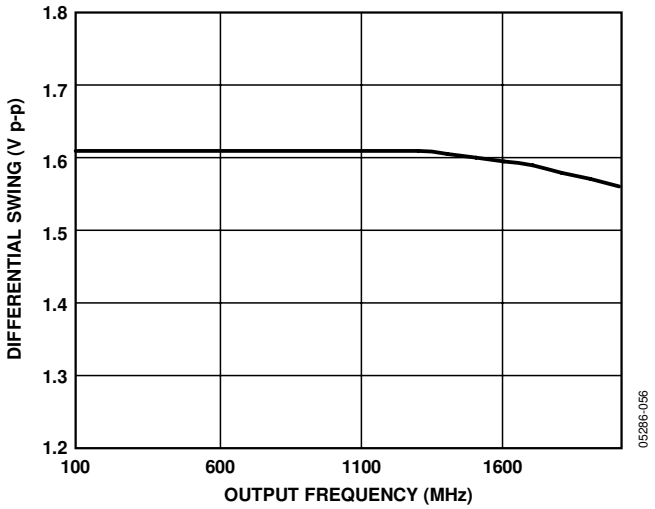

Figure 21. LVPECL Differential Output Swing vs. Frequency

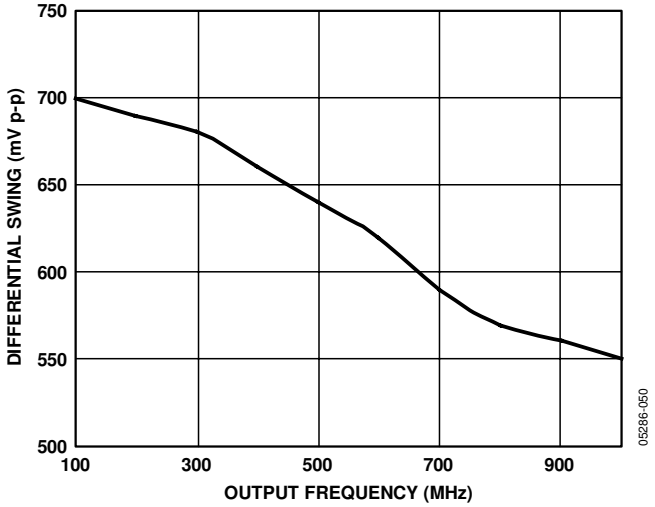

Figure 22. LVDS Differential Output Swing vs. Frequency

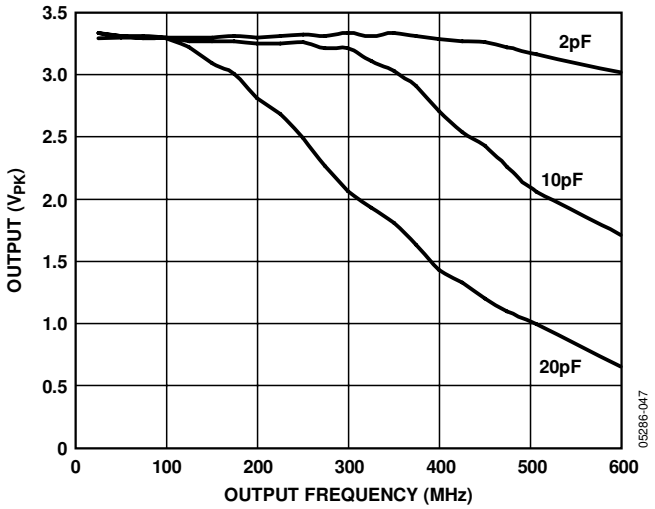

Figure 23. CMOS Single-Ended Output Swing vs. Frequency and Load