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1.2 GHz Clock Distribution IC, 1.6 GHz Inputs, Dividers, Delay Adjust, Five Outputs

AD9512

FEATURES

- Two 1.6 GHz, differential clock inputs
- 5 programmable dividers, 1 to 32, all integers
- Phase select for output-to-output coarse delay adjust
- 3 independent 1.2 GHz LVPECL outputs
  - Additive output jitter 225 fs rms
- 2 independent 800 MHz/250 MHz LVDS/CMOS clock outputs
  - Additive output jitter 275 fs rms
  - Fine delay adjust on 1 LVDS/CMOS output
- Serial control port
- Space-saving 48-lead LFCSP

APPLICATIONS

- Low jitter, low phase noise clock distribution
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- High performance wireless transceivers
- High performance instrumentation
- Broadband infrastructure

FUNCTIONAL BLOCK DIAGRAM

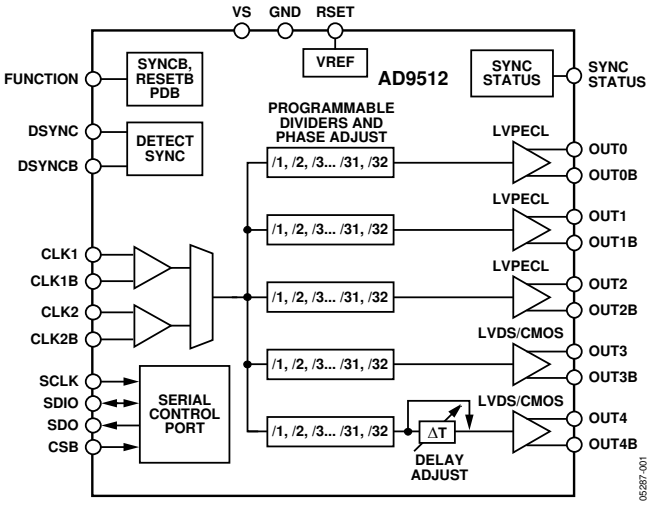

Figure 1.

GENERAL DESCRIPTION

The AD9512 provides a multi-output clock distribution in a design that emphasizes low jitter and low phase noise to maximize data converter performance. Other applications with demanding phase noise and jitter requirements can also benefit from this part.

There are five independent clock outputs. Three outputs are LVPECL (1.2 GHz), and two are selectable as either LVDS (800 MHz) or CMOS (250 MHz) levels.

Each output has a programmable divider that may be bypassed or set to divide by any integer up to 32. The phase of one clock output relative to another clock output may be varied by means of a divider phase select function that serves as a coarse timing adjustment.

One of the LVDS/CMOS outputs features a programmable delay element with a range of up to 10 ns of delay. This fine tuning delay block has 5-bit resolution, giving 32 possible delays from which to choose.

The AD9512 is ideally suited for data converter clocking applications where maximum converter performance is achieved by encode signals with subpicosecond jitter.

The AD9512 is available in a 48-lead LFCSP and can be operated from a single 3.3 V supply. The temperature range is −40°C to +85°C.

Rev. A

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AD9512* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9512 Evaluation Board

DOCUMENTATION

Application Notes

- AN-0974: Multicarrier TD-SCMA Feasibility
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal

Data Sheet

- AD9512-DSCC: Military Data Sheet
- AD9512-EP: Enhanced Product Data Sheet
- AD9512: 1.2 GHz Clock Distribution IC, 1.6 GHz Inputs, Dividers, Delay Adjust, Five Outputs Data Sheet

TOOLS AND SIMULATIONS

- ADIsimCLK Design and Evaluation Software
- AD9512 IBIS Models

REFERENCE DESIGNS

- CN0109

REFERENCE MATERIALS

Press

- Analog Devices' Dual 14-bit A/D Converter Reduces Power and Size in Communications, Instrumentation, Test and Measurement Applications

Technical Articles

- ADI Buys Korean Mobile TV Chip Maker
- Design A Clock-Distribution Strategy With Confidence
- Improved DDS Devices Enable Advanced Comm Systems
- Low-power direct digital synthesizer cores enable high level of integration
- Speedy A/Ds Demand Stable Clocks
- Understand the Effects of Clock Jitter and Phase Noise on Sampled Systems

DESIGN RESOURCES

- AD9512 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9512 EngineerZone Discussions.

SAMPLE AND BUY

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4/05—Revision 0: Initial Version

SPECIFICATIONS

Typical (Typ) is given for V_S = 3.3 V ± 5%; T_A = 25°C, R_{SET} = 4.12 kΩ, unless otherwise noted. Minimum (Min) and Maximum (Max) values are given over full V_S and T_A (−40°C to +85°C) variation.

CLOCK INPUTS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUTS (CLK1, CLK2)[1]					
Input Frequency	0		1.6	GHz	
Input Sensitivity		150[2]		mV p-p	Jitter performance can be improved with higher slew rates (greater swing).
Input Level			2[3]	V p-p	Larger swings turn on the protection diodes and can degrade jitter performance.
Input Common-Mode Voltage, V_{CM}	1.5	1.6	1.7	V	Self-biased; enables ac coupling.
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled.
Input Sensitivity, Single-Ended		150		mV p-p	CLK2 ac-coupled; CLK2B ac bypassed to RF ground.
Input Resistance	4.0	4.8	5.6	kΩ	Self-biased.
Input Capacitance		2		pF	

[1] CLK1 and CLK2 are electrically identical; each can be used as either differential or single-ended input.
[2] With a 50 Ω termination, this is −12.5 dBm.
[3] With a 50 Ω termination, this is +10 dBm.

CLOCK OUTPUTS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					Termination = 50 Ω to V_S − 2 V
OUT0, OUT1, OUT2; Differential					Output level 3Dh (3Eh) (3Fh)<3:2> = 10b
Output Frequency			1200	MHz	See Figure 14
Output High Voltage (V_{OH})	V_S − 1.22	V_S − 0.98	V_S − 0.93	V	
Output Low Voltage (V_{OL})	V_S − 2.10	V_S − 1.80	V_S − 1.67	V	
Output Differential Voltage (V_{OD})	660	810	965	mV	
LVDS CLOCK OUTPUTS					Termination = 100 Ω differential; default
OUT3, OUT4; Differential					Output level 40h (41h)<2:1> = 01b 3.5 mA termination current
Output Frequency			800	MHz	See Figure 15
Differential Output Voltage (V_{OD})	250	360	450	mV	
Delta V_{OD}			25	mV	
Output Offset Voltage (V_{OS})	1.125	1.23	1.375	V	
Delta V_{OS}			25	mV	
Short-Circuit Current (I_{SA}, I_{SB})		14	24	mA	Output shorted to GND
CMOS CLOCK OUTPUTS					
OUT3, OUT4					Single-ended measurements; B outputs: inverted, termination open
Output Frequency			250	MHz	With 5 pF load each output; see Figure 16
Output Voltage High (V_{OH})	V_S − 0.1			V	@ 1 mA load
Output Voltage Low (V_{OL})			0.1	V	@ 1 mA load

TIMING CHARACTERISTICS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL					Termination = 50 Ω to V_S − 2 V Output level 3Dh (3Eh) (3Fh)<3:2> = 10b
Output Rise Time, t_{RP}		130	180	ps	20% to 80%, measured differentially
Output Fall Time, t_{FP}		130	180	ps	80% to 20%, measured differentially
PROPAGATION DELAY, t_{PECL}, CLK-TO-LVPECL OUT[1]					
Divide = Bypass	335	490	635	ps	
Divide = 2 − 32	375	545	695	ps	
Variation with Temperature		0.5		ps/°C	
OUTPUT SKEW, LVPECL OUTPUTS					
OUT1 to OUT0 on Same Part, t_{SKP}[2]	70	100	140	ps	
OUT1 to OUT2 on Same Part, t_{SKP}[2]	15	45	80	ps	
OUT0 to OUT2 on Same Part, t_{SKP}[2]	45	65	90	Ps	
All LVPECL OUT Across Multiple Parts, t_{SKP_AB}[3]			275	ps	
Same LVPECL OUT Across Multiple Parts, t_{SKP_AB}[3]			130	ps	
LVDS					Termination = 100 Ω differential Output level 40h (41h) <2:1> = 01b 3.5 mA termination current
Output Rise Time, t_{RL}		200	350	ps	20% to 80%, measured differentially
Output Fall Time, t_{FL}		210	350	ps	80% to 20%, measured differentially
PROPAGATION DELAY, t_{LVDS}, CLK-TO-LVDS OUT[1]					Delay off on OUT4
OUT3 to OUT4					
Divide = Bypass	0.99	1.33	1.59	ns	
Divide = 2 − 32	1.04	1.38	1.64	ns	
Variation with Temperature		0.9		ps/°C	
OUTPUT SKEW, LVDS OUTPUTS					Delay off on OUT4
OUT3 to OUT4 on Same Part, t_{SKV}[2]	−85		+270	ps	
All LVDS OUTs Across Multiple Parts, t_{SKV_AB}[3]			450	ps	
Same LVDS OUT Across Multiple Parts, t_{SKV_AB}[3]			325	ps	
CMOS					B outputs are inverted; termination = open
Output Rise Time, t_{RC}		681	865	ps	20% to 80%; C_{LOAD} = 3 pF
Output Fall Time, t_{FC}		646	992	ps	80% to 20%; C_{LOAD} = 3 pF
PROPAGATION DELAY, t_{CMOS}, CLK-TO-CMOS OUT[1]					Delay off on OUT4
Divide = Bypass	1.02	1.39	1.71	ns	
Divide = 2 − 32	1.07	1.44	1.76	ns	
Variation with Temperature		1		ps/°C	
OUTPUT SKEW, CMOS OUTPUTS					Delay off on OUT4
OUT3 to OUT4 on Same Part, t_{SKC}[2]	−140	+145	+300		
All CMOS OUT Across Multiple Parts, t_{SKC_AB}[3]			650	ps	
Same CMOS OUT Across Multiple Parts, t_{SKC_AB}[3]			500	ps	
LVPECL-TO-LVDS OUT					Everything the same; different logic type
Output Skew, t_{SKP_V}	0.74	0.92	1.14	ns	LVPECL to LVDS on same part
LVPECL-TO-CMOS OUT					Everything the same; different logic type
Output Skew, t_{SKP_C}	0.88	1.14	1.43	ns	LVPECL to CMOS on same part
LVDS-TO-CMOS OUT					Everything the same; different logic type
Output Skew, t_{SKV_C}	158	353	506	ps	LVDS to CMOS on same part

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DELAY ADJUST					OUT4; LVDS and CMOS
Shortest Delay Range[4]					35h <5:1> 11111b
Zero Scale	0.05	0.36	0.68	ns	36h <5:1> 00000b
Full Scale	0.72	1.12	1.51	ns	36h <5:1> 11111b
Linearity, DNL		0.5		LSB	
Linearity, INL		0.8		LSB	
Longest Delay Range[4]					35h <5:1> 00000b
Zero Scale	0.20	0.57	0.95	ns	36h <5:1> 00000b
Full Scale	9.0	10.2	11.6	ns	36h <5:1> 11111b
Linearity, DNL		0.3		LSB	
Linearity, INL		0.6		LSB	
Delay Variation with Temperature					
Long Delay Range, 10 ns[5]					
Zero Scale		0.35		ps/°C	
Full Scale		−0.14		ps/°C	
Short Delay Range, 1 ns[5]					
Zero Scale		0.51		ps/°C	
Full Scale		0.67		ps/°C	

[1] The measurements are for CLK1. For CLK2, add approximately 25 ps.
[2] This is the difference between any two similar delay paths within a single device operating at the same voltage and temperature.
[3] This is the difference between any two similar delay paths across multiple devices operating at the same voltage and temperature.
[4] Incremental delay; does not include propagation delay.
[5] All delays between the zero scale and full scale can be estimated by linear interpolation.

CLOCK OUTPUT PHASE NOISE

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK1-TO-LVPECL ADDITIVE PHASE NOISE					
CLK1 = 622.08 MHz, OUT = 622.08 MHz					Input slew rate > 1 V/ns
Divide Ratio = 1					
@ 10 Hz Offset		−125		dBc/Hz	
@ 100 Hz Offset		−132		dBc/Hz	
@ 1 kHz Offset		−140		dBc/Hz	
@ 10 kHz Offset		−148		dBc/Hz	
@ 100 kHz Offset		−153		dBc/Hz	
>1 MHz Offset		−154		dBc/Hz	
CLK1 = 622.08 MHz, OUT = 155.52 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−128		dBc/Hz	
@ 100 Hz Offset		−140		dBc/Hz	
@ 1 kHz Offset		−148		dBc/Hz	
@ 10 kHz Offset		−155		dBc/Hz	
@ 100 kHz Offset		−161		dBc/Hz	
>1 MHz Offset		−161		dBc/Hz	
CLK1 = 622.08 MHz, OUT = 38.88 MHz					
Divide Ratio = 16					
@ 10 Hz Offset		−135		dBc/Hz	
@ 100 Hz Offset		−145		dBc/Hz	
@ 1 kHz Offset		−158		dBc/Hz	
@ 10 kHz Offset		−165		dBc/Hz	
@ 100 kHz Offset		−165		dBc/Hz	
>1 MHz Offset		−166		dBc/Hz	
CLK1 = 491.52 MHz, OUT = 61.44 MHz					
Divide Ratio = 8					
@ 10 Hz Offset		−131		dBc/Hz	
@ 100 Hz Offset		−142		dBc/Hz	
@ 1 kHz Offset		−153		dBc/Hz	
@ 10 kHz Offset		−160		dBc/Hz	
@ 100 kHz Offset		−165		dBc/Hz	
>1 MHz Offset		−165		dBc/Hz	
CLK1 = 491.52 MHz, OUT = 245.76 MHz					
Divide Ratio = 2					
@ 10 Hz Offset		−125		dBc/Hz	
@ 100 Hz Offset		−132		dBc/Hz	
@ 1 kHz Offset		−140		dBc/Hz	
@ 10 kHz Offset		−151		dBc/Hz	
@ 100 kHz Offset		−157		dBc/Hz	
>1 MHz Offset		−158		dBc/Hz	
CLK1 = 245.76 MHz, OUT = 61.44 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−138		dBc/Hz	
@ 100 Hz Offset		−144		dBc/Hz	
@ 1 kHz Offset		−154		dBc/Hz	
@ 10 kHz Offset		−163		dBc/Hz	
@ 100 kHz Offset		−164		dBc/Hz	
>1 MHz Offset		−165		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK1-TO-LVDS ADDITIVE PHASE NOISE					
CLK1 = 622.08 MHz, OUT = 622.08 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−100		dBc/Hz	
@ 100 Hz Offset		−110		dBc/Hz	
@ 1 kHz Offset		−118		dBc/Hz	
@ 10 kHz Offset		−129		dBc/Hz	
@ 100 kHz Offset		−135		dBc/Hz	
@ 1 MHz Offset		−140		dBc/Hz	
>10 MHz Offset		−148		dBc/Hz	
CLK1 = 622.08 MHz, OUT = 155.52 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−112		dBc/Hz	
@ 100 Hz Offset		−122		dBc/Hz	
@ 1 kHz Offset		−132		dBc/Hz	
@ 10 kHz Offset		−142		dBc/Hz	
@ 100 kHz Offset		−148		dBc/Hz	
@ 1 MHz Offset		−152		dBc/Hz	
>10 MHz Offset		−155		dBc/Hz	
CLK1 = 491.52 MHz, OUT = 245.76 MHz					
Divide Ratio = 2					
@ 10 Hz Offset		−108		dBc/Hz	
@ 100 Hz Offset		−118		dBc/Hz	
@ 1 kHz Offset		−128		dBc/Hz	
@ 10 kHz Offset		−138		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ 1 MHz Offset		−148		dBc/Hz	
>10 MHz Offset		−154		dBc/Hz	
CLK1 = 491.52 MHz, OUT = 122.88 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−118		dBc/Hz	
@ 100 Hz Offset		−129		dBc/Hz	
@ 1 kHz Offset		−136		dBc/Hz	
@ 10 kHz Offset		−147		dBc/Hz	
@ 100 kHz Offset		−153		dBc/Hz	
@ 1 MHz Offset		−156		dBc/Hz	
>10 MHz Offset		−158		dBc/Hz	
CLK1 = 245.76 MHz, OUT = 245.76 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−108		dBc/Hz	
@ 100 Hz Offset		−118		dBc/Hz	
@ 1 kHz Offset		−128		dBc/Hz	
@ 10 kHz Offset		−138		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ 1 MHz Offset		−148		dBc/Hz	
>10 MHz Offset		−155		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK1 = 245.76 MHz, OUT = 122.88 MHz					
Divide Ratio = 2					
@ 10 Hz Offset		−118		dBc/Hz	
@ 100 Hz Offset		−127		dBc/Hz	
@ 1 kHz Offset		−137		dBc/Hz	
@ 10 kHz Offset		−147		dBc/Hz	
@ 100 kHz Offset		−154		dBc/Hz	
@ 1 MHz Offset		−156		dBc/Hz	
>10 MHz Offset		−158		dBc/Hz	
CLK1-TO-CMOS ADDITIVE PHASE NOISE					
CLK1 = 245.76 MHz, OUT = 245.76 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−110		dBc/Hz	
@ 100 Hz Offset		−121		dBc/Hz	
@ 1 kHz Offset		−130		dBc/Hz	
@ 10 kHz Offset		−140		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ 1 MHz Offset		−149		dBc/Hz	
> 10 MHz Offset		−156		dBc/Hz	
CLK1 = 245.76 MHz, OUT = 61.44 MHz					
Divide Ratio = 4					
@ 10 Hz Offset		−122		dBc/Hz	
@ 100 Hz Offset		−132		dBc/Hz	
@ 1 kHz Offset		−143		dBc/Hz	
@ 10 kHz Offset		−152		dBc/Hz	
@ 100 kHz Offset		−158		dBc/Hz	
@ 1 MHz Offset		−160		dBc/Hz	
>10 MHz Offset		−162		dBc/Hz	
CLK1 = 78.6432 MHz, OUT = 78.6432 MHz					
Divide Ratio = 1					
@ 10 Hz Offset		−122		dBc/Hz	
@ 100 Hz Offset		−132		dBc/Hz	
@ 1 kHz Offset		−140		dBc/Hz	
@ 10 kHz Offset		−150		dBc/Hz	
@ 100 kHz Offset		−155		dBc/Hz	
@ 1 MHz Offset		−158		dBc/Hz	
>10 MHz Offset		−160		dBc/Hz	
CLK1 = 78.6432 MHz, OUT = 39.3216 MHz					
Divide Ratio = 2					
@ 10 Hz Offset		−128		dBc/Hz	
@ 100 Hz Offset		−136		dBc/Hz	
@ 1 kHz Offset		−146		dBc/Hz	
@ 10 kHz Offset		−155		dBc/Hz	
@ 100 kHz Offset		−161		dBc/Hz	
>1 MHz Offset		−162		dBc/Hz	

CLOCK OUTPUT ADDITIVE TIME JITTER

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					
CLK1 = 622.08 MHz Any LVPECL (OUT0 to OUT2) = 622.08 MHz Divide Ratio = 1		40		fs rms	BW = 12 kHz – 20 MHz (OC-12)
CLK1 = 622.08 MHz Any LVPECL (OUT0 to OUT2) = 155.52 MHz Divide Ratio = 4		55		fs rms	BW = 12 kHz – 20 MHz (OC-3)
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4		215		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 100 MHz Both LVDS (OUT3, OUT4) = 100 MHz		215		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 50 MHz Both LVDS (OUT3, OUT4) = 50 MHz		222		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 50 MHz Both CMOS (OUT3, OUT4) = 50 MHz (B Outputs Off)		225		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)
CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 50 MHz Both CMOS (OUT3, OUT4) = 50 MHz (B Outputs On)		225		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)
LVDS OUTPUT ADDITIVE TIME JITTER					
CLK1 = 400 MHz LVDS (OUT3) = 100 MHz Divide Ratio = 4		264		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
CLK1 = 400 MHz LVDS (OUT4) = 100 MHz Divide Ratio = 4		319		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
CLK1 = 400 MHz LVDS (OUT3) = 100 MHz Divide Ratio = 4 LVDS (OUT4) = 50 MHz All LVPECL = 50 MHz		395		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz Interferer(s) Interferer(s)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK1 = 400 MHz		395		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
LVDS (OUT4) = 100 MHz					
Divide Ratio = 4					
LVDS (OUT3) = 50 MHz					Interferer(s)
All LVPECL = 50 MHz					Interferer(s)
CLK1 = 400 MHz		367		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
LVDS (OUT3) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT4) = 50 MHz (B Outputs Off)					Interferer(s)
All LVPECL = 50 MHz					Interferer(s)
CLK1 = 400 MHz		367		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
LVDS (OUT4) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT3) = 50 MHz (B Outputs Off)					Interferer(s)
All LVPECL = 50 MHz					Interferer(s)
CLK1 = 400 MHz		548		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
LVDS (OUT3) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT4) = 50 MHz (B Outputs On)					Interferer(s)
All LVPECL = 50 MHz					Interferer(s)
CLK1 = 400 MHz		548		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
LVDS (OUT4) = 100 MHz					
Divide Ratio = 4					
CMOS (OUT3) = 50 MHz (B Outputs On)					Interferer(s)
All LVPECL = 50 MHz					Interferer(s)
CMOS OUTPUT ADDITIVE TIME JITTER					
CLK1 = 400 MHz		275		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
Both CMOS (OUT3, OUT4) = 100 MHz (B Output On)					
Divide Ratio = 4					
CLK1 = 400 MHz		400		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
CMOS (OUT3) = 100 MHz (B Output On)					
Divide Ratio = 4					
All LVPECL = 50 MHz					Interferer(s)
LVDS (OUT4) = 50 MHz					Interferer(s)
CLK1 = 400 MHz		374		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
CMOS (OUT3) = 100 MHz (B Output On)					
Divide Ratio = 4					
All LVPECL = 50 MHz					Interferer(s)
CMOS (OUT4) = 50 MHz (B Output Off)					Interferer(s)
CLK1 = 400 MHz		555		fs rms	Calculated from SNR of ADC method; F_C = 100 MHz with A_{IN} = 170 MHz
CMOS (OUT3) = 100 MHz (B Output On)					
Divide Ratio = 4					
All LVPECL = 50 MHz					Interferer(s)
CMOS (OUT4) = 50 MHz (B Output On)					Interferer(s)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DELAY BLOCK ADDITIVE TIME JITTER[1]					Incremental additive jitter[1]
100 MHz Output					
Delay FS = 1 ns (1600 µA, 1C) Fine Adj. 00000		0.61		ps	
Delay FS = 1 ns (1600 µA, 1C) Fine Adj. 11111		0.73		ps	
Delay FS = 2 ns (800 µA, 1C) Fine Adj. 00000		0.71		ps	
Delay FS = 2 ns (800 µA, 1C) Fine Adj. 11111		1.2		ps	
Delay FS = 3 ns (800 µA, 4C) Fine Adj. 00000		0.86		ps	
Delay FS = 3 ns (800 µA, 4C) Fine Adj. 11111		1.8		ps	
Delay FS = 4 ns (400 µA, 4C) Fine Adj. 00000		1.2		ps	
Delay FS = 4 ns (400 µA, 4C) Fine Adj. 11111		2.1		ps	
Delay FS = 5 ns (200 µA, 1C) Fine Adj. 00000		1.3		ps	
Delay FS = 5 ns (200 µA, 1C) Fine Adj. 11111		2.7		ps	
Delay FS = 11 ns (200 µA, 4C) Fine Adj. 00000		2.0		ps	
Delay FS = 11 ns (200 µA, 4C) Fine Adj. 00100		2.8		ps	

[1] This value is incremental. That is, it is in addition to the jitter of the LVDS or CMOS output without the delay. To estimate the total jitter, the LVDS or CMOS output jitter should be added to this value using the root sum of the squares (RSS) method.

SERIAL CONTROL PORT

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CSB, SCLK (INPUTS)					CSB and SCLK have 30 kΩ internal pull-down resistors
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		110		µA	
Input Logic 0 Current			1	µA	
Input Capacitance		2		pF	
SDIO (WHEN INPUT)					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		10		nA	
Input Logic 0 Current		10		nA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, $1/t_{SCLK}$)			25	MHz	
Pulse Width High, t_{PWH}	16			ns	
Pulse Width Low, t_{PWL}	16			ns	
SDIO to SCLK Setup, t_{DS}	2			ns	
SCLK to SDIO Hold, t_{DH}	1			ns	
SCLK to Valid SDIO and SDO, t_{DV}	6			ns	
CSB to SCLK Setup and Hold, t_S, t_H	2			ns	
CSB Minimum Pulse Width High, t_{PWH}	3			ns	

FUNCTION PIN

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					The FUNCTION pin has a 30 kΩ internal pull-down resistor. This pin should normally be held high. Do not leave NC.
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current		110		µA	
Logic 0 Current			1	µA	
Capacitance		2		pF	
RESET TIMING					
Pulse Width Low	50			ns	
SYNC TIMING					
Pulse Width Low	1.5			High speed clock cycles	High speed clock is CLK1 or CLK2, whichever is being used for distribution.

SYNC STATUS PIN

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					
Output Voltage High (V_{OH})	2.7			V	
Output Voltage Low (V_{OL})			0.4	V	

POWER

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-UP DEFAULT MODE POWER DISSIPATION		550	600	mW	Power-up default state; does not include power dissipated in output load resistors. No clock.
POWER DISSIPATION			800	mW	All outputs on. Three LVPECL outputs @ 800 MHz, two CMOS out @ 62 MHz (5 pF load). Does not include power dissipated in external resistors.
			850	mW	All outputs on. Three LVPECL outputs @ 800 MHz, two CMOS out @ 125 MHz (5 pF load). Does not include power dissipated in external resistors.
Full Sleep Power-Down		35	60	mW	Maximum sleep is entered by setting 0Ah<1:0> = 01b and 58h<4> = 1b. This powers off all band gap references. Does not include power dissipated in terminations.
Power-Down (PDB)		60	80	mW	Set FUNCTION pin for PDB operation by setting 58h<6:5> = 11b. Pull PDB low. Does not include power dissipated in terminations.
POWER DELTA					
CLK1, CLK2 Power-Down	10	15	25	mW	
Divider, DIV 2 – 32 to Bypass	23	27	33	mW	For each divider.
LVPECL Output Power-Down (PD2, PD3)	50	65	75	mW	For each output. Does not include dissipation in termination (PD2 only).
LVDS Output Power-Down	80	92	110	mW	For each output.
CMOS Output Power-Down (Static)	56	70	85	mW	For each output. Static (no clock).
CMOS Output Power-Down (Dynamic)	115	150	190	mW	For each CMOS output, single-ended. Clocking at 62 MHz with 5 pF load.
CMOS Output Power-Down (Dynamic)	125	165	210	mW	For each CMOS output, single-ended. Clocking at 125 MHz with 5 pF load.
Delay Block Bypass	20	24	60	mW	Vs. delay block operation at 1 ns fs with maximum delay; output clocking at 25 MHz.

TIMING DIAGRAMS

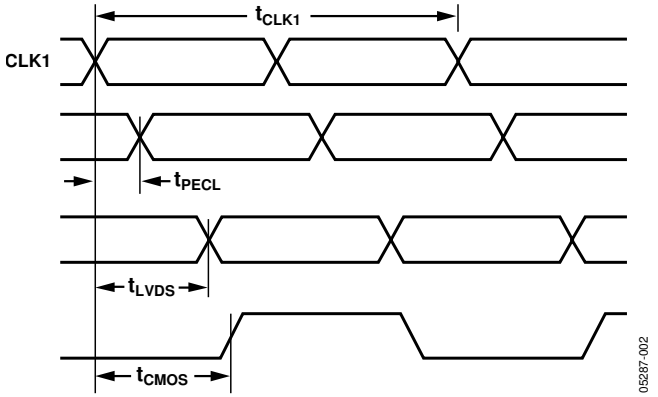

Figure 2. CLK1/CLK1B to Clock Output Timing, DIV = 1 Mode

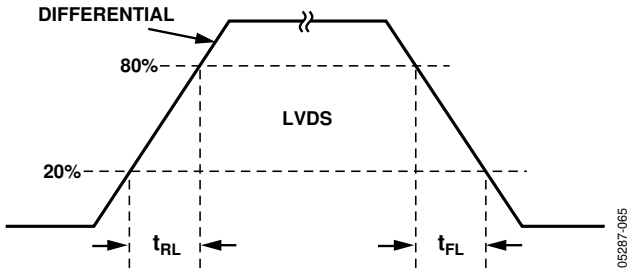

Figure 4. LVDS Timing, Differential

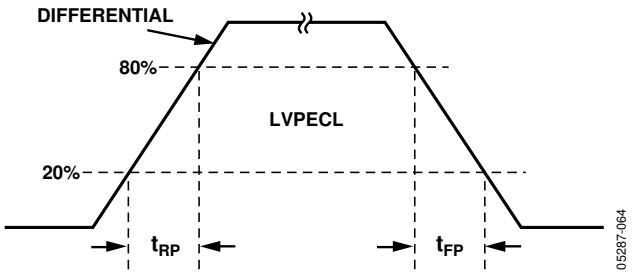

Figure 3. LVPECL Timing, Differential

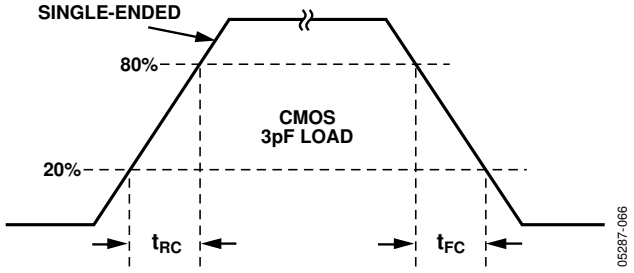

Figure 5. CMOS Timing, Single-Ended, 3 pF Load

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter or Pin	With Respect to	Min	Max	Unit
VS	GND	−0.3	+3.6	V
DSYNC/DSYNCB	GND	−0.3	V_S + 0.3	V
RSET	GND	−0.3	V_S + 0.3	V
CLK1, CLK1B, CLK2, CLK2B	GND	−0.3	V_S + 0.3	V
CLK1	CLK1B	−1.2	+1.2	V
CLK2	CLK2B	−1.2	+1.2	V
SCLK, SDIO, SDO, CSB	GND	−0.3	V_S + 0.3	V
OUT0, OUT1, OUT2, OUT3, OUT4	GND	−0.3	V_S + 0.3	V
FUNCTION	GND	−0.3	V_S + 0.3	V
SYNC STATUS	GND	−0.3	V_S + 0.3	V
Junction Temperature			150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			300	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance[1]

48-Lead LFCSP
θ_{JA} = 28.5°C/W

[1] Thermal impedance measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-7.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

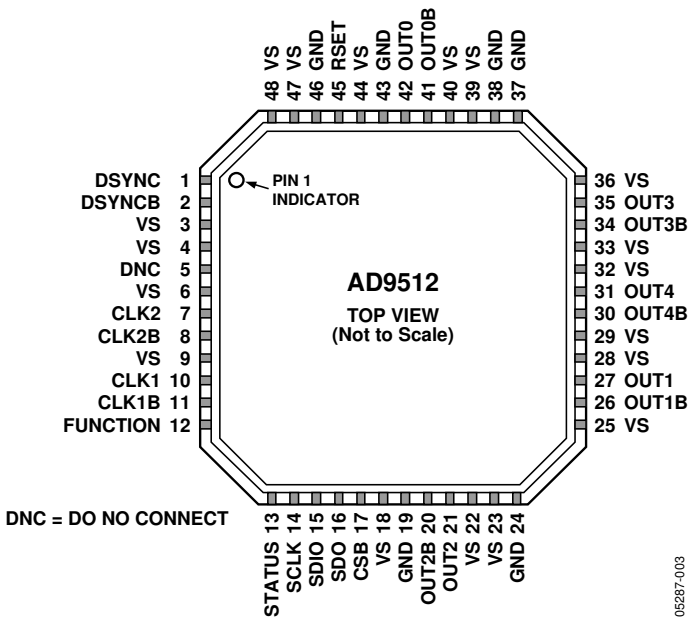

Figure 6. 48-Lead LFCSP Pin Configuration

Note that the exposed paddle on this package is an electrical connection as well as a thermal enhancement. For the device to function properly, the paddle must be attached to ground, GND.

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DSYNC	Detect Sync. Used for multichip synchronization.
2	DSYNCB	Detect Sync Complement. Used for multichip synchronization.
3, 4, 6, 9, 18, 22, 23, 25, 28, 29, 32, 33, 36, 39, 40, 44, 47, 48	VS	Power Supply (3.3 V).
5	DNC	Do Not Connect.
7	CLK2	Clock Input.
8	CLK2B	Complementary Clock Input. Used in conjunction with CLK2.
10	CLK1	Clock Input.
11	CLK1B	Complementary Clock Input. Used in conjunction with CLK1.
12	FUNCTION	Multipurpose Input. Can be programmed as a reset (RESETB), sync (SYNCB), or power-down (PDB) pin.
13	STATUS	Output Used to Monitor the Status of Multichip Synchronization.
14	SCLK	Serial Data Clock.
15	SDIO	Serial Data I/O.
16	SDO	Serial Data Output.
17	CSB	Serial Port Chip Select.
19, 24, 37, 38, 43, 46	GND	Ground.
20	OUT2B	Complementary LVPECL Output.
21	OUT2	LVPECL Output.
26	OUT1B	Complementary LVPECL Output.
27	OUT1	LVPECL Output.
30	OUT4B	Complementary LVDS/Inverted CMOS Output. OUT4 includes a delay block.
31	OUT4	LVDS/CMOS Output. OUT4 includes a delay block.
34	OUT3B	Complementary LVDS/Inverted CMOS Output.
35	OUT3	LVDS/CMOS Output.
41	OUT0B	Complementary LVPECL Output.
42	OUT0	LVPECL Output.
45	RSET	Current Set Resistor to Ground. Nominal value = 4.12 kΩ.

Note that the exposed paddle on this package is an electrical connection as well as a thermal enhancement. For the device to function properly, the paddle must be attached to ground, GND.

TERMINOLOGY

Phase Jitter and Phase Noise
An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0 degrees to 360 degrees for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in dB) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter
Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings is seen to vary. In a square wave, the time jitter is seen as a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Since these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the SNR and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise
It is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources has been subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contribute their own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise.

Additive Time Jitter
It is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources has been subtracted. This makes it possible to predict the degree to which the device will impact the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contribute their own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

TYPICAL PERFORMANCE CHARACTERISTICS

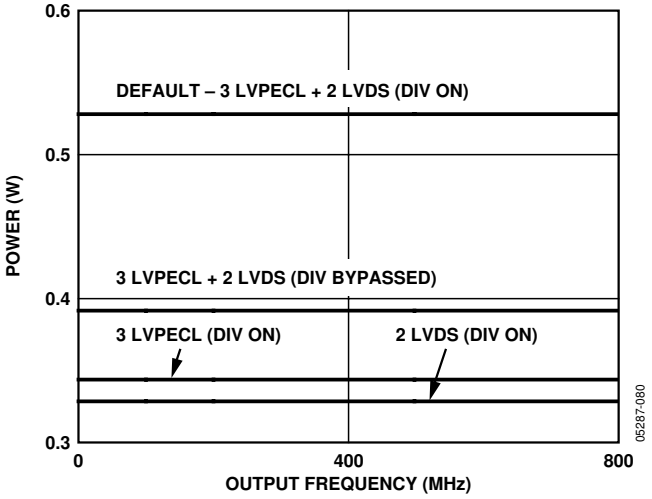

Figure 7. Power vs. Frequency—LVPECL, LVDS

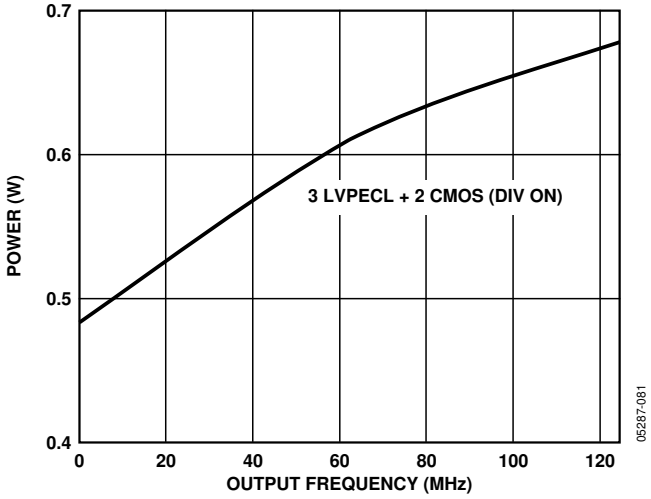

Figure 9. Power vs. Frequency—LVPECL, CMOS

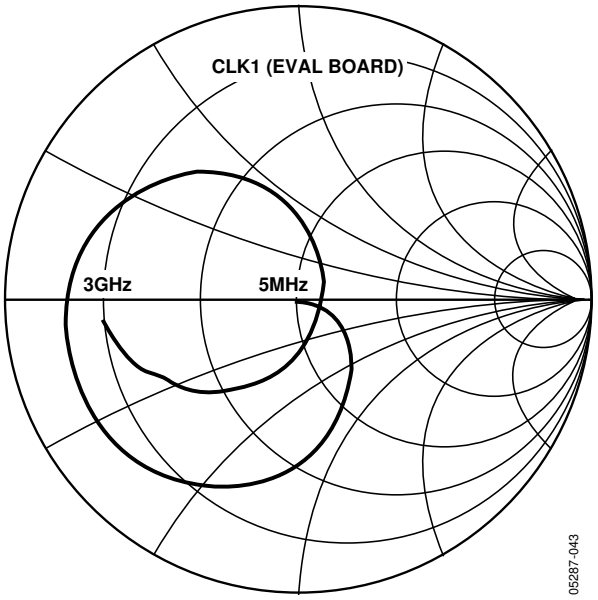

Figure 8. CLK1 Smith Chart (Evaluation Board)

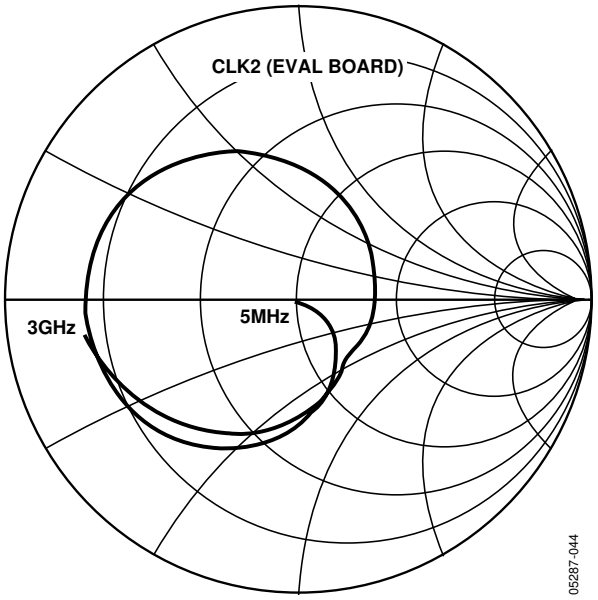

Figure 10. CLK2 Smith Chart (Evaluation Board)

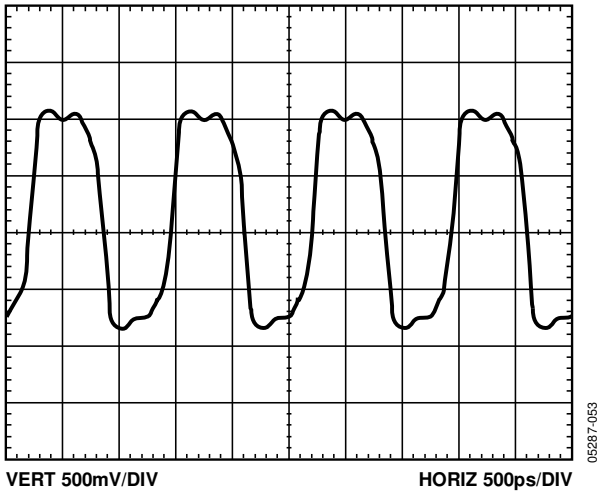

Figure 11. LVPECL Differential Output @ 800 MHz

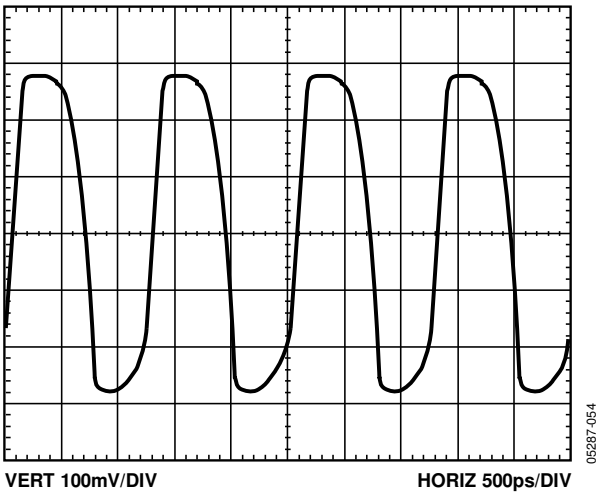

Figure 12. LVDS Differential Output @ 800 MHz

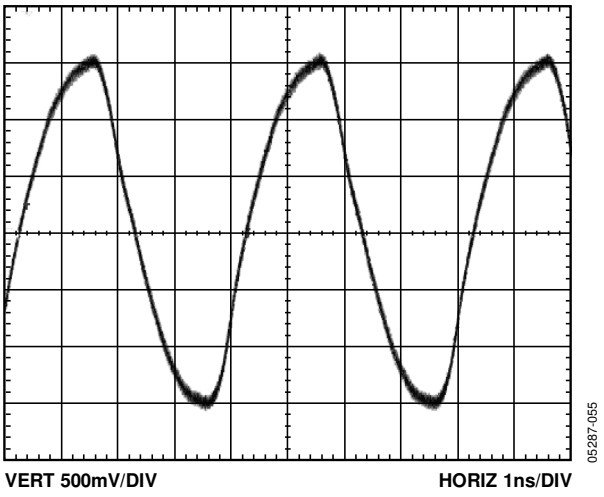

Figure 13. CMOS Single-Ended Output @ 250 MHz with 10 pF Load

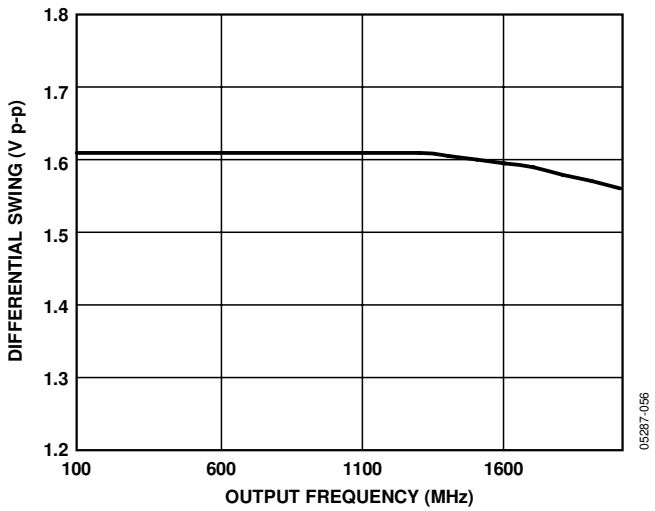

Figure 14. LVPECL Differential Output Swing vs. Frequency

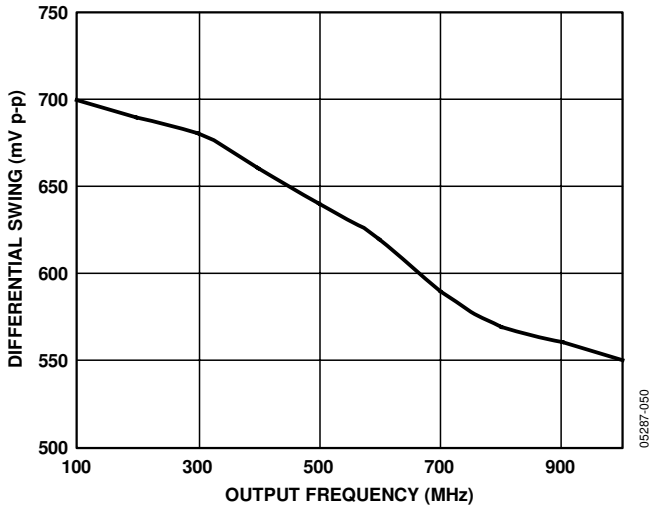

Figure 15. LVDS Differential Output Swing vs. Frequency

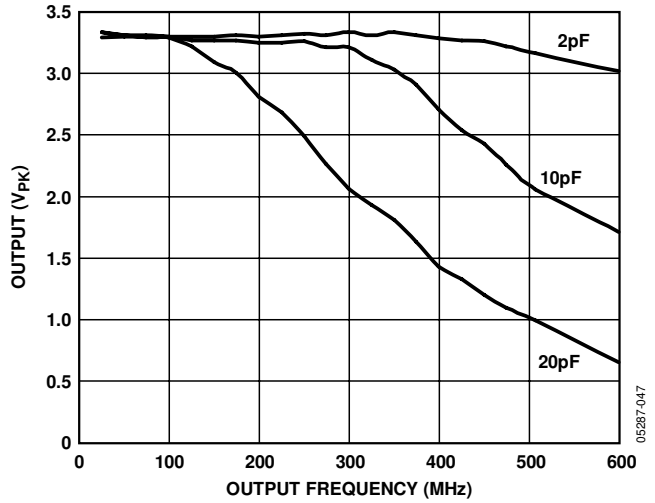

Figure 16. CMOS Single-Ended Output Swing vs. Frequency and Load

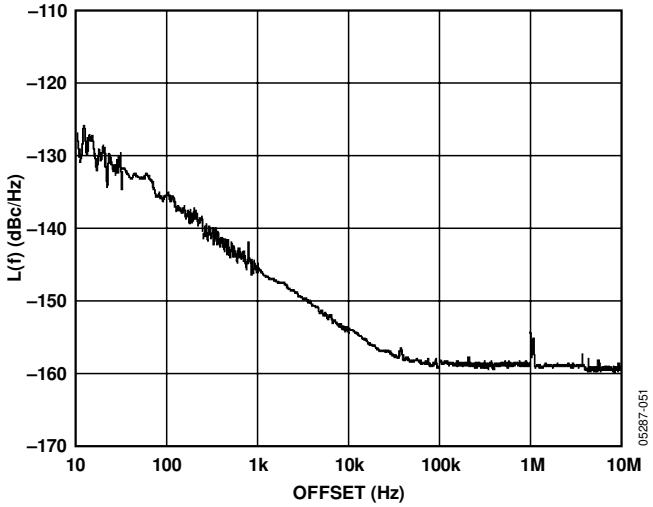

Figure 17. Additive Phase Noise—LVPECL DIV1, 245.76 MHz Distribution Section Only

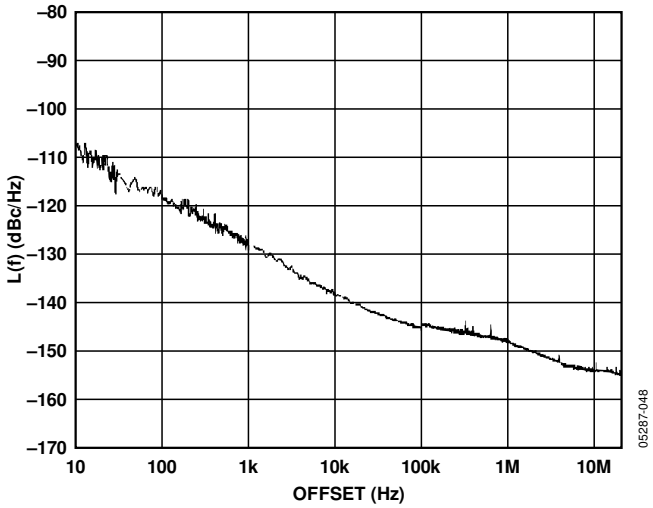

Figure 18. Additive Phase Noise—LVDS DIV1, 245.76 MHz

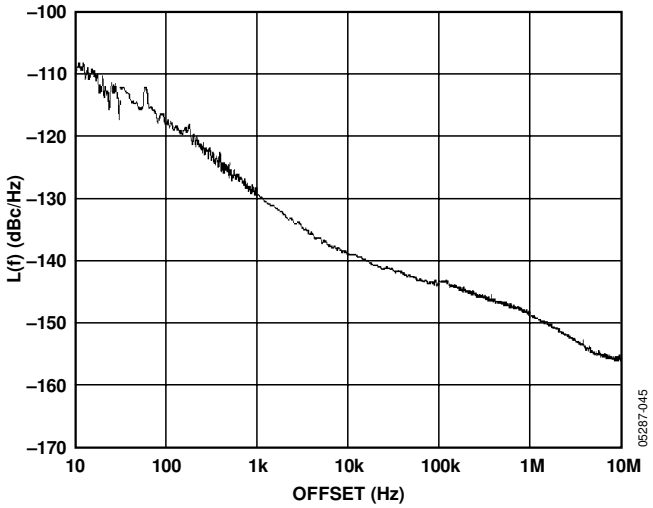

Figure 19. Additive Phase Noise—CMOS DIV1, 245.76 MHz

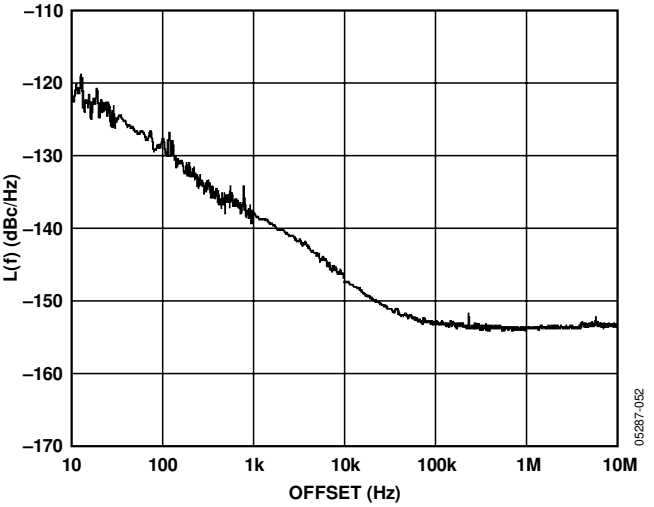

Figure 20. Additive Phase Noise—LVPECL DIV1, 622.08 MHz

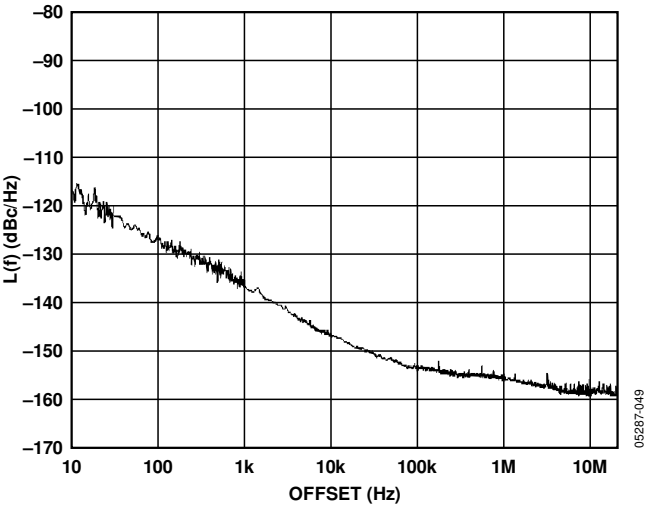

Figure 21. Additive Phase Noise—LVDS DIV2, 122.88 MHz

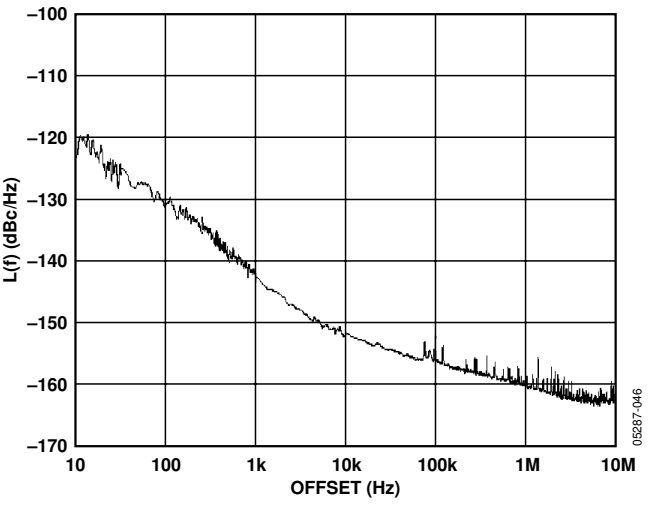

Figure 22. Additive Phase Noise—CMOS DIV4, 61.44 MHz

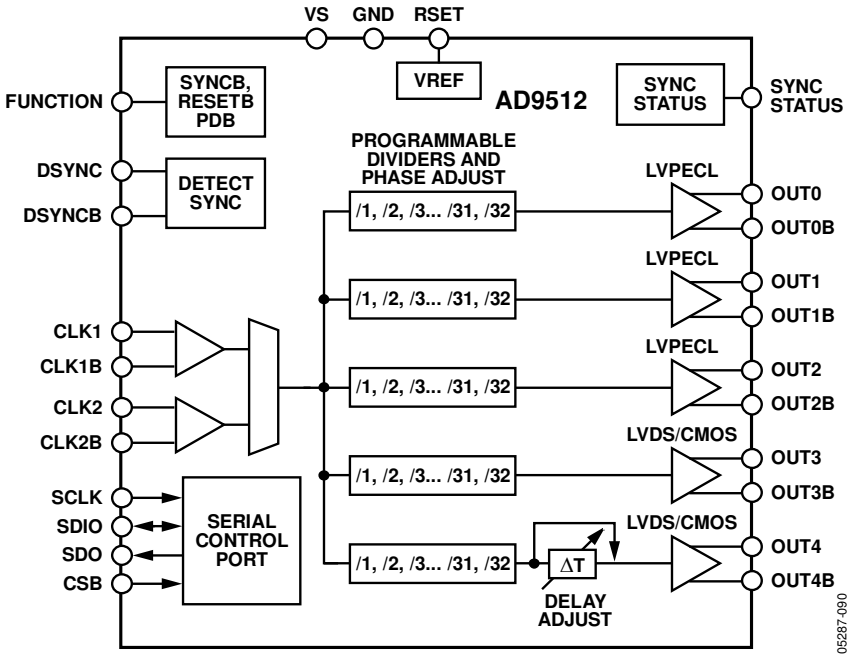

Figure 23. Functional Block Diagram Showing Maximum Frequencies

FUNCTIONAL DESCRIPTION

OVERALL

Figure 23 shows a block diagram of the AD9512. The AD9512 accepts inputs on either of two clock inputs (CLK1 or CLK2). This clock can be divided by any integer value from 1 to 32. The duty cycle and relative phase of the outputs can be selected. There are three LVPECL outputs (OUT0, OUT1, OUT2) and two outputs that can be either LVDS or CMOS level outputs (OUT3, OUT4). OUT4 can also make use of a variable delay block.

The AD9512 provides clock distribution function only; there is no clock clean-up. The jitter of the input clock signal is passed along directly to the distribution section and can dominate at the clock outputs.

See Figure 24 for the equivalent circuit of CLK1 and CLK2.

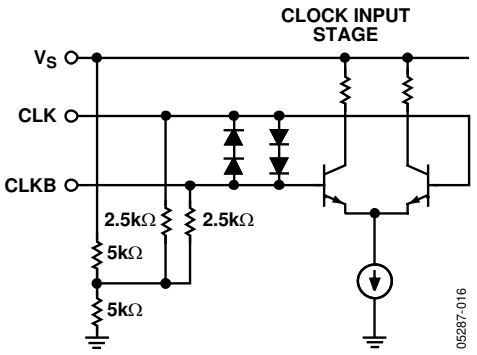

Figure 24. CLK1, CLK2 Equivalent Input Circuit

FUNCTION PIN

The FUNCTION pin (Pin 12) has three functions that are selected by the value in Register 58h<6:5>. There is an internal 30 kΩ pull-down resistor on this pin.

RESETB: 58h<6:5> = 00b (Default)

In its default mode, the FUNCTION pin acts as RESETB, which generates an asynchronous reset or hard reset when pulled low. The resulting reset writes the default values into the serial control port buffer registers as well as loading them into the chip control registers. The AD9512 immediately resumes operation according to the default values. When the pin is taken high again, an asynchronous sync is issued (see the SYNCB: 58h<6:5> = 01b section).

SYNCB: 58h<6:5> = 01b

The FUNCTION pin can be used to cause a synchronization or alignment of phase among the various clock outputs. The synchronization applies only to clock outputs that:

- are not powered down
- the divider is not masked (no sync = 0)
- are not bypassed (bypass = 0)

SYNCB is level and rising edge sensitive. When SYNCB is low, the set of affected outputs are held in a predetermined state, defined by each divider's start high bit. On a rising edge, the dividers begin after a predefined number of fast clock cycles (fast clock is the selected clock input, CLK1 or CLK2) as determined by the values in the divider's phase offset bits.

The SYNCB application of the FUNCTION pin is always active, regardless of whether the pin is also assigned to perform reset or power-down. When the SYNCB function is selected, the FUNCTION pin does not act as either RESETB or PDB.

PDB: 58h<6:5> = 11b

The FUNCTION pin can also be programmed to work as an asynchronous full power-down, PDB. Even in this full power-down mode, there is still some residual V_S current because some on-chip references continue to operate. In PDB mode, the FUNCTION pin is active low. The chip remains in a power-down state until PDB is returned to logic high. The chip returns to the settings programmed prior to the power-down.

See the Chip Power-Down or Sleep Mode—PDB section for more details on what occurs during a PDB initiated power-down.

DSYNC AND DSYNCB PINS

The DSYNC and DSYNCB pins (Pin 1 and Pin 2) are used when the AD9512 is used in a multichip synchronized configuration (see the Multichip Synchronization section).

CLOCK INPUTS

Two clock inputs (CLK1, CLK2) are available for use on the AD9512. CLK1 and CLK2 can accept inputs up to 1600 MHz. See Figure 24 for the CLK1 and CLK2 equivalent input circuit.

The clock inputs are fully differential and self-biased. The signal should be ac-coupled using capacitors. If a single-ended input must be used, this can be accommodated by ac coupling to one side of the differential input only. The other side of the input should be bypassed to a quiet ac ground by a capacitor.

The unselected clock input (either CLK1 or CLK2) should be powered down to eliminate any possibility of unwanted crosstalk between the selected clock input and the unselected clock input.