



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## FEATURES

- Low phase noise, phase-locked loop (PLL)
  - On-chip VCO tunes from 2.30 GHz to 2.65 GHz
  - External VCO/VCXO to 2.4 GHz optional
  - 1 differential or 2 single-ended reference inputs
  - Reference monitoring capability
  - Automatic revertive and manual reference switchover/holdover modes
  - Accepts LVPECL, LVDS, or CMOS references to 250 MHz
  - Programmable delays in path to PFD
  - Digital or analog lock detect, selectable
- 6 pairs of 1.6 GHz LVPECL outputs
  - Each output pair shares a 1-to-32 divider with coarse phase delay
  - Additive output jitter: 225 fs rms
  - Channel-to-channel skew paired outputs of <10 ps
- 4 pairs of 800 MHz LVDS clock outputs
  - Each output pair shares two cascaded 1-to-32 dividers with coarse phase delay
  - Additive output jitter: 275 fs rms
  - Fine delay adjust ( $\Delta t$ ) on each LVDS output
- Each LVDS output can be reconfigured as two 250 MHz CMOS outputs
- Automatic synchronization of all outputs on power-up
- Manual output synchronization available
- 64-lead LFCSP

## APPLICATIONS

- Low jitter, low phase noise clock distribution
- 10/40/100 Gb/sec networking line cards, including SONET, Synchronous Ethernet, OTU2/3/4
- Forward error correction (G.710)
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- High performance wireless transceivers
- ATE and high performance instrumentation

## GENERAL DESCRIPTION

The AD9516-1<sup>1</sup> provides a multi-output clock distribution function with subpicosecond jitter performance, along with an on-chip PLL and VCO. The on-chip VCO tunes from 2.30 GHz to 2.65 GHz. Optionally, an external VCO/VCXO of up to 2.4 GHz can be used.

The AD9516-1 emphasizes low jitter and phase noise to maximize data converter performance, and it can benefit other applications with demanding phase noise and jitter requirements.

## FUNCTIONAL BLOCK DIAGRAM

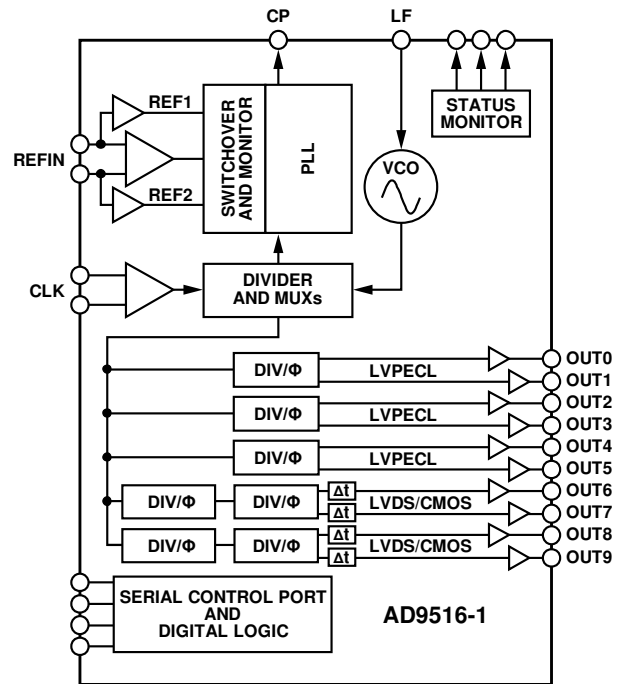


Figure 1.

The AD9516-1 features six LVPECL outputs (in three pairs) and four LVDS outputs (in two pairs). Each LVDS output can be reconfigured as two CMOS outputs. The LVPECL outputs operate to 1.6 GHz, the LVDS outputs operate to 800 MHz, and the CMOS outputs operate to 250 MHz.

Each pair of outputs has dividers that allow both the divide ratio and coarse delay (or phase) to be set. The range of division for the LVPECL outputs is 1 to 32. The LVDS/CMOS outputs allow a range of divisions up to a maximum of 1024.

The AD9516-1 is available in a 64-lead LFCSP and can be operated from a single 3.3 V supply. An external VCO, which requires an extended voltage range, can be accommodated by connecting the charge pump supply (VCP) to 5 V. A separate LVPECL power supply can be from 2.5 V to 3.3 V (nominal).

The AD9516-1 is specified for operation over the industrial range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

<sup>1</sup> AD9516 is used throughout to refer to all the members of the AD9516 family. However, when AD9516-1 is used, it refers to that specific member of the AD9516 family.

# AD9516-1\* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

---

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD9516-1 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-0974: Multicarrier TD-SCMA Feasibility
- AN-0983: Introduction to Zero-Delay Clock Timing Techniques
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal

### Data Sheet

- AD9516-1: 14-Output Clock Generator with Integrated 2.5 GHz VCO Data Sheet

### User Guides

- UG-075: AD9516-x, AD9517-x, and AD9518-x Evaluation Board User Guide
- UG-093: Evaluation Board User Guide for the Dual, Continuous Time Sigma-Delta Modulator

## TOOLS AND SIMULATIONS

- ADIsimCLK Design and Evaluation Software
- AD9516 IBIS Models

## REFERENCE DESIGNS

- CN0243

## REFERENCE MATERIALS

### Product Selection Guide

- RF Source Booklet

### Technical Articles

- ADI Buys Korean Mobile TV Chip Maker
- Design A Clock-Distribution Strategy With Confidence
- Improved DDS Devices Enable Advanced Comm Systems
- Low-power direct digital synthesizer cores enable high level of integration
- Speedy A/Ds Demand Stable Clocks
- Understand the Effects of Clock Jitter and Phase Noise on Sampled Systems

## DESIGN RESOURCES

- AD9516-1 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD9516-1 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

## TABLE OF CONTENTS

Features .....	1	Thermal Resistance .....	16
Applications .....	1	ESD Caution .....	16
General Description .....	1	Pin Configuration and Function Descriptions .....	17
Functional Block Diagram .....	1	Typical Performance Characteristics .....	19
Revision History .....	3	Terminology .....	25
Specifications .....	4	Detailed Block Diagram .....	26
Power Supply Requirements .....	4	Theory of Operation .....	27
PLL Characteristics .....	4	Operational Configurations .....	27
Clock Inputs .....	6	Digital Lock Detect (DLD) .....	36
Clock Outputs .....	6	Clock Distribution .....	40
Timing Characteristics .....	7	Reset Modes .....	48
Clock Output Additive Phase Noise (Distribution Only; VCO Divider Not Used) .....	8	Power-Down Modes .....	49
Clock Output Absolute Phase Noise (Internal VCO Used) .....	9	Serial Control Port .....	50
Clock Output Absolute Time Jitter (Clock Generation Using Internal VCO) .....	10	Serial Control Port Pin Descriptions .....	50
Clock Output Absolute Time Jitter (Clock Cleanup Using Internal VCO) .....	10	General Operation of Serial Control Port .....	50
Clock Output Absolute Time Jitter (Clock Generation Using External VCXO) .....	10	The Instruction Word (16 Bits) .....	51
Clock Output Additive Time Jitter (VCO Divider Not Used) .....	11	MSB/LSB First Transfers .....	51
Clock Output Additive Time Jitter (VCO Divider Used) .....	11	Thermal Performance .....	54
Delay Block Additive Time Jitter .....	12	Register Map Overview .....	55
Serial Control Port .....	12	Register Map Descriptions .....	59
$\overline{\text{PD}}$ , $\overline{\text{RESET}}$ , and $\overline{\text{SYNC}}$ Pins .....	13	Applications Information .....	77
LD, STATUS, and REFMON Pins .....	13	Frequency Planning Using the AD9516 .....	77
Power Dissipation .....	14	Using the AD9516 Outputs for ADC Clock Applications .....	77
Timing Diagrams .....	15	LVPECL Clock Distribution .....	78
Absolute Maximum Ratings .....	16	LVDS Clock Distribution .....	78
		CMOS Clock Distribution .....	79
		Outline Dimensions .....	80
		Ordering Guide .....	80

**REVISION HISTORY****2/13—Rev. B to Rev. C**

Changes to Register 0x140 to Register 0x143 Default Values; Table 52 .....	56
Changes to Register 0x140 to Register 0x143 Default Values; Table 57 .....	71
Updated Outline Dimensions.....	80

**1/12—Rev. A to Rev. B**

Changes to 0x232 Description Column, Table 62 .....	76
---	----

**12/10—Rev. 0 to Rev. A**

Changes to Features, Applications, and General Description.....	1
Change to CPRSET Pin Resistor Parameter in Table 1 .....	4
Change to P = 2 DM (2/3) Parameter in Table 2 .....	5
Changes to Table 4 .....	6
Changes to $V_{CP}$ Supply Parameter in Table 17.....	14
Change to $\theta_{JA}$ Value and Endnote in Table 19 .....	16
Added Exposed Paddle Notation to Figure 6; Changes to Table 20.....	17
Added Figure 41; Renumbered Sequentially.....	24
Change to High Frequency Clock Distribution—CLK or External VCO > 1600 MHz Section; Change to Table 22.....	27
Changes to Table 24 .....	29
Change to Configuration and Register Settings Section.....	31
Change to Phase Frequency Detector (PFD) Section .....	32
Changes to Charge Pump (CP), On-Chip VCO, PLL External Loop Filter, and PLL Reference Inputs Sections .....	33
Change to Figure 47; Added Figure 48.....	33

Changes to Reference Switchover and VCXO/VCO Feedback Divider N—P, A, B, R Sections .....	34
Changes to Table 28 .....	35
Change to Holdover Section.....	37
Changes to VCO Calibration Section.....	39
Changes to Clock Distribution Section.....	40
Added Endnote to Table 34 .....	41
Changes to Channel Dividers—LVDS/CMOS Outputs Section; Added Endnote to Table 39 .....	43
Changes to Write Section.....	50
Change to the Instruction Word (16 Bits) Section .....	51
Change to Figure 65 .....	52
Added Thermal Performance Section.....	54
Changes to Register Address 0x003 in Table 52.....	55
Changes to Table 53 .....	59
Changes to Table 54 .....	60
Changes to Table 55 .....	66
Changes to Table 56 .....	68
Changes to Table 57 .....	71
Changes to Table 58 .....	73
Changes to Table 59 .....	74
Changes to Table 60 and Table 61 .....	76
Added Frequency Planning Using the AD9516 Section.....	77
Changes to Figure 71 and Figure 73; Added Figure 72.....	78
Changes to LVPECL Clock Distribution and LVDS Clock Distribution Sections .....	78
Updated Outline Dimensions.....	80

**4/07—Revision 0: Initial Version**

## SPECIFICATIONS

Typical is given for  $V_S = V_{S\_LVPECL} = 3.3 \text{ V} \pm 5\%$ ;  $V_S \leq V_{CP} \leq 5.25 \text{ V}$ ;  $T_A = 25^\circ\text{C}$ ;  $R_{SET} = 4.12 \text{ k}\Omega$ ;  $CP_{RSET} = 5.1 \text{ k}\Omega$ , unless otherwise noted. Minimum and maximum values are given over full  $V_S$  and  $T_A$  ( $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) variation.

### POWER SUPPLY REQUIREMENTS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$V_S$	3.135	3.3	3.465	V	$3.3 \text{ V} \pm 5\%$
$V_{S\_LVPECL}$	2.375		$V_S$	V	Nominally 2.5 V to $3.3 \text{ V} \pm 5\%$
$V_{CP}$	$V_S$		5.25	V	Nominally 3.3 V to $5.0 \text{ V} \pm 5\%$
RSET Pin Resistor		4.12		k $\Omega$	Sets internal biasing currents; connect to ground
CPRSET Pin Resistor	2.7	5.1	10	k $\Omega$	Sets internal CP current range, nominally 4.8 mA ( $CP\_I_{sb} = 600 \mu\text{A}$ ); actual current can be calculated by: $CP\_I_{sb} = 3.06/CPRSET$ ; connect to ground
BYPASS Pin Capacitor		220		nF	Bypass for internal LDO regulator; necessary for LDO stability; connect to ground

### PLL CHARACTERISTICS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO (ON-CHIP)					
Frequency Range	2300		2650	MHz	See Figure 15
VCO Gain ( $K_{VCO}$ )		50		MHz/V	See Figure 10
Tuning Voltage ( $V_T$ )	0.5		$V_{CP} - 0.5$	V	$V_{CP} \leq V_S$ when using internal VCO; outside of this range, the CP spurs may increase due to CP up/down mismatch
Frequency Pushing (Open-Loop)		1		MHz/V	
Phase Noise at 100 kHz Offset		-105		dBc/Hz	$f = 2475 \text{ MHz}$
Phase Noise at 1 MHz Offset		-124		dBc/Hz	$f = 2475 \text{ MHz}$
REFERENCE INPUTS					
Differential Mode ( $\overline{REFIN}$ , $\overline{REFIN}$ )					Differential mode (can accommodate single-ended input by ac grounding undriven input)
Input Frequency	0		250	MHz	Frequencies below about 1 MHz should be dc-coupled; be careful to match $V_{CM}$ (self-bias voltage)
Input Sensitivity		250		mV p-p	PLL figure of merit (FOM) increases with increasing slew rate; see Figure 14
Self-Bias Voltage, $\overline{REFIN}$	1.35	1.60	1.75	V	Self-bias voltage of $\overline{REFIN}^1$
Self-Bias Voltage, $\overline{REFIN}$	1.30	1.50	1.60	V	Self-bias voltage of $\overline{REFIN}^1$
Input Resistance, $\overline{REFIN}$	4.0	4.8	5.9	k $\Omega$	Self-biased <sup>1</sup>
Input Resistance, $\overline{REFIN}$	4.4	5.3	6.4	k $\Omega$	Self-biased <sup>1</sup>
Dual Single-Ended Mode ( $\overline{REF1}$ , $\overline{REF2}$ )					Two single-ended CMOS-compatible inputs
Input Frequency (AC-Coupled)	20		250	MHz	Slew rate > 50 V/ $\mu\text{s}$
Input Frequency (DC-Coupled)	0		250	MHz	Slew rate > 50 V/ $\mu\text{s}$ ; CMOS levels
Input Sensitivity (AC-Coupled)		0.8		V p-p	Should not exceed $V_S$ p-p
Input Logic High	2.0			V	
Input Logic Low			0.8	V	
Input Current	-100		+100	$\mu\text{A}$	
Input Capacitance		2		pF	Each pin, $\overline{REFIN}/\overline{REFIN}$ ( $\overline{REF1}/\overline{REF2}$ )
PHASE/FREQUENCY DETECTOR (PFD)					
PFD Input Frequency			100	MHz	Antibacklash pulse width = 1.3 ns, 2.9 ns
			45	MHz	Antibacklash pulse width = 6.0 ns
Antibacklash Pulse Width		1.3		ns	Register 0x017[1:0] = 01b
		2.9		ns	Register 0x017[1:0] = 00b; Register 0x017[1:0] = 11b
		6.0		ns	Register 0x017[1:0] = 10b

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CHARGE PUMP (CP)					
$I_{CP}$ Sink/Source					Programmable
High Value		4.8		mA	With $CP_{RSET} = 5.1 \text{ k}\Omega$
Low Value		0.60		mA	
Absolute Accuracy		2.5		%	$CP_V = V_{CP}/2$
$CP_{RSET}$ Range		2.7/10		$\text{k}\Omega$	
$I_{CP}$ High Impedance Mode Leakage		1		nA	
Sink-and-Source Current Matching		2		%	$0.5 < CP_V < V_{CP} - 0.5 \text{ V}$
$I_{CP}$ vs. $CP_V$		1.5		%	$0.5 < CP_V < V_{CP} - 0.5 \text{ V}$
$I_{CP}$ vs. Temperature		2		%	$CP_V = V_{CP}/2$
PRESCALER (PART OF N DIVIDER)					See the VCXO/VCO Feedback Divider N—P, A, B, R section
Prescaler Input Frequency					
P = 1 FD			300	MHz	
P = 2 FD			600	MHz	
P = 3 FD			900	MHz	
P = 2 DM (2/3)			200	MHz	
P = 4 DM (4/5)			1000	MHz	
P = 8 DM (8/9)			2400	MHz	
P = 16 DM (16/17)			3000	MHz	
P = 32 DM (32/33)			3000	MHz	
Prescaler Output Frequency			300	MHz	A, B counter input frequency (prescaler input frequency divided by P)
PLL DIVIDER DELAYS					Register 0x019: R, Bits[5:3]; N, Bits[2:0]; see Table 54
000		Off		ps	
001		330		ps	
010		440		ps	
011		550		ps	
100		660		ps	
101		770		ps	
110		880		ps	
111		990		ps	
NOISE CHARACTERISTICS					
In-Band Phase Noise of the Charge Pump/Phase Frequency Detector (In-Band Is Within the LBW of the PLL)					The PLL in-band phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting $20\log(N)$ (where N is the value of the N divider)
At 500 kHz PFD Frequency		-165		dBc/Hz	
At 1 MHz PFD Frequency		-162		dBc/Hz	
At 10 MHz PFD Frequency		-151		dBc/Hz	
At 50 MHz PFD Frequency		-143		dBc/Hz	
PLL Figure of Merit (FOM)		-220		dBc/Hz	Reference slew rate $> 0.25 \text{ V/ns}$ ; $FOM + 10\log(f_{PFD})$ is an approximation of the PFD/CP in-band phase noise (in the flat region) inside the PLL loop bandwidth; when running closed-loop, the phase noise, as observed at the VCO output, is increased by $20\log(N)$
PLL DIGITAL LOCK DETECT WINDOW <sup>2</sup>					Signal available at LD, STATUS, and REFMON pins when selected by appropriate register settings
Required to Lock (Coincidence of Edges)					Selected by Register 0x017[1:0] and Register 0x018[4]
Low Range (ABP 1.3 ns, 2.9 ns)		3.5		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		7.5		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6.0 ns)		3.5		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b
To Unlock After Lock (Hysteresis) <sup>2</sup>					
Low Range (ABP 1.3 ns, 2.9 ns)		7		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		15		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6.0 ns)		11		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b

<sup>1</sup> REF $\overline{IN}$  and  $\overline{REFIN}$  self-bias points are offset slightly to avoid chatter on an open input condition.

<sup>2</sup> For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the unlock-after-lock time.

## CLOCK INPUTS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUTS (CLK, $\overline{\text{CLK}}$ )					Differential input
Input Frequency	0 <sup>1</sup>		2.4	GHz	High frequency distribution (VCO divider)
	0 <sup>1</sup>		1.6	GHz	Distribution only (VCO divider bypassed)
Input Sensitivity, Differential		150		mV p-p	Measured at 2.4 GHz; jitter performance is improved with slew rates > 1 V/ns
Input Level, Differential			2	V p-p	Larger voltage swings may turn on the protection diodes and may degrade jitter performance
Input Common-Mode Voltage, $V_{\text{CM}}$	1.3	1.57	1.8	V	Self-biased; enables ac coupling
Input Common-Mode Range, $V_{\text{CMR}}$	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled
Input Sensitivity, Single-Ended		150		mV p-p	CLK ac-coupled; $\overline{\text{CLK}}$ ac-bypassed to RF ground
Input Resistance	3.9	4.7	5.7	k $\Omega$	Self-biased
Input Capacitance		2		pF	

<sup>1</sup> Below about 1 MHz, the input should be dc-coupled. Care should be taken to match  $V_{\text{CM}}$ .

## CLOCK OUTPUTS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					Termination = 50 $\Omega$ to $V_{\text{S}} - 2$ V
OUT0, OUT1, OUT2, OUT3, OUT4, OUT5					Differential (OUT, $\overline{\text{OUT}}$ )
Output Frequency, Maximum	2950			MHz	Using direct to output; see Figure 25 for peak-to-peak differential amplitude
Output High Voltage ( $V_{\text{OH}}$ )	$V_{\text{S}} - 1.12$	$V_{\text{S}} - 0.98$	$V_{\text{S}} - 0.84$	V	
Output Low Voltage ( $V_{\text{OL}}$ )	$V_{\text{S}} - 2.03$	$V_{\text{S}} - 1.77$	$V_{\text{S}} - 1.49$	V	
Output Differential Voltage ( $V_{\text{OD}}$ )	550	790	980	mV	$V_{\text{OH}} - V_{\text{OL}}$ for each leg of a differential pair for default amplitude setting with driver not toggling; see Figure 25 for variation over frequency
LVDS CLOCK OUTPUTS					Differential termination 100 $\Omega$ at 3.5 mA
OUT6, OUT7, OUT8, OUT9					Differential (OUT, $\overline{\text{OUT}}$ )
Output Frequency			800	MHz	The AD9516 outputs toggle at higher frequencies, but the output amplitude may not meet the $V_{\text{OD}}$ specification; see Figure 26
Differential Output Voltage ( $V_{\text{OD}}$ )	247	360	454	mV	$V_{\text{OH}} - V_{\text{OL}}$ measurement across a differential pair at the default amplitude setting with output driver not toggling; see Figure 26 for variation over frequency
Delta $V_{\text{OD}}$			25	mV	This is the absolute value of the difference between $V_{\text{OD}}$ when the normal output is high vs. when the complementary output is high
Output Offset Voltage ( $V_{\text{OS}}$ )	1.125	1.24	1.375	V	$(V_{\text{OH}} + V_{\text{OL}})/2$ across a differential pair
Delta $V_{\text{OS}}$			25	mV	This is the absolute value of the difference between $V_{\text{OS}}$ when the normal output is high vs. when the complementary output is high
Short-Circuit Current ( $I_{\text{SA}}, I_{\text{SB}}$ )		14	24	mA	Output shorted to GND
CMOS CLOCK OUTPUTS					Single-ended; termination = 10 pF
OUT6A, OUT6B, OUT7A, OUT7B, OUT8A, OUT8B, OUT9A, OUT9B					
Output Frequency			250	MHz	See Figure 27
Output Voltage High ( $V_{\text{OH}}$ )	$V_{\text{S}} - 0.1$			V	At 1 mA load
Output Voltage Low ( $V_{\text{OL}}$ )			0.1	V	At 1 mA load



## TIMING CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL					Termination = 50 $\Omega$ to $V_s - 2$ V; level = 810 mV
Output Rise Time, $t_{RP}$		70	180	ps	20% to 80%, measured differentially
Output Fall Time, $t_{FP}$		70	180	ps	80% to 20%, measured differentially
PROPAGATION DELAY, $t_{PECL}$ , CLK-TO-LVPECL OUTPUT					
High Frequency Clock Distribution Configuration	835	995	1180	ps	See Figure 43
Clock Distribution Configuration	773	933	1090	ps	See Figure 45
Variation with Temperature		0.8		ps/ $^{\circ}$ C	
OUTPUT SKEW, LVPECL OUTPUTS <sup>1</sup>					
LVPECL Outputs That Share the Same Divider		5	15	ps	
LVPECL Outputs on Different Dividers		13	40	ps	
All LVPECL Outputs Across Multiple Parts			220	ps	
LVDS					Termination = 100 $\Omega$ differential; 3.5 mA
Output Rise Time, $t_{RL}$		170	350	ps	20% to 80%, measured differentially <sup>2</sup>
Output Fall Time, $t_{FL}$		160	350	ps	20% to 80%, measured differentially <sup>2</sup>
PROPAGATION DELAY, $t_{LVDS}$ , CLK-TO-LVDS OUTPUT					Delay off on all outputs
OUT6, OUT7, OUT8, OUT9					
For All Divide Values	1.4	1.8	2.1	ns	
Variation with Temperature		1.25		ps/ $^{\circ}$ C	
OUTPUT SKEW, LVDS OUTPUTS <sup>1</sup>					Delay off on all outputs
LVDS Outputs That Share the Same Divider		6	62	ps	
LVDS Outputs on Different Dividers		25	150	ps	
All LVDS Outputs Across Multiple Parts			430	ps	
CMOS					Termination = open
Output Rise Time, $t_{RC}$		495	1000	ps	20% to 80%; $C_{LOAD} = 10$ pF
Output Fall Time, $t_{FC}$		475	985	ps	80% to 20%; $C_{LOAD} = 10$ pF
PROPAGATION DELAY, $t_{CMOS}$ , CLK-TO-CMOS OUTPUT					Fine delay off
For All Divide Values	1.6	2.1	2.6	ns	
Variation with Temperature		2.6		ps/ $^{\circ}$ C	
OUTPUT SKEW, CMOS OUTPUTS <sup>1</sup>					Fine delay off
CMOS Outputs That Share the Same Divider		4	66	ps	
All CMOS Outputs on Different Dividers		28	180	ps	
All CMOS Outputs Across Multiple Parts			675	ps	
DELAY ADJUST <sup>3</sup>					LVDS and CMOS
Shortest Delay Range <sup>4</sup>					Register 0xA1 (0xA4, 0xA7, 0xAA), Bits[5:0] = 101111b
Zero Scale	50	315	680	ps	Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 000000b
Full Scale	540	880	1180	ps	Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 101111b
Longest Delay Range <sup>4</sup>					Register 0xA1 (0xA4, 0xA7, 0xAA), Bits[5:0] = 000000b
Zero Scale	200	570	950	ps	Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 000000b
Quarter Scale	1.72	2.31	2.89	ns	Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 001100b
Full Scale	5.7	8.0	10.1	ns	Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 101111b
Delay Variation with Temperature					
Short Delay Range <sup>5</sup>					
Zero Scale		0.23		ps/ $^{\circ}$ C	
Full Scale		-0.02		ps/ $^{\circ}$ C	
Long Delay Range <sup>5</sup>					
Zero Scale		0.3		ps/ $^{\circ}$ C	
Full Scale		0.24		ps/ $^{\circ}$ C	

<sup>1</sup> This is the difference between any two similar delay paths while operating at the same voltage and temperature.

<sup>2</sup> Corresponding CMOS drivers set to A for noninverting and B for inverting.

<sup>3</sup> The maximum delay that can be used is a little less than one-half the period of the clock. A longer delay disables the output.

<sup>4</sup> Incremental delay; does not include propagation delay.

<sup>5</sup> All delays between zero scale and full scale can be estimated by linear interpolation.

**CLOCK OUTPUT ADDITIVE PHASE NOISE (DISTRIBUTION ONLY; VCO DIVIDER NOT USED)**

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-LVPECL ADDITIVE PHASE NOISE CLK = 1 GHz, Output = 1 GHz Divider = 1					Distribution section only; does not include PLL and VCO Input slew rate > 1 V/ns
At 10 Hz Offset		-109		dBc/Hz	
At 100 Hz Offset		-118		dBc/Hz	
At 1 kHz Offset		-130		dBc/Hz	
At 10 kHz Offset		-139		dBc/Hz	
At 100 kHz Offset		-144		dBc/Hz	
At 1 MHz Offset		-146		dBc/Hz	
At 10 MHz Offset		-147		dBc/Hz	
At 100 MHz Offset		-149		dBc/Hz	
CLK = 1 GHz, Output = 200 MHz Divider = 5					Input slew rate > 1 V/ns
At 10 Hz Offset		-120		dBc/Hz	
At 100 Hz Offset		-126		dBc/Hz	
At 1 kHz Offset		-139		dBc/Hz	
At 10 kHz Offset		-150		dBc/Hz	
At 100 kHz Offset		-155		dBc/Hz	
At 1 MHz Offset		-157		dBc/Hz	
>10 MHz Offset		-157		dBc/Hz	
CLK-TO-LVDS ADDITIVE PHASE NOISE CLK = 1.6 GHz, Output = 800 MHz Divider = 2					Distribution section only; does not include PLL and VCO Input slew rate > 1 V/ns
At 10 Hz Offset		-103		dBc/Hz	
At 100 Hz Offset		-110		dBc/Hz	
At 1 kHz Offset		-120		dBc/Hz	
At 10 kHz Offset		-127		dBc/Hz	
At 100 kHz Offset		-133		dBc/Hz	
At 1 MHz Offset		-138		dBc/Hz	
At 10 MHz Offset		-147		dBc/Hz	
At 100 MHz Offset		-149		dBc/Hz	
CLK = 1.6 GHz, Output = 400 MHz Divider = 4					Input slew rate > 1 V/ns
At 10 Hz Offset		-114		dBc/Hz	
At 100 Hz Offset		-122		dBc/Hz	
At 1 kHz Offset		-132		dBc/Hz	
At 10 kHz Offset		-140		dBc/Hz	
At 100 kHz Offset		-146		dBc/Hz	
At 1 MHz Offset		-150		dBc/Hz	
>10 MHz Offset		-155		dBc/Hz	
CLK-TO-CMOS ADDITIVE PHASE NOISE CLK = 1 GHz, Output = 250 MHz Divider = 4					Distribution section only; does not include PLL and VCO Input slew rate > 1 V/ns
At 10 Hz Offset		-110		dBc/Hz	
At 100 Hz Offset		-120		dBc/Hz	
At 1 kHz Offset		-127		dBc/Hz	
At 10 kHz Offset		-136		dBc/Hz	
At 100 kHz Offset		-144		dBc/Hz	
At 1 MHz Offset		-147		dBc/Hz	
>10 MHz Offset		-154		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK = 1 GHz, Output = 50 MHz Divider = 20					Input slew rate > 1 V/ns
At 10 Hz Offset		-124		dBc/Hz	
At 100 Hz Offset		-134		dBc/Hz	
At 1 kHz Offset		-142		dBc/Hz	
At 10 kHz Offset		-151		dBc/Hz	
At 100 kHz Offset		-157		dBc/Hz	
At 1 MHz Offset		-160		dBc/Hz	
>10 MHz Offset		-163		dBc/Hz	

### CLOCK OUTPUT ABSOLUTE PHASE NOISE (INTERNAL VCO USED)

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL ABSOLUTE PHASE NOISE					Internal VCO; direct to LVPECL output
VCO = 2.65 GHz; Output = 2.65 GHz					
At 1 kHz Offset		-46		dBc/Hz	
At 10 kHz Offset		-76		dBc/Hz	
At 100 kHz Offset		-104		dBc/Hz	
At 1 MHz Offset		-123		dBc/Hz	
At 10 MHz Offset		-140		dBc/Hz	
At 40 MHz Offset		-146		dBc/Hz	
VCO = 2.475 GHz; Output = 2.475 GHz					
At 1 kHz Offset		-47		dBc/Hz	
At 10 kHz Offset		-77		dBc/Hz	
At 100 kHz Offset		-105		dBc/Hz	
At 1 MHz Offset		-124		dBc/Hz	
At 10 MHz Offset		-141		dBc/Hz	
At 40 MHz Offset		-146		dBc/Hz	
VCO = 2.3 GHz; Output = 2.3 GHz					
At 1 kHz Offset		-54		dBc/Hz	
At 10 kHz Offset		-78		dBc/Hz	
At 100 kHz Offset		-106		dBc/Hz	
At 1 MHz Offset		-125		dBc/Hz	
At 10 MHz Offset		-141		dBc/Hz	
At 40 MHz Offset		-146		dBc/Hz	

**CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING INTERNAL VCO)**

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is clean, so a wider PLL loop bandwidth is used; reference = 15.36 MHz; R = 1
VCO = 2.46 GHz; LVPECL = 491.52 MHz; PLL LBW = 55 kHz		142		fs rms	Integration BW = 200 kHz to 10 MHz
		370		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.46 GHz; LVPECL = 122.88 MHz; PLL LBW = 55 kHz		145		fs rms	Integration BW = 200 kHz to 10 MHz
		356		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.46 GHz; LVPECL = 61.44 MHz; PLL LBW = 55 kHz		195		fs rms	Integration BW = 200 kHz to 10 MHz
		402		fs rms	Integration BW = 12 kHz to 20 MHz

**CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK CLEANUP USING INTERNAL VCO)**

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is jittery, so a narrower PLL loop bandwidth is used; reference = 10.0 MHz; R = 20
VCO = 2.49 GHz; LVPECL = 622.08 MHz; PLL LBW = 125 Hz		745		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.49 GHz; LVPECL = 155.52 MHz; PLL LBW = 125 Hz		712		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.46 GHz; LVPECL = 122.88 MHz; PLL LBW = 125 Hz		700		fs rms	Integration BW = 12 kHz to 20 MHz

**CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL VCXO)**

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 245.76 MHz VCXO (Toyocom TCO-2112); reference = 15.36 MHz; R = 1
LVPECL = 245.76 MHz; PLL LBW = 125 Hz		54		fs rms	Integration BW = 200 kHz to 5 MHz
		77		fs rms	Integration BW = 200 kHz to 10 MHz
		109		fs rms	Integration BW = 12 kHz to 20 MHz
LVPECL = 122.88 MHz; PLL LBW = 125 Hz		79		fs rms	Integration BW = 200 kHz to 5 MHz
		114		fs rms	Integration BW = 200 kHz to 10 MHz
		163		fs rms	Integration BW = 12 kHz to 20 MHz
LVPECL = 61.44 MHz; PLL LBW = 125 Hz		124		fs rms	Integration BW = 200 kHz to 5 MHz
		176		fs rms	Integration BW = 200 kHz to 10 MHz
		259		fs rms	Integration BW = 12 kHz to 20 MHz

**CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER NOT USED)**

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 622.08 MHz; LVPECL = 622.08 MHz; Divider = 1		40		fs rms	BW = 12 kHz to 20 MHz
CLK = 622.08 MHz; LVPECL = 155.52 MHz; Divider = 4		80		fs rms	BW = 12 kHz to 20 MHz
CLK = 1.6 GHz; LVPECL = 100 MHz; Divider = 16		215		fs rms	Calculated from SNR of ADC method; DCC not used for even divides
CLK = 500 MHz; LVPECL = 100 MHz; Divider = 5		245		fs rms	Calculated from SNR of ADC method; DCC on
LVDS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 1.6 GHz; LVDS = 800 MHz; Divider = 2; VCO Divider Not Used		85		fs rms	BW = 12 kHz to 20 MHz
CLK = 1 GHz; LVDS = 200 MHz; Divider = 5		113		fs rms	BW = 12 kHz to 20 MHz
CLK = 1.6 GHz; LVDS = 100 MHz; Divider = 16		280		fs rms	Calculated from SNR of ADC method; DCC not used for even divides
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 1.6 GHz; CMOS = 100 MHz; Divider = 16		365		fs rms	Calculated from SNR of ADC method; DCC not used for even divides

**CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER USED)**

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 2.4 GHz; VCO DIV = 2; LVPECL = 100 MHz; Divider = 12; Duty-Cycle Correction = Off		210		fs rms	Calculated from SNR of ADC method
LVDS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 2.4 GHz; VCO DIV = 2; LVDS = 100 MHz; Divider = 12; Duty-Cycle Correction = Off		285		fs rms	Calculated from SNR of ADC method
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 2.4 GHz; VCO DIV = 2; CMOS = 100 MHz; Divider = 12; Duty-Cycle Correction = Off		350		fs rms	Calculated from SNR of ADC method

**DELAY BLOCK ADDITIVE TIME JITTER**

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DELAY BLOCK ADDITIVE TIME JITTER <sup>1</sup>					Incremental additive jitter
100 MHz Output					
Delay (1600 $\mu$ A, 0x1C) Fine Adj. 000000		0.54		ps rms	
Delay (1600 $\mu$ A, 0x1C) Fine Adj. 101111		0.60		ps rms	
Delay (800 $\mu$ A, 0x1C) Fine Adj. 000000		0.65		ps rms	
Delay (800 $\mu$ A, 0x1C) Fine Adj. 101111		0.85		ps rms	
Delay (800 $\mu$ A, 0x4C) Fine Adj. 000000		0.79		ps rms	
Delay (800 $\mu$ A, 0x4C) Fine Adj. 101111		1.2		ps rms	
Delay (400 $\mu$ A, 0x4C) Fine Adj. 000000		1.2		ps rms	
Delay (400 $\mu$ A, 0x4C) Fine Adj. 101111		2.0		ps rms	
Delay (200 $\mu$ A, 0x1C) Fine Adj. 000000		1.3		ps rms	
Delay (200 $\mu$ A, 0x1C) Fine Adj. 101111		2.5		ps rms	
Delay (200 $\mu$ A, 0x4C) Fine Adj. 000000		1.9		ps rms	
Delay (200 $\mu$ A, 0x4C) Fine Adj. 101111		3.8		ps rms	

<sup>1</sup> This value is incremental. That is, it is in addition to the jitter of the LVDS or CMOS output without the delay. To estimate the total jitter, the LVDS or CMOS output jitter should be added to this value using the root sum of the squares (RSS) method.

**SERIAL CONTROL PORT**

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CS (INPUT)					CS has an internal 30 k $\Omega$ pull-up resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current			3	$\mu$ A	
Input Logic 0 Current		110		$\mu$ A	
Input Capacitance		2		pF	
SCLK (INPUT)					SCLK has an internal 30 k $\Omega$ pull-down resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		110		$\mu$ A	
Input Logic 0 Current			1	$\mu$ A	
Input Capacitance		2		pF	
SDIO (WHEN INPUT)					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		10		nA	
Input Logic 0 Current		20		nA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, 1/ $t_{SCLK}$ )			25	MHz	
Pulse Width High, $t_{HIGH}$	16			ns	
Pulse Width Low, $t_{LOW}$	16			ns	
SDIO to SCLK Setup, $t_{DS}$	2			ns	
SCLK to SDIO Hold, $t_{DH}$	1.1			ns	
SCLK to Valid SDIO and SDO, $t_{DV}$			8	ns	
$\overline{CS}$ to SCLK Setup and Hold, $t_s, t_H$	2			ns	
$\overline{CS}$ Minimum Pulse Width High, $t_{PWH}$	3			ns	

**PD, RESET, AND SYNC PINS**

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					
Logic 1 Voltage	2.0			V	These pins each have a 30 kΩ internal pull-up resistor
Logic 0 Voltage			0.8	V	
Logic 1 Current		110		μA	
Logic 0 Current			1	μA	
Capacitance		2		pF	
RESET TIMING					
Pulse Width Low	50			ns	
SYNC TIMING					
Pulse Width Low	1.5			High speed clock cycles	High speed clock is CLK input signal

**LD, STATUS, AND REFMON PINS**

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					
Output Voltage High ( $V_{OH}$ )	2.7			V	When selected as a digital output (CMOS); there are other modes in which these pins are not CMOS digital outputs; see Table 54, Register 0x017, Register 0x01A, and Register 0x01B
Output Voltage Low ( $V_{OL}$ )			0.4	V	
MAXIMUM TOGGLE RATE		100		MHz	Applies when mux is set to any divider or counter output or PFD up/down pulse; also applies in analog lock detect mode; usually debug mode only; beware that spurs may couple to output when any of these pins are toggling
ANALOG LOCK DETECT Capacitance		3		pF	On-chip capacitance; used to calculate RC time constant for analog lock detect readback; use a pull-up resistor
REF1, REF2, AND VCO FREQUENCY STATUS MONITOR Normal Range	1.02			MHz	Frequency above which the monitor always indicates the presence of the reference
Extended Range (REF1 and REF2 Only)	8			kHz	Frequency above which the monitor always indicates the presence of the reference
LD PIN COMPARATOR					
Trip Point		1.6		V	
Hysteresis		260		mV	

## POWER DISSIPATION

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION, CHIP					
Power-On Default		1.0	1.2	W	No clock; no programming; default register values; does not include power dissipated in external resistors
Full Operation; CMOS Outputs at 206 MHz		1.6	2.2	W	PLL on; internal VCO = 2476 MHz; VCO divider = 2; all channel dividers on; six LVPECL outputs at 619 MHz; eight CMOS outputs (10 pF load) at 206 MHz; all fine delay on, maximum current; does not include power dissipated in external resistors
Full Operation; LVDS Outputs at 206 MHz		1.6	2.3	W	PLL on; internal VCO = 2476 MHz; VCO divider = 2; all channel dividers on; six LVPECL outputs at 619 MHz; four LVDS outputs at 206 MHz; all fine delay on, maximum current; does not include power dissipated in external resistors
$\overline{\text{PD}}$ Power-Down		75	185	mW	$\overline{\text{PD}}$ pin pulled low; does not include power dissipated in terminations
$\overline{\text{PD}}$ Power-Down, Maximum Sleep		31		mW	$\overline{\text{PD}}$ pin pulled low; PLL power-down, Register 0x010[1:0] = 01b; SYNC power-down, Register 0x230[2] = 1b; REF for distribution power-down, Register 0x230[1] = 1b
$V_{\text{CP}}$ Supply		4	4.8	mW	PLL operating; typical closed-loop configuration
POWER DELTAS, INDIVIDUAL FUNCTIONS					
VCO Divider		30		mW	VCO divider bypassed
REFIN (Differential)		20		mW	All references off to differential reference enabled
REF1, REF2 (Single-Ended)		4		mW	All references off to REF1 or REF2 enabled; differential reference not enabled
VCO		70		mW	CLK input selected to VCO selected
PLL		75		mW	PLL off to PLL on, normal operation; no reference enabled
Channel Divider		30		mW	Divider bypassed to divide-by-2 to divide-by-32
LVPECL Channel (Divider Plus Output Driver)		160		mW	No LVPECL output on to one LVPECL output on, independent of frequency
LVPECL Driver		90		mW	Second LVPECL output turned on, same channel
LVDS Channel (Divider Plus Output Driver)		120		mW	No LVDS output on to one LVDS output on; see Figure 8 for dependence on output frequency
LVDS Driver		50		mW	Second LVDS output turned on, same channel
CMOS Channel (Divider Plus Output Driver)		100		mW	Static; no CMOS output on to one CMOS output on; see Figure 9 for variation over output frequency
CMOS Driver (Second in Pair)		0		mW	Static; second CMOS output, same pair, turned on
CMOS Driver (First in Second Pair)		30		mW	Static; first output, second pair, turned on
Fine Delay Block		50		mW	Delay block off to delay block enabled; maximum current setting



# TIMING DIAGRAMS

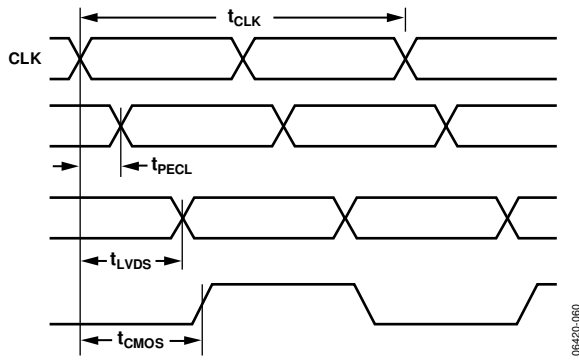


Figure 2. CLK/ $\overline{\text{CLK}}$  to Clock Output Timing, DIV = 1

06420-060

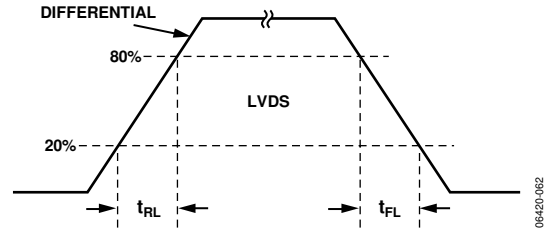


Figure 4. LVDS Timing, Differential

06420-062

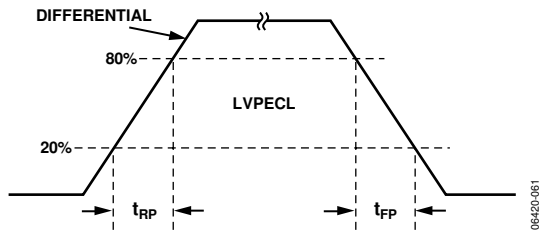


Figure 3. LVPECL Timing, Differential

06420-061

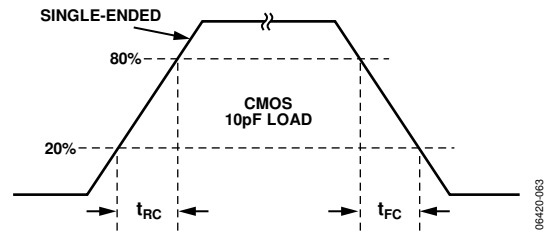


Figure 5. CMOS Timing, Single-Ended, 10 pF Load

06420-063

## ABSOLUTE MAXIMUM RATINGS

Table 18.

Parameter	Rating
VS, VS_LVPECL to GND	−0.3 V to +3.6 V
VCP to GND	−0.3 V to +5.8 V
REFIN, $\overline{\text{REFIN}}$ to GND	−0.3 V to $V_S + 0.3$ V
REFIN to $\overline{\text{REFIN}}$	−3.3 V to +3.3 V
RSET to GND	−0.3 V to $V_S + 0.3$ V
CPRSET to GND	−0.3 V to $V_S + 0.3$ V
CLK, $\overline{\text{CLK}}$ to GND	−0.3 V to $V_S + 0.3$ V
CLK to $\overline{\text{CLK}}$	−1.2 V to +1.2 V
SCLK, SDIO, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to $V_S + 0.3$ V
OUT0, $\overline{\text{OUT0}}$ , OUT1, $\overline{\text{OUT1}}$ , OUT2, $\overline{\text{OUT2}}$ , OUT3, $\overline{\text{OUT3}}$ , OUT4, $\overline{\text{OUT4}}$ , OUT5, $\overline{\text{OUT5}}$ , OUT6, $\overline{\text{OUT6}}$ , OUT7, $\overline{\text{OUT7}}$ , OUT8, $\overline{\text{OUT8}}$ , OUT9, $\overline{\text{OUT9}}$ to GND	−0.3 V to $V_S + 0.3$ V
$\overline{\text{SYNC}}$ to GND	−0.3 V to $V_S + 0.3$ V
REFMON, STATUS, LD to GND	−0.3 V to $V_S + 0.3$ V
Junction Temperature <sup>1</sup>	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

<sup>1</sup> See Table 19 for  $\theta_{JA}$ .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

Table 19.

Package Type <sup>1</sup>	$\theta_{JA}$	Unit
64-Lead LFCSP	24	°C/W

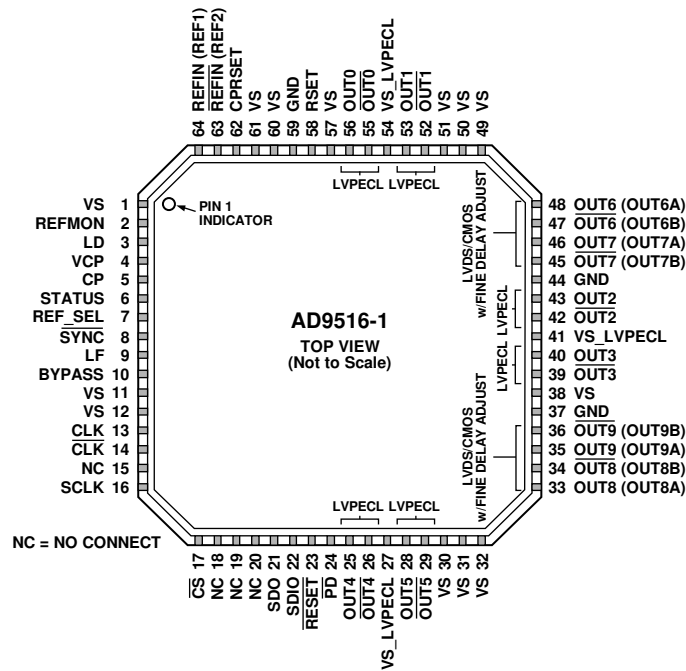
<sup>1</sup> Thermal impedance measurements were taken on a 4-layer board in still air in accordance with EIA/JESD51-2.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NC = NO CONNECT
- NOTES
1. THE EXTERNAL PADDLE ON THE BOTTOM OF THE PACKAGE MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.
  2. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

06420-003

Figure 6. Pin Configuration

Table 20. Pin Function Descriptions

Pin No.	Input/Output	Pin Type	Mnemonic	Description
1, 11, 12, 30, 31, 32, 38, 49, 50, 51, 57, 60, 61	I	Power	VS	3.3 V Power Pins.
2	I	3.3 V CMOS	REFMON	Reference Monitor (Output). This pin has multiple selectable outputs; see Table 54, Register 0x01B.
3	O	3.3 V CMOS	LD	Lock Detect (Output). This pin has multiple selectable outputs; see Table 54, Register 0x1A.
4	I	Power	VCP	Power Supply for Charge Pump (CP); $V_S \leq V_{CP} \leq 5.0V$ .
5	O	3.3 V CMOS	CP	Charge Pump (Output). Connects to external loop filter.
6	O	3.3 V CMOS	STATUS	Status (Output). This pin has multiple selectable outputs; see Table 54, Register 0x017.
7	I	3.3 V CMOS	REF_SEL	Reference Select. Selects REF1 (low) or REF2 (high). This pin has an internal 30 kΩ pull-down resistor.
8	I	3.3 V CMOS	SYNC	Manual Synchronizations and Manual Holdover. This pin initiates a manual synchronization and is also used for manual holdover. Active low. This pin has an internal 30 kΩ pull-up resistor.
9	I	Loop filter	LF	Loop Filter (Input). Connects to VCO control voltage node internally. This pin has 31 pF of internal capacitance to ground, which may influence the loop filter design for large (>500 kHz) loop bandwidths.
10	O	Loop filter	BYPASS	This pin is for bypassing the LDO to ground with a capacitor.
13	I	Differential clock input	CLK	Along with CLK, this is the differential input for the clock distribution section.
14	I	Differential clock input	CLK	Along with CLK, this is the differential input for the clock distribution section.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
15, 18, 19, 20	N/A	NC	NC	No Connect. Do not connect to this pin.
16	I	3.3 V CMOS	SCLK	Serial Control Port Data Clock Signal.
17	I	3.3 V CMOS	$\overline{CS}$	Serial Control Port Chip Select, Active Low. This pin has an internal 30 k $\Omega$ pull-up resistor.
21	O	3.3 V CMOS	SDO	Serial Control Port Unidirectional Serial Data Out.
22	I/O	3.3 V CMOS	SDIO	Serial Control Port Bidirectional Serial Data In/Out.
23	I	3.3 V CMOS	$\overline{RESET}$	Chip Reset, Active Low. This pin has an internal 30 k $\Omega$ pull-up resistor.
24	I	3.3 V CMOS	$\overline{PD}$	Chip Power-Down, Active Low. This pin has an internal 30 k $\Omega$ pull-up resistor.
27, 41, 54	I	Power	VS_LVPECL	Extended Voltage 2.5 V to 3.3 V LVPECL Power Pins.
37, 44, 59, EPAD	N/A	GND	GND	Ground Pins, Including External Paddle (EPAD). The external paddle on the bottom of the package must be connected to ground for proper operation.
56	O	LVPECL	$\overline{OUT0}$	LVPECL Output; One Side of a Differential LVPECL Output.
55	O	LVPECL	$\overline{OUT0}$	LVPECL Output; One Side of a Differential LVPECL Output.
53	O	LVPECL	$\overline{OUT1}$	LVPECL Output; One Side of a Differential LVPECL Output.
52	O	LVPECL	$\overline{OUT1}$	LVPECL Output; One Side of a Differential LVPECL Output.
43	O	LVPECL	$\overline{OUT2}$	LVPECL Output; One Side of a Differential LVPECL Output.
42	O	LVPECL	$\overline{OUT2}$	LVPECL Output; One Side of a Differential LVPECL Output.
40	O	LVPECL	$\overline{OUT3}$	LVPECL Output; One Side of a Differential LVPECL Output.
39	O	LVPECL	$\overline{OUT3}$	LVPECL Output; One Side of a Differential LVPECL Output.
25	O	LVPECL	$\overline{OUT4}$	LVPECL Output; One Side of a Differential LVPECL Output.
26	O	LVPECL	$\overline{OUT4}$	LVPECL Output; One Side of a Differential LVPECL Output.
28	O	LVPECL	$\overline{OUT5}$	LVPECL Output; One Side of a Differential LVPECL Output.
29	O	LVPECL	$\overline{OUT5}$	LVPECL Output; One Side of a Differential LVPECL Output.
48	O	LVDS or CMOS	$\overline{OUT6}$ (OUT6A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
47	O	LVDS or CMOS	$\overline{OUT6}$ (OUT6B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
46	O	LVDS or CMOS	$\overline{OUT7}$ (OUT7A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
45	O	LVDS or CMOS	$\overline{OUT7}$ (OUT7B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
33	O	LVDS or CMOS	$\overline{OUT8}$ (OUT8A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
34	O	LVDS or CMOS	$\overline{OUT8}$ (OUT8B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
35	O	LVDS or CMOS	$\overline{OUT9}$ (OUT9A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
36	O	LVDS or CMOS	$\overline{OUT9}$ (OUT9B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
58	O	Current set resistor	RSET	A resistor connected to this pin sets internal bias currents. Nominal value = 4.12 k $\Omega$ .
62	O	Current set resistor	CPRSET	A resistor connected to this pin sets the CP current range. Nominal value = 5.1 k $\Omega$ .
63	I	Reference input	$\overline{REFIN}$ (REF2)	Along with $\overline{REFIN}$ , this pin is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF2.
64	I	Reference input	REFIN (REF1)	Along with $\overline{REFIN}$ , this pin is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF1.

# TYPICAL PERFORMANCE CHARACTERISTICS

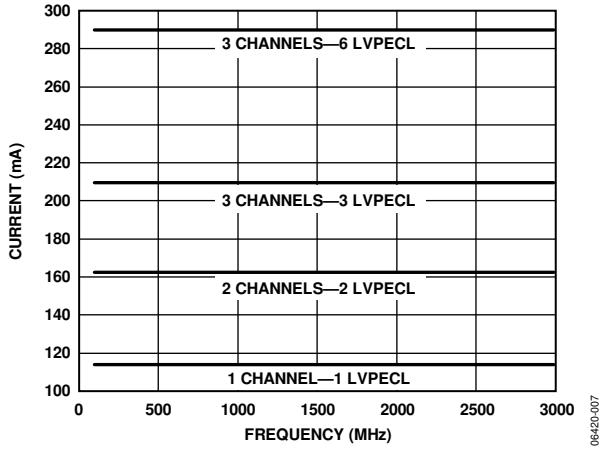


Figure 7. Current vs. Frequency, Direct to Output, LVPECL Outputs

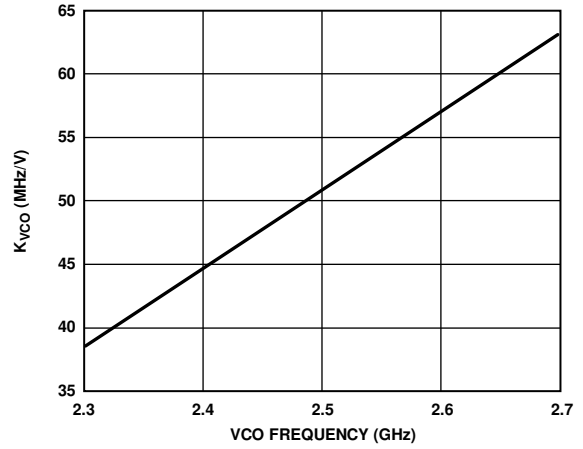


Figure 10. VCO  $K_{VCO}$  vs. Frequency

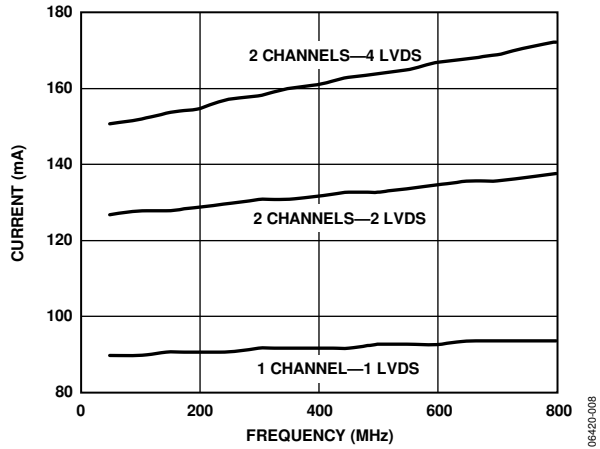


Figure 8. Current vs. Frequency—LVDS Outputs (Includes Clock Distribution Current Draw)

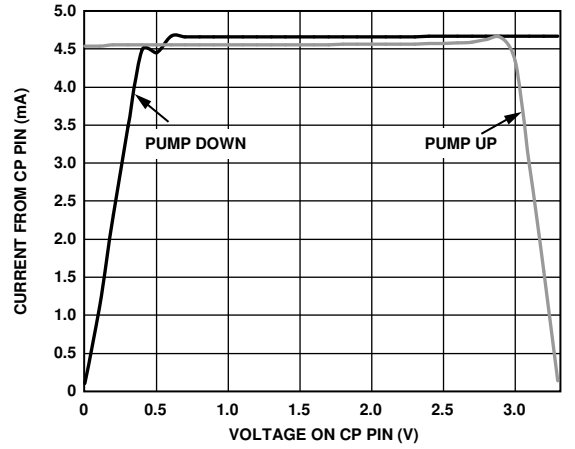


Figure 11. Charge Pump Characteristics at  $V_{CP} = 3.3 V$

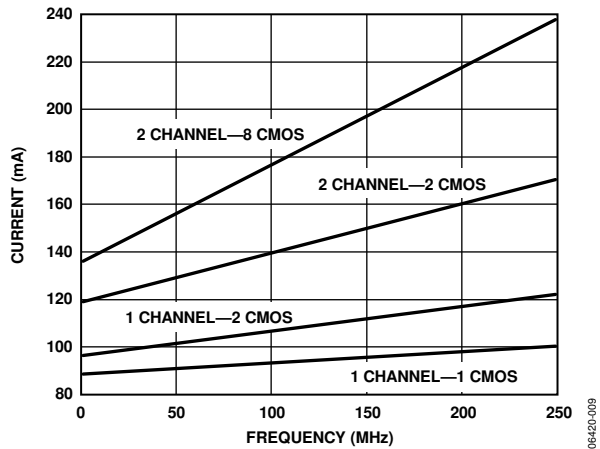


Figure 9. Current vs. Frequency—CMOS Outputs

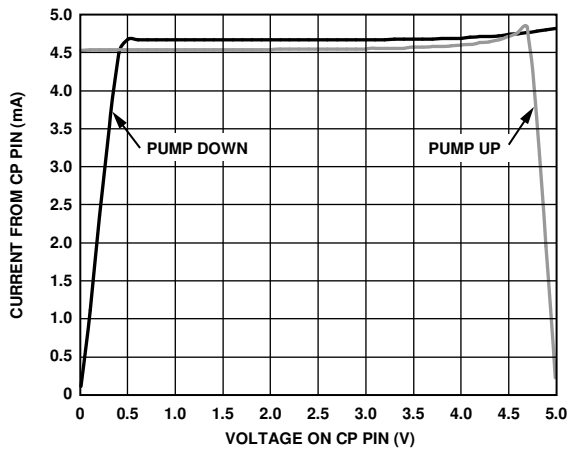


Figure 12. Charge Pump Characteristics at  $V_{CP} = 5.0 V$

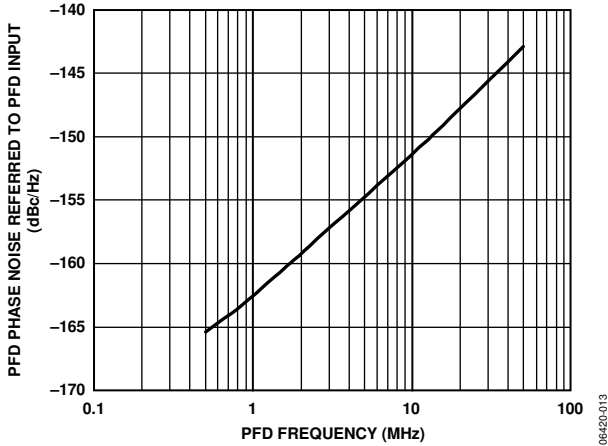


Figure 13. PFD Phase Noise Referred to PFD Input vs. PFD Frequency

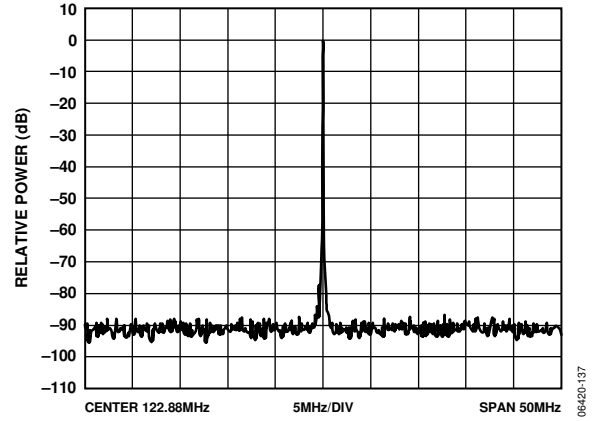


Figure 16. PFD/CP Spurs; 122.88 MHz; PFD = 15.36 MHz; LBW = 55 kHz;  $I_{CP} = 4.8$  mA;  $F_{VCO} = 2.46$  GHz

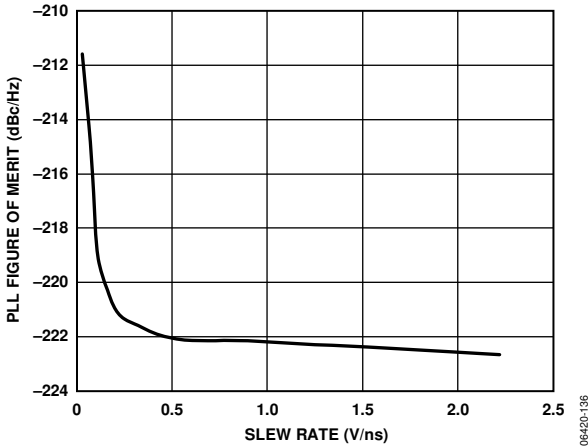


Figure 14. PLL Figure of Merit (FOM) vs. Slew Rate at REFIN/REFIN

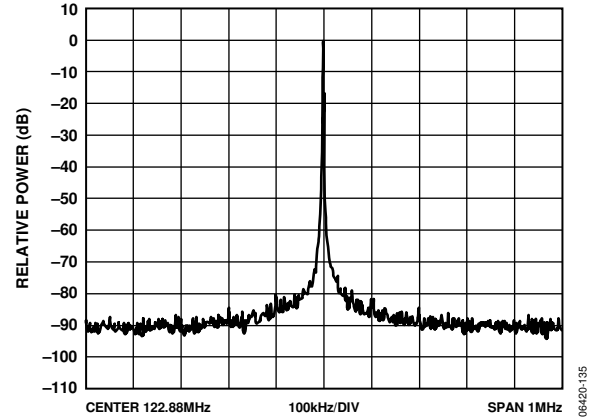


Figure 17. Output Spectrum, LVPECL; 122.88 MHz; PFD = 15.36 MHz; LBW = 55 kHz;  $I_{CP} = 4.8$  mA;  $F_{VCO} = 2.46$  GHz

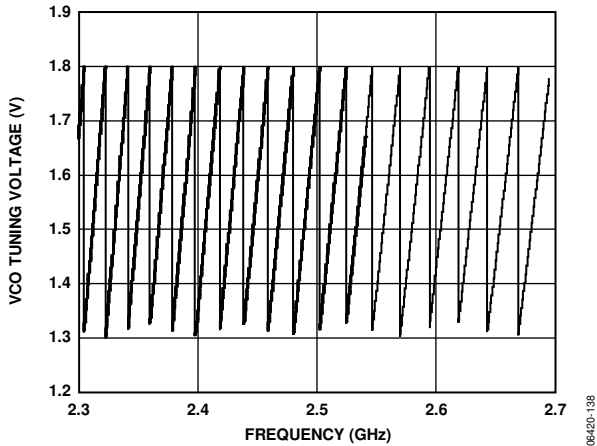


Figure 15. VCO Tuning Voltage vs. Frequency  
(Note that VCO calibration centers the dc tuning voltage for the PLL setup that is active during calibration.)

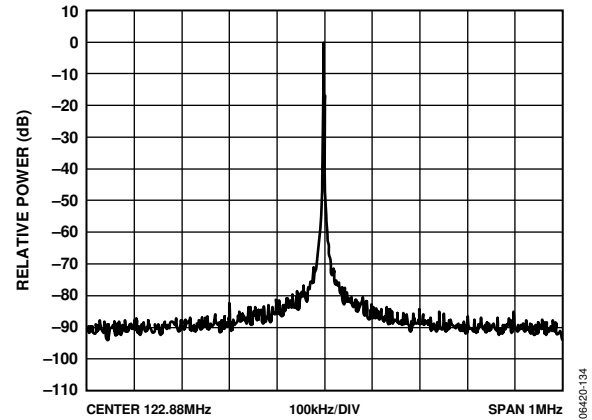


Figure 18. Output Spectrum, LVDS; 122.88 MHz; PFD = 15.36 MHz; LBW = 55 kHz;  $I_{CP} = 4.8$  mA;  $F_{VCO} = 2.46$  GHz

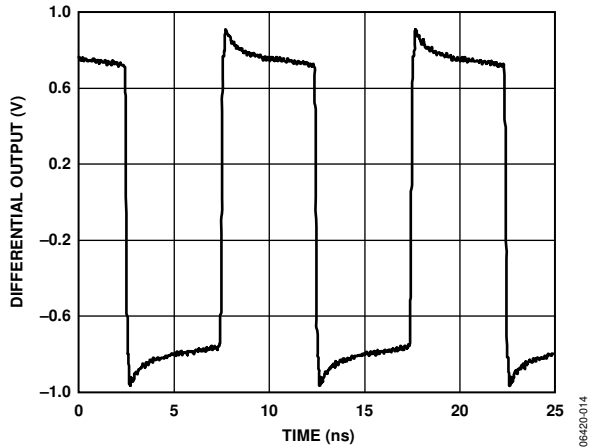


Figure 19. LVPECL Output (Differential) at 100 MHz

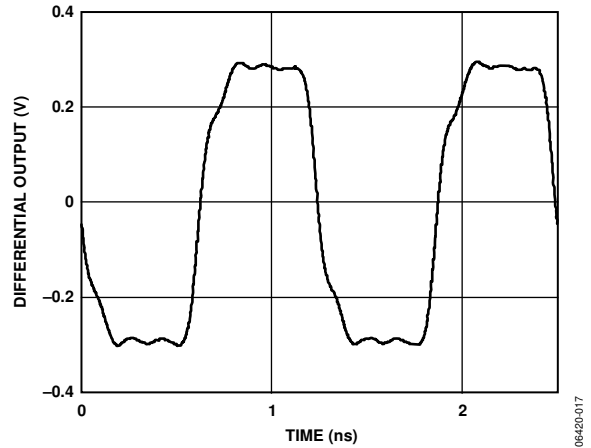


Figure 22. LVDS Output (Differential) at 800 MHz

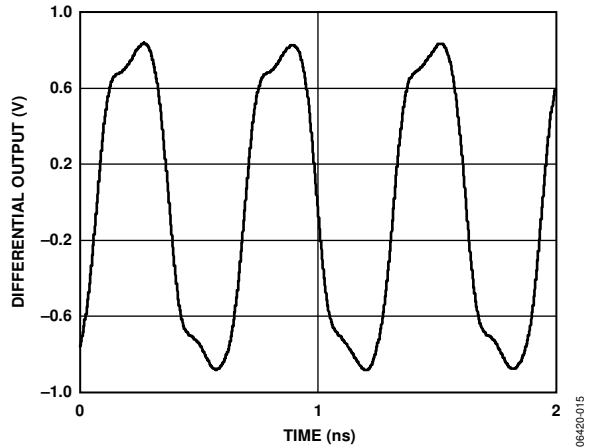


Figure 20. LVPECL Output (Differential) at 1600 MHz

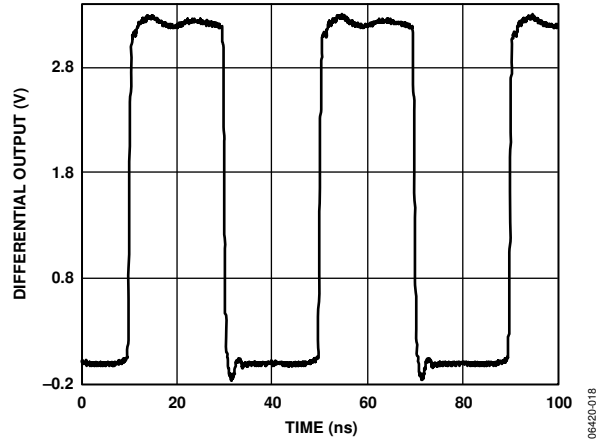


Figure 23. CMOS Output at 25 MHz

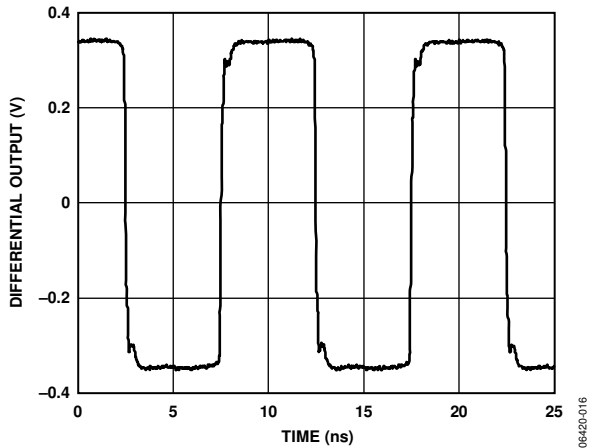


Figure 21. LVDS Output (Differential) at 100 MHz

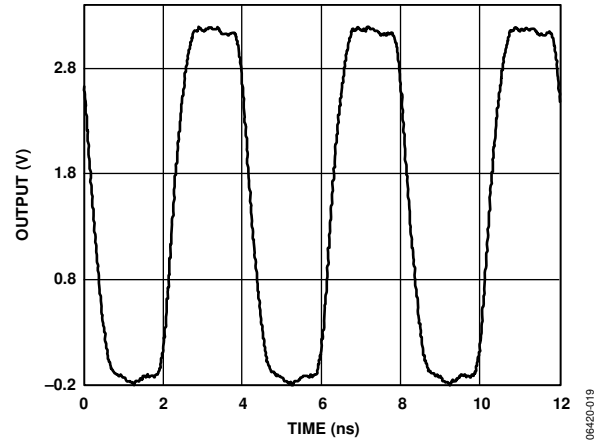


Figure 24. CMOS Output at 250 MHz

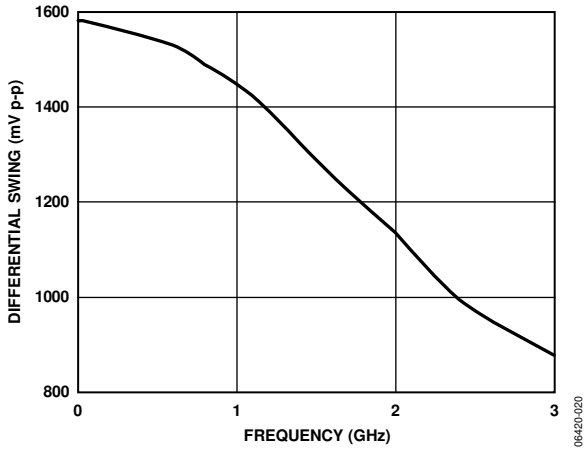


Figure 25. LVPECL Differential Swing vs. Frequency Using a Differential Probe Across the Output Pair

06420-020

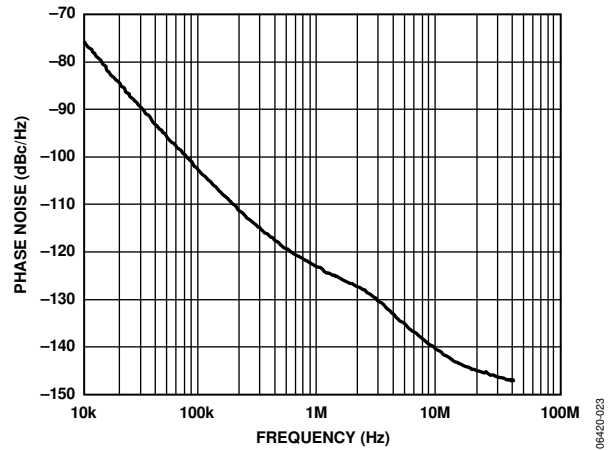


Figure 28. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 2650 MHz

06420-023

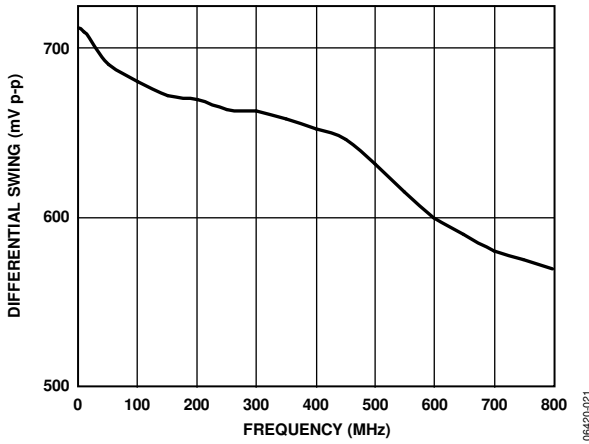


Figure 26. LVDS Differential Swing vs. Frequency Using a Differential Probe Across the Output Pair

06420-021

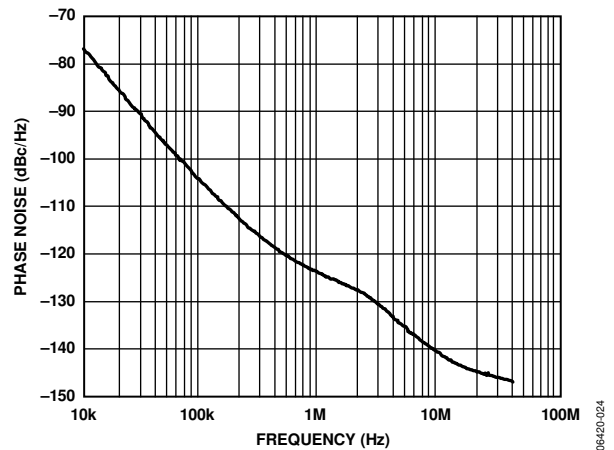


Figure 29. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 2475 MHz

06420-024

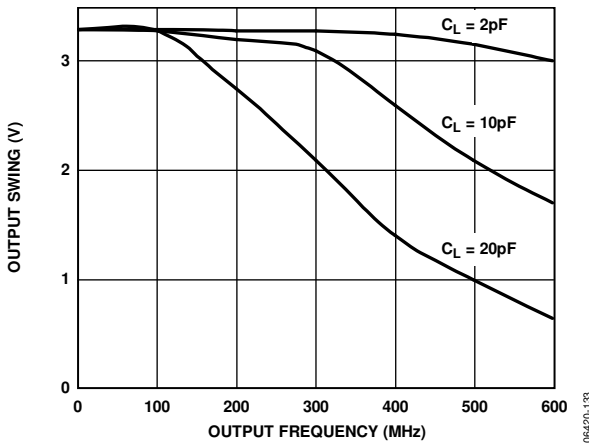


Figure 27. CMOS Output Swing vs. Frequency and Capacitive Load

06420-133

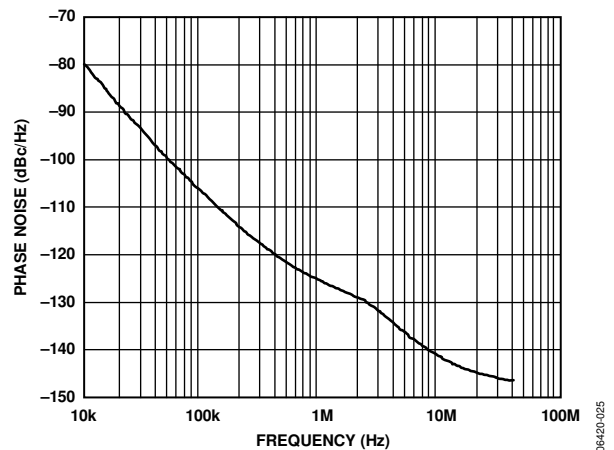


Figure 30. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 2300 MHz

06420-025



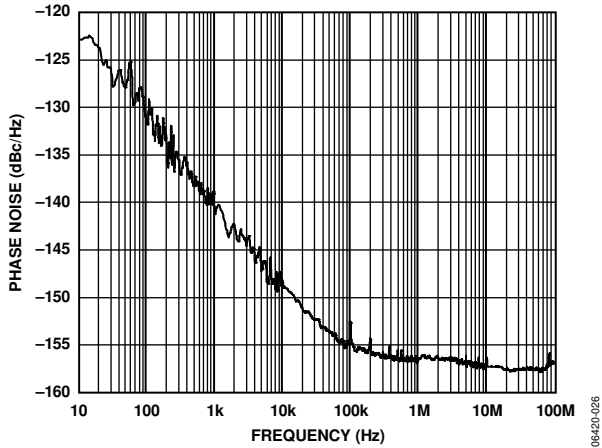


Figure 31. Phase Noise (Additive) LVPECL at 245.76 MHz, Divide-by-1

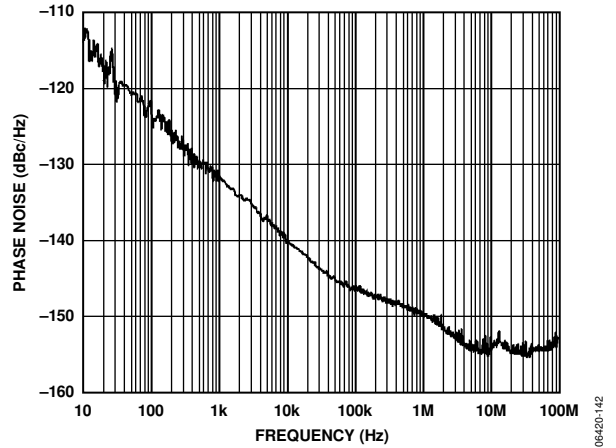


Figure 34. Phase Noise (Additive) LVDS at 200 MHz, Divide-by-1

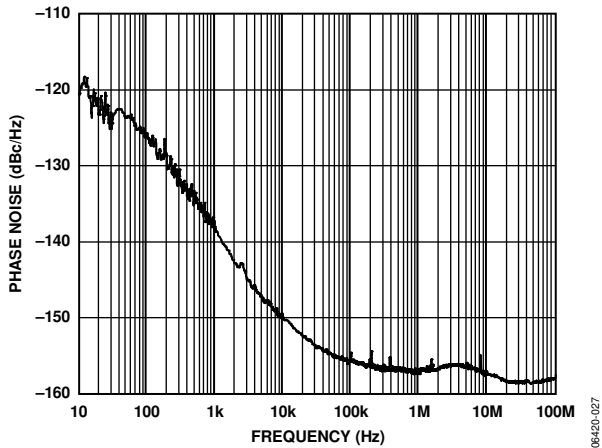


Figure 32. Phase Noise (Additive) LVPECL at 200 MHz, Divide-by-5

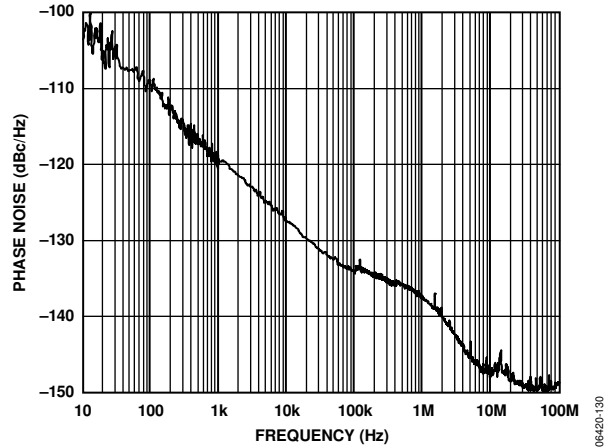


Figure 35. Phase Noise (Additive) LVDS at 800 MHz, Divide-by-2

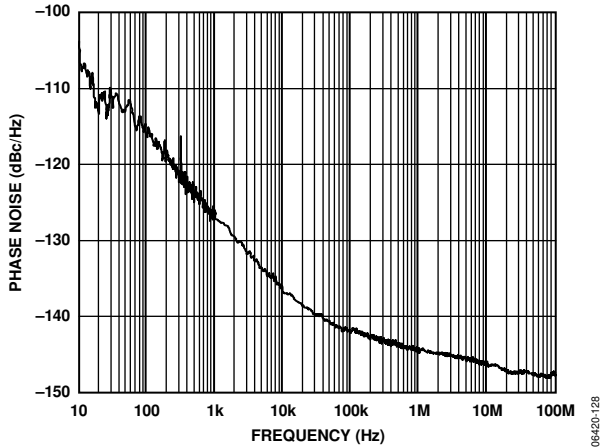


Figure 33. Phase Noise (Additive) LVPECL at 1600 MHz, Divide-by-1

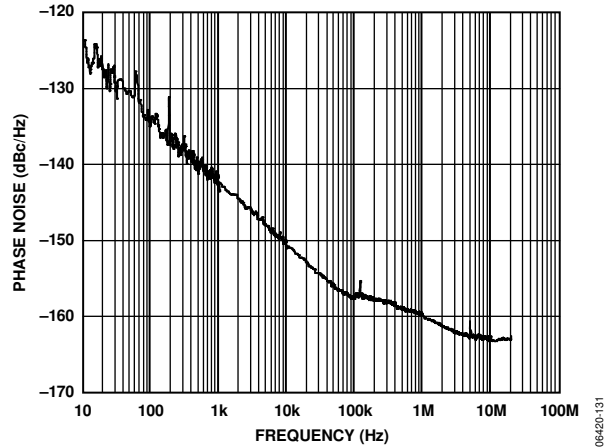


Figure 36. Phase Noise (Additive) CMOS at 50 MHz, Divide-by-20

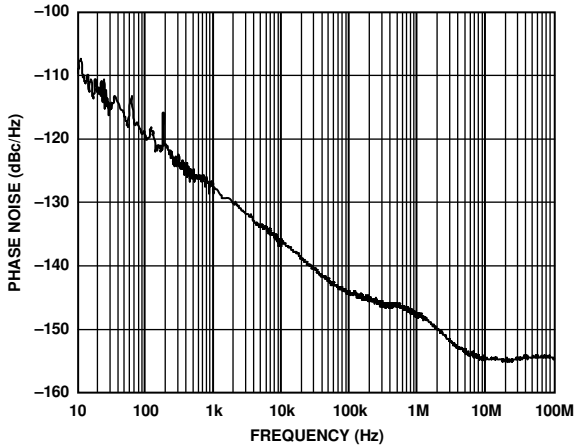


Figure 37. Phase Noise (Additive) CMOS at 250 MHz, Divide-by-4

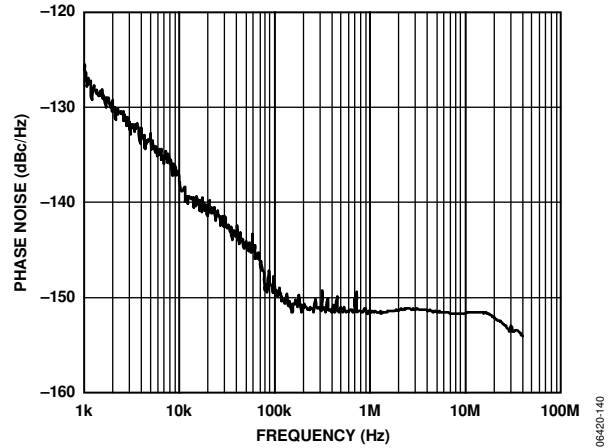


Figure 40. Phase Noise (Absolute), External VCXO (Toyocom TCO-2112) at 245.76 MHz; PFD = 15.36 MHz; LBW = 250 Hz; LVPECL Output = 245.76 MHz

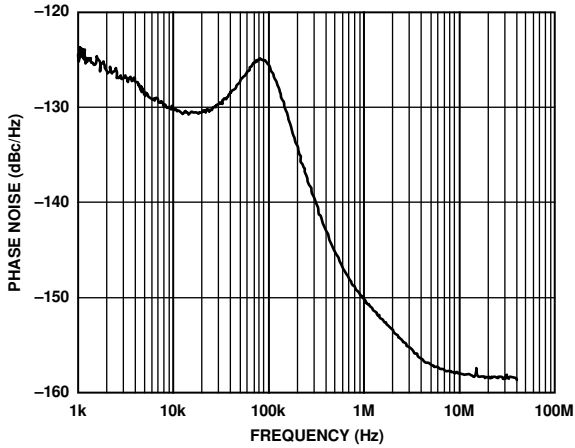


Figure 38. Phase Noise (Absolute) Clock Generation; Internal VCO at 2.4576 GHz; PFD = 15.36 MHz; LBW = 55 kHz; LVPECL Output = 122.88 MHz

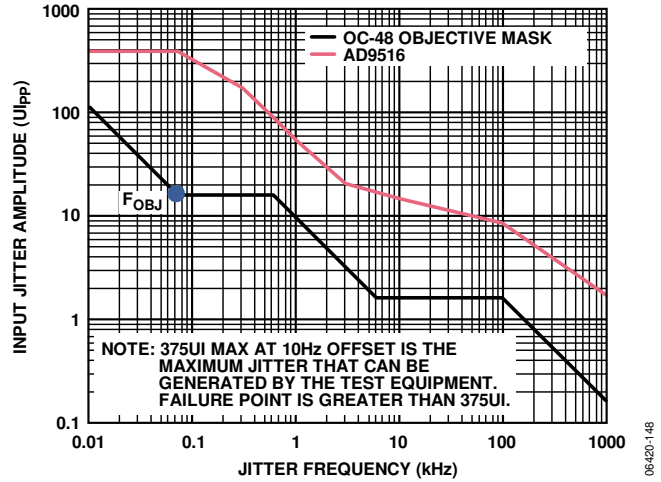


Figure 41. GR-253 Jitter Tolerance Plot

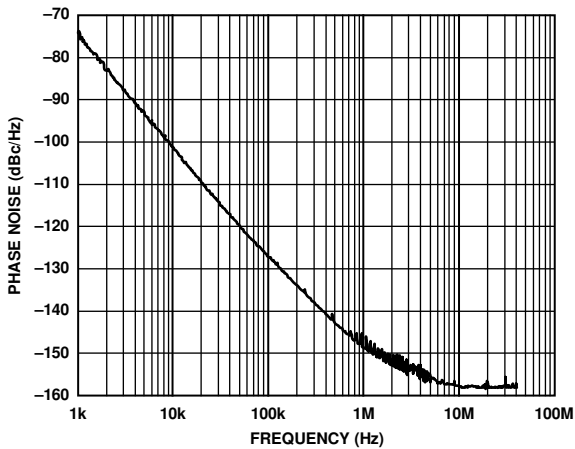


Figure 39. Phase Noise (Absolute) Clock Cleanup; Internal VCO at 2.488 GHz; PFD = 19.44 MHz; LBW = 12.8 kHz; LVPECL Output = 155.52 MHz