14-Output Clock Generator with Integrated 1.6 GHz VCO

Data Sheet **AD9516-4**

FEATURES

Low phase noise, phase-locked loop (PLL)
- **On-chip VCO tunes from 1.45 GHz to 1.80 GHz**
- **External VCO/VCXO to 2.4 GHz optional**
- **1 differential or 2 single-ended reference inputs**
- **Reference monitoring capability**
- **Automatic revertive and manual reference switchover/holdover modes**
- **Accepts LVPECL, LVDS, or CMOS references to 250 MHz**
- **Programmable delays in path to PFD**
- **Digital or analog lock detect, selectable**

6 pairs of 1.6 GHz LVPECL outputs
- **Each output pair shares a 1-to-32 divider with coarse phase delay**
- **Additive output jitter: 225 fs rms**
- **Channel-to-channel skew paired outputs of <10 ps**

4 pairs of 800 MHz LVDS clock outputs
- **Each output pair shares two cascaded 1-to-32 dividers with coarse phase delay**
- **Additive output jitter: 275 fs rms**
- **Fine delay adjust (Δt) on each LVDS output**
- **Each LVDS output can be reconfigured as two 250 MHz CMOS outputs**

Automatic synchronization of all outputs on power-up
Manual output synchronization available
64-lead LFCSP

APPLICATIONS

Low jitter, low phase noise clock distribution
10/40/100 Gb/sec networking line cards, including SONET, Synchronous Ethernet, OTU2/3/4
Forward error correction (G.710)
Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
High performance wireless transceivers
ATE and high performance instrumentation

GENERAL DESCRIPTION

The AD9516-4[1] provides a multi-output clock distribution function with subpicosecond jitter performance, along with an on-chip PLL and VCO. The on-chip VCO tunes from 1.45 GHz to 1.80 GHz. Optionally, an external VCO/VCXO of up to 2.4 GHz can be used.

The AD9516-4 emphasizes low jitter and phase noise to maximize data converter performance, and it can benefit other applications with demanding phase noise and jitter requirements.

FUNCTIONAL BLOCK DIAGRAM

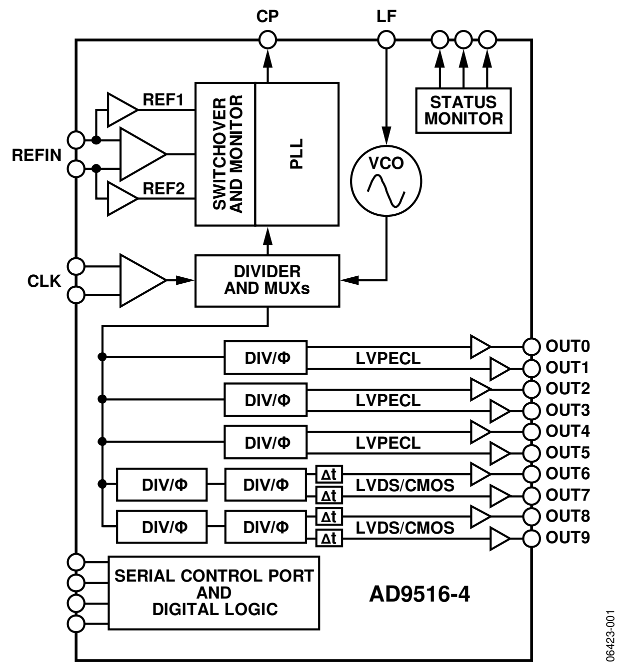

Figure 1.

The AD9516-4 features six LVPECL outputs (in three pairs) and four LVDS outputs (in two pairs). Each LVDS output can be reconfigured as two CMOS outputs. The LVPECL outputs operate to 1.6 GHz, the LVDS outputs operate to 800 MHz, and the CMOS outputs operate to 250 MHz.

Each pair of outputs has dividers that allow both the divide ratio and coarse delay (or phase) to be set. The range of division for the LVPECL outputs is 1 to 32. The LVDS/CMOS outputs allow a range of divisions, up to a maximum of 1024.

The AD9516-4 is available in a 64-lead LFCSP and can be operated from a single 3.3 V supply. An external VCO, which requires an extended voltage range, can be accommodated by connecting the charge pump supply (VCP to 5 V. A separate LVPECL power supply can be from 2.5 V to 3.3 V (nominal).

The AD9516-4 is specified for operation over the industrial range of −40°C to +85°C.

[1] AD9516 is used throughout to refer to all the members of the AD9516 family. However, when AD9516-4 is used, it refers to that specific member of the AD9516 family.

Rev. C Document Feedback

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AD9516-4* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

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EVALUATION KITS

- AD9516-4 Evaluation Board

DOCUMENTATION

Application Notes

- AN-0974: Multicarrier TD-SCMA Feasibility
- AN-0983: Introduction to Zero-Delay Clock Timing Techniques
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal

Data Sheet

- AD9516-4: 14-Output Clock Generator with Integrated 1.6 GHz VCO Data Sheet

User Guides

- UG-075: AD9516-x, AD9517-x, and AD9518-x Evaluation Board User Guide
- UG-093: Evaluation Board User Guide for the Dual, Continuous Time Sigma-Delta Modulator

TOOLS AND SIMULATIONS

- ADIsimCLK Design and Evaluation Software
- AD9516 IBIS Models

REFERENCE DESIGNS

- CN0243

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- ADI Buys Korean Mobile TV Chip Maker
- Design A Clock-Distribution Strategy With Confidence
- Improved DDS Devices Enable Advanced Comm Systems
- Low-power direct digital synthesizer cores enable high level of integration
- Speedy A/Ds Demand Stable Clocks
- Understand the Effects of Clock Jitter and Phase Noise on Sampled Systems

DESIGN RESOURCES

- AD9516-4 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9516-4 EngineerZone Discussions.

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REVISION HISTORY

2/13—Rev. B to Rev. C

1/12—Rev. A to Rev. B

12/10—Rev. 0 to Rev. A

4/07—Revision 0: Initial Version

SPECIFICATIONS

Typical is given for $V_S = V_{S\_LVPECL}$ = 3.3 V ± 5%; $V_S \le V_{CP} \le$ 5.25 V; T_A = 25°C; R_{SET} = 4.12 kΩ; CP_{RSET} = 5.1 kΩ, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

POWER SUPPLY REQUIREMENTS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
V_S	3.135	3.3	3.465	V	3.3 V ± 5%
V_{S_LVPECL}	2.375		V_S	V	Nominally 2.5 V to 3.3 V ± 5%
V_{CP}	V_S		5.25	V	Nominally 3.3 V to 5.0 V ± 5%
RSET Pin Resistor		4.12		kΩ	Sets internal biasing currents; connect to ground
CPRSET Pin Resistor	2.7	5.1	10	kΩ	Sets internal CP current range, nominally 4.8 mA (CP_lsb = 600 μA); actual current can be calculated by: CP_lsb = 3.06/CPRSET; connect to ground
BYPASS Pin Capacitor		220		nF	Bypass for internal LDO regulator; necessary for LDO stability; connect to ground

PLL CHARACTERISTICS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO (ON-CHIP)					
Frequency Range	1450		1800	MHz	See Figure 15
VCO Gain (K_{VCO})		50		MHz/V	See Figure 10
Tuning Voltage (V_T)	0.5		V_{CP} − 0.5	V	$V_{CP} \le V_S$ when using internal VCO; outside of this range, the CP spurs may increase due to CP up/down mismatch
Frequency Pushing (Open-Loop)		1		MHz/V	
Phase Noise at 100 kHz Offset		−109		dBc/Hz	f = 1625 MHz
Phase Noise at 1 MHz Offset		−128		dBc/Hz	f = 1625 MHz
REFERENCE INPUTS					
Differential Mode (REFIN, $\overline{\text{REFIN}}$)					Differential mode (can accommodate single-ended input by ac grounding undriven input)
Input Frequency	0		250	MHz	Frequencies below about 1 MHz should be dc-coupled; be careful to match V_{CM} (self-bias voltage)
Input Sensitivity		250		mV p-p	PLL figure of merit (FOM) increases with increasing slew rate; see Figure 14
Self-Bias Voltage, REFIN	1.35	1.60	1.75	V	Self-bias voltage of REFIN[1]
Self-Bias Voltage, $\overline{\text{REFIN}}$	1.30	1.50	1.60	V	Self-bias voltage of $\overline{\text{REFIN}}$[1]
Input Resistance, REFIN	4.0	4.8	5.9	kΩ	Self-biased[1]
Input Resistance, $\overline{\text{REFIN}}$	4.4	5.3	6.4	kΩ	Self-biased[1]
Dual Single-Ended Mode (REF1, REF2)					Two single-ended CMOS-compatible inputs
Input Frequency (AC-Coupled)	20		250	MHz	Slew rate > 50 V/μs
Input Frequency (DC-Coupled)	0		250	MHz	Slew rate > 50 V/μs; CMOS levels
Input Sensitivity (AC-Coupled)		0.8		V p-p	Should not exceed V_S p-p
Input Logic High	2.0			V	
Input Logic Low			0.8	V	
Input Current	−100		+100	μA	
Input Capacitance		2		pF	Each pin, REFIN/$\overline{\text{REFIN}}$ (REF1/REF2)
PHASE/FREQUENCY DETECTOR (PFD)					
PFD Input Frequency			100	MHz	Antibacklash pulse width = 1.3 ns, 2.9 ns
			45	MHz	Antibacklash pulse width = 6.0 ns
Antibacklash Pulse Width		1.3		ns	Register 0x017[1:0] = 01b
		2.9		ns	Register 0x017[1:0] = 00b; Register 0x017[1:0] = 11b
		6.0		ns	Register 0x017[1:0] = 10b

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CHARGE PUMP (CP)					
I_{CP} Sink/Source					Programmable
High Value		4.8		mA	With CP_{RSET} = 5.1 kΩ
Low Value		0.60		mA	
Absolute Accuracy		2.5		%	$CP_V = V_{CP}/2$
CP_{RSET} Range		2.7/10		kΩ	
I_{CP} High Impedance Mode Leakage		1		nA	
Sink-and-Source Current Matching		2		%	$0.5 < CP_V < V_{CP} - 0.5$ V
I_{CP} vs. CP_V		1.5		%	$0.5 < CP_V < V_{CP} - 0.5$ V
I_{CP} vs. Temperature		2		%	$CP_V = V_{CP}/2$
PRESCALER (PART OF N DIVIDER)					See the VCXO/VCO Feedback Divider N—P, A, B, R section
Prescaler Input Frequency					
P = 1 FD			300	MHz	
P = 2 FD			600	MHz	
P = 3 FD			900	MHz	
P = 2 DM (2/3)			200	MHz	
P = 4 DM (4/5)			1000	MHz	
P = 8 DM (8/9)			2400	MHz	
P = 16 DM (16/17)			3000	MHz	
P = 32 DM (32/33)			3000	MHz	
Prescaler Output Frequency			300	MHz	A, B counter input frequency (prescaler input frequency divided by P)
PLL DIVIDER DELAYS					Register 0x019: R, Bits[5:3], N, Bits[2:0]; see Table 54
000		Off		ps	
001		330		ps	
010		440		ps	
011		550		ps	
100		660		ps	
101		770		ps	
110		880		ps	
111		990		ps	
NOISE CHARACTERISTICS					
In-Band Phase Noise of the Charge Pump/Phase Frequency Detector (In-Band Is Within the LBW of the PLL)					The PLL in-band phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20log(N) (where N is the value of the N divider)
At 500 kHz PFD Frequency		−165		dBc/Hz	
At 1 MHz PFD Frequency		−162		dBc/Hz	
At 10 MHz PFD Frequency		−151		dBc/Hz	
At 50 MHz PFD Frequency		−143		dBc/Hz	
PLL Figure of Merit (FOM)		−220		dBc/Hz	Reference slew rate > 0.25 V/ns; FOM + 10log (f_{PFD}) is an approximation of the PFD/CP in-band phase noise (in the flat region) inside the PLL loop bandwidth; when running closed loop, the phase noise, as observed at the VCO output, is increased by 20log(N)
PLL DIGITAL LOCK DETECT WINDOW[2]					Signal available at LD, STATUS, and REFMON pins when selected by appropriate register settings
Required to Lock (Coincidence of Edges)					Selected by Register 0x017[1:0] and Register 0x018[4]
Low Range (ABP 1.3 ns, 2.9 ns)		3.5		ns	Register 0x017[1:0] = 00b, 01b,11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		7.5		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6 ns)		3.5		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b
To Unlock After Lock (Hysteresis)[2]					
Low Range (ABP 1.3 ns, 2.9 ns)		7		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		15		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6 ns)		11		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b

[1] REFIN and $\overline{\text{REFIN}}$ self-bias points are offset slightly to avoid chatter on an open input condition.
[2] For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the unlock-after-lock time.

CLOCK INPUTS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUTS (CLK, $\overline{\text{CLK}}$)					Differential input
Input Frequency	0[1]		2.4	GHz	High frequency distribution (VCO divider)
	0[1]		1.6	GHz	Distribution only (VCO divider bypassed)
Input Sensitivity, Differential		150		mV p-p	Measured at 2.4 GHz; jitter performance is improved with slew rates > 1 V/ns
Input Level, Differential			2	V p-p	Larger voltage swings may turn on the protection diodes and may degrade jitter performance
Input Common-Mode Voltage, V_{CM}	1.3	1.57	1.8	V	Self-biased; enables ac coupling
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled
Input Sensitivity, Single-Ended		150		mV p-p	CLK ac-coupled; $\overline{\text{CLK}}$ ac-bypassed to RF ground
Input Resistance	3.9	4.7	5.7	kΩ	Self-biased
Input Capacitance		2		pF	

[1] Below about 1 MHz, the input should be dc-coupled. Care should be taken to match V_{CM}.

CLOCK OUTPUTS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					Termination = 50 Ω to V_S − 2 V
OUT0, OUT1, OUT2, OUT3, OUT4, OUT5					Differential (OUT, $\overline{\text{OUT}}$)
Output Frequency, Maximum	2950			MHz	Using direct to output; see Figure 25 for peak-to – peak differential amplitude
Output High Voltage (V_{OH})	V_S − 1.12	V_S − 0.98	V_S − 0.84	V	
Output Low Voltage (V_{OL})	V_S − 2.03	V_S − 1.77	V_S − 1.49	V	
Output Differential Voltage (V_{OD})	550	790	980	mV	V_{OH} − V_{OL} for each leg of a differential pair for default amplitude setting with driver not toggling; see Figure 25 for variation over frequency
LVDS CLOCK OUTPUTS					Differential termination 100 Ω at 3.5 mA
OUT6, OUT7, OUT8, OUT9					Differential (OUT, $\overline{\text{OUT}}$)
Output Frequency			800	MHz	The AD9516 outputs toggle at higher frequencies, but the output amplitude may not meet the V_{OD} specification; see Figure 26
Differential Output Voltage (V_{OD})	247	360	454	mV	V_{OH} − V_{OL} measurement across a differential pair at the default amplitude setting with output driver not toggling; see Figure 26 for variation over frequency
Delta V_{OD}			25	mV	This is the absolute value of the difference between V_{OD} when the normal output is high vs. when the complementary output is high
Output Offset Voltage (V_{OS})	1.125	1.24	1.375	V	(V_{OH} + V_{OL})/2 across a differential pair
Delta V_{OS}			25	mV	This is the absolute value of the difference between V_{OS} when the normal output is high vs. when the complementary output is high
Short-Circuit Current (I_{SA}, I_{SB})		14	24	mA	Output shorted to GND
CMOS CLOCK OUTPUTS					
OUT6A, OUT6B, OUT7A, OUT7B, OUT8A, OUT8B, OUT9A, OUT9B					Single-ended; termination = 10 pF
Output Frequency			250	MHz	See Figure 27
Output Voltage High (V_{OH})	V_S − 0.1			V	At 1 mA load
Output Voltage Low (V_{OL})			0.1	V	At 1 mA load

TIMING CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL					Termination = 50 Ω to V_S − 2 V; level = 810 mV
Output Rise Time, t_{RP}		70	180	ps	20% to 80%, measured differentially
Output Fall Time, t_{FP}		70	180	ps	80% to 20%, measured differentially
PROPAGATION DELAY, t_{PECL}, CLK-TO-LVPECL OUTPUT					
High Frequency Clock Distribution Configuration	835	995	1180	ps	See Figure 43
Clock Distribution Configuration	773	933	1090	ps	See Figure 45
Variation with Temperature		0.8		ps/°C	
OUTPUT SKEW, LVPECL OUTPUTS[1]					
LVPECL Outputs That Share the Same Divider		5	15	ps	
LVPECL Outputs on Different Dividers		13	40	ps	
All LVPECL Outputs Across Multiple Parts			220	ps	
LVDS					Termination = 100 Ω differential; 3.5 mA
Output Rise Time, t_{RL}		170	350	ps	20% to 80%, measured differentially[2]
Output Fall Time, t_{FL}		160	350	ps	20% to 80%, measured differentially[2]
PROPAGATION DELAY, t_{LVDS}, CLK-TO-LVDS OUTPUT					Delay off on all outputs
OUT6, OUT7, OUT8, OUT9					
For All Divide Values	1.4	1.8	2.1	ns	
Variation with Temperature		1.25		ps/°C	
OUTPUT SKEW, LVDS OUTPUTS[1]					Delay off on all outputs
LVDS Outputs That Share the Same Divider		6	62	ps	
LVDS Outputs on Different Dividers		25	150	ps	
All LVDS Outputs Across Multiple Parts			430	ps	
CMOS					Termination = open
Output Rise Time, t_{RC}		495	1000	ps	20% to 80%; C_{LOAD} = 10 pF
Output Fall Time, t_{FC}		475	985	ps	80% to 20%; C_{LOAD} = 10 pF
PROPAGATION DELAY, t_{CMOS}, CLK-TO-CMOS OUTPUT					Fine delay off
For All Divide Values	1.6	2.1	2.6	ns	
Variation with Temperature		2.6		ps/°C	
OUTPUT SKEW, CMOS OUTPUTS[1]					Fine delay off
CMOS Outputs That Share the Same Divider		4	66	ps	
All CMOS Outputs on Different Dividers		28	180	ps	
All CMOS Outputs Across Multiple Parts			675	ps	
DELAY ADJUST[3]					LVDS and CMOS
Shortest Delay Range[4]					Register 0xA1 (0xA4, 0xA7, 0xAA), Bits[5:0] = 101111b
Zero Scale	50	315	680	ps	Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 000000b
Full Scale	540	880	1180	ps	Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 101111b
Longest Delay Range[4]					Register 0xA1 (0xA4, 0xA7, 0xAA), Bits[5:0] = 000000b
Zero Scale	200	570	950	ps	Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 000000b
Quarter Scale	1.72	2.31	2.89	ns	Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 001100b
Full Scale	5.7	8.0	10.1	ns	Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 101111b
Delay Variation with Temperature					
Short Delay Range[5]					
Zero Scale		0.23		ps/°C	
Full Scale		−0.02		ps/°C	
Long Delay Range[5]					
Zero Scale		0.3		ps/°C	
Full Scale		0.24		ps/°C	

[1] This is the difference between any two similar delay paths while operating at the same voltage and temperature.
[2] Corresponding CMOS drivers set to A for noninverting, and B for inverting.
[3] The maximum delay that can be used is a little less than one-half the period of the clock. A longer delay disables the output.
[4] Incremental delay; does not include propagation delay.
[5] All delays between zero scale and full scale can be estimated by linear interpolation.

CLOCK OUTPUT ADDITIVE PHASE NOISE (DISTRIBUTION ONLY; VCO DIVIDER NOT USED)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-LVPECL ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 1 GHz, Output = 1 GHz					Input slew rate > 1 V/ns
Divider = 1					
At 10 Hz Offset		−109		dBc/Hz	
At 100 Hz Offset		−118		dBc/Hz	
At 1 kHz Offset		−130		dBc/Hz	
At 10 kHz Offset		−139		dBc/Hz	
At 100 kHz Offset		−144		dBc/Hz	
At 1 MHz Offset		−146		dBc/Hz	
At 10 MHz Offset		−147		dBc/Hz	
At 100 MHz Offset		−149		dBc/Hz	
CLK = 1 GHz, Output = 200 MHz					Input slew rate > 1 V/ns
Divider = 5					
At 10 Hz Offset		−120		dBc/Hz	
At 100 Hz Offset		−126		dBc/Hz	
At 1 kHz Offset		−139		dBc/Hz	
At 10 kHz Offset		−150		dBc/Hz	
At 100 kHz Offset		−155		dBc/Hz	
At 1 MHz Offset		−157		dBc/Hz	
>10 MHz Offset		−157		dBc/Hz	
CLK-TO-LVDS ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 1.6 GHz, Output = 800 MHz					Input slew rate > 1 V/ns
Divider = 2					
At 10 Hz Offset		−103		dBc/Hz	
At 100 Hz Offset		−110		dBc/Hz	
At 1 kHz Offset		−120		dBc/Hz	
At 10 kHz Offset		−127		dBc/Hz	
At 100 kHz Offset		−133		dBc/Hz	
At 1 MHz Offset		−138		dBc/Hz	
At 10 MHz Offset		−147		dBc/Hz	
At 100 MHz Offset		−149		dBc/Hz	
CLK = 1.6 GHz, Output = 400 MHz					Input slew rate > 1 V/ns
Divider = 4					
At 10 Hz Offset		−114		dBc/Hz	
At 100 Hz Offset		−122		dBc/Hz	
At 1 kHz Offset		−132		dBc/Hz	
At 10 kHz Offset		−140		dBc/Hz	
At 100 kHz Offset		−146		dBc/Hz	
At 1 MHz Offset		−150		dBc/Hz	
>10 MHz Offset		−155		dBc/Hz	
CLK-TO-CMOS ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 1 GHz, Output = 250 MHz					Input slew rate > 1 V/ns
Divider = 4					
At 10 Hz Offset		−110		dBc/Hz	
At 100 Hz Offset		−120		dBc/Hz	
At 1 kHz Offset		−127		dBc/Hz	
At 10 kHz Offset		−136		dBc/Hz	
At 100 kHz Offset		−144		dBc/Hz	
At 1 MHz Offset		−147		dBc/Hz	
>10 MHz Offset		−154		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK = 1 GHz, Output = 50 MHz					Input slew rate > 1 V/ns
Divider = 20					
At 10 Hz Offset		−124		dBc/Hz	
At 100 Hz Offset		−134		dBc/Hz	
At 1 kHz Offset		−142		dBc/Hz	
At 10 kHz Offset		−151		dBc/Hz	
At 100 kHz Offset		−157		dBc/Hz	
At 1 MHz Offset		−160		dBc/Hz	
>10 MHz Offset		−163		dBc/Hz	

CLOCK OUTPUT ABSOLUTE PHASE NOISE (INTERNAL VCO USED)

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL ABSOLUTE PHASE NOISE					Internal VCO; direct to LVPECL output
VCO = 1800 MHz; Output = 1800 MHz					
At 1 kHz Offset		−47		dBc/Hz	
At 10 kHz Offset		−82		dBc/Hz	
At 100 kHz Offset		−106		dBc/Hz	
At 1 MHz Offset		−125		dBc/Hz	
At 10 MHz Offset		−142		dBc/Hz	
At 40 MHz Offset		−146		dBc/Hz	
VCO = 1625 MHz; Output = 1625 MHz					
At 1 kHz Offset		−55		dBc/Hz	
At 10 kHz Offset		−85		dBc/Hz	
At 100 kHz Offset		−109		dBc/Hz	
At 1 MHz Offset		−128		dBc/Hz	
At 10 MHz Offset		−143		dBc/Hz	
At 40 MHz Offset		−147		dBc/Hz	
VCO = 1450 MHz; Output = 1450 MHz					
At 1 kHz Offset		−61		dBc/Hz	
At 10 kHz Offset		−90		dBc/Hz	
At 100 kHz Offset		−113		dBc/Hz	
At 1 MHz Offset		−131		dBc/Hz	
At 10 MHz Offset		−144		dBc/Hz	
At 40 MHz Offset		−148		dBc/Hz	

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING INTERNAL VCO)

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is clean, so a wider PLL loop bandwidth is used; reference = 15.36 MHz; R = 1
VCO = 1475 MHz; LVPECL = 491.52 MHz; PLL LBW = 135 kHz		135		fs rms	Integration BW = 200 kHz to 10 MHz
		275		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 1475 MHz; LVPECL = 122.88 MHz; PLL LBW = 135 kHz		145		fs rms	Integration BW = 200 kHz to 10 MHz
		275		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 1475 MHz; LVPECL = 61.44 MHz; PLL LBW = 135 kHz		170		fs rms	Integration BW = 200 kHz to 10 MHz
		305		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK CLEANUP USING INTERNAL VCO)

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is jittery, so a narrower PLL loop bandwidth is used; reference = 10.0 MHz; R = 20
VCO = 1555 MHz; LVPECL = 155.52 MHz; PLL LBW = 500 Hz		500		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 1475 MHz; LVPECL = 122.88 MHz; PLL LBW = 500 Hz		400		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL VCXO)

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 245.76 MHz VCXO (Toyocom TCO-2112); reference = 15.36 MHz; R = 1
LVPECL = 245.76 MHz; PLL LBW = 125 Hz		54		fs rms	Integration BW = 200 kHz to 5 MHz
		77		fs rms	Integration BW = 200 kHz to 10 MHz
		109		fs rms	Integration BW = 12 kHz to 20 MHz
LVPECL = 122.88 MHz; PLL LBW = 125 Hz		79		fs rms	Integration BW = 200 kHz to 5 MHz
		114		fs rms	Integration BW = 200 kHz to 10 MHz
		163		fs rms	Integration BW = 12 kHz to 20 MHz
LVPECL = 61.44 MHz; PLL LBW = 125 Hz		124		fs rms	Integration BW = 200 kHz to 5 MHz
		176		fs rms	Integration BW = 200 kHz to 10 MHz
		259		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER NOT USED)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 622.08 MHz; LVPECL = 622.08 MHz; Divider = 1		40		fs rms	BW = 12 kHz to 20 MHz
CLK = 622.08 MHz; LVPECL = 155.52 MHz; Divider = 4		80		fs rms	BW = 12 kHz to 20 MHz
CLK = 1.6 GHz; LVPECL = 100 MHz; Divider = 16		215		fs rms	Calculated from SNR of ADC method; DCC not used for even divides
CLK = 500 MHz; LVPECL = 100 MHz; Divider = 5		245		fs rms	Calculated from SNR of ADC method; DCC on
LVDS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 1.6 GHz; LVDS = 800 MHz; Divider = 2; VCO Divider Not Used		85		fs rms	BW = 12 kHz to 20 MHz
CLK = 1 GHz; LVDS = 200 MHz; Divider = 5		113		fs rms	BW = 12 kHz to 20 MHz
CLK = 1.6 GHz; LVDS= 100 MHz; Divider = 16		280		fs rms	Calculated from SNR of ADC method; DCC not used for even divides
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 1.6 GHz; CMOS = 100 MHz; Divider = 16		365		fs rms	Calculated from SNR of ADC method; DCC not used for even divides

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER USED)

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 2.4 GHz; VCO DIV = 2; LVPECL = 100 MHz; Divider = 12; Duty-Cycle Correction = Off		210		fs rms	Calculated from SNR of ADC method
LVDS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 2.4 GHz; VCO DIV = 2; LVDS = 100 MHz; Divider = 12; Duty-Cycle Correction = Off		285		fs rms	Calculated from SNR of ADC method
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 2.4 GHz; VCO DIV = 2; CMOS = 100 MHz; Divider = 12; Duty-Cycle Correction = Off		350		fs rms	Calculated from SNR of ADC method

DELAY BLOCK ADDITIVE TIME JITTER

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DELAY BLOCK ADDITIVE TIME JITTER[1]					Incremental additive jitter
100 MHz Output					
Delay (1600 µA, 0x1C) Fine Adj. 000000		0.54		ps rms	
Delay (1600 µA, 0x1C) Fine Adj. 101111		0.60		ps rms	
Delay (800 µA, 0x1C) Fine Adj. 000000		0.65		ps rms	
Delay (800 µA, 0x1C) Fine Adj. 101111		0.85		ps rms	
Delay (800 µA, 0x4C) Fine Adj. 000000		0.79		ps rms	
Delay (800 µA, 0x4C) Fine Adj. 101111		1.2		ps rms	
Delay (400 µA, 0x4C) Fine Adj. 000000		1.2		ps rms	
Delay (400 µA, 0x4C) Fine Adj. 101111		2.0		ps rms	
Delay (200 µA, 0x1C) Fine Adj. 000000		1.3		ps rms	
Delay (200 µA, 0x1C) Fine Adj. 101111		2.5		ps rms	
Delay (200 µA, 0x4C) Fine Adj. 000000		1.9		ps rms	
Delay (200 µA, 0x4C) Fine Adj. 101111		3.8		ps rms	

[1] This value is incremental. That is, it is in addition to the jitter of the LVDS or CMOS output without the delay. To estimate the total jitter, the LVDS or CMOS output jitter should be added to this value using the root sum of the squares (RSS) method.

SERIAL CONTROL PORT

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)					$\overline{CS}$ has an internal 30 kΩ pull-up resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current			3	µA	
Input Logic 0 Current		110		µA	
Input Capacitance		2		pF	
SCLK (INPUT)					SCLK has an internal 30 kΩ pull-down resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		110		µA	
Input Logic 0 Current			1	µA	
Input Capacitance		2		pF	
SDIO (WHEN INPUT)					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		10		nA	
Input Logic 0 Current		20		nA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, 1/t_{SCLK})			25	MHz	
Pulse Width High, t_{HIGH}	16			ns	
Pulse Width Low, t_{LOW}	16			ns	
SDIO to SCLK Setup, t_{DS}	2			ns	
SCLK to SDIO Hold, t_{DH}	1.1			ns	
SCLK to Valid SDIO and SDO, t_{DV}			8	ns	
$\overline{CS}$ to SCLK Setup and Hold, t_S, t_H	2			ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	3			ns	

$\overline{PD}$, $\overline{RESET}$, AND $\overline{SYNC}$ PINS

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					These pins each have a 30 kΩ internal pull-up resistor
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current		110		µA	
Logic 0 Current			1	µA	
Capacitance		2		pF	
$\overline{RESET}$ TIMING					
Pulse Width Low	50			ns	
$\overline{SYNC}$ TIMING					
Pulse Width Low	1.5			High speed clock cycles	High speed clock is CLK input signal

LD, STATUS, AND REFMON PINS

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					When selected as a digital output (CMOS); there are other modes in which these pins are not CMOS digital outputs; see Table 54, Register 0x017, Register 0x01A, and Register 0x01B
Output Voltage High (V_{OH})	2.7			V	
Output Voltage Low (V_{OL})			0.4	V	
MAXIMUM TOGGLE RATE		100		MHz	Applies when mux is set to any divider or counter output or PFD up/down pulse; also applies in analog lock detect mode; usually debug mode only; beware that spurs may couple to output when any of these pins are toggling
ANALOG LOCK DETECT					
Capacitance		3		pF	On-chip capacitance; used to calculate RC time constant for analog lock detect readback; use a pull-up resistor
REF1, REF2, AND VCO FREQUENCY STATUS MONITOR					
Normal Range	1.02			MHz	Frequency above which the monitor always indicates the presence of the reference
Extended Range (REF1 and REF2 Only)	8			kHz	Frequency above which the monitor always indicates the presence of the reference
LD PIN COMPARATOR					
Trip Point		1.6		V	
Hysteresis		260		mV	

POWER DISSIPATION

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION, CHIP					
Power-On Default		1.0	1.2	W	No clock; no programming; default register values; does not include power dissipated in external resistors
Full Operation; CMOS Outputs at 229 MHz		1.6	2.2	W	PLL on; internal VCO = 1625 MHz; VCO divider = 2; all channel dividers on; six LVPECL outputs at 406 MHz; eight CMOS outputs (10 pF load) at 203 MHz; all fine delay on, maximum current; does not include power dissipated in external resistors
Full Operation; LVDS Outputs at 200 MHz		1.6	2.3	W	PLL on; internal VCO = 1625 MHz, VCO divider = 2; all channel dividers on; six LVPECL outputs at 406 MHz; four LVDS outputs at 203 MHz; all fine delay on, maximum current; does not include power dissipated in external resistors
$\overline{PD}$ Power-Down		75	185	mW	$\overline{PD}$ pin pulled low; does not include power dissipated in terminations
$\overline{PD}$ Power-Down, Maximum Sleep		31		mW	$\overline{PD}$ pin pulled low; PLL power-down, Register 0x010[1:0] = 01b; SYNC power-down, Register 0x230[2] = 1b; REF for distribution power-down, Register 0x230[1] = 1b
V_{CP} Supply		4	4.8	mW	PLL operating; typical closed loop configuration
POWER DELTAS, INDIVIDUAL FUNCTIONS					Power delta when a function is enabled/disabled
VCO Divider		30		mW	VCO divider bypassed
REFIN (Differential)		20		mW	All references off to differential reference enabled
REF1, REF2 (Single-Ended)		4		mW	All references off to REF1 or REF2 enabled; differential reference not enabled
VCO		70		mW	CLK input selected to VCO selected
PLL		75		mW	PLL off to PLL on, normal operation; no reference enabled
Channel Divider		30		mW	Divider bypassed to divide-by-2 to divide-by-32
LVPECL Channel (Divider Plus Output Driver)		160		mW	No LVPECL output on to one LVPECL output on, independent of frequency
LVPECL Driver		90		mW	Second LVPECL output turned on, same channel
LVDS Channel (Divider Plus Output Driver)		120		mW	No LVDS output on to one LVDS output on; see Figure 8 for dependence on output frequency
LVDS Driver		50		mW	Second LVDS output turned on, same channel
CMOS Channel (Divider Plus Output Driver)		100		mW	Static; no CMOS output on to one CMOS output on; see Figure 9 for variation over output frequency
CMOS Driver (Second in Pair)		0		mW	Static; second CMOS output, same pair, turned on
CMOS Driver (First in Second Pair)		30		mW	Static; first output, second pair, turned on
Fine Delay Block		50		mW	Delay block off to delay block enabled; maximum current setting

TIMING DIAGRAMS

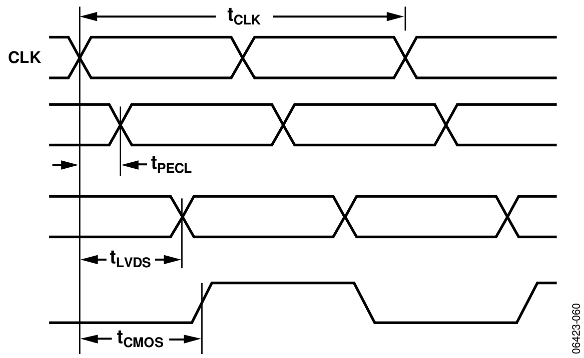


Figure 2. CLK/$\overline{CLK}$ to Clock Output Timing, DIV = 1

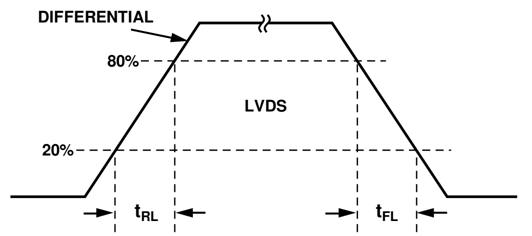


Figure 4. LVDS Timing, Differential

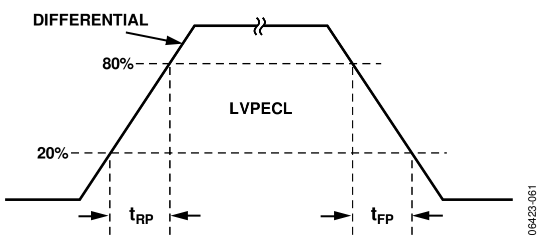


Figure 3. LVPECL Timing, Differential

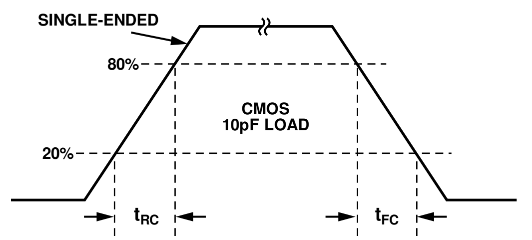


Figure 5. CMOS Timing, Single-Ended, 10 pF Load

ABSOLUTE MAXIMUM RATINGS

Table 18.

Parameter	Rating
VS, VS_LVPECL to GND	−0.3 V to +3.6 V
VCP to GND	−0.3 V to+5.8 V
REFIN, $\overline{\text{REFIN}}$ to GND	−0.3 V to V_S + 0.3 V
REFIN to $\overline{\text{REFIN}}$	−3.3 V to +3.3 V
RSET to GND	−0.3 V to V_S + 0.3 V
CPRSET to GND	−0.3 V to V_S + 0.3 V
CLK, $\overline{\text{CLK}}$ to GND	−0.3 V to V_S + 0.3 V
CLK to $\overline{\text{CLK}}$	−1.2 V to +1.2 V
SCLK, SDIO, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to V_S + 0.3 V
OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$, OUT6, $\overline{\text{OUT6}}$, OUT7, $\overline{\text{OUT7}}$, OUT8, $\overline{\text{OUT8}}$, OUT9, $\overline{\text{OUT9}}$ to GND	−0.3 V to V_S + 0.3 V
$\overline{\text{SYNC}}$ to GND	−0.3 V to V_S + 0.3 V
REFMON, STATUS, LD to GND	−0.3 V to V_S + 0.3 V
Junction Temperature[1]	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

[1] See Table 19 for θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 19.

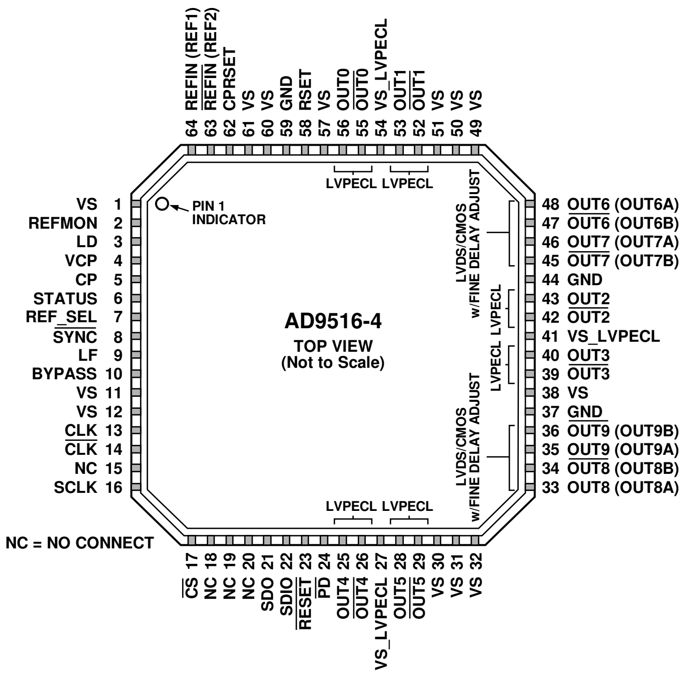
Package Type[1]	θ_{JA}	Unit
64-Lead LFCSP	24	°C/W

[1] Thermal impedance measurements were taken on a 4-layer board in still air in accordance with EIA/JESD51-2.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXTERNAL PADDLE ON THE BOTTOM OF THE PACKAGE MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.
2. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

06423-003

Figure 6. Pin Configuration

Table 20. Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1, 11, 12, 30, 31, 32, 38, 49, 50, 51, 57, 60, 61	I	Power	VS	3.3 V Power Pins.
2	I	3.3 V CMOS	REFMON	Reference Monitor (Output). This pin has multiple selectable outputs; see Table 54, Register 0x01B.
3	O	3.3 V CMOS	LD	Lock Detect (Output). This pin has multiple selectable outputs; see Table 54, Register 0x1A.
4	I	Power	VCP	Power Supply for Charge Pump (CP); $V_S \leq V_{CP} \leq 5.0$ V.
5	O	3.3 V CMOS	CP	Charge Pump (Output). Connects to external loop filter.
6	O	3.3 V CMOS	STATUS	Status (Output). This pin has multiple selectable outputs; see Table 54, Register 0x017.
7	I	3.3 V CMOS	REF_SEL	Reference Select. Selects REF1 (low) or REF2 (high). This pin has an internal 30 kΩ pull-down resistor.
8	I	3.3 V CMOS	$\overline{\text{SYNC}}$	Manual Synchronizations and Manual Holdover. This pin initiates a manual synchronization and is also used for manual holdover. Active low. This pin has an internal 30 kΩ pull-up resistor.
9	I	Loop filter	LF	Loop Filter (Input). Connects to VCO control voltage node internally. This pin has 31 pF of internal capacitance to ground, which may influence the loop filter design for large (>500 kHz) loop bandwidths.
10	O	Loop filter	BYPASS	This pin is for bypassing the LDO to ground with a capacitor.
13	I	Differential clock input	CLK	Along with $\overline{\text{CLK}}$, this is the differential input for the clock distribution section.
14	I	Differential clock input	$\overline{\text{CLK}}$	Along with CLK, this is the differential input for the clock distribution section.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
15, 18, 19, 20	N/A	NC	NC	No Connect. Do not connect to this pin.
16	I	3.3 V CMOS	SCLK	Serial Control Port Data Clock Signal.
17	I	3.3 V CMOS	$\overline{\text{CS}}$	Serial Control Port Chip Select, Active Low. This pin has an internal 30 kΩ pull-up resistor.
21	O	3.3 V CMOS	SDO	Serial Control Port Unidirectional Serial Data Out.
22	I/O	3.3 V CMOS	SDIO	Serial Control Port Bidirectional Serial Data In/Out.
23	I	3.3 V CMOS	$\overline{\text{RESET}}$	Chip Reset, Active Low. This pin has an internal 30 kΩ pull-up resistor.
24	I	3.3 V CMOS	$\overline{\text{PD}}$	Chip Power-Down, Active Low. This pin has an internal 30 kΩ pull-up resistor.
27, 41, 54	I	Power	VS_LVPECL	Extended Voltage 2.5 V to 3.3 V LVPECL Power Pins.
37, 44, 59, EPAD	N/A	GND	GND	Ground Pins, Including External Paddle (EPAD). The external paddle on the bottom of the package must be connected to ground for proper operation.
56	O	LVPECL	OUT0	LVPECL Output; One Side of a Differential LVPECL Output.
55	O	LVPECL	$\overline{\text{OUT0}}$	LVPECL Output; One Side of a Differential LVPECL Output.
53	O	LVPECL	OUT1	LVPECL Output; One Side of a Differential LVPECL Output.
52	O	LVPECL	$\overline{\text{OUT1}}$	LVPECL Output; One Side of a Differential LVPECL Output.
43	O	LVPECL	OUT2	LVPECL Output; One Side of a Differential LVPECL Output.
42	O	LVPECL	$\overline{\text{OUT2}}$	LVPECL Output; One Side of a Differential LVPECL Output.
40	O	LVPECL	OUT3	LVPECL Output; One Side of a Differential LVPECL Output.
39	O	LVPECL	$\overline{\text{OUT3}}$	LVPECL Output; One Side of a Differential LVPECL Output.
25	O	LVPECL	OUT4	LVPECL Output; One Side of a Differential LVPECL Output.
26	O	LVPECL	$\overline{\text{OUT4}}$	LVPECL Output; One Side of a Differential LVPECL Output.
28	O	LVPECL	OUT5	LVPECL Output; One Side of a Differential LVPECL Output.
29	O	LVPECL	$\overline{\text{OUT5}}$	LVPECL Output; One Side of a Differential LVPECL Output.
48	O	LVDS or CMOS	OUT6 (OUT6A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
47	O	LVDS or CMOS	$\overline{\text{OUT6}}$ (OUT6B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
46	O	LVDS or CMOS	OUT7 (OUT7A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
45	O	LVDS or CMOS	$\overline{\text{OUT7}}$ (OUT7B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
33	O	LVDS or CMOS	OUT8 (OUT8A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
34	O	LVDS or CMOS	$\overline{\text{OUT8}}$ (OUT8B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
35	O	LVDS or CMOS	OUT9 (OUT9A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
36	O	LVDS or CMOS	$\overline{\text{OUT9}}$ (OUT9B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
58	O	Current set resistor	RSET	A resistor connected to this pin sets internal bias currents. Nominal value = 4.12 kΩ.
62	O	Current set resistor	CPRSET	A resistor connected to this pin sets the CP current range. Nominal value = 5.1 kΩ.
63	I	Reference input	$\overline{\text{REFIN}}$ (REF2)	Along with REFIN, this pin is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF2.
64	I	Reference input	REFIN (REF1)	Along with $\overline{\text{REFIN}}$, this pin is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF1.

TYPICAL PERFORMANCE CHARACTERISTICS

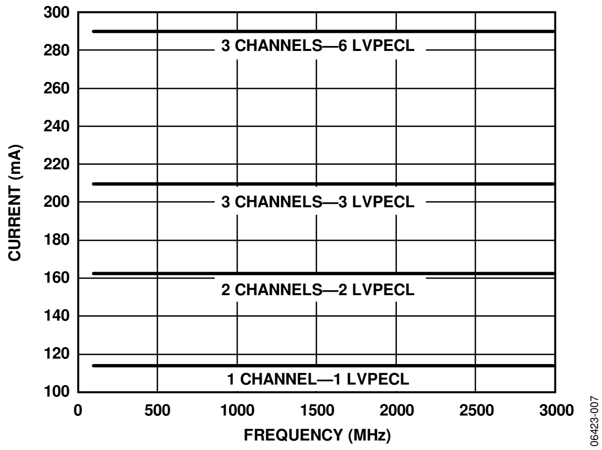


Figure 7. Current vs. Frequency, Direct to Output, LVPECL Outputs

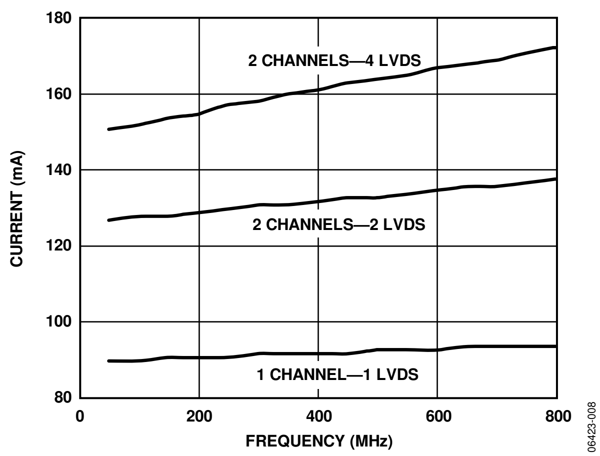


Figure 8. Current vs. Frequency—LVDS Outputs (Includes Clock Distribution Current Draw)

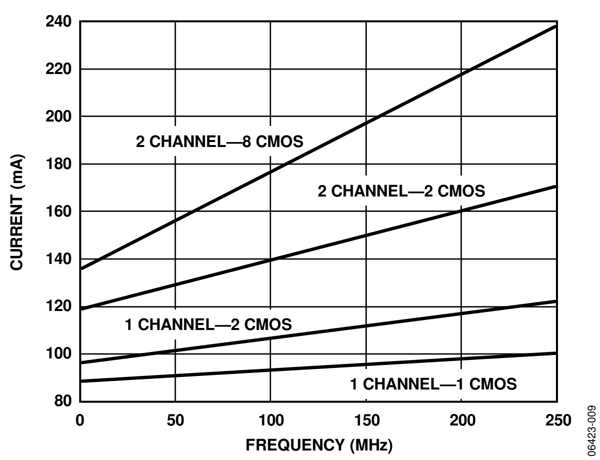


Figure 9. Current vs. Frequency—CMOS Outputs

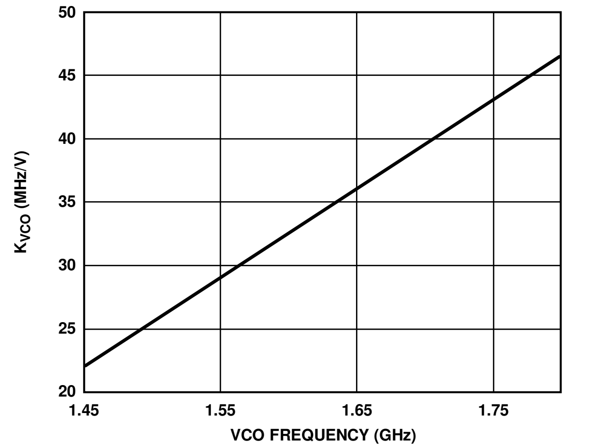


Figure 10. VCO K_{VCO} vs. Frequency

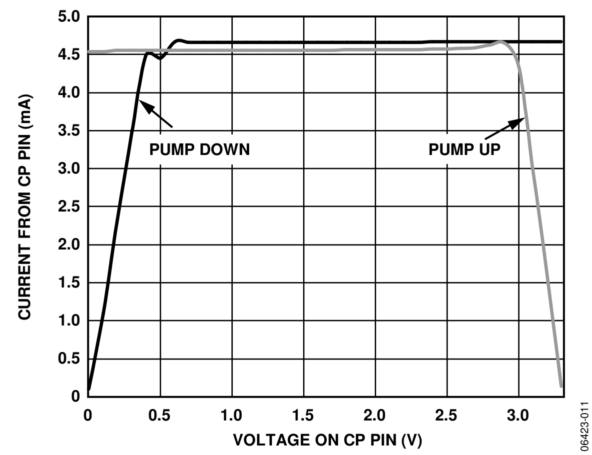


Figure 11. Charge Pump Characteristics at V_{CP} = 3.3 V

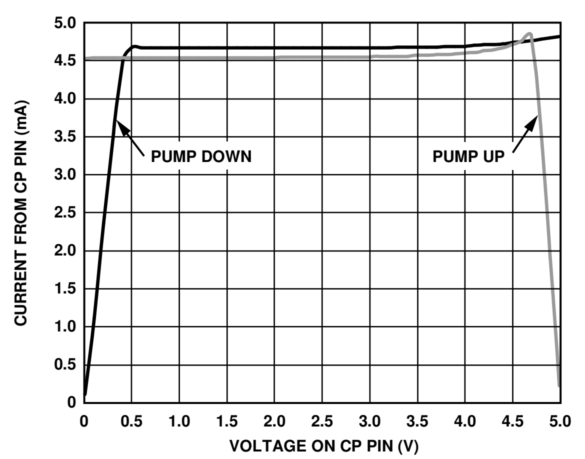


Figure 12. Charge Pump Characteristics at V_{CP} = 5.0 V

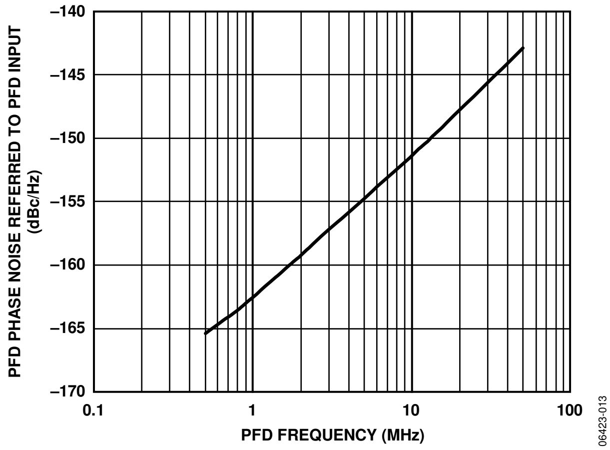


Figure 13. PFD Phase Noise Referred to PFD Input vs. PFD Frequency

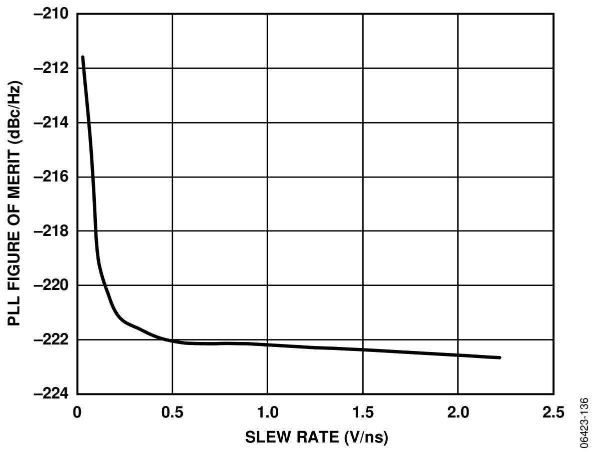


Figure 14. PLL Figure of Merit (FOM) vs. Slew Rate at REFIN/$\overline{\text{REFIN}}$

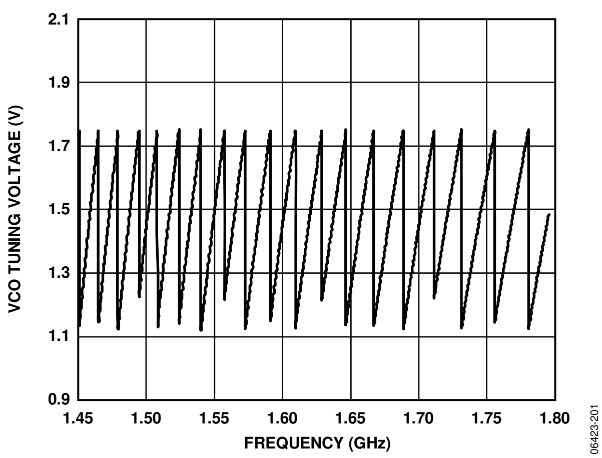


Figure 15. VCO Tuning Voltage vs. Frequency (Note that VCO calibration centers the dc tuning voltage for the PLL setup that is active during calibration.)

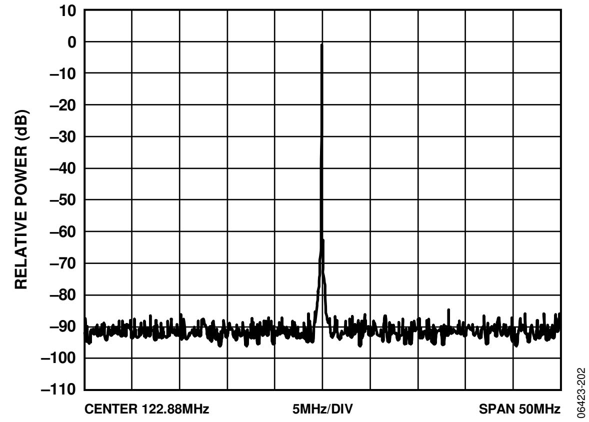


Figure 16. PFD/CP Spurs; 122.88 MHz; PFD = 15.36 MHz; LBW = 135 kHz; I_{CP} = 3 mA; F_{VCO} = 1.475 GHz

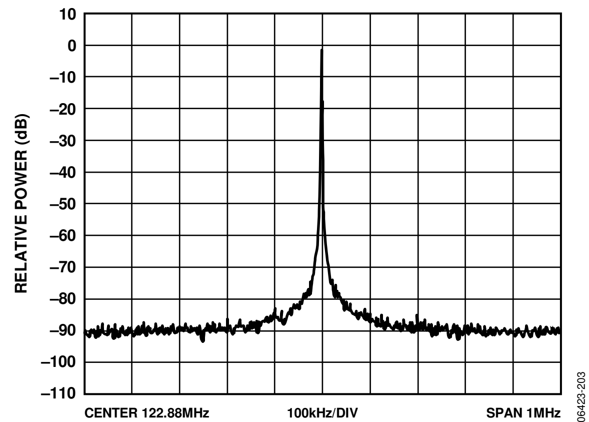


Figure 17. Output Spectrum, LVPECL; 122.88 MHz; PFD = 15.36 MHz; LBW = 135 kHz; I_{CP} = 3 mA; F_{VCO} = 1.475 GHz

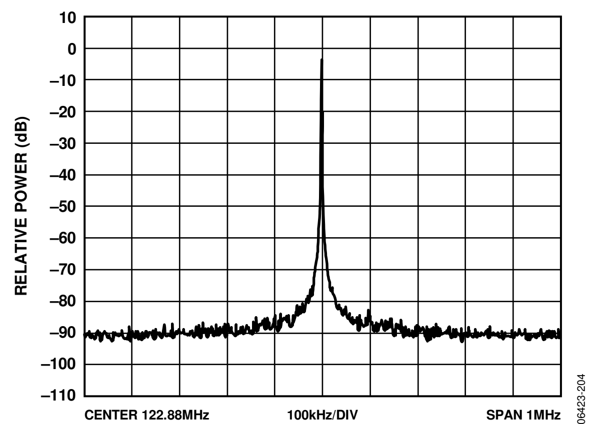


Figure 18. Output Spectrum, LVDS; 122.88 MHz; PFD = 15.36 MHz; LBW = 135 kHz; I_{CP} = 3 mA; F_{VCO} = 1.475 GHz

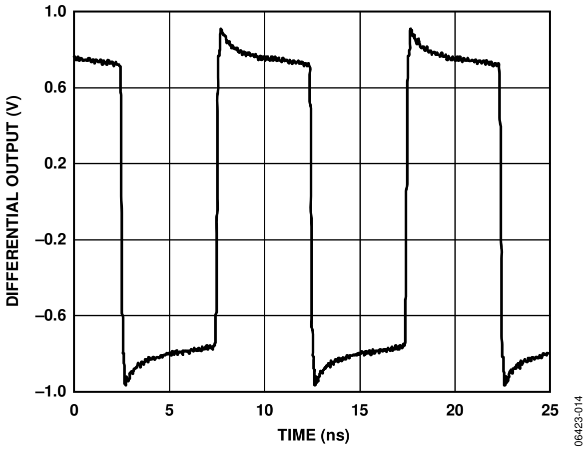


Figure 19. LVPECL Output (Differential) at 100 MHz

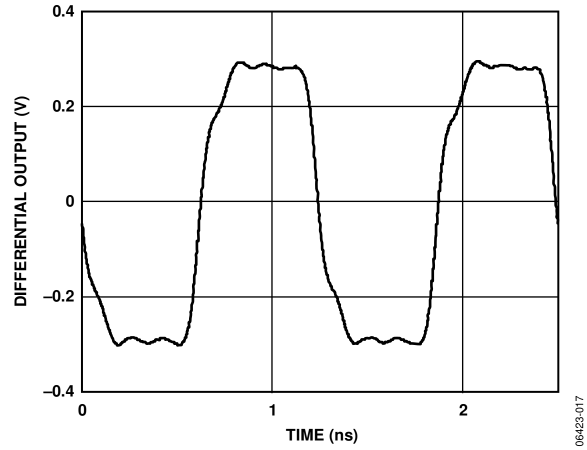


Figure 22. LVDS Output (Differential) at 800 MHz

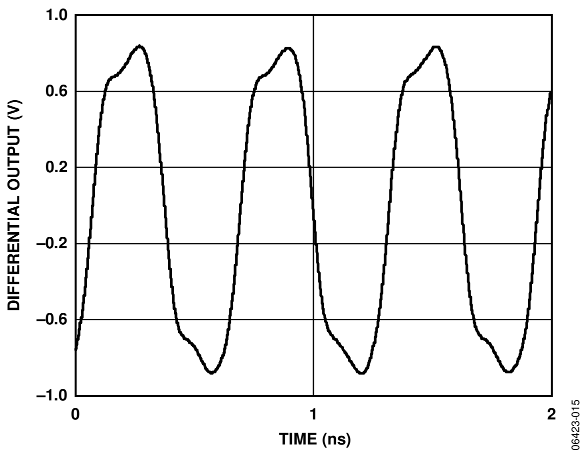


Figure 20. LVPECL Output (Differential) at 1600 MHz

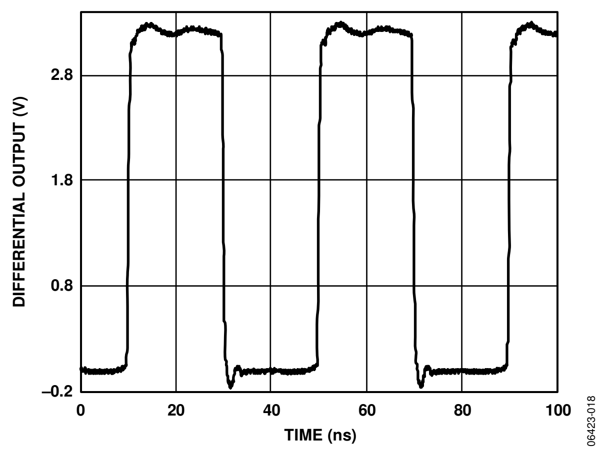


Figure 23.CMOS Output at 25 MHz

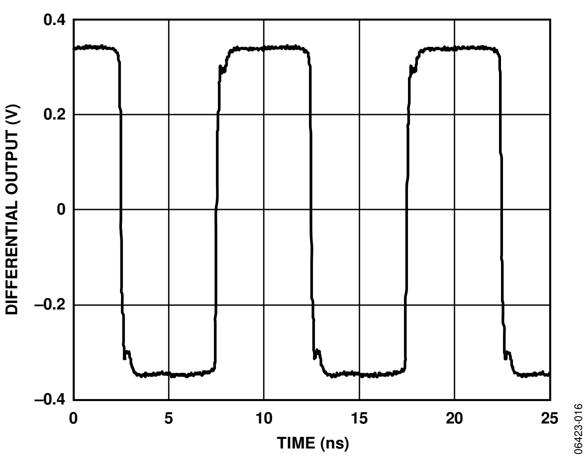


Figure 21. LVDS Output (Differential) at 100 MHz

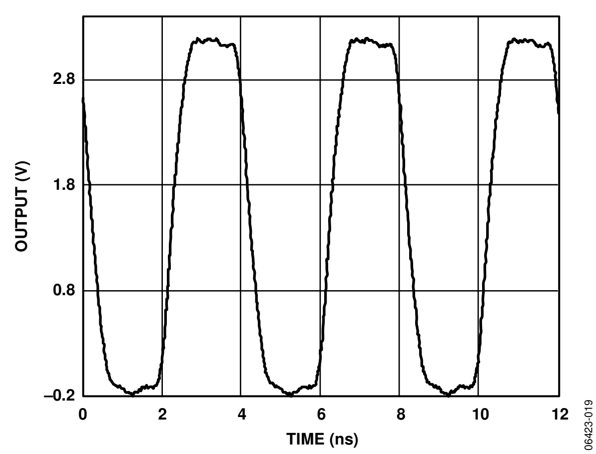


Figure 24. CMOS Output at 250 MHz

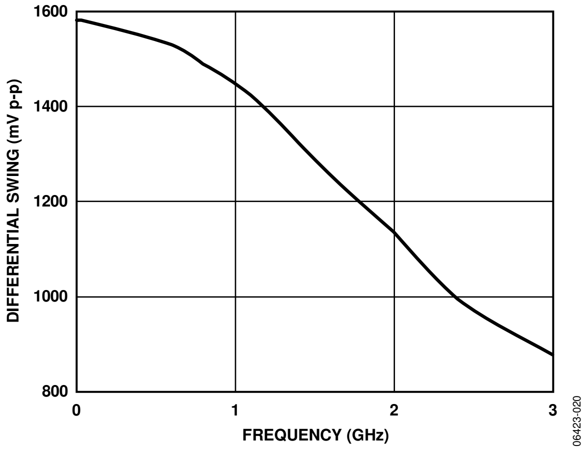


Figure 25. LVPECL Differential Swing vs. Frequency Using a Differential Probe Across the Output Pair

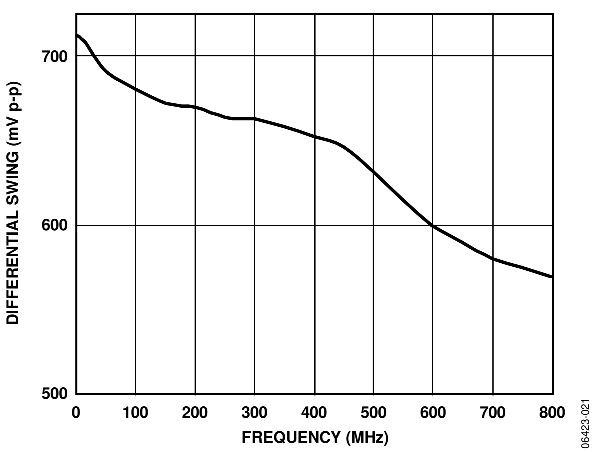


Figure 26. LVDS Differential Swing vs. Frequency Using a Differential Probe Across the Output Pair

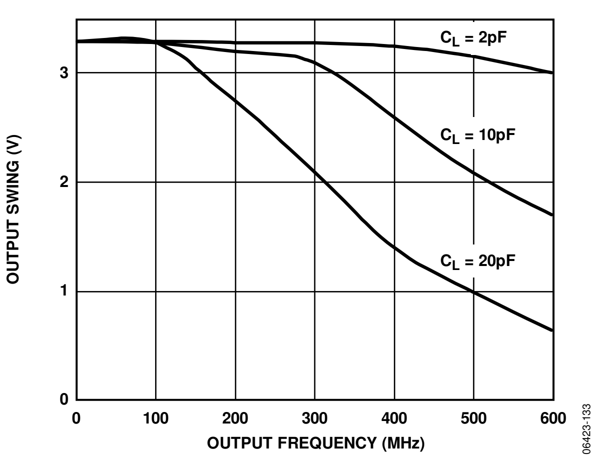


Figure 27. CMOS Output Swing vs. Frequency and Capacitive Load

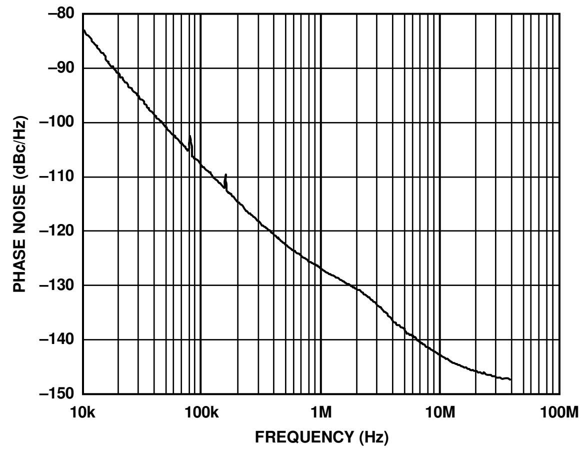


Figure 28. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 1800 MHz

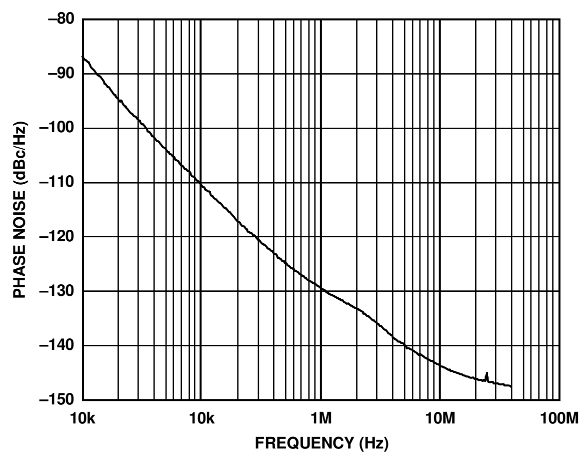


Figure 29. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 1625 MHz

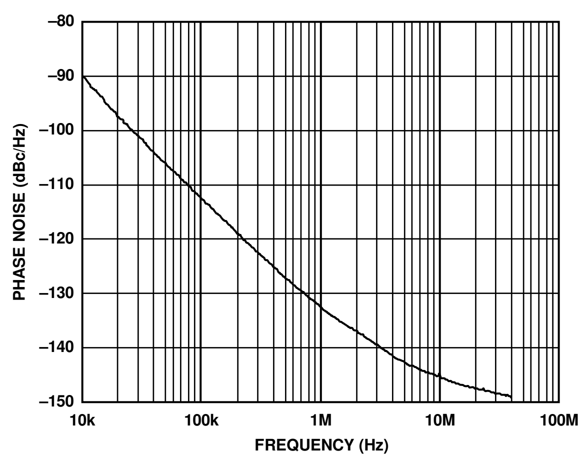


Figure 30. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 1450 MHz

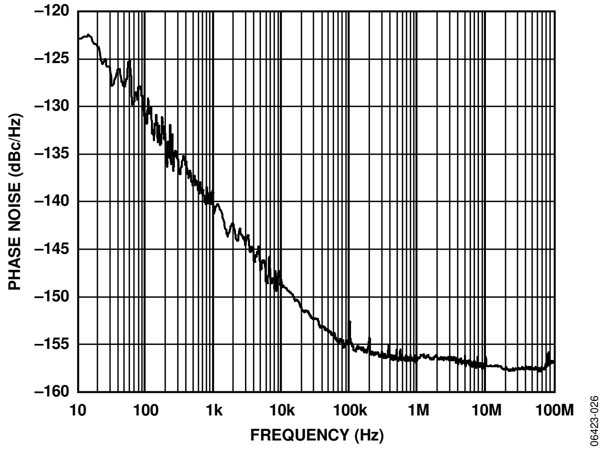


Figure 31. Phase Noise (Additive) LVPECL at 245.76 MHz, Divide-by-1

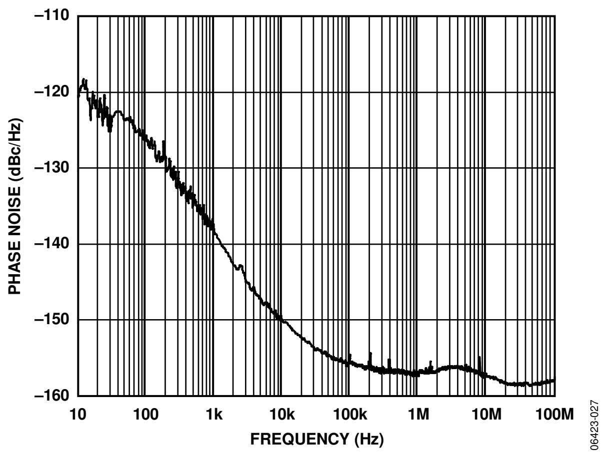


Figure 32. Phase Noise (Additive) LVPECL at 200 MHz, Divide-by-5

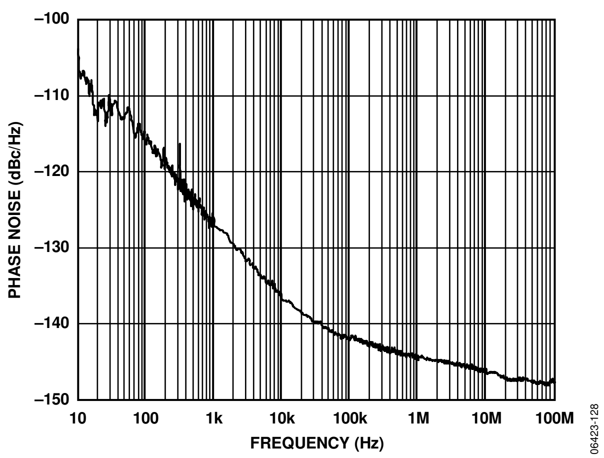


Figure 33. Phase Noise (Additive) LVPECL at 1600 MHz, Divide-by-1

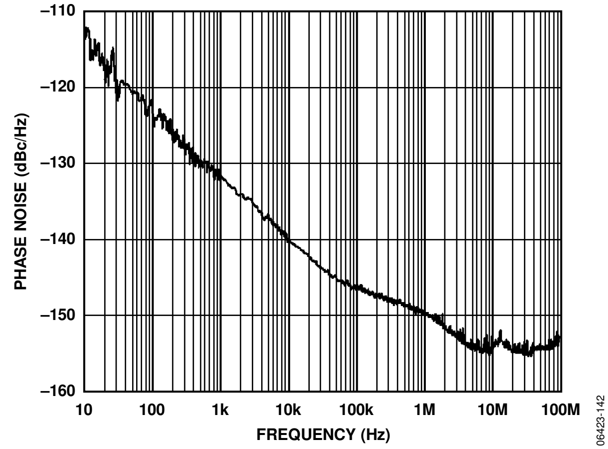


Figure 34. Phase Noise (Additive) LVDS at 200 MHz, Divide-by-1

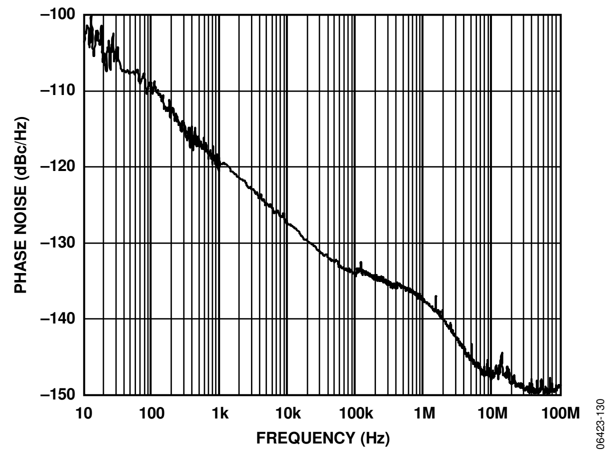


Figure 35. Phase Noise (Additive) LVDS at 800 MHz, Divide-by-2

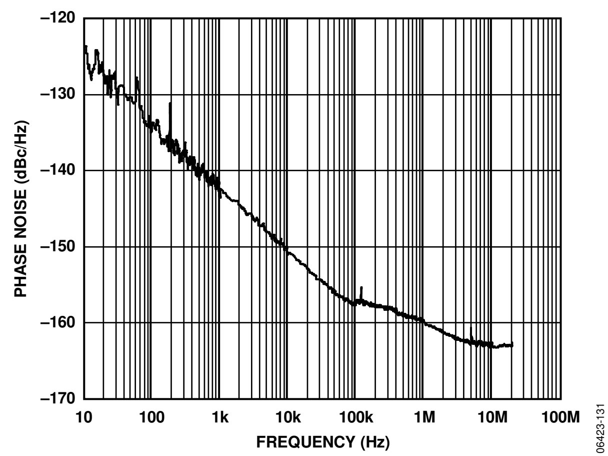


Figure 36. Phase Noise (Additive) CMOS at 50 MHz, Divide-by-20

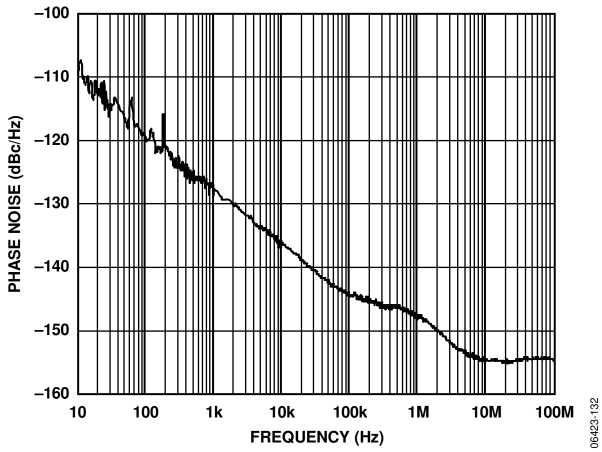


Figure 37. Phase Noise (Additive) CMOS at 250 MHz, Divide-by-4

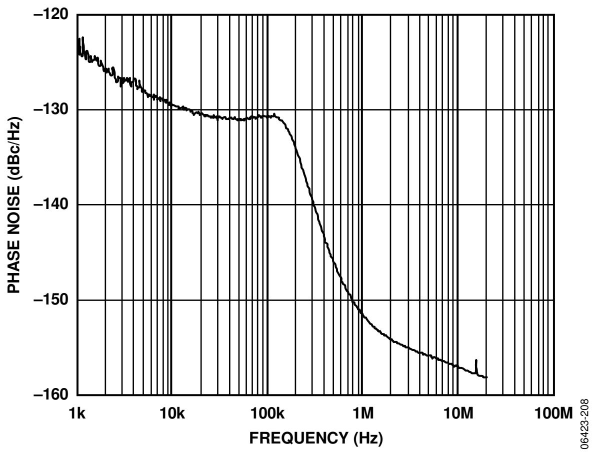


Figure 38. Phase Noise (Absolute) Clock Generation; Internal VCO at 1.475 GHz; PFD = 15.36 MHz; LBW = 135 kHz; LVPECL Output = 122.88 MHz

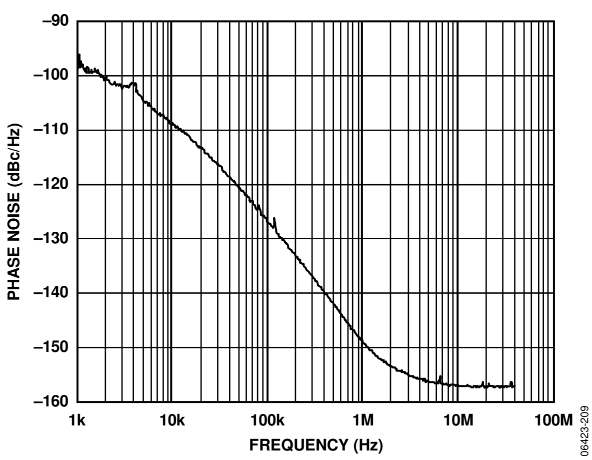


Figure 39. Phase Noise (Absolute) Clock Cleanup; Internal VCO at 1.556 GHz; PFD = 19.44 MHz; LBW = 12.8 kHz; LVPECL Output = 155.52 MHz

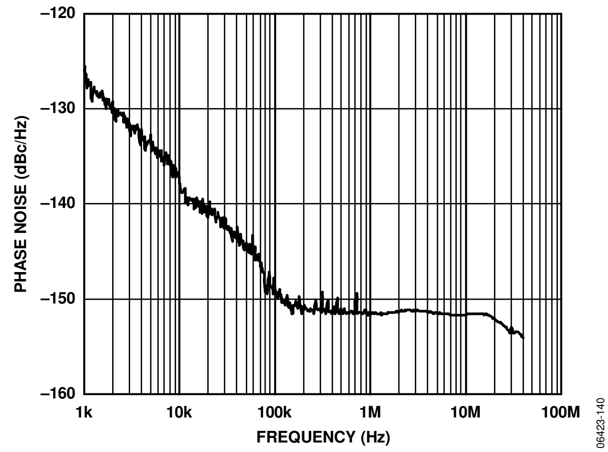


Figure 40. Phase Noise (Absolute), External VCXO (Toyocom TCO-2112) at 245.76 MHz; PFD = 15.36 MHz; LBW = 250 Hz; LVPECL Output = 245.76 MHz

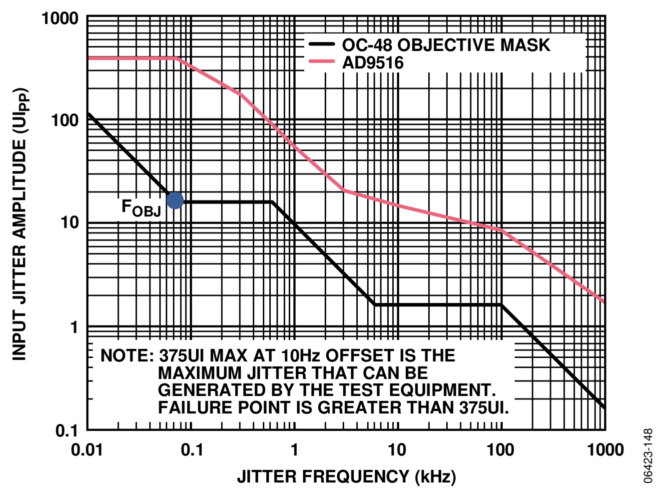


Figure 41. GR-253 Jitter Tolerance Plot